

**SG2002**

Hardware Design User Guide

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Revision History

|  |  |
| --- | --- |
| Specifications are subject to change without notice | ***SG2002***  ***Technical Reference Manual*** |

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CONTENTS

[Revision History 2](#_Toc167268819)

[CONTENTS 3](#_Toc167268820)

[1 Product Overview 6](#_Toc167268821)

[1.1 Overview 6](#_Toc167268822)

[1.2 Product Version 6](#_Toc167268823)

[1.3 Readership 6](#_Toc167268824)

[2 Schematic Design 7](#_Toc167268825)

[2.1 Chip SCH Package 7](#_Toc167268826)

[2.2 Chip IO Pin Voltage Withstand Description 7](#_Toc167268827)

[2.3 Power Supply Design Requirements 7](#_Toc167268828)

[2.3.1 CORE/TPU Power Supply Design 7](#_Toc167268829)

[2.3.2 DDR Power Supply Design 8](#_Toc167268830)

[2.3.3 IO Power Domain Design 9](#_Toc167268831)

[2.3.4 eMMC and SDIO0 Power Domain Design 9](#_Toc167268832)

[2.3.5 RTC Power Supply Design 10](#_Toc167268833)

[2.3.6 Power Management and Low Power Consumption Mode 10](#_Toc167268834)

[2.3.7 Power Sequencing Design 11](#_Toc167268835)

[2.3.8 Power Ripple & Noise Requirements Standards and Measurement Methods 13](#_Toc167268836)

[2.3.9 DCDC and LDO Design 14](#_Toc167268837)

[2.3.10 Power MOSFET Switch Design 16](#_Toc167268838)

[2.3.11 Main Chip Side Capacitance Requirements 16](#_Toc167268839)

[2.4 Minimum System Design Requirements 17](#_Toc167268840)

[2.4.1 Clock Circuit 17](#_Toc167268841)

[2.4.2 Reset Circuit 18](#_Toc167268842)

[2.4.3 Hardware Initialization System Configuration Circuit 19](#_Toc167268843)

[2.4.4 JTAG Circuit 19](#_Toc167268844)

[2.4.5 DDR Circuit Design 20](#_Toc167268845)

[2.4.6 Flash Circuit 20](#_Toc167268846)

[2.5 Peripheral Interface Design Recommendations 23](#_Toc167268847)

[2.5.1 EPHY-RJ45/RMII/RGMII Interface 23](#_Toc167268848)

[2.5.2 Video Interface 23](#_Toc167268849)

[2.5.3 Audio Interface 24](#_Toc167268850)

[2.5.4 IIC Interface 24](#_Toc167268851)

[2.5.5 SDIO Circuit 25](#_Toc167268852)

[2.5.6 SD 25](#_Toc167268853)

[2.5.7 USB 25](#_Toc167268854)

[2.5.8 ADC 26](#_Toc167268855)

[2.5.9 PWM 26](#_Toc167268856)

[2.5.10 UART 27](#_Toc167268857)

[2.5.11 GPIO 27](#_Toc167268858)

[2.5.12 Update Key 27](#_Toc167268859)

[2.5.13 Other Common Circuit Descriptions 28](#_Toc167268860)

[3 PCB Design 31](#_Toc167268861)

[3.1 General PCB Design Principles 31](#_Toc167268862)

[3.1.1 Learning and Mastering Relevant Design Materials 31](#_Toc167268863)

[3.1.2 Confirmation of Layer and Stack Structure 31](#_Toc167268864)

[3.1.3 No Concessions on Major Principles 31](#_Toc167268865)

[3.2 Power, Ground Layer and Filter Capacitor 31](#_Toc167268866)

[3.2.1 Power Net Trace Width and Via Quantity 31](#_Toc167268867)

[3.2.2 Main Power Routing 32](#_Toc167268868)

[3.2.3 Ground Layer 33](#_Toc167268869)

[3.2.4 Filter Capacitor 34](#_Toc167268870)

[3.2.5 DCDC and LDO 35](#_Toc167268871)

[3.3 Crystal Routing 36](#_Toc167268872)

[3.4 DRAM (VDDQ) 36](#_Toc167268873)

[3.5 Flash 37](#_Toc167268874)

[3.5.1 SPI Flash 37](#_Toc167268875)

[3.5.2 eMMC Flash 37](#_Toc167268876)

[3.6 Video Signal 38](#_Toc167268877)

[3.6.1 MIPI TX/MIPI RX 38](#_Toc167268878)

[3.6.2 VI\_DATA and VO\_DATA 39](#_Toc167268879)

[3.7 Audio Signal 39](#_Toc167268880)

[3.7.1 Analog Audio 39](#_Toc167268881)

[3.7.2 Digital Audio 40](#_Toc167268882)

[3.8 SDIO and SD Card 40](#_Toc167268883)

[3.9 USB2.0 40](#_Toc167268884)

[3.10 RJ45 with RMII/RGMII Routing 41](#_Toc167268885)

[3.11 PCB Thermal Design 42](#_Toc167268886)

[3.12 Copper Laying Rule Design 42](#_Toc167268887)

[4 Whole Machine ESD Design 43](#_Toc167268888)

[4.1 Background 43](#_Toc167268889)

[4.2 Whole Machine ESD 43](#_Toc167268890)

[5 Whole Machine EMI DESIGN 45](#_Toc167268891)

[6 Debug Methods for Debugging Common Problems 46](#_Toc167268892)

[6.1 Power Short to Ground 46](#_Toc167268893)

[6.2 Incorrect Supply Voltage 46](#_Toc167268894)

[6.3 eMMC Cannot be Burned 46](#_Toc167268895)

[6.4 Unable to Boot and Unable to Read eMMC Data 47](#_Toc167268896)

[6.5 DDR Init Fail 47](#_Toc167268897)

[6.6 No Printing on Power Up 47](#_Toc167268898)

[6.7 The Burning Program Cannot Run 48](#_Toc167268899)

[7 eMMC and DDR Reliability Software Test Methodology 49](#_Toc167268900)

[8 Heat Dissipation Design 50](#_Toc167268901)

[8.1 Main Chip Heat Dissipation 50](#_Toc167268902)

[8.2 Critical Component Heat Dissipation 50](#_Toc167268903)

[8.3 Temperature Rise Rectification 50](#_Toc167268904)

[9 List of Attachments 51](#_Toc167268905)

# Product Overview

## Overview

This document mainly introduces the schematic design, PCB design, whole-machine ESD design, whole-machine EMI design, ingle-board thermal design suggestions, production process suggestions, etc., for the SG2002 chip solution. The purpose of this document is to help customers shorten the product design cycle, improve product design stability and reduce the failure rate. Please refer to the requirements of this guide for hardware design, and try to use the relevant core templates released by Sophgo. If changes are required for special reasons, please follow the high-speed digital circuit design requirements and the PCB design requirements of Sophgo products.

## Product Version

The product versions corresponding to this document are listed below.

| Product Name | Product Version |
| --- | --- |
| SG2002 | V01 |

## Readership

This document (this guide) applies primarily to the following engineers:

* Technical Support Engineer
* Single Board Hardware Development Engineer
* PCB Layout Design Engineer
* PCBA Process Engineer

# Schematic Design

## Chip SCH Package

In order to ensure that there is no error as well as to facilitate Review, it is recommended to directly copy some circuits of key components such as the main chip and SPI-FLASH.

If you use other circuit design software tools, you can apply for an IC Ball out Excel file from Sophgo HW and build the SCH package of the chip through table import.

Attention:

At the very least, make sure that the SCH package of the main chip is going to be an exact copy or exactly the same!

## Chip IO Pin Voltage Withstand Description

The main chip’s VDDIO\_SD0\_EMMC and VDDIO\_SD1 Domain IO supports a withstand voltage and level of 1.8V/3.3V.

Other IO interfaces have 1.8V withstand voltage and level. When designing the circuit, special attention should be paid to the levels and voltages supported by other components to prevent level mismatches from causing signal anomalies and damage to the main chip.

Attention:

The voltage of the IO should be consistent with the corresponding Power Domain!

## Power Supply Design Requirements

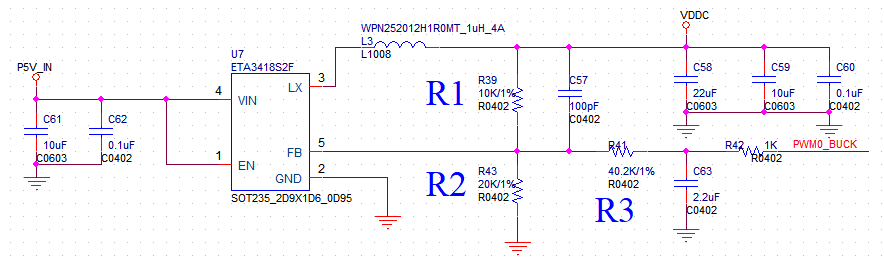
### CORE/TPU Power Supply Design

CORE and TPU power supply is VDDC.

The typical voltage is 0.9V (SG2002 voltage is 0.95V), which can be controlled by the PWM0\_BUCK dynamic regulator circuit after its normal power-up initialization, with a value of 0.9V ± 0.0XV (the range of X is still being refined, currently X=0);

**DCDC Selection:**

When replacing other models, it is crucial to ensure that the FB voltage of the DCDC must be 0.6V! In this case, the value of the voltage-regulating resistor is: series resistance R3 should be twice the value of the FB voltage divider resistor R2; If the FB of the DCDC is not 0.6V, the voltage-regulating resistor need to be recalculated. Please consult Sophgo HW engineer for assistance; The DCDC output capacity is required to be not less than 1.2A, and it should support a switching frequency of over 1MHz with fast dynamic response.



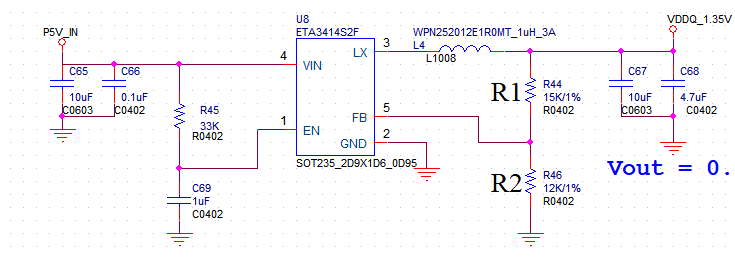
*Figure 2-1 VDDC/VDDC\_TPU Power Supply Circuit Diagram*

Attention:

R41, R42, C63 Reserved for VDDC dynamic regulator function, default can be NC.

### DDR Power Supply Design

* SG2002 has a Built-in DDR3L\*1, typical voltage 1.35V.
* DDR is powered by a separate DCDC.
* The power supply schematic diagram is shown below. The DCDC is recommended to select a switching frequency offset of 1MHz or above and an output capacity of 1A.



*Figure 2-2 DDR Power Supply Circuit Diagram*

### IO Power Domain Design

* VDDIO\_RTC: The Power Domain of PTEST, PWR\_VBAT\_DET, PWR\_ON, PWR\_SEQ, PWR\_WAKEUP, PWR\_BUTTON, PWR\_GPIO, etc.
* VDD18A\_AUDIO: the Power Domain of AUDIO.
* VDDIO18A\_USB\_PLL\_ETH: The Power Domain of USB\_DP, USB\_DM, ADC1, EPHY, PWM0\_BUCK, etc.
* VDD18A\_MIPI: The Power Domain of MIPI TX, MIPI RX.
* VDDIO\_SD1: The Power Domain of SD1.
* VDDIO\_SD0\_EMMC: The Power Domain of SD0, IIC0, JTAG, UART0, EMMC, etc.

Please refer to the schematic diagram of the reference board for the branch connection relationship of each IO power supply. For the current requirement of each power supply, please refer to the "Current Reference Table" section below, and make sure that the DCDC, LDO, inductor, capacitor, etc. must meet both the effective value (MAX) and the peak value (OCP) requirements.

Attention:

VDDIO\_SD0\_EMMC and VDDIO\_SD1 can be connected to 1.8V or 3.3V, and the corresponding PowerDomain PIN also changes to the corresponding level.

### eMMC and SDIO0 Power Domain Design

* VDDIO\_SD0\_EMMC: The Power Domain of eMMC and SD0. The selection for the power supply of VDDIO\_EMMC (PIN13) is as follows.

*Table 2-1 eMMC Domain Settings*

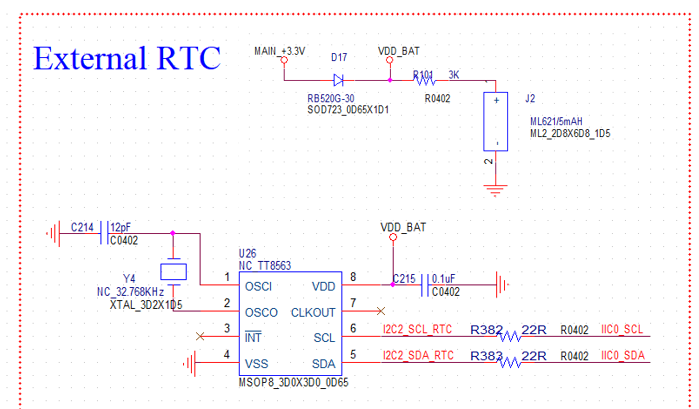
|  |  |
| --- | --- |
| VDDIO\_EMMC | eMMC Version |
| 3.3V | Version 4.4 and below |
| 1.8V | Version 4.5 and above |

Attention:

Because SDIO0 and EMMC share the same Power Domain, and the SD Card interface operates at 3.3V, it does not support the simultaneous presence of 1.8V EMMC and SD Card.

### RTC Power Supply Design

SG2002 does not have RTC Only Mode, if you need RTC, you have to plug-in RTC.



*Figure 2-3 RTC Power Supply Circuit Diagram*

### Power Management and Low Power Consumption Mode

#### Introduction

The power management module of the main chip can enable/disable the power supply module for different functional areas, receive button signals, rising edge signals for power up and down control as well as receive wake-up signals from peripherals, so as to achieving the standby and wake-up functions of the product.

#### RTC Only

The chip does not support built-in RTC function. Please use external RTC if needed.

The chip features a 32kless function that can also achieve RTC function. However, it must be in MCU only mode to keep time, and the power consumption is about 150uA. It may not be suitable to use Farad capacitor or small lithium battery alone.

#### MCU Only-Power Down

At this time, the power consumption of the chip is about 150uA. Except for VDDIO\_RTC which keeps 1.8V constant power supply, the rest of the voltages have been disconnected (PWR\_SEQ1, PWR\_SEQ2 are both 0), and can be turned on by PWR\_BUTTON1.

Attention:

VDDC\_RTC (PIN\_37) only requires a filtering capacitor and does not need to be connected to an external power supply.

VDDIO\_RTC will automatically boot from Power down mode to Active mode upon first power-up.

#### MCU Only-Sleep Mode

Similar to power down mode, but the wake-up sources are expanded to include PWR\_WAKEUP0 and other VDDIO\_RTC domain’s IO.

#### Active

In normal operation mode, all power supplies of the main chip work normally, and the VDDC Domain is able to make voltage adjustments to match its operating frequency.

### Power Sequencing Design

Chip power can be divided into the following categories: within the same domain, power up and down simultaneously; while across different domains, power up and down separately according to the following application scenarios.

RTC Domain：

VDDIO\_RTC (1.8V)

Core Power Domain：

VDDC

1.8V IO Domain：

VDD18A\_AUD

VDD18A\_USB\_PLL\_ETH

18OD33 IO Domain: depends on the input voltage to decide whether it is 1.8V or 3.3V Domain

VDDIO\_SD0\_EMMC

VDDIO\_SD1

3.3V Domain：

VDD33A\_EPHY\_USB

DDR IO Domain：

VDDQ

VDDQ\_DRAM

The general design requirements for the power-up and power-down sequencing of the main chip are as follows: 0.9V and 1.8V can be powered up simultaneously, or 0.9V can be powered up before 1.8V. However, 3.3V must wait until 1.8V is established before powering up. The power-down sequence should be the reverse of the power-up sequence. Peripheral components generally should not be powered up earlier than the IO Power Domain of the main chip they are connected to, in order to prevent voltage backflow that could lead to abnormal power-on or the main chip being damaged.

When powering the system with a battery, follow the reference circuit design for the power sequencing as per the reference board. It should not be altered casually. Utilize the main chip’s PWR\_SEQ1 and PWR\_SEQ2 pins to control the sequencing.

Power-up sequencing SEQ1 > SEQ2;

Power-down sequencing SEQ2 < SEQ1;

PWR\_VBAT\_DET is used as a monitor of the main power supply status. The software receives an interrupt when the voltage is low (for example, stopping reading or writing Flash to prevent system damage). When the voltage drops further, the RTC module will start the power-off procedure.

The application scenarios are supported in two main categories: plug-in applications and battery applications:

* Systems for plug-in applications

RTC Domain: VDDIO\_RTC connected to VCC\_+1.8V

SEQ1: Core Power Domain + 1.8V IO Domain + VDDQ (using HW SEQ)

SEQ2: 3.3V Domain

* Systems for Battery Applications

RTC Domain: VDDIO\_RTC, PWR\_GPIO0 (VDDBKUP) connected to a battery powered LDO

SEQ1: core power Domain + 1.8V IO Domain + VDDQ Domain (using HW SEQ)

SEQ2: 3.3V Domain

### Power Ripple & Noise Requirements Standards and Measurement Methods

#### Standard Requirement

All voltage amplitudes must be within ±3%. For power supplies of 3.3V and below, under normal circumstances, Power Ripple & Noise at the chip side is generally required to be controlled within ±100mV.

#### Test Description

Ripple & Noise is of great significance for analyzing power quality, system stability, DCDC selection, inductor and capacitor selection, troubleshooting certain issues and bugs, etc. Accurate measurements are essential to provide data support for these requirements.

#### Oscilloscope Probe Description

Probes have an equivalent capacitance, which to some extent will load onto the device under test. Probes are "thieves"; they introduce losses to the device being tested. It is best to use the high-quality probes originally supplied with the oscilloscope for testing.

#### Test Methods

1. Select voltage mode: Press the oscilloscope channel menu, then press Volt, then select "Voltage";
2. Set the oscilloscope parameters: set the coupling mode "DC", "Impedance 1M”; Select "DC RMS for N Cycles" and "Maximum Level" for Measures; Choose "Statistics", and then select "Reset Statistics"; select "Time Base Mode" "100us/div”; The waveform swing should occupy 2/3 of the entire oscilloscope display area. The default oscilloscope impedance is 1MΩ; if the impedance is mistakenly set to 50Ω, the signal will be halved; Select bandwidth limit to only measure the Ripple part, and " Bandwidth Limit " cannot be used for Noise part measurement.
3. Parameter descriptions:
4. DC RMS Average Over N Cycles: This parameter measures the effective value of Ripple & Noise. Typically, it should be measured at an ambient temperature of 60 °C, and for thermal (maximum load) conditions, the statistical value taken over at least 2 minutes is considered the effective value of Ripple & Noise under maximum load.
5. Maximum value of maximum level: This is the highest value recorded over the entire measurement period from the start to the present. If there is no interference, this value represents the upper limit of Ripple@Noise.
6. Peak-to-peak value: This is the peak-to-peak value of the Ripple waveform swing from the start of the measurement to the present over the entire cycle.

We generally record the average RMS value over N cycles and the peak-to-peak value. The peak-to-peak maximum value is used for reverse evaluation of inductor selection, as the formula for calculating the inductance of the inductor is L = Vout \* (1-Vout/Vin\_max) / Fsw \* Iload\_max \* 30% (uH), Iload\_Max \* 30% represents this peak-to-peak value.

#### Measuring Position Requirements

When measuring Ripple, it is necessary to use a short ground connection. The grounding point should be soldered next to the measurement point on the ground plane, and the measurement point should be directly beneath the IC. Additionally, remove the ground wire from the probe.

### DCDC and LDO Design

#### DCDC Selection

1) Selection of DC-DC rated input voltage Vin\_rating

Usually DC-DC manufacturers have different input voltage ranges to choose from. The price of wide range input is higher than narrow range input, and you should choose a suitable DC-DC according to the actual input voltage Vin.

Design requirements: Vin\*1.2<Vin\_rating<Vin\*2

2) Evaluation of DC-DC output current

It is necessary to ensure that under an ambient temperature of 60°C, the DC-DC converter continuously outputs an effective current Imax (60) that is greater than or equal to the maximum effective current value Iload of the load. It is important to note that the maximum current value specified in the actual datasheet of the DCDC is usually at 25°C. We need to calculate the continuous output effective current of the DC-DC at 60°C ambient temperature based on parameters such as thermal resistance mentioned in the datasheet. This can be calculated using the table "Method for Calculating DC-DC Imax(60°C)".

Design requirements: Iload≤Imax(60°C) <Iload+0.5A

3) Selection of DC-DC OCP parameters

The OCP protection point should be greater than the maximum peak current of the load, Iload\_peak. Normal operation does not allow the OCP to be triggered, otherwise there will be a drop in the output.

Design requirements: OCP>Iload\_peak

#### Efficiency and Working Patterns

Efficiency needs to be considered in two ways:

1. Choose a DC-DC converter that is efficient under light load condition, with a preference for COT/ACOT architectures;
2. Ensure a low voltage drop conversion while maintaining response speed, to improve the efficiency of the DC-DC conversion.

#### Inductor Selection

1) Selection of temperature rise current

Temperature Rise Current: Defined by most manufacturers in the industry as the current at which the self-heating temperature of the inductor product does not exceed 40°C. It is denoted by Irms (or Idc2)

Design requirements: Iload<Irms<Iload\*1.2

2) Selection of saturation current

Saturation current: The rated current based on the rate of change in inductance value, denoted as Isat (or Idc1). It is the rated current indexed by the degree of reduction in inductance value. When the load current exceeds the inductor’s saturation current, it may cause instability in IC control due to an increase in ripple current.

Design requirement: Iload\_peak<Isat<Iload\_peak\*1.2

3) Calculation method of inductance value

Inductance Calculation Formula: L=Vout\*(1-Vout/Vin\_max)/Fsw\*Iload\_max\*30

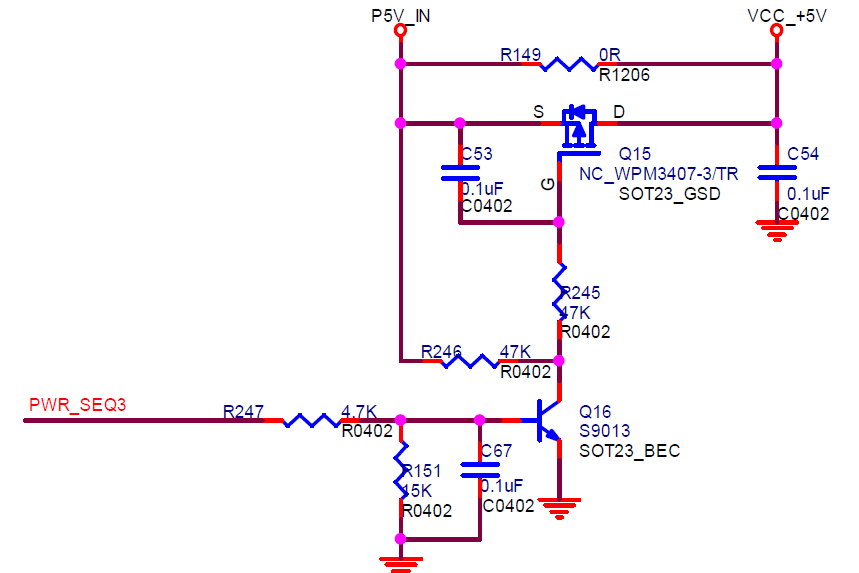
In switch-mode power supplies, the energy storage inductor is a key component that significantly affects the performance of the power supply. To ensure product performance while reducing the size of the switch-mode power supply inductor (the PCB area and height it occupies), a compromise between circuit performance and inductor parameters is necessary. Therefore, to reduce the output ripple voltage, you can opt for a larger inductance and low ESR high-capacity output capacitors. For the direct current resistance (Rdc), it is preferable to choose an inductor with as low an Rdc as possible.

#### LDO Design

For an adjustable LDO, voltage divider resistor using hundred ohms, K ohms (<5.6K) to ensure the LDO works normally and with low power consumption. When the LDO insertion power consumption is greater than 0.8W, you need to increase the power resistor. For standard LDO output voltage difference is guaranteed to be at least 1.3V. For specialized LDO, the minimum input and output voltage difference should meet the specifications provided in the datasheet.

### Power MOSFET Switch Design

In the design of a power MOSFET switch, it’s crucial to include a soft-start circuit to prevent spikes during turn-on that could damage the MOSFET or affect the work of other circuits. Typically, a bipolar junction transistor is used to control the MOSFET. If you’re considering controlling the MOSFET directly with a GPIO pin, please ensure that the GPIO’s parameters can meet the requirements of the MOSFET.



*Figure 2-4 MOSFET Switch Circuit*

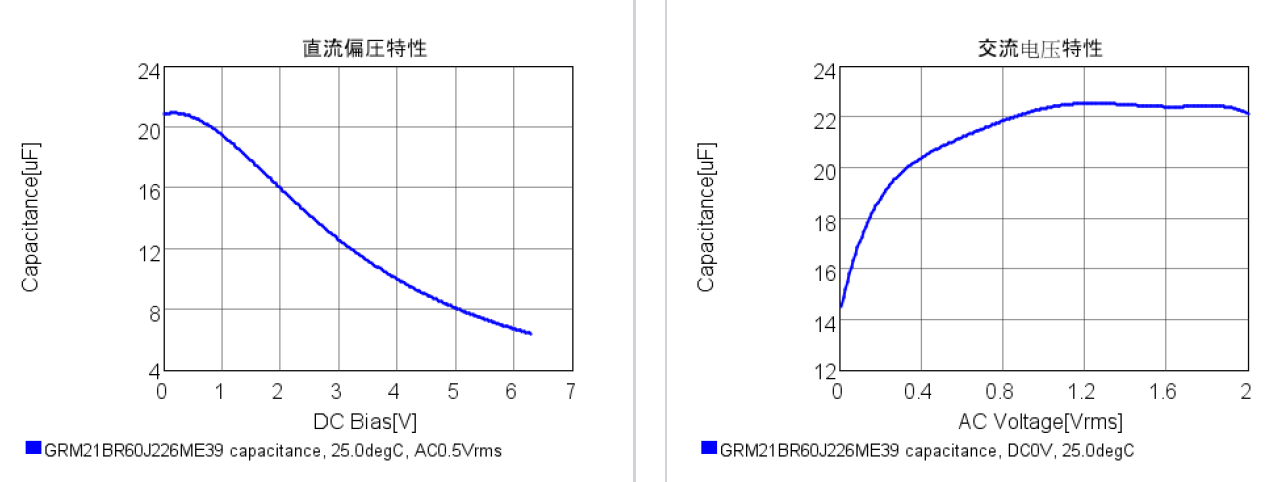
Attention:

1. GPIO High and Low correspond to the switch states of the MOSFET. If inversion is required, add a secondary stage of bipolar junction transistor.
2. The initial GPIO state (HW default state, before SW is controllable) must ensure that the MOS does not conduct.

### Main Chip Side Capacitance Requirements

In the PCB layout for the main chip, the capacitors located under the CPU package on the bottom layer are critical and cannot be removed or reduced in value. The capacitors on the main chip side must use X5R or X7R specifications, and types such as Y5V should not be used. The differences between X5R, X7R, Y5V, and Z5U mainly lie in their temperature ranges and how their capacitance values change with temperature. X5R has a normal working temperature range of -55℃~+85℃, with a corresponding capacitance change range of ±15%. Y5V has a temperature range of -30℃~+85℃, with a corresponding capacitance change range of ±22%.

Special attention should be paid to the DC/AC voltage and capacitance characteristics curve. Generally, the higher the voltage, the lower the capacitance. For example, a Murata 22uF\_6.3V, X5R capacitor, only has an electrostatic capacitance of 8uF at 5V.



*Figure 2-5 DC Voltage and Capacitance & AC Voltage and Capacitance Characteristics*

Attention:

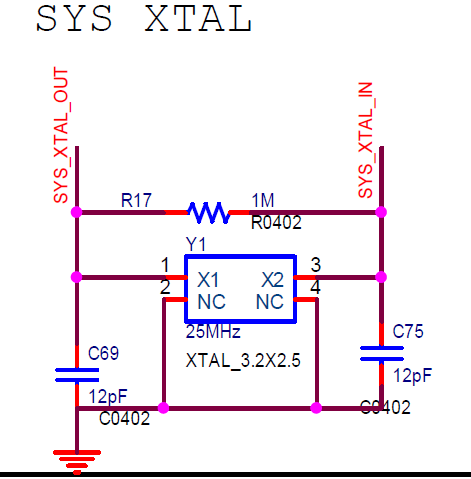
To control costs, the number and capacitance values of capacitors must be used judiciously. However, when reducing costs, it is imperative to carefully calculate and rigorously test for power ripple and noise, as well as conduct strict aging stress tests!

## Minimum System Design Requirements

### Clock Circuit

The main chip requires a 25MHz external clock with the following specifications:

1. Frequency deviation < ±30ppm;
2. ESR < 50Ω;
3. Load capacitance value = (crystal specification capacitance \* 2–5) times pF, to match the crystal specification capacitance; NPO material is recommended.
4. Drive power < 200uW;
5. It is recommended to choose a SMD crystal oscillator whose GND pin is fully connected to the board ground to enhance ESD resistance.



*Figure 2-6 System Crystal Circuit Diagram*

The main chip has a built-in RTC function with a 32.768K crystal. When the built-in RTC function is needed, it is recommended to use an external clock 32.768K crystal for the main chip in order to increase the accuracy.

Attention:

1. The 1M resistor in series with XTAL\_XIN\_XI and XTAL\_XIN\_XO cannot be omitted.
2. The load capacitance should be adjusted to the optimal state according to the test results of different crystal models, waveforms, and frequency deviations.
3. When the system and RTC use an active crystal, it is input from the XIN pin, and XOUT is left floating.

### Reset Circuit

Only one type of reset is available for the main chip, PWR\_RSTN (PIN\_39).

PWR\_RSTN controls the hardware reset of the entire chip

Peripherals related to the small system (for example: eMMC devices that store boot) must release the reset signal before or at the same time as the main chip, otherwise, there may be abnormal situations such as inability to start. The RESET of the main chip is currently directly connected to the power supply VCC\_+1.8V in the reference design.

### Hardware Initialization System Configuration Circuit

During the initialization of the main chip power-up, it is necessary to determine the working mode of each part according to the level status of the configuration pins. The hardware configuration signal descriptions are shown in the table below:

*Table 2-2 Boot Startup Method Configuration Description Table*

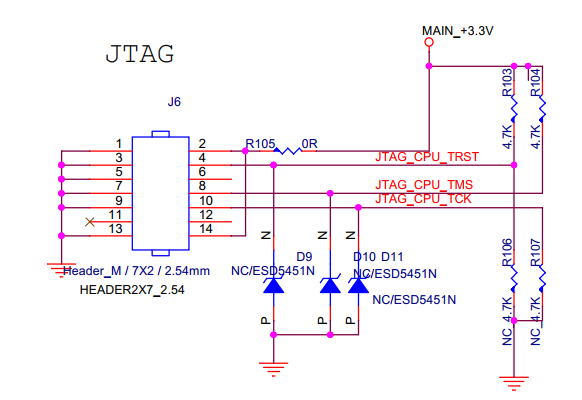
| Configuration Features | Pad Name | | Description |
| --- | --- | --- | --- |
| EMMC\_DAT0 (PIN22) | EMMC\_DAT3 (PIN23) | Peripherals |
| Boot  Startup Method | 1 | 1 | eMMC |
| 1 | 0 | SPI NOR |
| 0 | 0 | SPI NAND |

Attention:

1. The configuration of the Pad must refer to the EVB settings, only these PIN have this feature.
2. The configuration PIN must be pulled up to the power supply that is powered up the earliest.
3. If the configured PIN is left floating, the state of this PIN will be determined by the chip internally, so it will result in a high PU state.

### JTAG Circuit

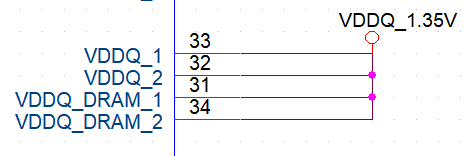
JTAG is in the VDDIO\_SD0\_EMMC Power Domain, so be careful with the voltage used. You don’t necessarily need a connector, but at least the pins should be pulled out or test points should be reserved.



*Figure 2-7 JTAG Module Circuit Diagram*

### DDR Circuit Design

The SG2002 main chip has a built-in DDR3L with a 16bit bit width. The voltage for VDDQ, VDDQ\_DDRAM is 1.35V.

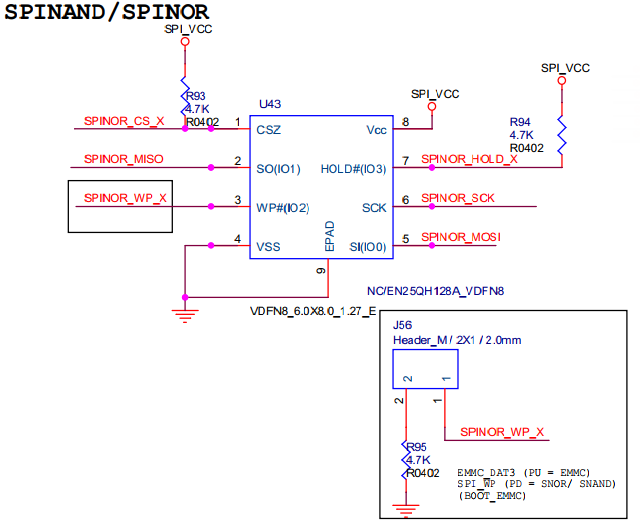


### Flash Circuit

The flash controller supports SPI NOR FLASH, SPI NAND FLASH and eMMC.

#### SPI Flash

When external SPI flash is connected, the reference circuit diagram is as follows: SPINOR\_WP\_X requires a 4.7KΩ pull-down; SPINOR\_HOLD\_X and SPINOR\_CS\_X require a 4.7KΩ pull-up.



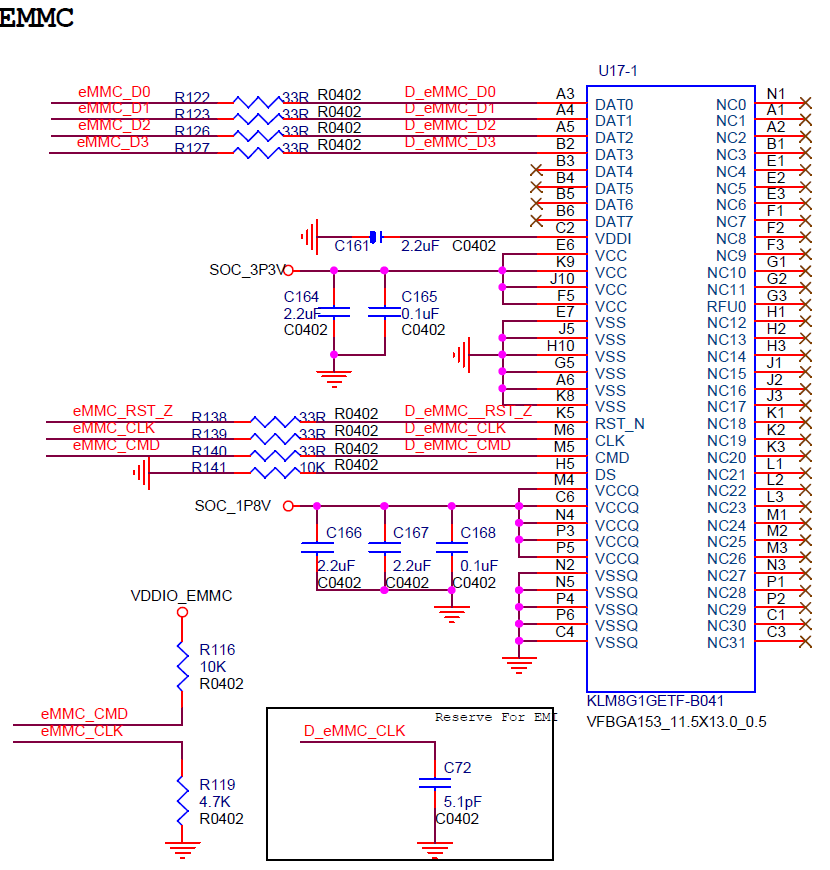
*Figure 2-8 SPI Flash Circuit Diagram*

Attention:

It is recommended to use an SPI flash device with a reset function to prevent the situation where the flash cannot reset synchronously when the main chip’s Watch Dog reset is triggered, thus unable to restart normally.

#### eMMC

When connecting an external eMMC, please refer to the following circuit diagram: the eMMC\_CMD requires a 10K pull-up; the eMMC\_CLK in series with a 33R resistor cannot be removed, and the reserved ground capacitor must not be removed as it is used for EMI issues; the ground capacitor under eMMC\_VDDI must be 2.2uF and cannot be reduced; the main chip only supports a 4-bit width.



*Figure 2-9 eMMC Circuit Diagram*

Attention:

The VCCQ of the eMMC, also known as VDDIO power level, must correspond to the eMMC SPEC. For example, if some eMMCs can only handle 3.3V IO, then the eMMC Power Domain should also be 3.3V.

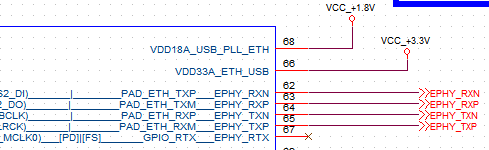
## Peripheral Interface Design Recommendations

### EPHY-RJ45/RMII/RGMII Interface

#### EPHY-RJ45

The main chip has a built-in 100MB PHY, which can be directly connected to the network port. The network differential lines between the main chip and the network transformer should be in series with a resistor of 5.1R or less to enhance resistance to network surges and to reduce network EMI. Add ESD devices when necessary. It is not recommended to use an RC circuit on the network differential lines to reduce EMI issues, as it can result in poor network differential signal eye diagrams.

When the EPHY interface is not in use, it can be utilized for other functions such as GPIO, note that the level is 1.8V.



### Video Interface

SG2002 supports dual sensor interfaces. It is important to note that the sensor configuration interface levels only support 1.8V. To ensure high-quality video signals, please choose sensor models that have been verified on the reference board.

When the VO interface outputs to panel, be careful that the timing of Panel's power supply cannot be earlier than the IO Domain of the main chip. When outputting BT.1120 signal, the upper 8bit represent the Y (luminance) signal, the low 8bit represent the C (chrominance) signal, be careful not to connect them incorrectly.

The order of MIPI TX and MIPI RX differential signal interfaces, SOC's MIPI 0,1,2,3,4 and the sensor's MIPI 0,1,2,3, CLK can be defined in software. Please refer to the "Detailed Description of Voltage Scenarios for Main Chip Sensor Input Interfaces and VO Output Interfaces" document for more information. Ensure that the SCH and PCB design maintain a smooth layout without any crossovers.

Attention:

When there are two sets of sensor interfaces, Sensor0 must be connected to MIPI\_RX0, MIPI\_RX1, MIPI\_RX2 and Sensor1 must be connected to MIPI\_RX3, MIPI\_RX4, MIPI\_RX5. The wire sequence between these two Sensors must not be swapped.

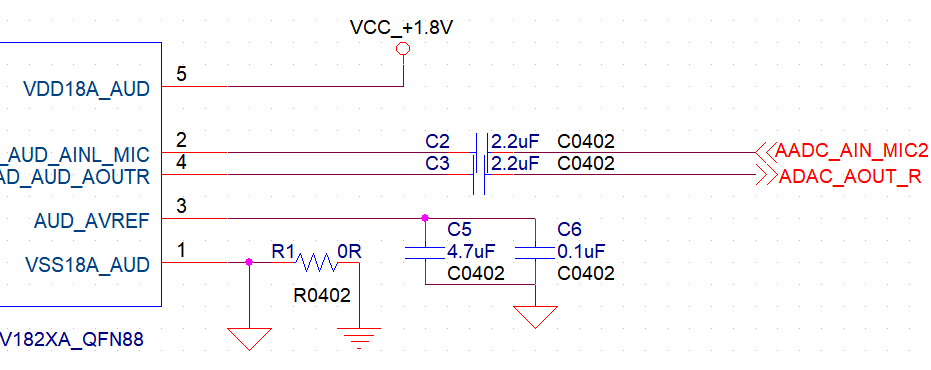
### Audio Interface

The filter capacitors on the AUD\_AVREF (PIN\_3) pins require 2 each, 4.7uF + 0.1uF respectively.

The decoupling capacitor for the audio input signal should be placed close to the main chip, with a recommended capacitance of 2.2uF. The output of AUD\_AOUTR should first be in series with a 2.2uF capacitor.

A 33Ω resistor should be connected in series with the MCLK of the I2S interface near the chip to obtain better signal quality.

If higher audio quality or headphone driving is required, it is recommended to add an audio amplifier around the audio output pins AC\_OUTL and AC\_OUTR.



Attention:

To avoid crosstalk between the analog and digital grounds, the AGND for the AUD\_AVREF (PIN3) capacitor and the AGND for the VSS18A\_AUD (PIN1) capacitors, should be kept separate from the system GND and being connected through a 0Ω resistor.

### IIC Interface

I2C0 is connected to general peripherals; I2C2 is used to configure Sensor0/1.

I2C is an OD interface and requires an external pull-up resistor. The resistor value should be chosen based on the number of devices on the bus and the length of the traces (including external wiring). The recommended range for I2C pull-up resistors is between 1K and 4.7K; the more slaves and the longer the trace, the smaller the resistor value should be.

Device addresses on the I2C bus should not conflict, and label the addresses directly on the SCH. For the convenience of software design, the allocation of the general slave’s I2C should refer to the reference board design.

### SDIO Circuit

The main chip has two SDIO interfaces. SDIO0 supports 1.8V/3.3V levels and is used for the SD storage card interface on the reference board. SDIO1 also supports 1.8V/3.3V levels, and this interface is designated for the Wi-Fi SDIO on the reference board and can be used as GPIO if not in use.

Attention:

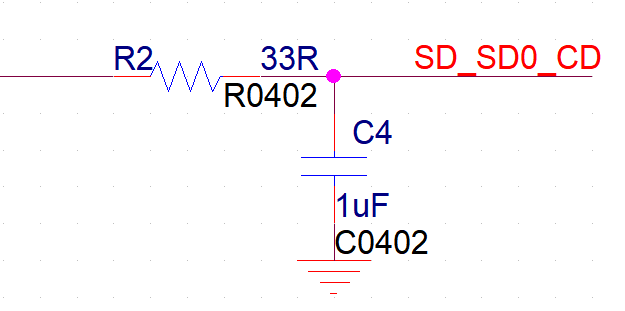
SD0\_PWR\_EN (PIN15) and SD0\_CD (PIN14) are on the VDDIO\_SD0\_EMMC POWER Domain. Be mindful of the voltage levels.

### SD

For products where the SD card slot is placed on a daughterboard and connected to the mainboard via a long cable:

The SD0\_CD Pin is prone to interference due to the long cable, which can cause false triggering and errors. It is necessary to reserve an RC circuit on the SD0\_CD line to mitigate this issue.

For products where the SD card slot and the main chip are on the same board, reserving an RC circuit is not required.



### USB

The USB port supports Host and Device Modes.

When the USB port is used for firmware burning, USB\_VBUS\_DET (PIN60) needs to detect through a resistor divider from 5V\_USB\_IN, and it must be high upon power-up to enter the SOC as Device Mode.

When the USB port is not used for burning, USB\_VBUS\_DET (PIN60) can be directly grounded, and the USB will be in Host Mode.

For the USB signal lines, a series resistor of no more than 5.1Ω should be used to address EMI issues. If an external USB device is connected, ESD protection devices should be added to the signal lines, with a parasitic capacitance requirement of less than 5pF.

For devices that connect to high-load current devices like portable hard drives, an electrolytic capacitor of more than 220µF should be placed near the connector end to prevent a voltage drop during insertion that could lower the system power supply or cause the device to be unrecognized.

Attention:

When selecting a USB Hub, it is essential to choose one that is compatible with the USB operating mode of the device that may be used. Some Hubs only support USB2.0, while others support both.

### ADC

The main chip features 3 ADC channels with a 12-bit sampling rate.

One of these channels, ADC1, is on the VDD18A\_USB\_PLL\_ETH Domain and operates at a 1.8V level when used as GPIO; For more details, see the “Function Signal Table” in section 2 of the “Main Chip\_PINOUT\_CN” document.

The other 2 channels are in the VDDIO\_RTC Domain

PWR\_VBAT\_DET (PIN38) is dedicated to system power-down detection and cannot be utilized for other functions.

PWR\_GPIO1 (PIN48) is used for battery level detection.

Attention:

The maximum sampling input voltage of the ADC is 1.5V.

### PWM

PWM0\_BUCK is fixed for VDDC voltage regulation;

Other PWMs can be cut out from the PIN multiplexing function.

### UART

The main chip features 4 UART channels. UART0 is fixed for system debugging.

The UART of the PIN MUX should correspond to the HW PIN MUX table.

Attention:

The power supply for the pull-up resistor must correspond to the POWER Domain of the respective UART.

### GPIO

The GPIO Level and withstand voltage of the main chip corresponds to its Power Domain. It is essential to ensure that its pull-up and peripheral levels are compatible and matched.

Ensure that the values of pull-up and pull-down resistors, as well as series resistors, meet the following level requirements:

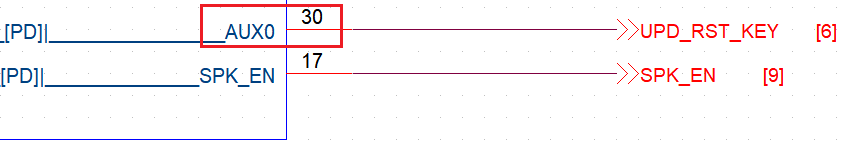
1. VIH and VIL are typically 70% and 30% of VDDIO, respectively.
2. VOH and VOL are typically 80% and 20% of VDDIO, respectively.

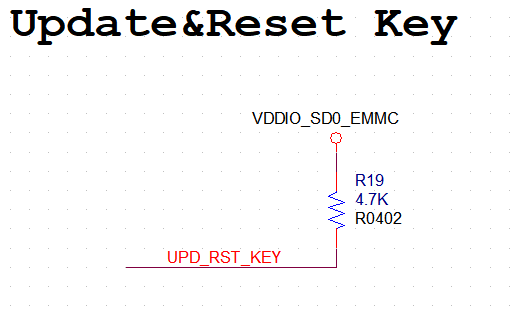
Attention:

When the SOC is connected to MCU or other devices (in scenarios where the SOC is powered down but the peripherals are not), in the "Main Chip\_PINOUT\_CN" file Pin Default Status page, only pins marked with **Fail-safe** will not leak current and can remain powered during the SOC’s power-down state.

### Update Key

PIN\_30 on the main chip is dedicated to the upgrade button. The chip will enter SD/USB upgrade mode only when it detects this button being pressed (low level) at power-up.

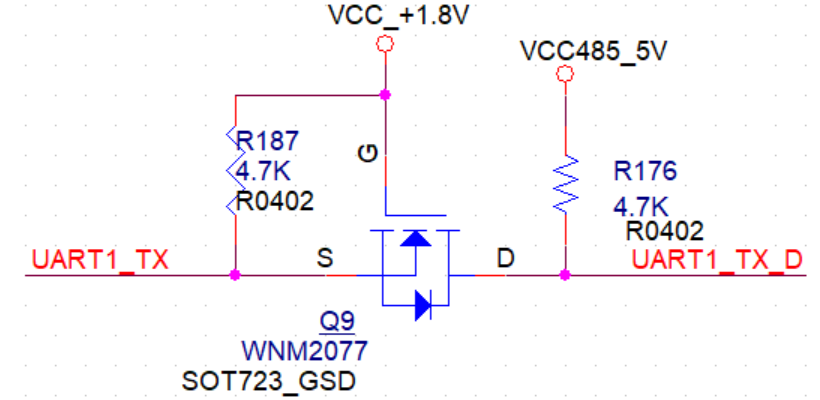




### Other Common Circuit Descriptions

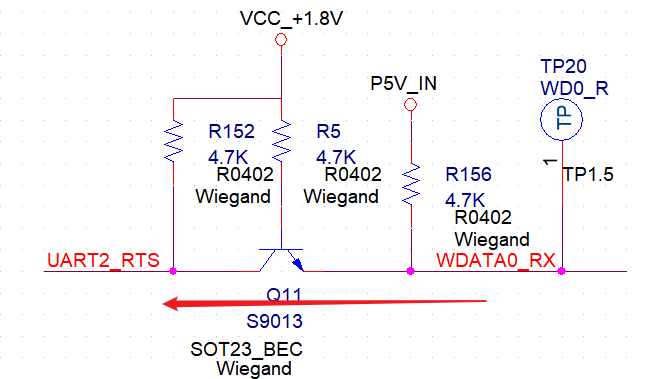
#### Level Shift Circuit

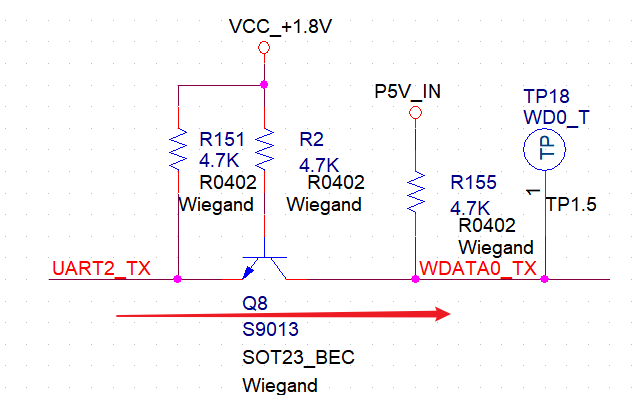
When the main chip and other chips have mismatched voltage levels, a level shift circuit is required. In the circuit below, the source (S) of the high-speed NMOS transistor is connected to the low voltage level, and the drain (D) is connected to the high voltage level, which can achieve level conversion for communication. This is more suitable for low-speed signals such as I2C and UART. For high-speed signals like SPI, SDIO, and USB, dedicated high-speed signal level conversion chips are required.



*Figure 2-10 Level Shift Circuit diagram*

For unidirectional low-speed communication level conversion, the following circuit can be used for level shifting. Note the data transmission direction as indicated by the red arrow.



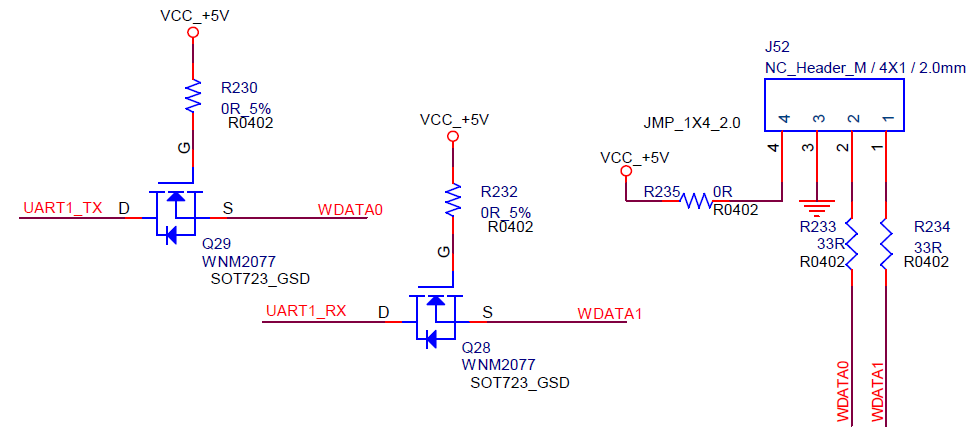


Attention:

For level circuits operating at 1.8V, it is particularly important to ensure that the NMOS selection meets the Vth specification of 1.8V for proper operation.

#### Wiegand Interface Circuit

For Wiegand interface selection, please refer to the “Function Signal Table” in section 2 of the "Main Chip\_PINOUT\_CN". When connecting the Wiegand interface to external devices on the board, it is crucial to strictly observe the surge and ESD protection levels and to add related components for safeguarding.



*Figure 2-11 Wiegand Interface Circuit Diagram*

#### RS232/RS485 Circuit

In designing this circuit, there are three important considerations:

1. It is important to choose an appropriate transceiver chip with a bit rate and IO level that corresponds to the requirements;
2. Consideration for an isolated DC power supply for the primary side to enhance surge resistance is important;
3. Use appropriate surge and ESD protection devices at the interface.

# PCB Design

## General PCB Design Principles

### Learning and Mastering Relevant Design Materials

Firstly, thoroughly read, learn, and master the “SG2002 Hardware Design Guide” and the “SG2002\_PCB\_Layout\_Guide”; grasp the design requirements, key points, and rules.

### Confirmation of Layer and Stack Structure

1. Determine whether additional board layers are needed based on interface layout and routing complexity.

If the board is larger and the routing does not have serious crossovers, it is recommended to maintain the minimum number of layers to reduce costs; if increasing layers, ensure that the stack-up structure meets the requirements.

1. Evaluate if additional board layers are needed for heat dissipation or EMI considerations.

For EMI considerations, signals such as MCLK, eMMC\_CLK, SDIO\_CLK, etc., must be routed in the inner layers.

### No Concessions on Major Principles

Ensure a complete copy under the SOC packaging for the bottom layer, including not adjusting the packaging of components. Make sure the number of core area capacitors is not reduced, the number of GND and Power vias is not reduced, and the GND pathways are as complete as possible and spread outwards.

Signal lines should be routed on the signal layers as much as possible, and Power Nets should be routed on the power layers as much as possible.

## Power, Ground Layer and Filter Capacitor

### Power Net Trace Width and Via Quantity

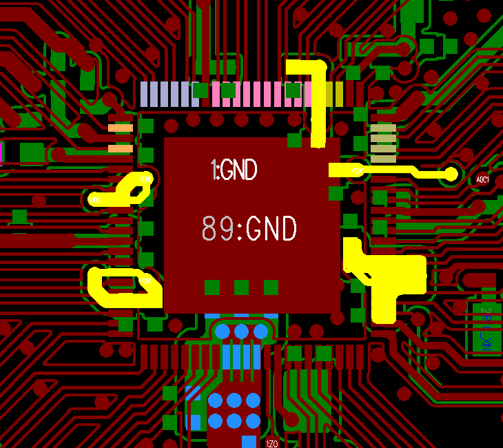
For a standard four-layer FR-4 board with 1-ounce copper thickness, the trace width should at least meet 40 mil/A. Pay attention to the bottom layer and power layer when using copper pour, as some areas may become very narrow; ensure the width satisfies the 40 mils/A requirement.

Generally, for 1-ounce copper thickness, a 10mil via inner diameter with a 20mil pad diameter corresponding to a 20mil trace can carry 0.5A of current. If there is a layer change in the power routing, place a sufficient number of vias at the connection point, at least two. If changing to an inner layer, double the number of vias to ensure good connectivity.

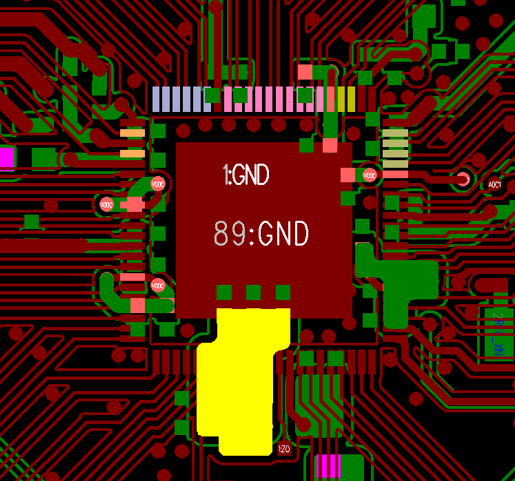
### Main Power Routing

Ensure that the trace width for critical power supplies such as VDDC and DDR is sufficient, and the number of vias is adequate.

VDDC



VDDQ

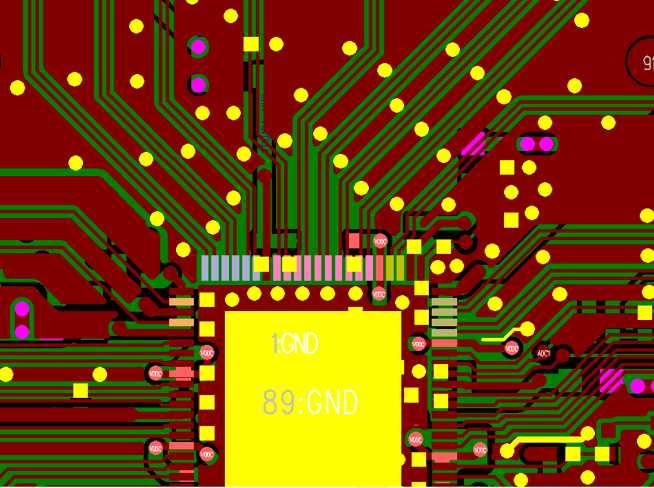


*Figure 3-1 Main Power Supply Routing PCB Diagram*

### Ground Layer

1. Power and Ground Layer Integrity Rule: In areas dense with vias, care must be taken to avoid connecting vias in the voided areas of the power and ground layers, which would segment the plane layers and compromise their integrity. This can lead to an increase in the loop area of signal lines on the ground layer.
2. Overlapping power and ground layer rule: Overlapping of the same power layer in space should be avoided. This is primarily to reduce interference between different power sources, especially those with significant voltage differences. Efforts must be made to avoid overlapping of power planes; if unavoidable, consider using an intermediate ground layer to mitigate the issue.

Ensure that the GND on the top and bottom layers r diverges in all directions and has a complete ground loop. Additionally, ensure that routing for differential signals and other lines requiring grounding have sufficient ground coverage.



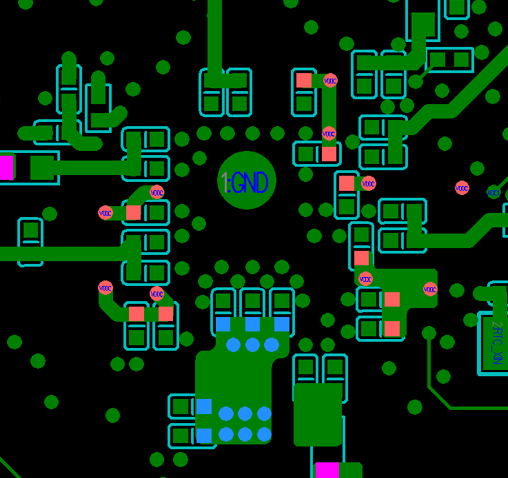
*Figure 3-2 Ground PCB Diagram*

### Filter Capacitor

General rules for device decoupling:

1. Necessary decoupling capacitors can filter out interference signals on the power supply, stabilizing the power signal. The layout of the decoupling capacitors and the routing method of the power supply will directly affect the stability of the entire system;
2. The layout of the IC decoupling capacitors should be as close as possible to the IC’s power supply pins, and the loop formed with the power supply and ground should be the shortest;
3. Power supply input: First, it goes through the input capacitor, then connects to the internal circuit;
4. Power supply output: First, it goes through the output capacitor, then to the output terminal;
5. Power supply to IC: First, it goes through the bypass capacitor, then to the IC.

The capacitance values beneath and surrounding the main chip, as well as the layout of the POWER/GND VIA, must fully refer to the reference board PCB design. This ensures that the capacitors can both support the power demands and filtering.



*Figure 3-3 Main Chip Decoupling Capacitor PCB Diagram*

### DCDC and LDO

General basic principles:

1. Multiple DCDC modules should not be placed too close to each other. If they are too close, the heat dissipation between the DCDC modules will be poor, leading to increased DCDC thermal output and reduced output capacity. Also, when modules are too close, the EMI intensity will be greater at adjacent switching frequencies;
2. DCDC modules dedicated to the main chip should be as close to the SOC side as possible. This minimizes power line attenuation and introduces less interference, resulting in cleaner power and ensuring a more timely and effective instantaneous current response from the SOC. However, they should not be too close, as the SOC’s heat dissipation could lead to increased DCDC thermal;
3. DCDC modules should be kept slightly away from audio, video, power amplifiers (including analog and digital amplifiers), and other analog signals to avoid interference;
4. For the DCDC module, it is ideal to place all peripheral components as close as possible to the DCDC IC itself, minimizing the length of the routing for the best layout.
5. Heat Dissipation: LDOs should have a heat dissipation copper foil on the back. When the power consumption is greater than 1W, consider switching to a package with better heat dissipation (such as TO252, TO263). For DCDC, avoid routing on the same layer; instead, use a large area of copper foil and open solder mask windows to enhance heat dissipation. Corresponding bottom layers should also open solder mask windows;
6. Feedback loops that require remote feedback must utilize remote sensing points and include grounding.

There are no strict requirements for the specific location of DCDC modules, but the general orientation should refer to the public board PCB design. Different DCDC modules should be placed in the corresponding direction according to the Power Net requirements, ensuring no interference with each other and no crossing of traces.

## Crystal Routing

For the crystal, signals such as XTAL\_XIN\_XI, XTAL\_XIN\_XOUT, RTC\_XIN, RTC\_XOUT, CLK25M, and other crystal oscillator signals should be completely shielded with a ground layer throughout their routing to ensure these signals have a complete reference plane. There should be no high-speed signals passing underneath the crystal circuit.

## DRAM (VDDQ)

Without special circumstances, to ensure system stability and software parameter consistency, it is not recommended to design DDR routing independently. It is required to completely copy the existing design of the reference board, including but not limited to the position number, component placement, routing method, trace width and spacing, power supply network, grounding rules, and so on.

Attention:

Any changes directly related to the DDR Layout must be informed to CViTEK HW for evaluation before making any changes!

## Flash

### SPI Flash

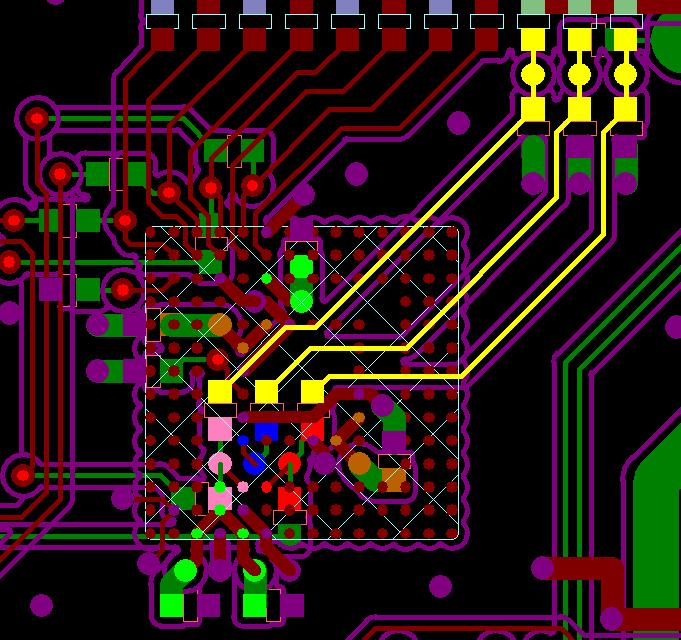
There are no special requirements for layout and routing, the SPI\_CLK signal line must be individually shielded with ground.

### eMMC Flash

The eMMC Power supply routing should be at least 20 mil, and the capacitors on the back should be as close to the eMMC Power Pad as possible, with a complete GND.

The eMMC generally does not require equal length routing; ensure that the eMMC CLK is fully shielded with ground and consider prioritizing the inner layers as much as possible.

Since the eMMC has a pitch of 0.65mm, special attention should be paid to the issue of the patch yield rate. If there is a higher incidence of PCBA short circuits, improvements should be made targeting the process issues.



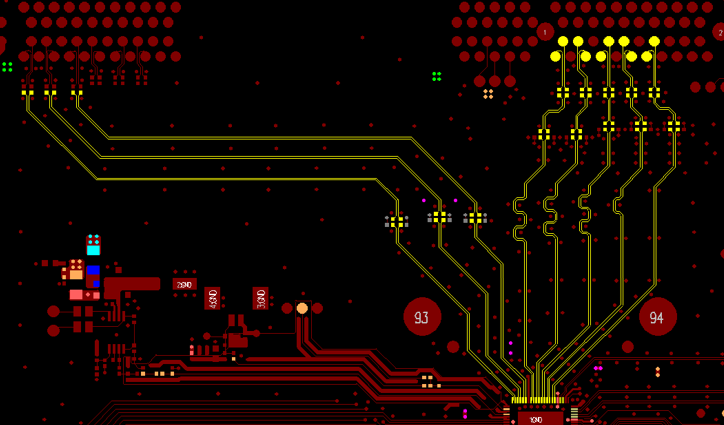
*Figure 3-4 eMMC PCB Diagram*

## Video Signal

### MIPI TX/MIPI RX

The design requirements are as follows:

* The trace width and spacing should follow a differential 100 Ohm routing, and try to avoid vias and layer transitions as much as possible. Please refer to the previous layout if there is an existing routing method; if not, please refer to the reference board layout;
* Use GND as the reference plane and try to maintain the integrity of the reference plane as much as possible;
* The differential pair inner P/N lengths should be controlled within 20 mils, and the length of the differential pair data signals should be based on the length of the clock signal, with a deviation controlled within ±300 mils; the differential impedance is controlled to be 100ohm +/- 10%;
* When passing through the connector, GND pins must be used to isolate adjacent differential signal pairs;
* The total length is recommended to be within 4 inches. Length matching constraints and the total bus length should consider the combined control of packaging, PCB, and external routing, etc.



*Figure 3-5 MIPI Signal PCB Diagram*

### VI\_DATA and VO\_DATA

The design requirements are as follows:

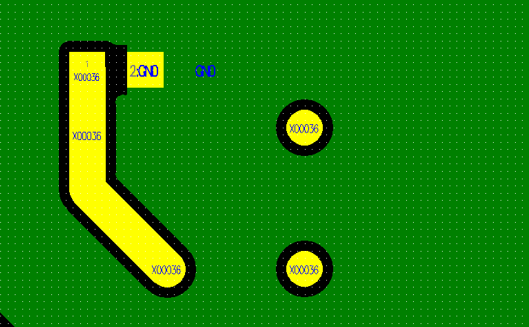
* Maintain a spacing of “3W principle” between adjacent signal traces;
* The length of the DATA lines should be based on the length of the CLK lines, with a deviation controlled within ±500 mil, and the CLK should be shielded with ground;
* Length matching constraints and the total bus length should consider the combined control of packaging, PCB, and external routing, etc.
* Due to the limited driving capability of CMOS and TTL interfaces, the overall length of the lines should not be too long.

## Audio Signal

### Analog Audio

The design requirements are as follows:

* The location of the lower ground capacitor and resistor of the AUD\_AVREF (PIN3) pin must be an exact copy of the reference board design;
* The splitting point resistor between Audio\_GND and system GND should be placed far from the SOC core area GND;
* The coupling capacitors for the analog audio input and output signals should be as close to the main chip end as possible, with grounding throughout the entire signal path.



*Figure 3-6 Analog Audio Signal PCB Diagram*

### Digital Audio

Each I2S signal should be individually shielded with ground as much as possible, with at least the MCLK being individually grounded, while the rest of the group should be grounded together.

## SDIO and SD Card

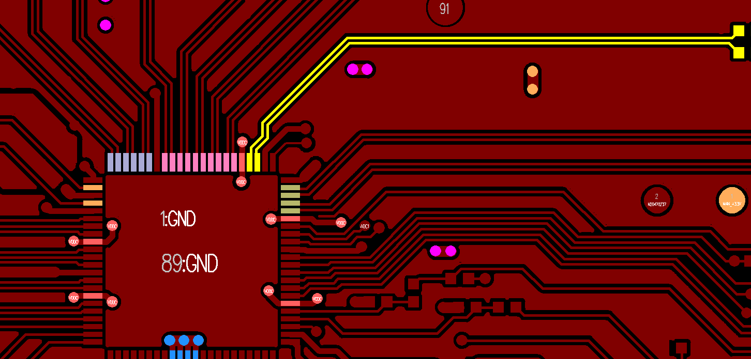
The design requirements are as follows:

* Maintain a spacing of “3W principle” between adjacent signal traces;
* The length of the DATA line should be based on the length of the CLK, with a deviation controlled within ±500 mil, and CLK should preferably be shielded with ground on the inner layers;
* Ensure the reference GND plane for the SDIO signal is as complete as possible;
* Length matching constraints and the total bus length should consider the combined control of packaging, PCB, and external routing, etc.
* Do not place high-power devices on the back of the SD card to prevent failure due to high temperatures;
* ESD devices should be placed close to the SD card slot.

## USB2.0

The design requirements are as follows:

* The series resistor should be close to the peripheral end, with the signal line length deviation controlled within 10 mil, differential impedance controlled at 90 Ω±10%, signal lines should be grounded and use GND as a reference, maintaining a complete reference plane;
* The signal line length should not exceed 5 inches, the number of vias should not exceed 2, the length of the external cable should be controlled within 1.5 meters, and when used as board-level cascading, the signal line length should not exceed 10 inches, and the number of vias should not exceed 2.



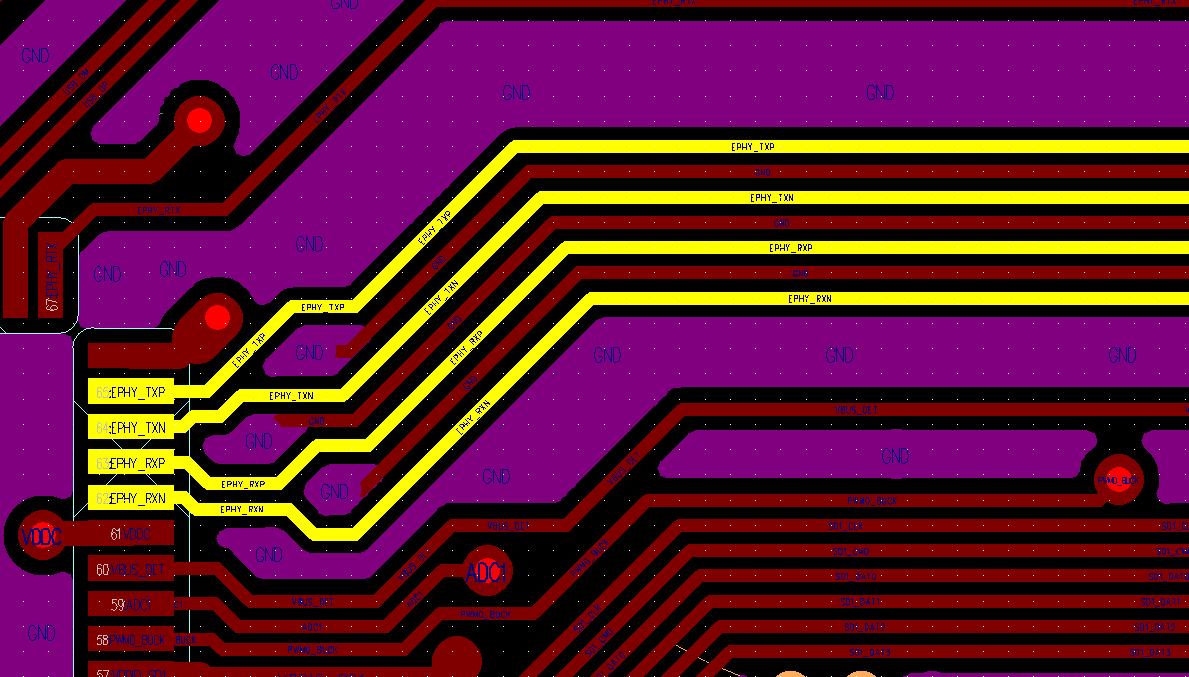
*Figure 3-7 USB2.0 Signal PCB Diagram*

## RJ45 with RMII/RGMII Routing

When routing the RMII module, refer to the reference board or follow the PHY chip manufacturer's requirements.

The RJ45 design requirements are as follows:

* RX0 and RX1, TX0 and TX1 are to be routed single-ended, with each signal wrapped separately to ground;
* RX0 and RX1, TX0 and TX1 should be routed single-ended, with each signal individually grounded.



*Figure 3-8 RJ45 Port Routing PCB Diagram*

## PCB Thermal Design

The primary method of heat dissipation in a PCB is through a large area of copper spread on the surface layer. After determining the appropriate board layers and stack-up structure, it’s best to minimize the surface layer routing as much as possible. If the board is small, consider increasing the number of layers.

For an SOC, it’s crucial to have as many GND VIAs as possible. Additionally, the GND in the core area should be as large as possible and spread outwards to dissipate the SOC’s heat throughout the entire PCB.

## Copper Laying Rule Design

The design requirements are as follows:

* DDR area: The design of copper laying in this area should refer to the reference board setup, including the inner layer;
* Other areas: you can set up your own, as long as the PCB and PCBA manufacturing processes meet the requirements.

# Whole Machine ESD Design

## Background

As the demand for system frequency and energy efficiency ratio in electronic product applications increases, chip fabrication processes continue to scale down, making the whole machine more sensitive to external interference. Customers must pay great attention to ESD design, lightning protection, surge protection, etc., in the overall design.

The main chip itself is tested for ESD according to JEDEC standards and can pass the ±2KV test, which meets industry standards. Customers need to evaluate and test the single-board hardware and the overall machine design according to their own ESD, lightning protection, and surge protection testing standards and levels.

## Whole Machine ESD

Some design recommendations and risk mitigation measures are provided below:

* The whole machine commonly used external interfaces: such as USB, SD Card slots, buttons, audio input/output ports, network indicator lights must be equipped with ESD or surge protection devices;
* The whole machine internal interface: such as video input/output ports, speaker interface, board-to-board interfaces, MIC interface, etc., assess the necessity of adding ESD protection based on product requirements, testing conditions, and production yield rates.
* Pay special attention to key components susceptible to ESD, as well as the ESD devices themselves. Ensure that the ESD parameters meet design requirements and do not compromise signal line quality.
* It is recommended to use metal housings for connector interfaces, ensuring they are fully connected to the device’s metal casing (e.g., USB ports with positioning holes, RJ45 sockets with spring clips). If necessary, use conductive pillars or conductive foam to achieve a full connection between the connector and the casing.
* For the system’s 25MHz clock, it is advised to use a 4-pin SMD crystal with two GND pins fully connected to the PCB to enhance the clock’s immunity to interference. Keep other traces as far away from the crystal as possible.
* For interfaces that require surge consideration, position them close to the edge of the board. Ensure there are screw holes near the secondary side for grounding to the chassis, and draw isolation strips between primary and secondary sides, such as for RS232/485, Wiegand, door sensors, POE, etc.
* Layout components of the small system section (clock, reset, main chip, DRAM, Flash, etc.) away from metal interfaces;
* Unless there are special circumstances, place signal line series resistors close to the peripheral end, and ESD devices as close to the interface as possible. If ESD device ground pins are connected through vias, the number of vias should be increased;
* If a metal heat sink is required, decide whether it should be grounded to the PCB based on actual ESD test results.;
* Use metallized vias for PCB positioning holes and connect them to the PCB GND. Choose screws without anti-rust coating to ensure full contact between the PCB and the device;
* When the whole machine is set up as a floating ground device, strictly prohibit the use of split ground design for PCB metallized interfaces;
* When the whole machine is a grounding device, ensure the metal casing is fully connected to the earth. Use a single-point connection between the segregated protective ground and the PCB digital ground, which can also include a 0R resistor. Position the single-point connection away from the small system circuitry, preferably near the device’s power connector;
* Implement ESD protection measures on both the PCB and the whole machine production line, including wearing antistatic wristbands, grounding related instruments and equipment, preventing hot-swapping, etc.

The above suggestions are mainly for reference, and the specific implementation should be based on the requirements of the individual enterprise.

# Whole Machine EMI DESIGN

* EMI issues should not only be addressed during the rectification stage, but it is even more important to fully consider EMI issues during the design of PCB, structure, routing layout, etc.
* Verify the interference between structure, routing, and layout;
* Determine the relationship between EMI exceeding frequency points and the fundamental frequency, the relationship between frequency points, and confirm whether it is harmonic or frequency leakage;
* Locate the frequency source;
* Common measures (increasing GND connectivity, shielding, winding, grounding, and RC);
* Lower the IO Driver and enable CLK spread spectrum function (spread spectrum can be implemented for eMMC, SDIO, MIPI, DDR, etc.).

For more details, please refer to “Sophgo EMI Common Analysis Approaches and Measures.”

# Debug Methods for Debugging Common Problems

## Power Short to Ground

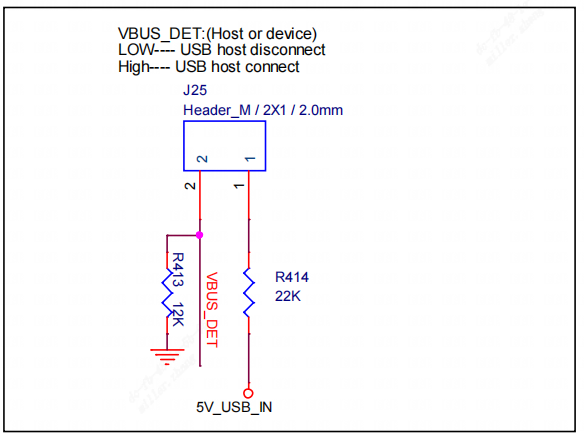
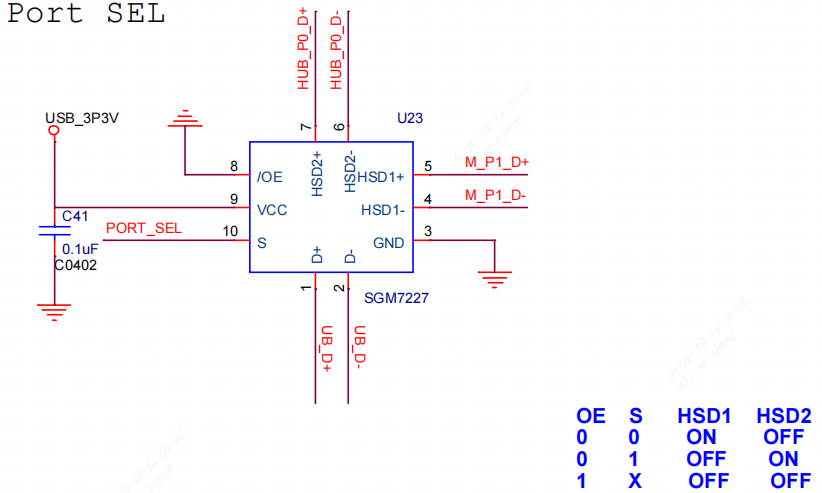
During single-board debugging or mass production, if a power network is found to be short-circuited to ground or has low impedance (usually poor soldering results in a short circuit, and it’s rare for impedance to be low), it is necessary to disconnect related nodes according to the Power tree one by one, to thoroughly investigate the cause of the short circuit, and to improve the design or production process.

## Incorrect Supply Voltage

If there is no short circuit to ground and the impedance to ground is within normal parameters, it is rare for the supply voltage to be too high or too low. If it occurs, it is generally caused by poor soldering of the DCDC/LDO or damage to the feedback loop resistance of the DCDC/LDO. First, observe the DCDC/LDO related components, then measure the feedback resistance, and finally replace the DCDC/LDO.

## eMMC Cannot be Burned

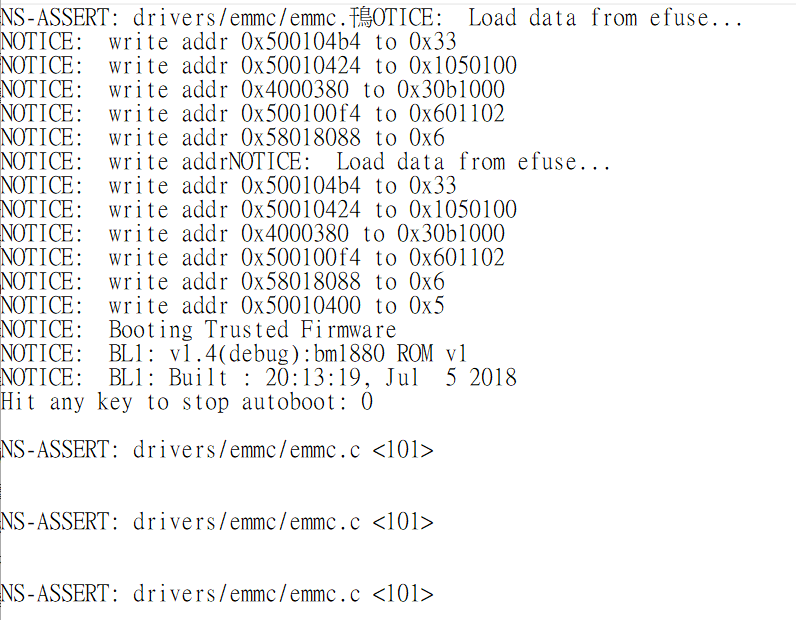
1. Ensure that the minimum system voltages such as VDDC and VDDQ are normal, and the HW Config configuration is confirmed to be verified;
2. Then check whether the impedance to ground of the serial port and USB port pins is normal;
3. When the USB port (the one that connects to the computer) is not recognized in the Windows command window, first check whether the control state of the USB signal path switching chip (such as the SGM7227 on the reference board) is correct, and then check whether VBUS\_DET is high.



4) Then see where the log shows, if it is stuck at DDR start done, then it means that DDR fail was called when burning. Therefore, the DDR is initially suspected to be faulty. You can inspect the DDR circuitry, and afterwards consider replacing the IC.

## Unable to Boot and Unable to Read eMMC Data

If you can't boot up and the log is stuck at NS-ASSERT: drivers/emmc/emmc.c <101>, it means the CPU can't read the data from the eMMC. In this case, measure the resistance to ground of the series resistors between the CPU and eMMC. Prioritize re-soldering the CPU and eMMC, and consider replacing the CPU before replacing the eMMC.

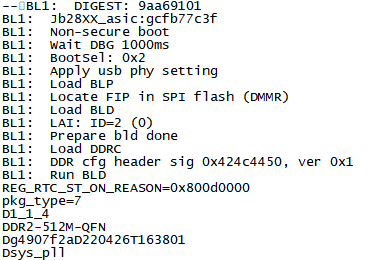


## DDR Init Fail

In general, when Ctrl bist fail or DDR init fail appears in the initial log location, check the DDR power supply voltage ripple and ZQ resistance, and then check if the chip is soldered properly.

## No Printing on Power Up

When the motherboard is powered up, even if the flash is empty and not yet burned, there will be a few lines of log information printed (as shown below).



If no information is printed on power-up, please check the following:

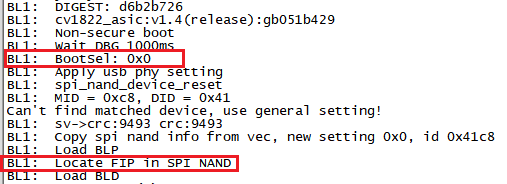
* 1. Confirm whether all voltage supplies are normal;
  2. Verify that the chip is properly soldered, focusing on checking the chip’s EPAD is well soldered to the ground;
  3. Confirm if the PWR\_VBAT\_DET level is above 1.0;
  4. Confirm if the UART0\_TX level is high;
  5. Confirm if the 25M crystal is oscillating;
  6. Check that the UART lines are operational.

## The Burning Program Cannot Run

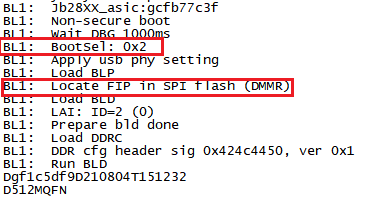
Review the printing log during the process and check the following:

* 1. Confirm whether the Flash model is supported by the reference board, and if the program has been fully burned;
  2. Confirm if there are DDR errors, such as software mistakes, for example, using DDR3 software on a DDR2 chip;
  3. Confirm if there is an HW Config error.

NAND Flash Boot:



Nor Flash Boot:



# eMMC and DDR Reliability Software Test Methodology

See the attached document for details.

It is required to select at least 2 pieces of each board type to run DDR tests for 12 hours.

# Heat Dissipation Design

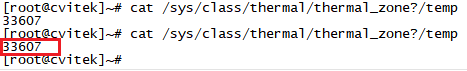
## Main Chip Heat Dissipation

Confirm the required operating temperature range for the whole machine. Sophgo demands that the chip surface temperature does not exceed 100°C, and the chip junction temperature does not exceed 125°C.

First, it is essential to ensure high-temperature aging conditions, using the standard conditions for normal shipment, with the complete system and all functions, including supplementary lights, algorithms, and other related applications, running normally. The Sophgo SOC has a built-in temperature sensor. After the high-temperature chamber and the system have been working for 3 hours and the state is basically stable, the chip junction temperature can be obtained through the following command and continuously monitor the chip junction temperature.

cat /sys/class/thermal/thermal\_zone0/temp

The following log represents the current junction temperature of the chip = 33.6°C.



## Critical Component Heat Dissipation

Ensure that the temperature rise of each key component, including but not limited to DCDC/LDO, Flash, DDR, etc., meets the requirements of their specifications.

## Temperature Rise Rectification

See “Sophgo Temperature Rise Rectification SOP\_V1.0” for details.

# List of Attachments

See the instructions in the Sophgo HDK table for details.