Memory modules are to be defined as follows: (do this twice – once each for RAM and ROM)

In Quartus II click on the tools tab on the top row of activities
click on the MegaWizzard Plug-in Manager
Select Create-a-new-one and click next.
On top right select Cyclone II or IV (depending on which DE2 you use)
Below that select Verilog HDL
Below that fill in the path and name (use RAM or ROM for name)
and place it in same directory as your .v file(s)
In the left panel go down to Memory Compiler and double click
Select RAM 1-port or ROM 1-port – click next
Make output bus 8
Number of words 512 for RAM 2048 for ROM
Auto block, single clock – click next
Deselect the 'q' output port – click next
For RAM no initialization
For ROM yes and use MiniS08CPUtest.mif – click next
(You probably have to download it first)
Click finish

My instantiation statements for using them were:

```
ram S08ram(abus[8:0],clk50,dbus,Write&RAMsel,RAMout);
rom S08rom(abus,clk50,ROMout);
```

RAMout and ROMout were both added to the dbus assign. They became the dbus value when Read was true and the appropriate decoding of the abus (RAMsel or ROMsel) was true for each.