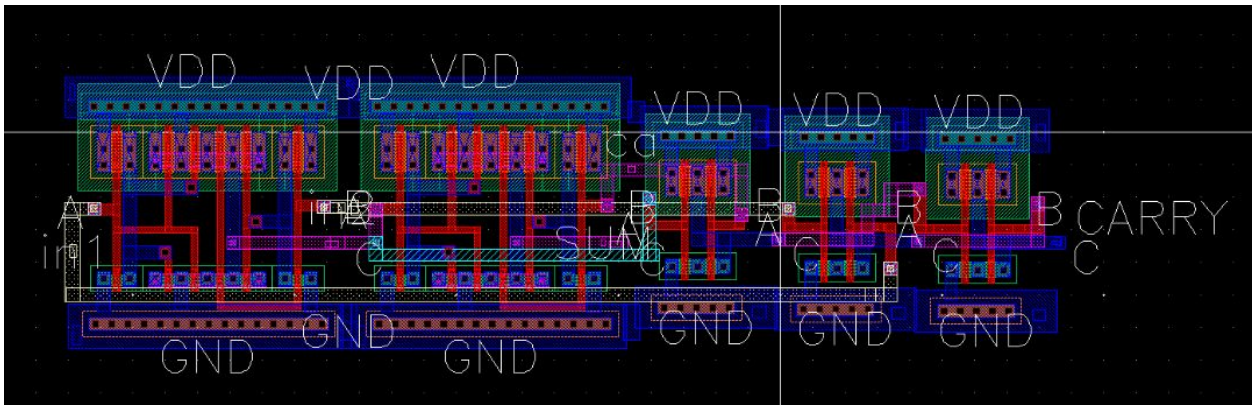
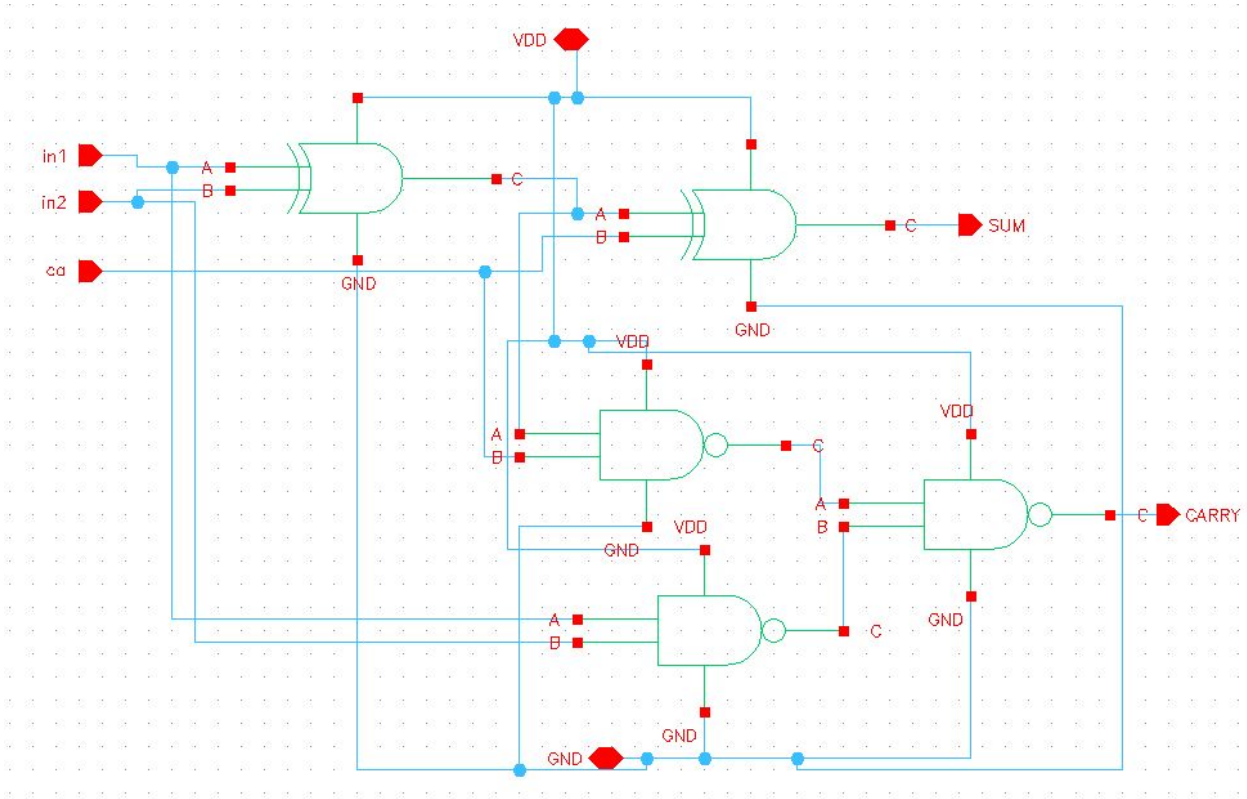
Khoa Diep
Lab 4
10/07/2020

1-bit adder layout



1-bit adder schematic



DRC

```
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "1bitadder layout"   *********
   Total errors found: 0
```

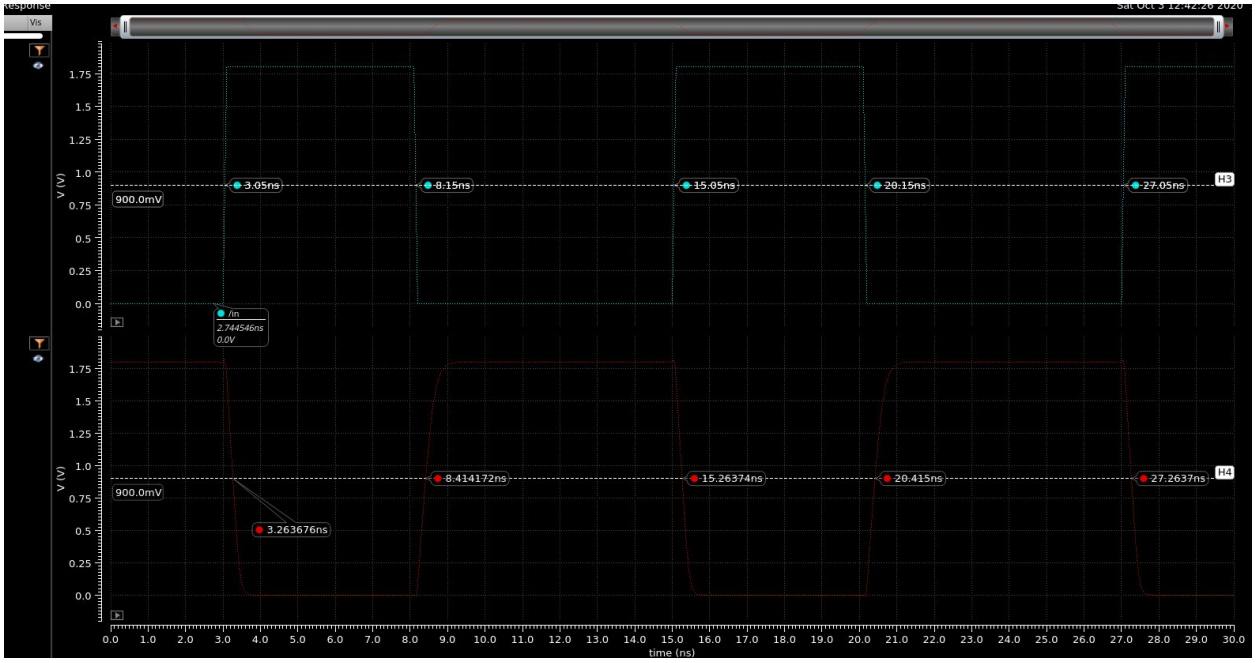
LVS

```
    Net-list summary for /home/ugrads/k/khoadiep/cadence/LVS/schematic/netlist
       count
        25              nets
        7               terminals
        18              pmos
        18              nmos


    Terminal correspondence points
    N24       N3        CARRY
    N18       N1        GND
    N19       N5        SUM
    N23       N4        VDD
    N20       N7        ca
    N22       N0        in1
    N21       N9        in2

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  36      36
        total                   36      36

                                 nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  25      25
        total                   25      25

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   7       7
```

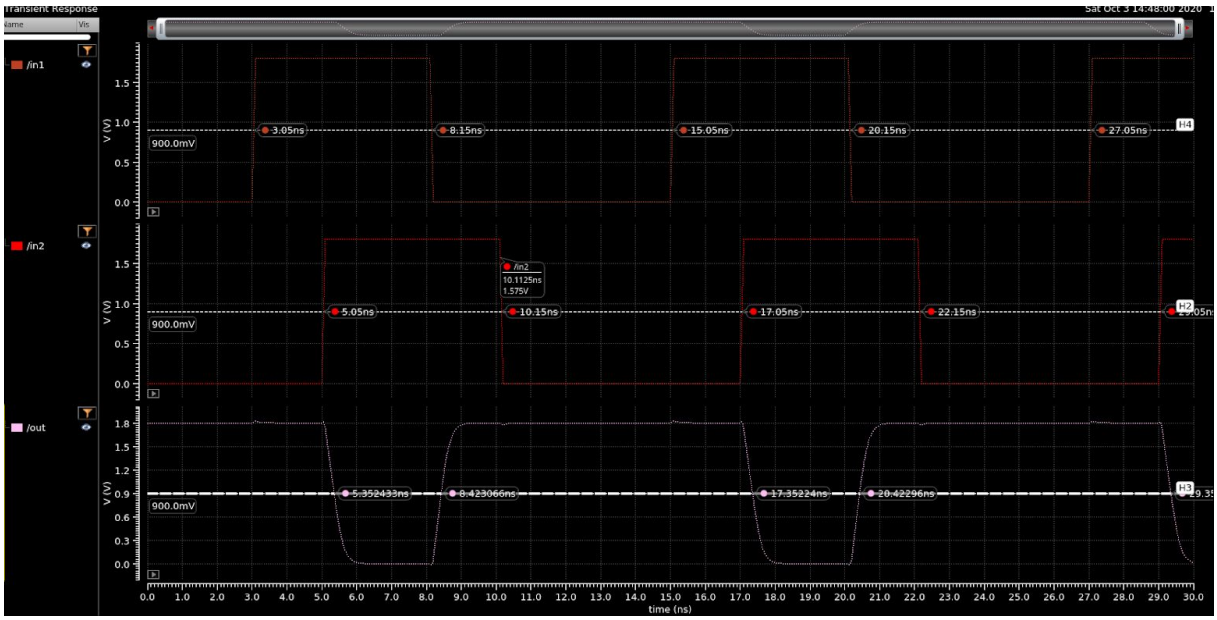
Delays

Gate	Rising Delay (ns)	Falling Delay(ns)	% Error
Inverter	0.234	0.214	8.92857
NAND	0.2924	0.2731	6.84953
XOR	0.423958	0.41072	3.172

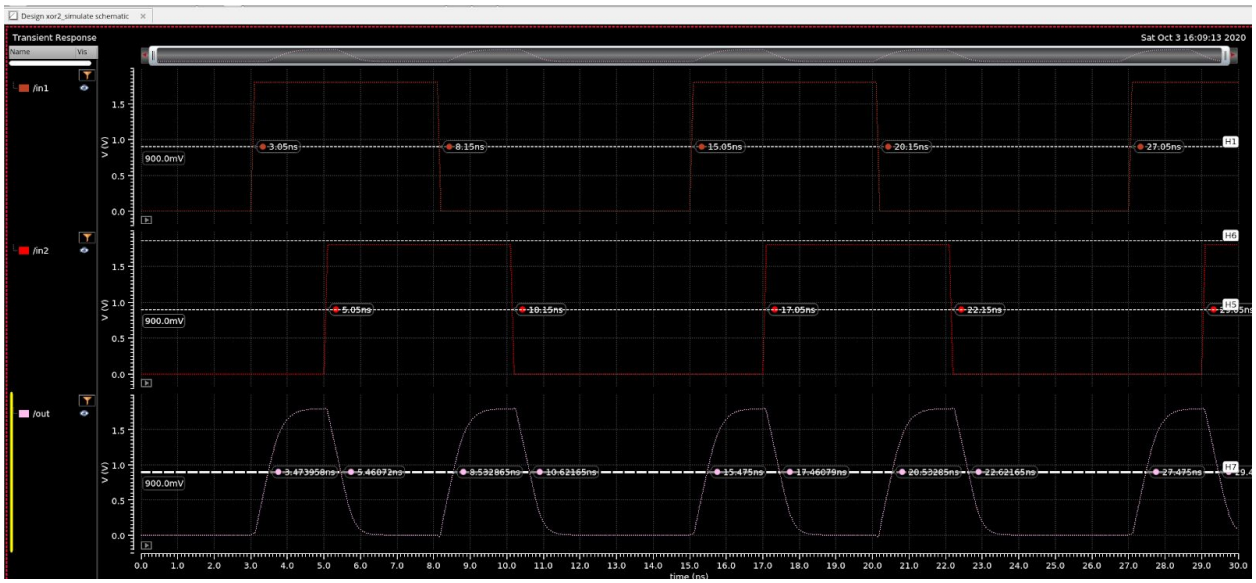
Inverter Waveform



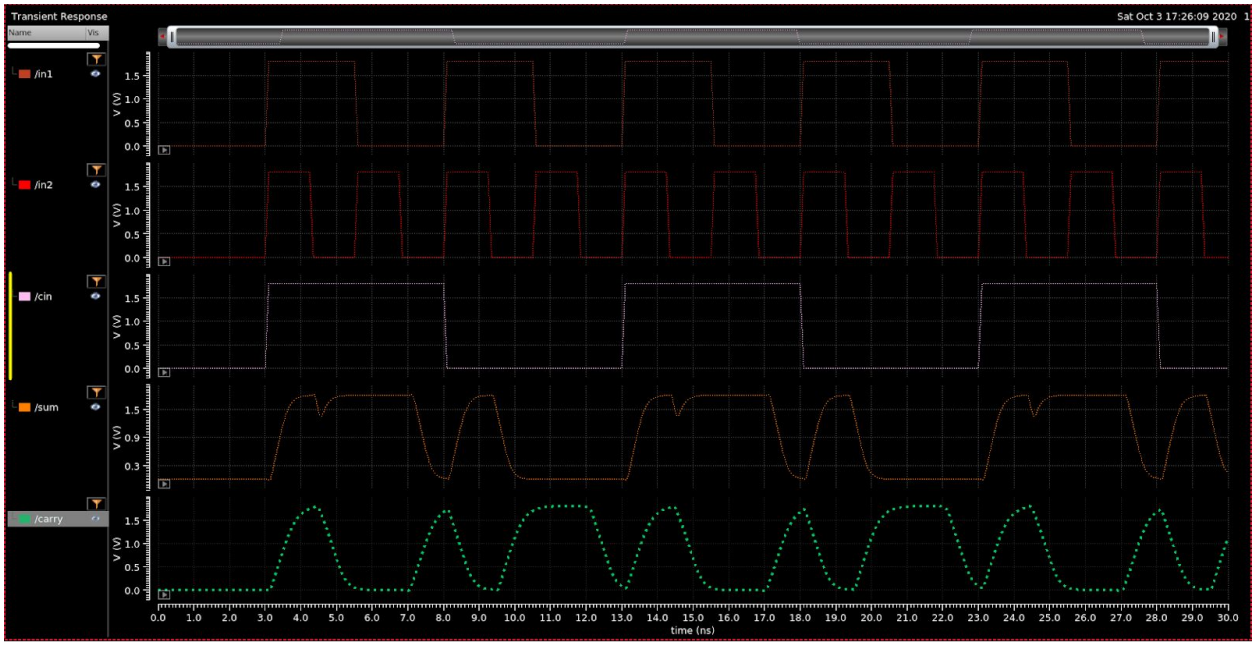
NAND Waveform



XOR Waveform



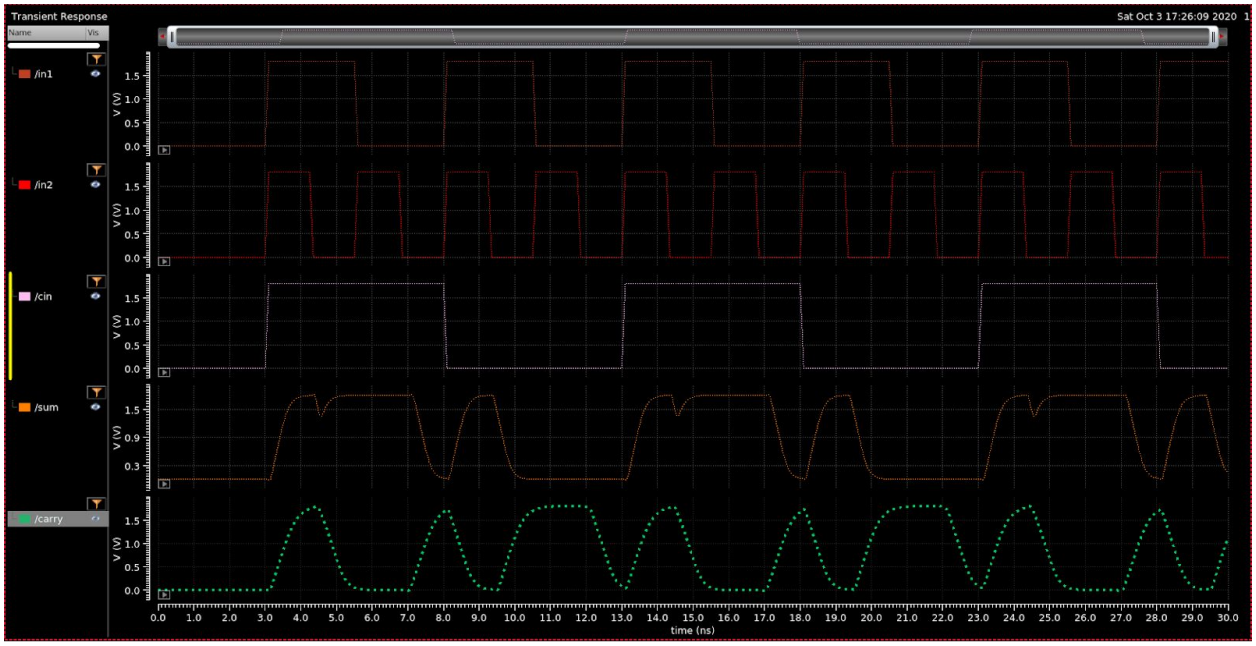
Full Adder



Power Dissipations

Gate	Voltage Source	Value
Inverter	VDD	-0.00001162
Inverter	in	-0.0000004526
NAND	VDD	-0.0000004116
NAND	in1	-0.0000001804
NAND	in2	-0.0000001671
XOR	VDD	-0.00003639
XOR	in1	-0.000000320
XOR	in2	-0.0000003334
Full Adder	VDD	-0.0001436
Full Adder	A	-0.000004268
Full Adder	B	-0.000000008149
Full Adder	Cin	-0.00000001195

Maximum Frequency



Period: 13ns
Max Frequency: 77 MHz