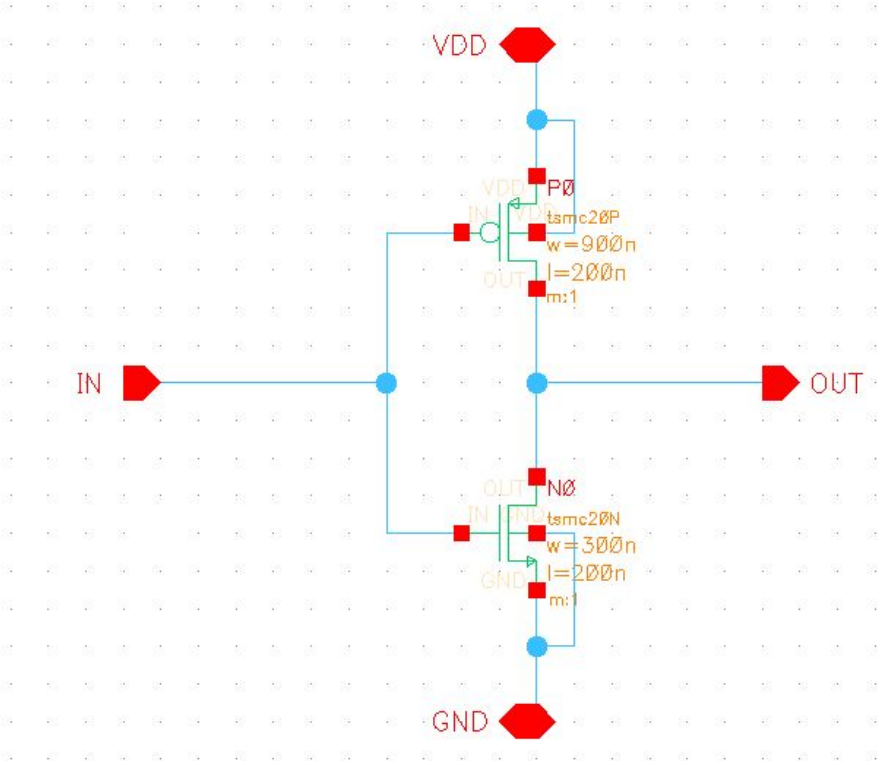
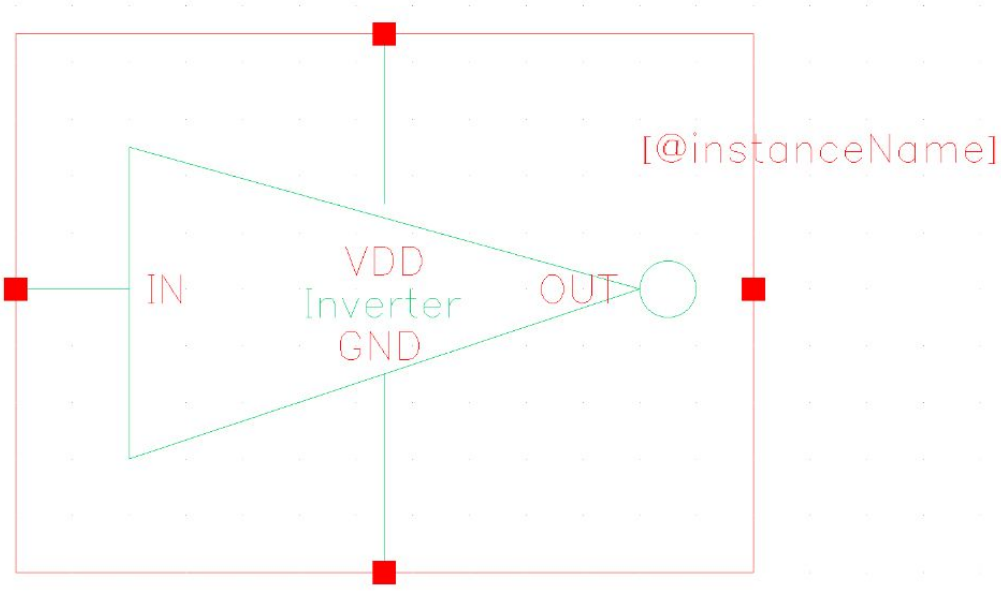
Khoa Diep
Lab 2

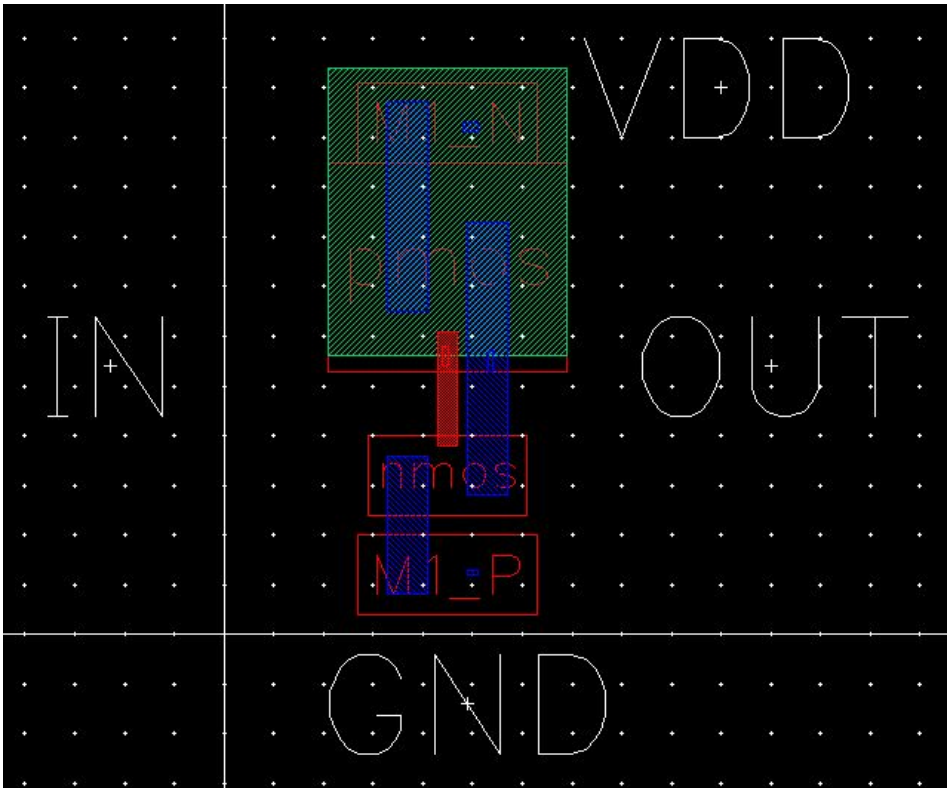
Inverter Schematic



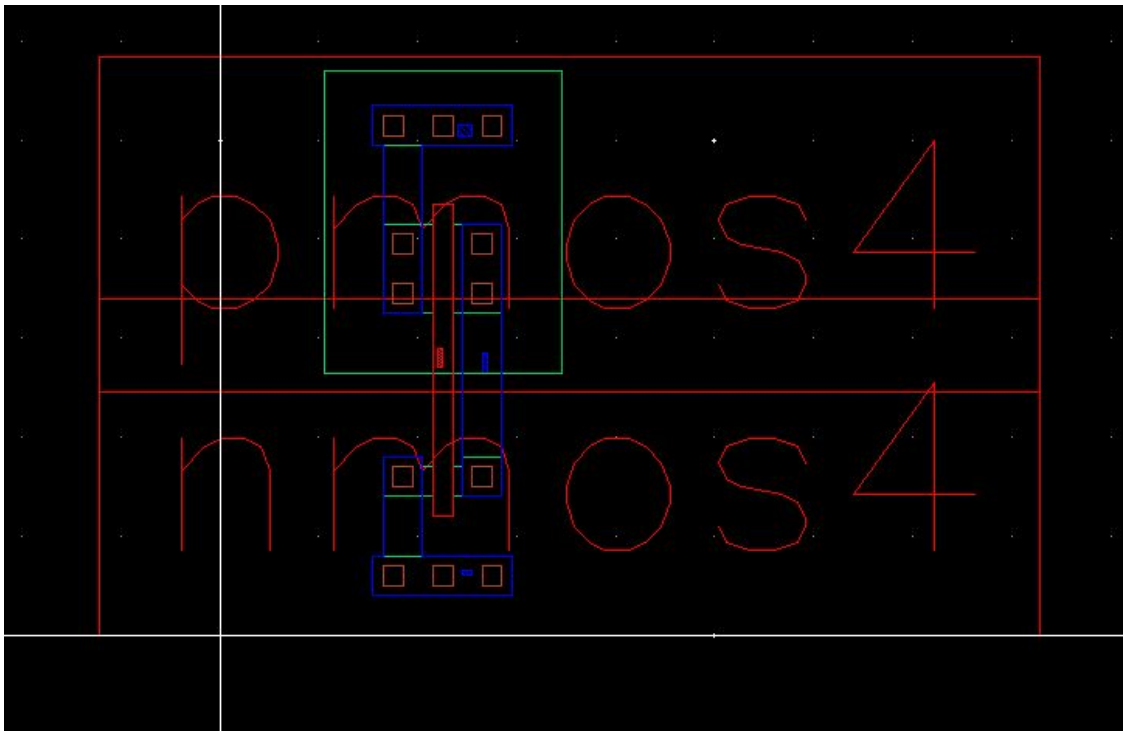
Inverter Symbol



Inverter Layout



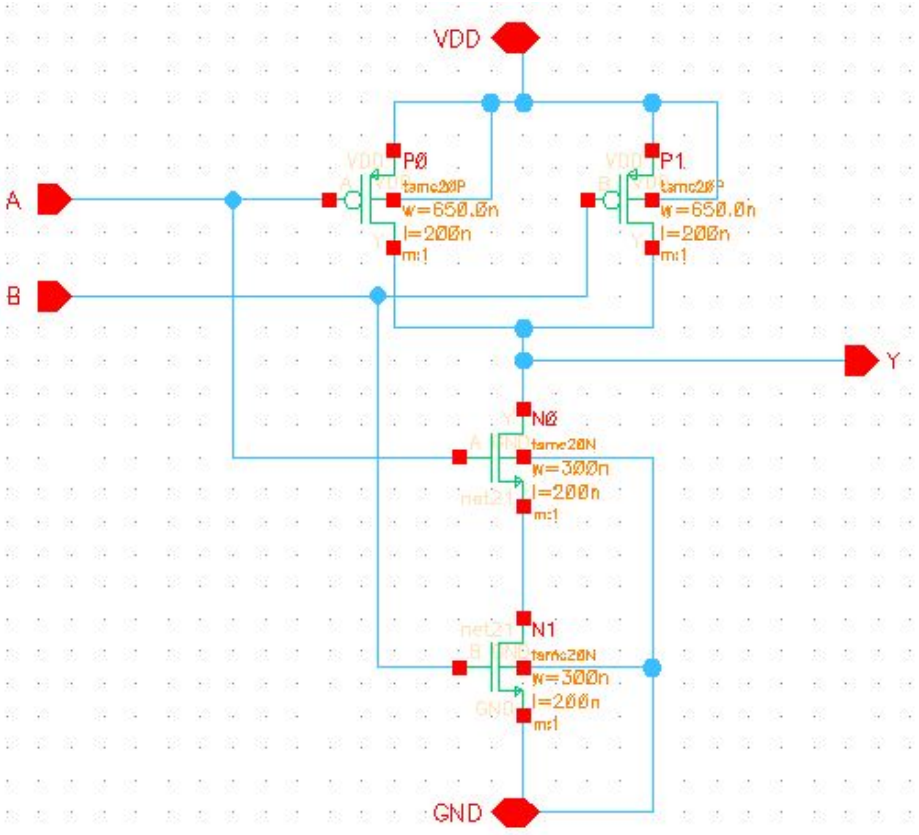
Inverter Extracted



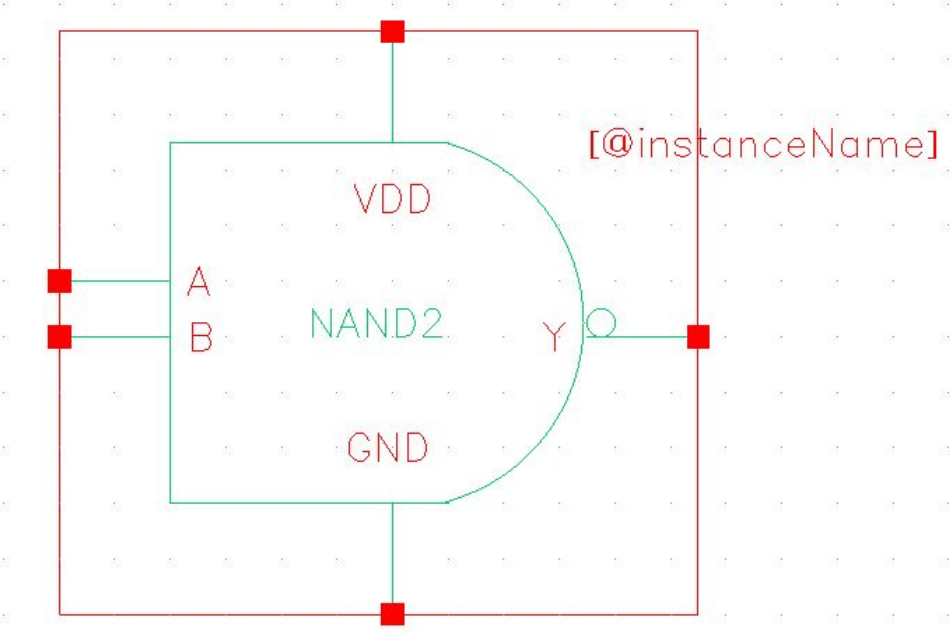
Inverter LVS output file

```
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/k/khoadiep/LVS -l -s -t /home/ugrads/k/khoadiep/LVS/layout /home/ugrads/k/khoadiep/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/k/khoadiep/LVS/layout/netlist
       count
         4               nets
         4               terminals
         1               pmos
         1               nmos

    Net-list summary for /home/ugrads/k/khoadiep/LVS/schematic/netlist
       count
         4               nets
         4               terminals
         1               pmos
         1               nmos


    Terminal correspondence points
    N0          N1          GND
    N2          N0          IN
    N1          N3          OUT
    N3          N2          VDD

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   2       2
        total                    2       2

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   4       4
        total                    4       4

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    4       4
```

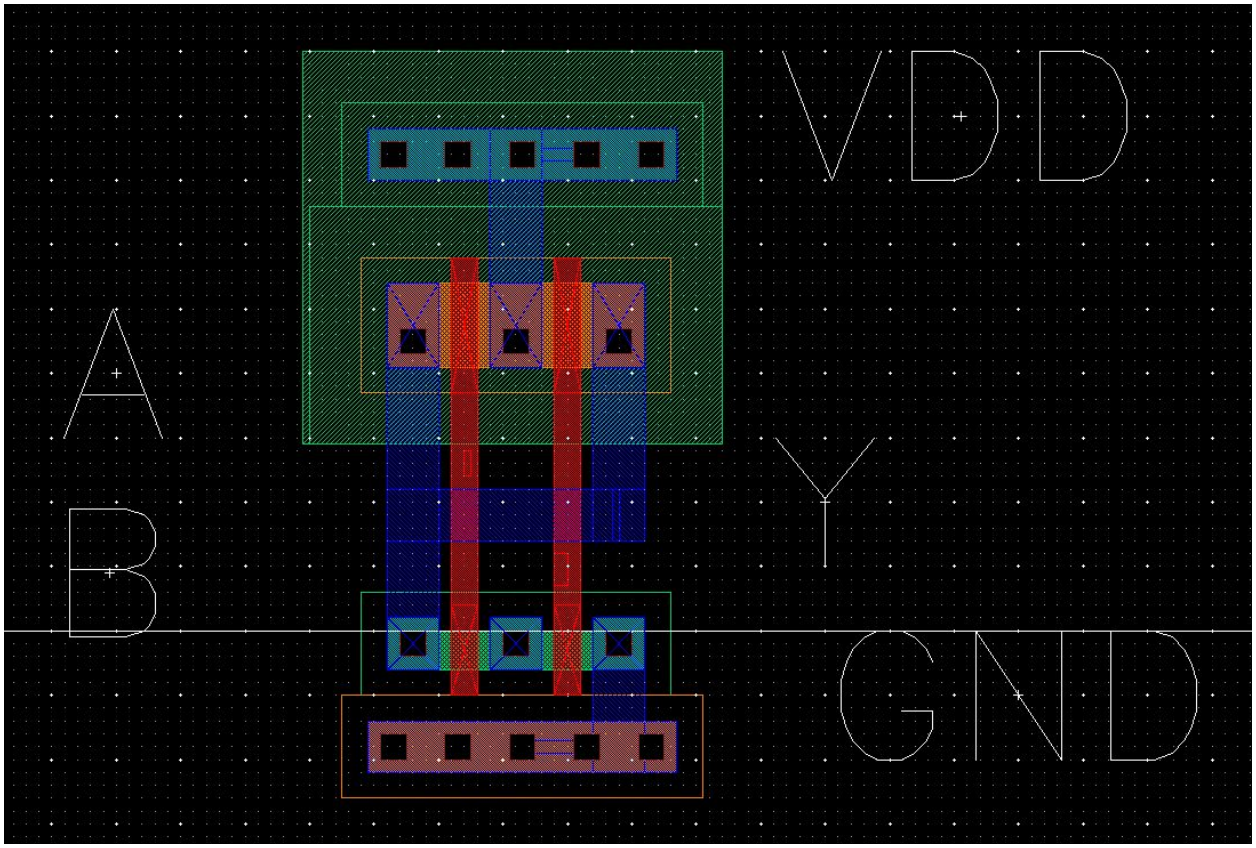
NAND Schematic



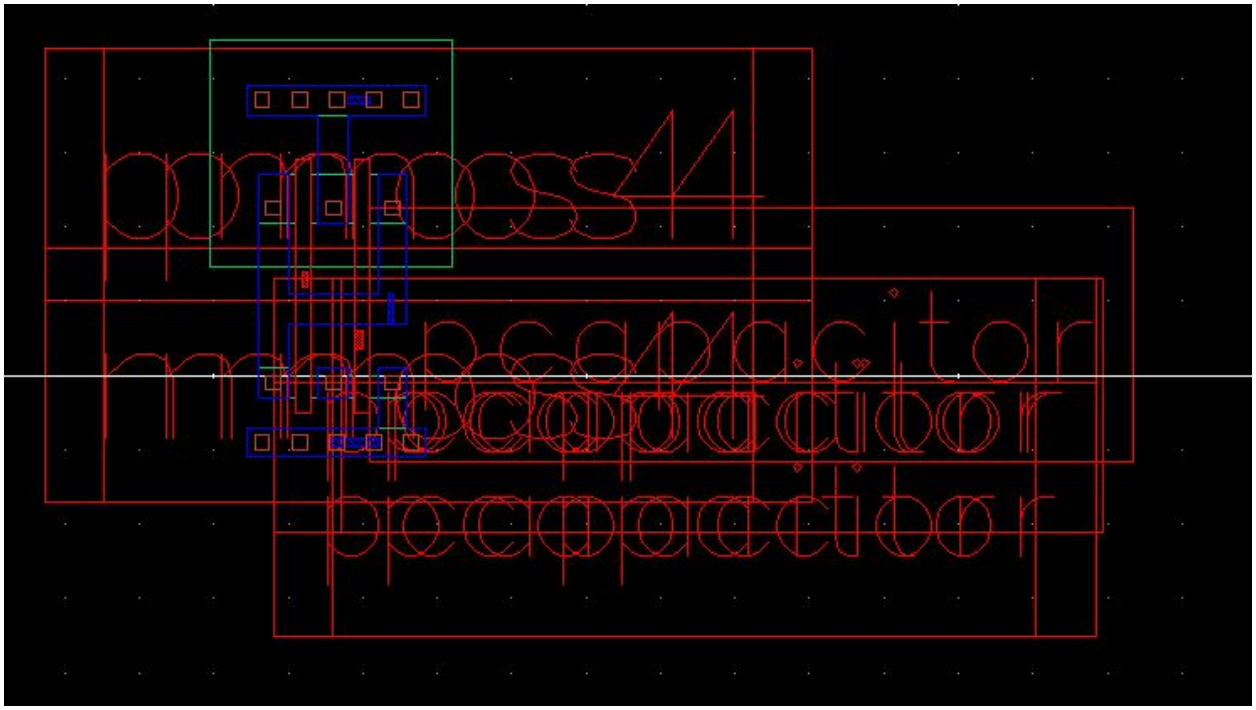
NAND Symbol



NAND Layout



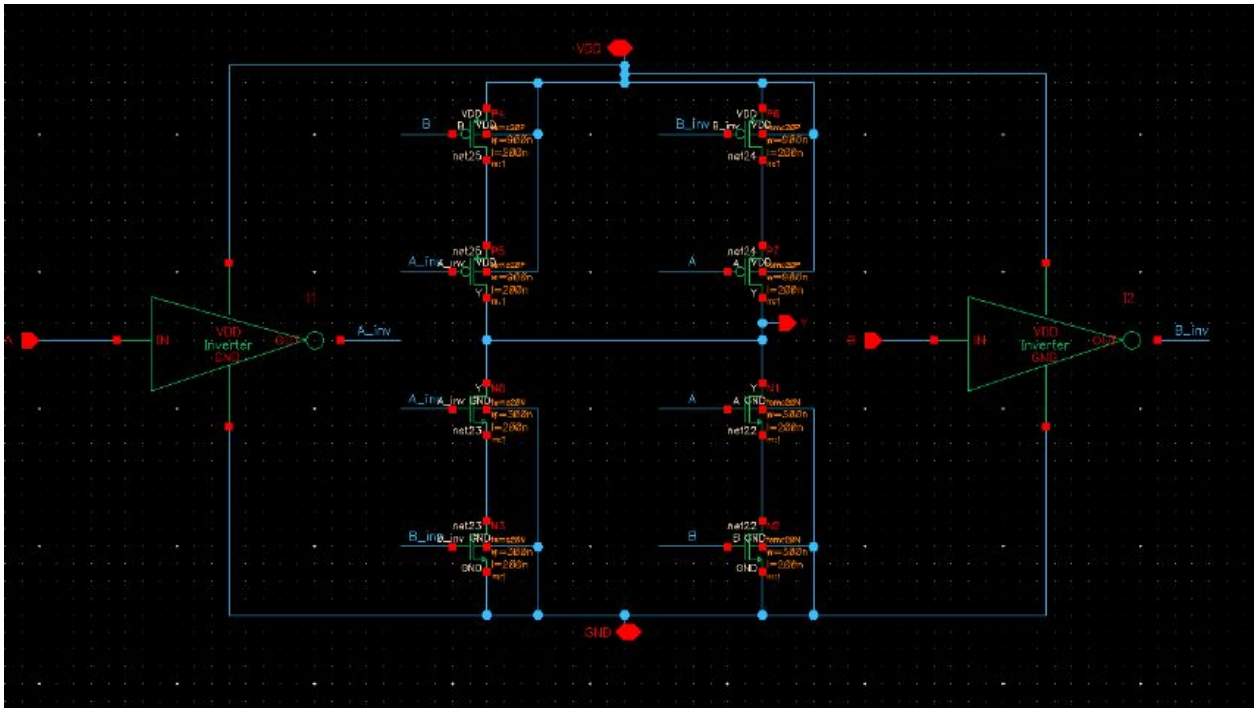
NAND Extracted



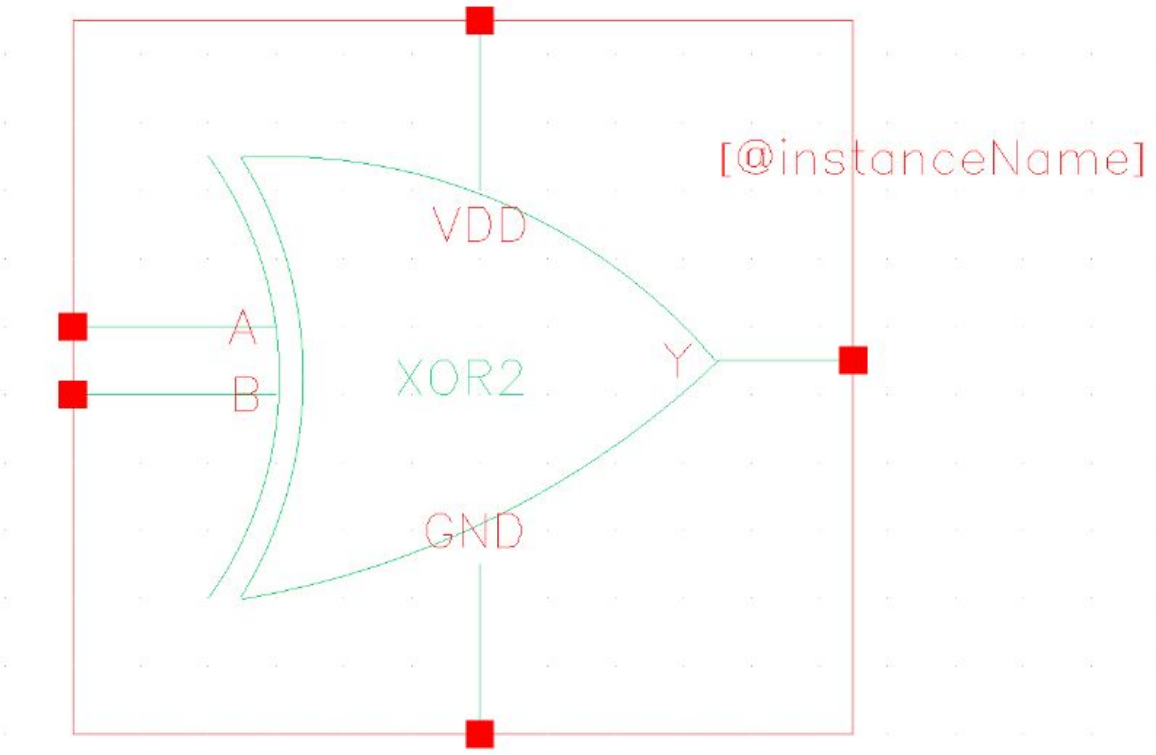
NAND LVS output file

```
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/k/khoadiep/LVS -l -s -t /home/ugrads/k/khoadiep/LVS/layout /home/ugrads/k/khoadiep/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/k/khoadiep/LVS/layout/netlist
       count
         6               nets
         5               terminals
         2               pmos
         2               nmos

    Net-list summary for /home/ugrads/k/khoadiep/LVS/schematic/netlist
       count
         6               nets
         5               terminals
         2               pmos
         2               nmos


    Terminal correspondence points
    N4          N1          A
    N3          N5          B
    N2          N0          GND
    N5          N4          VDD
    N1          N2          Y

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   4       4
        total                    4       4

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   6       6
        total                    6       6

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    5       5


Probe files from /home/ugrads/k/khoadiep/LVS/schematic
```

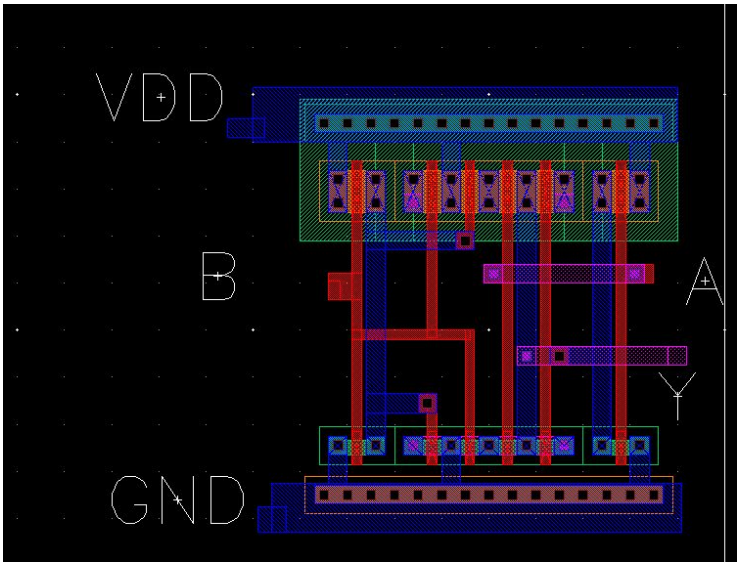
XOR Schematic



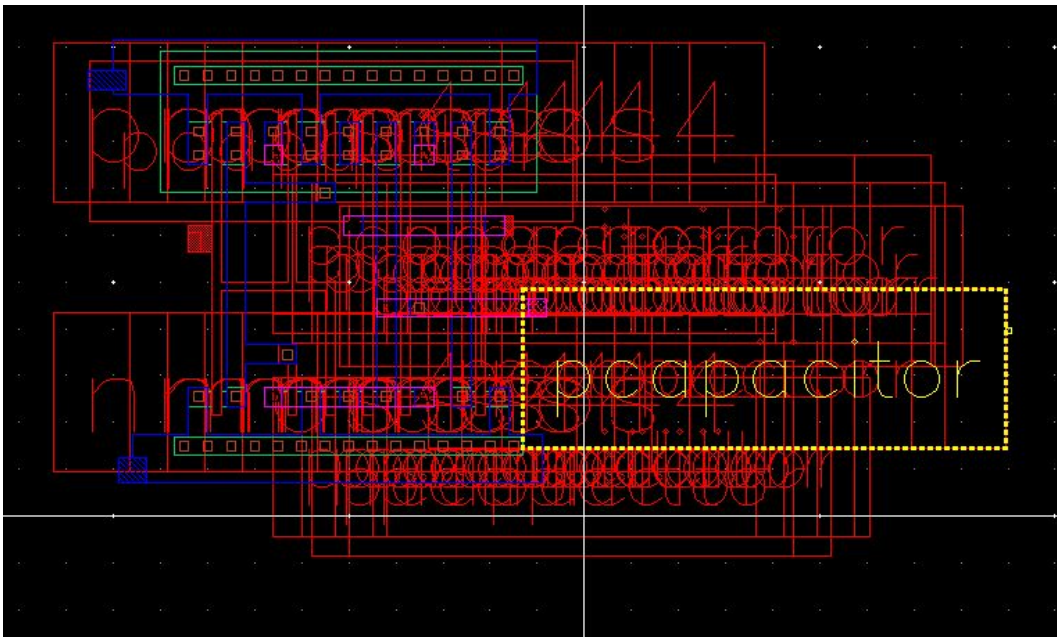
XOR Symbol



XOR Layout



XOR Extracted



XOR LVS output file

```
Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/k/khoadiep/LVS -l -s -t /home/ugrads/k/khoadiep/LVS/layout /home/ugrads/k/khoadiep/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/k/khoadiep/LVS/layout/netlist
       count
        11              nets
        5               terminals
        6               pmos
        6               nmos

    Net-list summary for /home/ugrads/k/khoadiep/LVS/schematic/netlist
       count
        11              nets
        5               terminals
        6               pmos
        6               nmos


    Terminal correspondence points
    N12         N3          A
    N11         N6          B
    N10         N10         GND
    N13         N5          VDD
    N9          N0          Y

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   12      12
        total                    12      12

                                   nets
        un-matched               11      11
        merged                   0       0
        pruned                   0       0
        active                   11      11
        total                    11      11
```