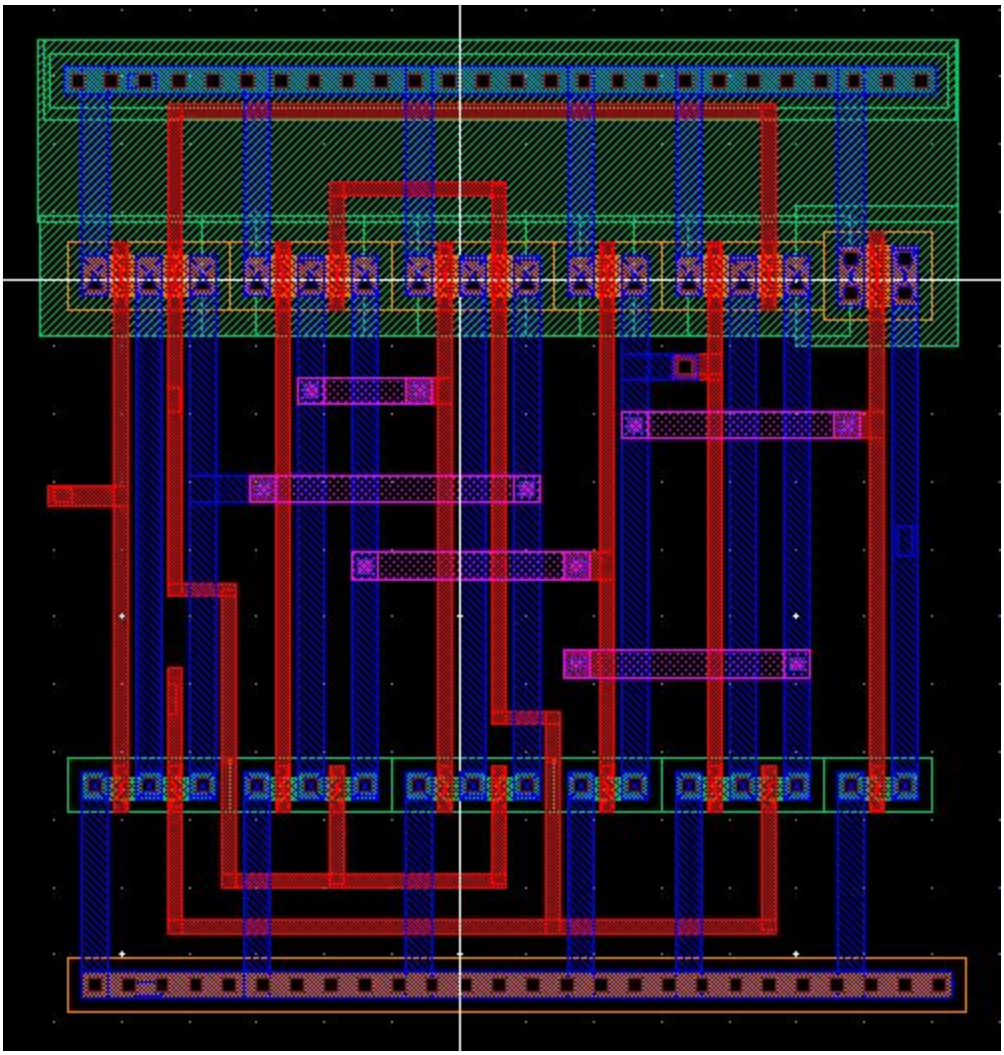
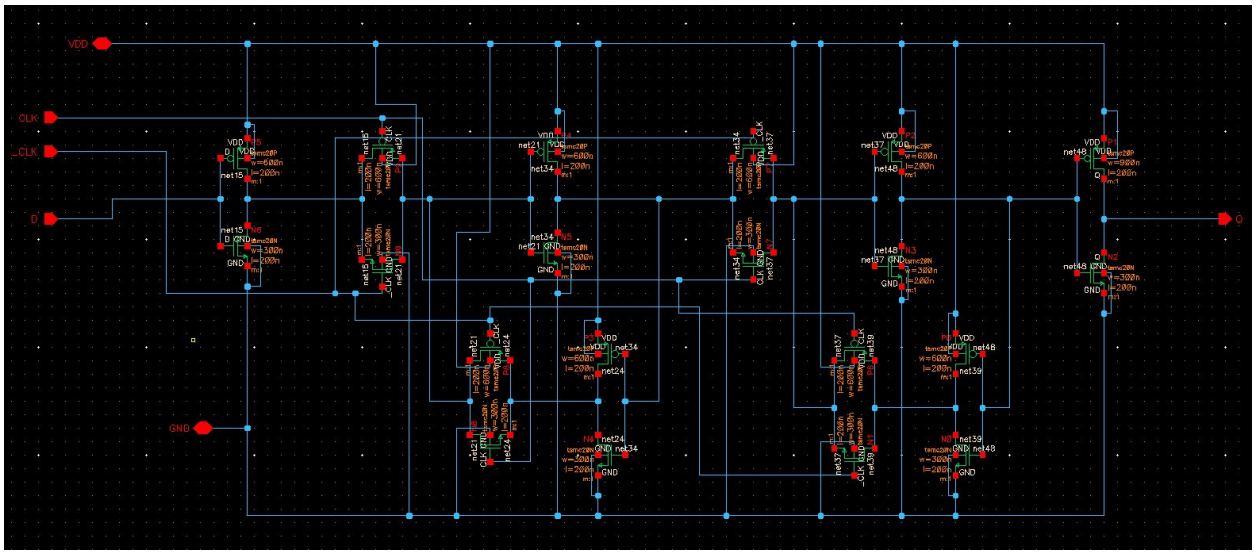
Khoa Diep
Lab 6
10/21/2020

Flip Flop Layout



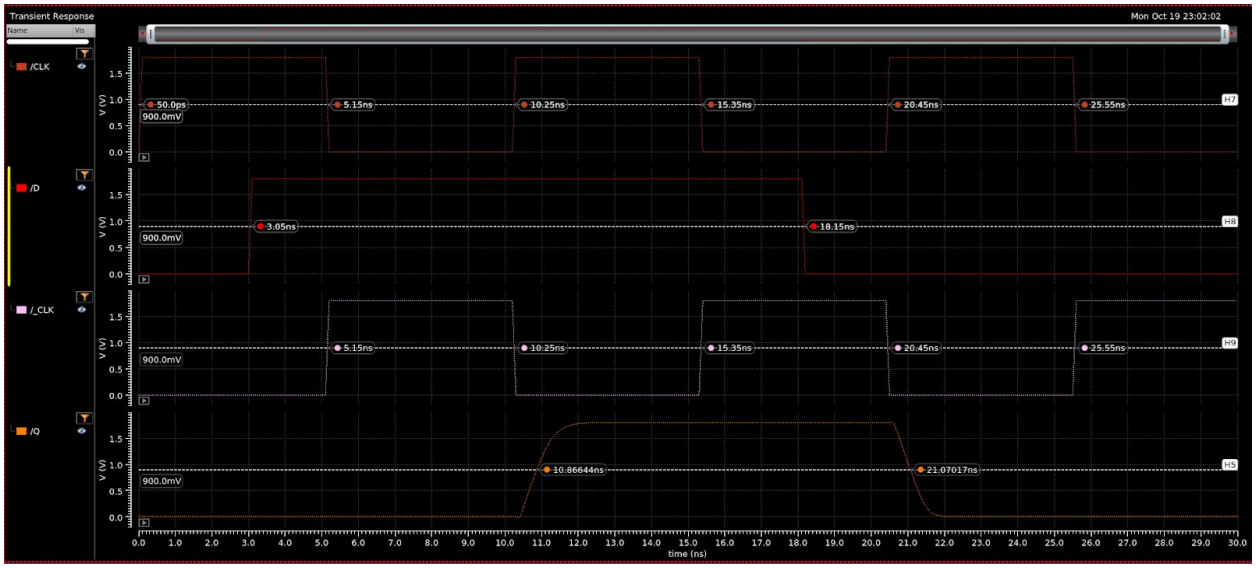
Flip flop schematic



LVS

```
    Net-list summary for /home/ugrads/k/khoadiep/cadence/LVS/schematic/netlist
       count
         13              nets
         6               terminals
         10              pmos
         10              nmos


    Terminal correspondence points
    N10         N3          CLK
    N11         N11         D
    N7          N1          GND
    N8          N2          Q
    N12         N4          VDD
    N9          N0          _CLK

)evices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   20      20
        total                    20      20

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   13      13
        total                    13      13

                                 terminals
        un-matched               0       0
        matched but
        different type           0       0
        total                    6       6
```

Waveform

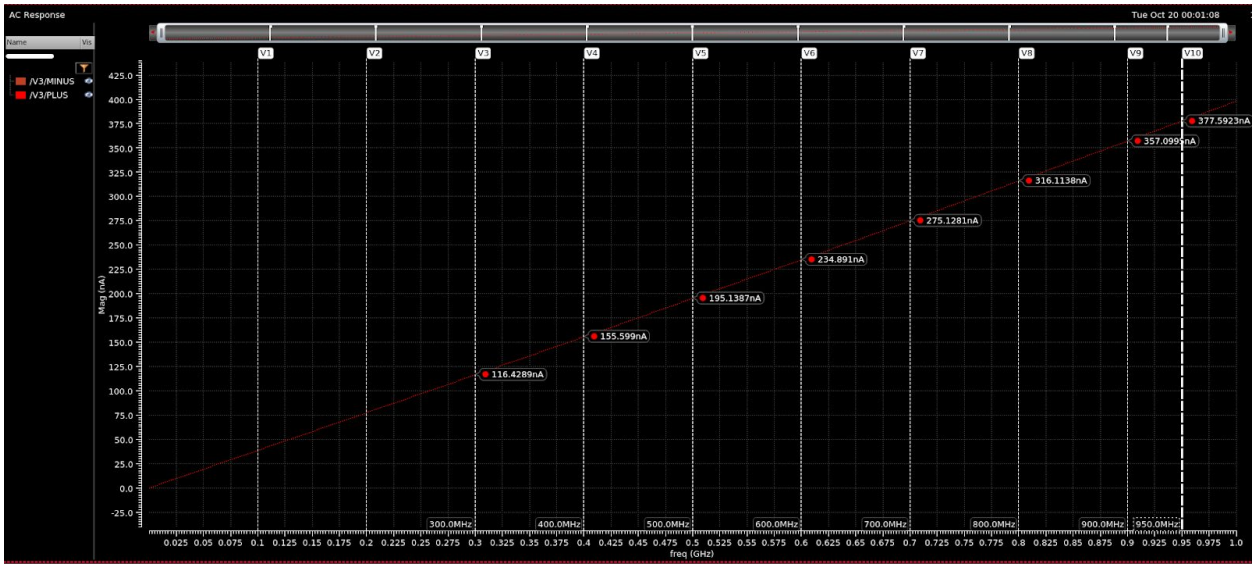


Rising Delay of Q = 0.6164ns
Falling Delay of Q = 0.6202ns
% Error = 0.613%

Delay and Load Capacitance

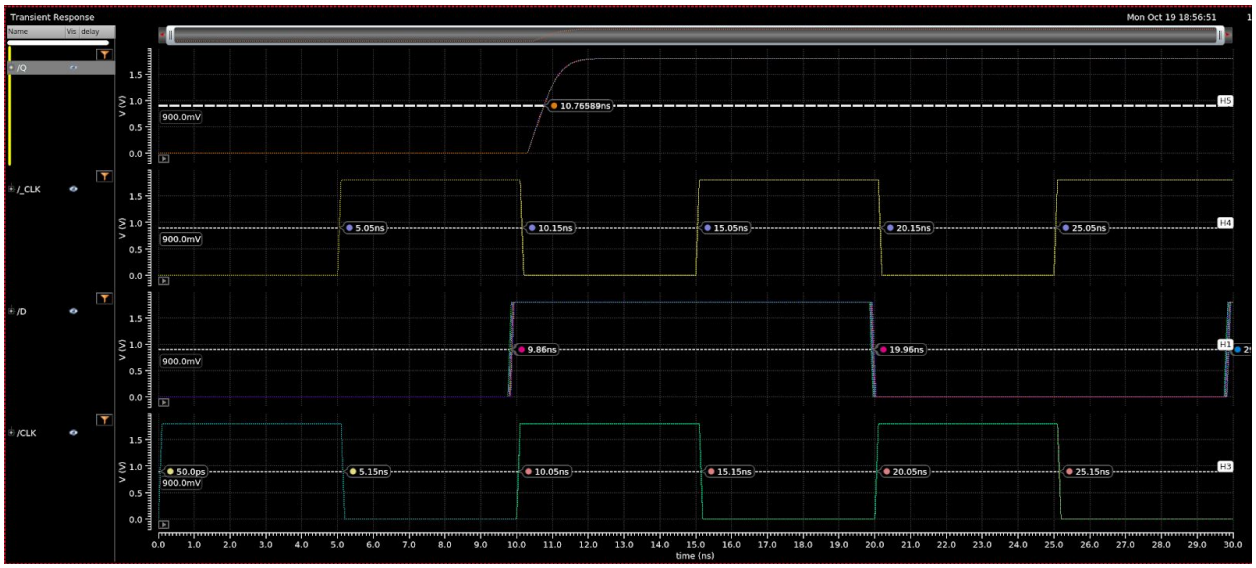
Capacitance (F)	Rising Delay (ns)	Falling Delay (ns)	% Error
1	0.1726	0.1688	2.201622248
5	0.1945	0.1949	0.205233453
10	0.2184	0.2211	1.221166893
25	0.2858	0.2899	1.414280786
40	0.352	0.3561	1.151361977
65	0.4622	0.4659	0.794161837
80	0.5283	0.532	0.695488722
90	0.5721	0.5756	0.608061154
95	0.5945	0.5977	0.535385645
100	0.6164	0.6202	0.612705579

AC Analysis



Frequency (MHz)	Current (nA)	Capacitance (mF)
100	38.7084	61.60633199
200	77.49314	61.66708143
300	116.4289	61.76744985
400	155.599	61.91087498
500	195.1387	62.11457739
600	234.891	62.3067729
700	275.1281	62.55428157
800	316.1138	62.88884231
900	357.0995	63.14905622
950	377.592	63.25856134
AVERAGE		**62.322383**

Setup time



setup_r = 0.12ns

setup_f = 0.26ns

Setup time is the maximum between setup_r and setup_f. Thus the Setup time is 0.26 ns