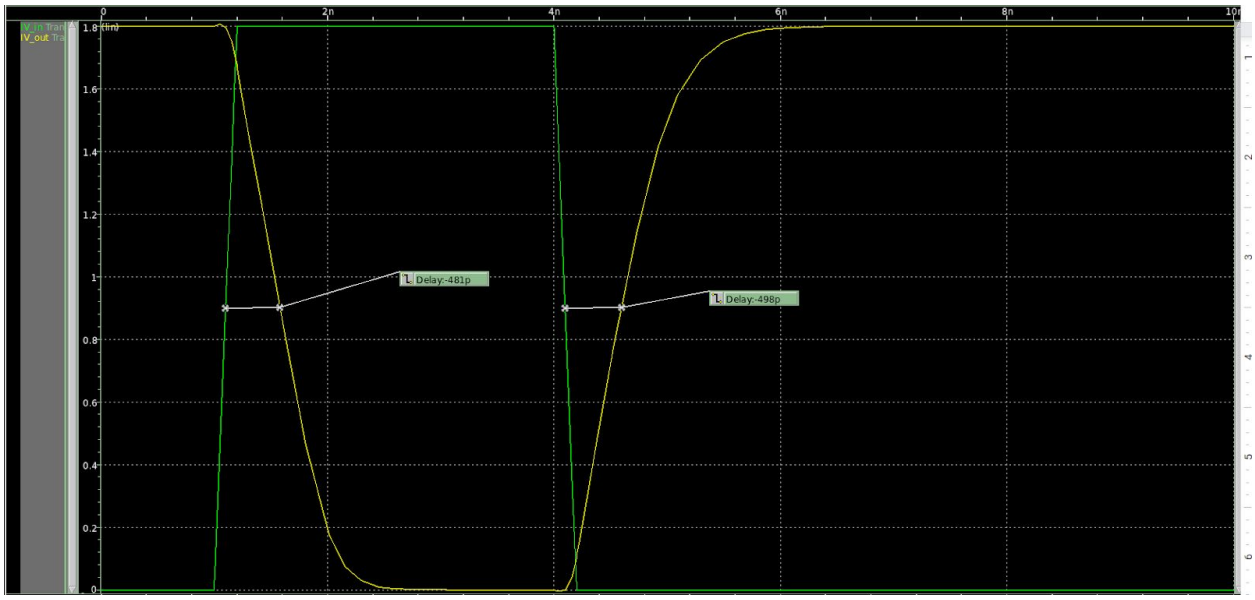
Khoa Diep
Lab 3
9/21/2020

Inverter Waveform



Rising delay: -481p
Falling delay: -498p
Difference: 17
Error: 3.47%

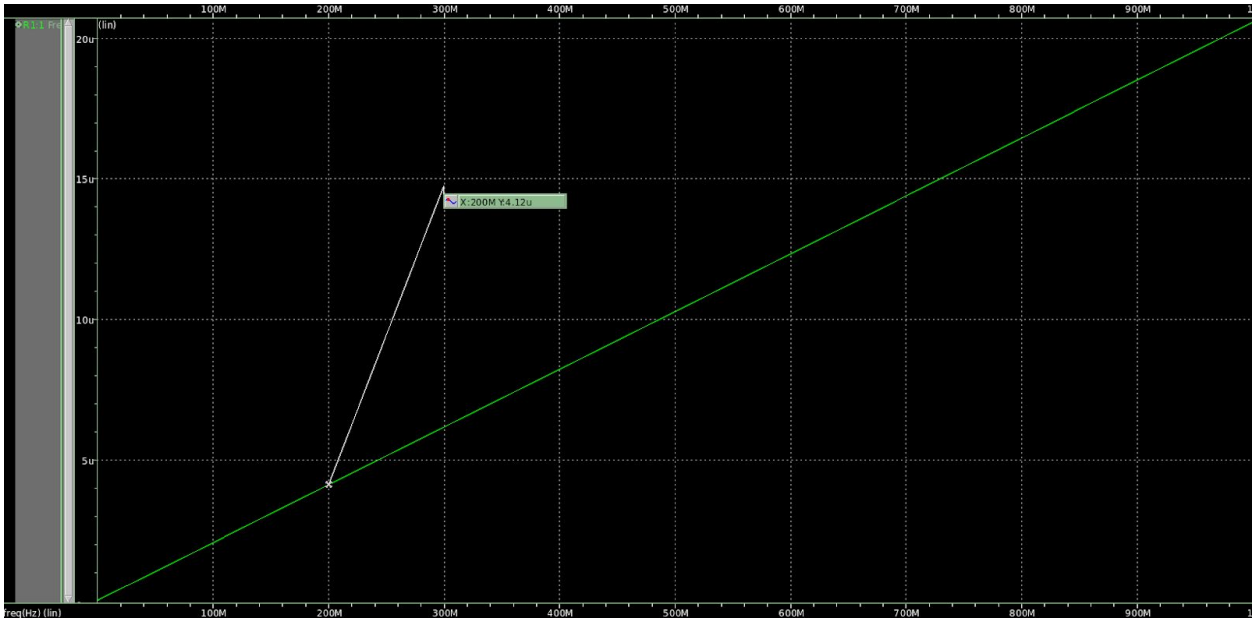
Inverter Simulation File

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

Inverter Delay Table

Capacitance	Rising Delay	Falling Delay	Error (% difference)
1	-27.1	-45.2	50.0692
10	-85.8	-101	16.2741
20	-131	-144	9.45455
25	-153	-166	8.15047
30	-175	-188	7.16253
35	-197	-210	6.38821
40	-219	-232	5.76497
50	-262	-277	5.56586
60	-306	-321	4.78469
65	-329	-345	4.74777
70	-351	-368	4.72879
75	-372	-389	4.46781
80	-393	-410	4.23412
90	-439	-451	2.69663
100	-481	-498	3.47293

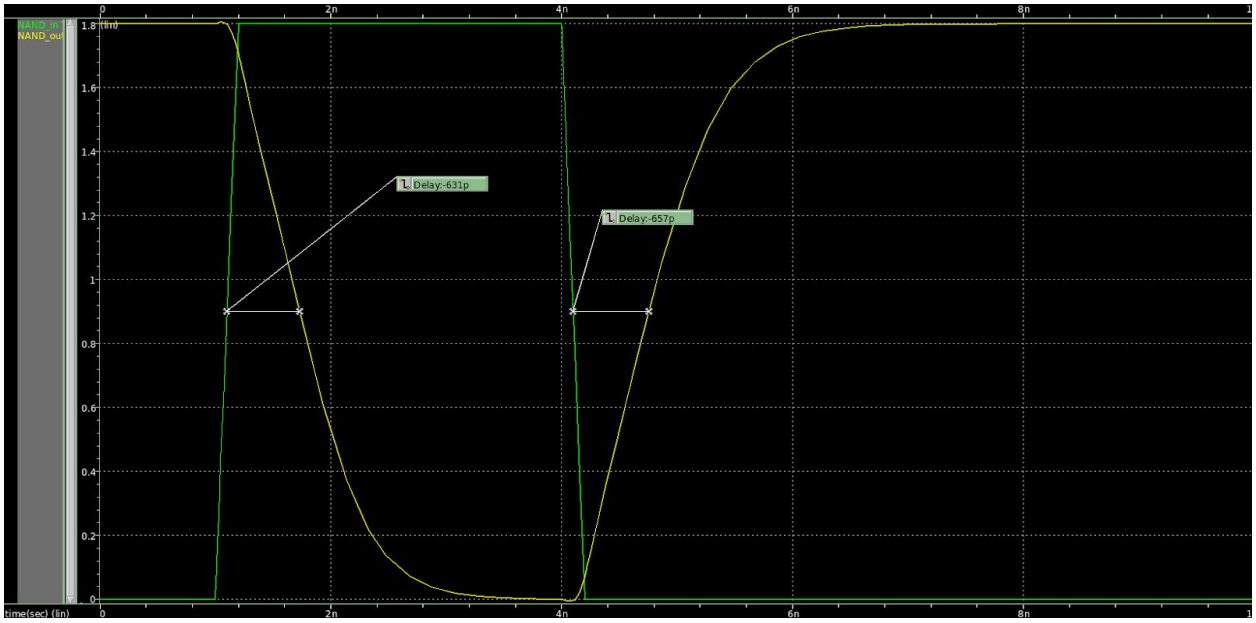
Inverter AC Waveform, Sink Capacitance, and Frequency Table



f (MHz)	If (uA)	C (nF)
100	2.06	3.278591828
150	3.08	3.267981498
200	4.12	3.278591828
250	5.16	3.284958025
300	6.17	3.273286663
350	7.2	3.274044544
400	8.23	3.274612954
500	10.3	3.278591828
600	12.3	3.262676333
750	15.4	3.267981498
900	18.5	3.271518275
Mean C		3.273894116

Sink Capacitance: = 3.273894116 nF

NAND Waveform



Rising delay: -631p
Falling delay: -657p
Difference: 26
Error: 4.03727%

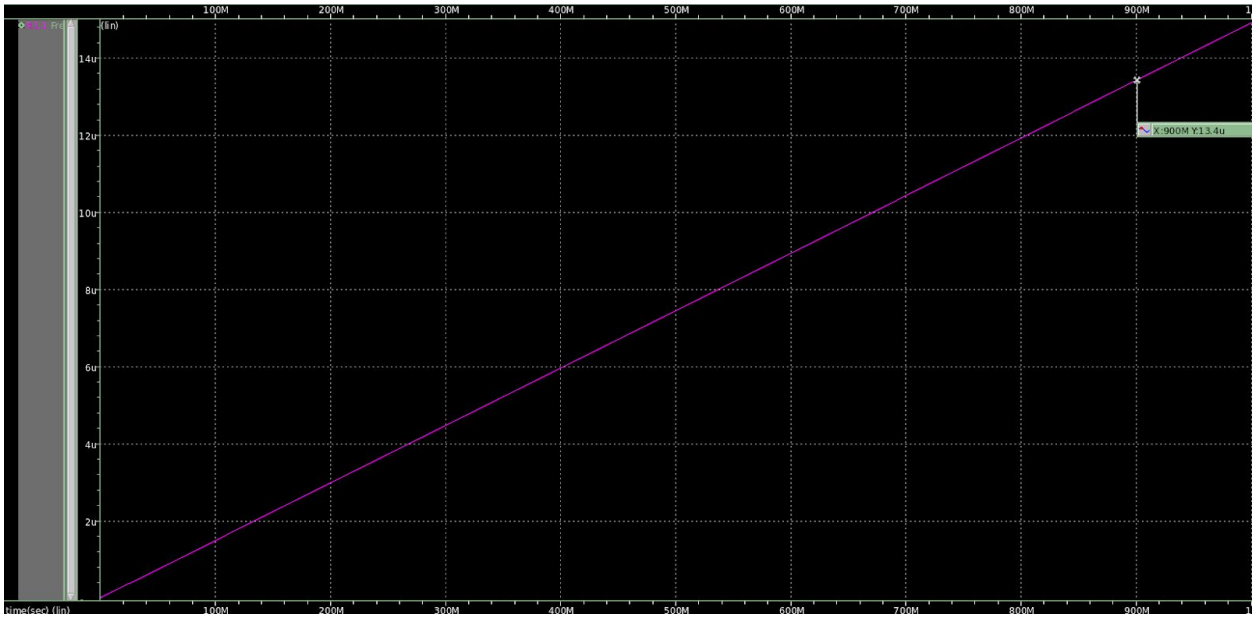
NAND Simulation File

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (NAND_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

//    A       B  output    VDD GND
X1 (NAND_in vdd NAND_out vdd gnd) NAND wp=0.65u lp=0.2u wn=0.3u ln=0.2u

R1 (NAND_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND_in NAND_out
```

NAND Delay Table

Capacitance	Rising Delay	Falling Delay	Error (% difference)
1	-35.5	-56	44.80874317
10	-105	-121	14.15929204
20	-163	-180	9.912536443
25	-193	-209	7.960199005
30	-222	-239	7.37527115
35	-252	-269	6.525911708
40	-280	-299	6.563039724
50	-341	-360	5.420827389
60	-398	-420	5.378973105
65	-427	-448	4.8
70	-457	-477	4.282655246
75	-487	-507	4.024144869
80	-516	-538	4.174573055
90	-574	-597	3.928266439
100	-631	-657	4.037267081

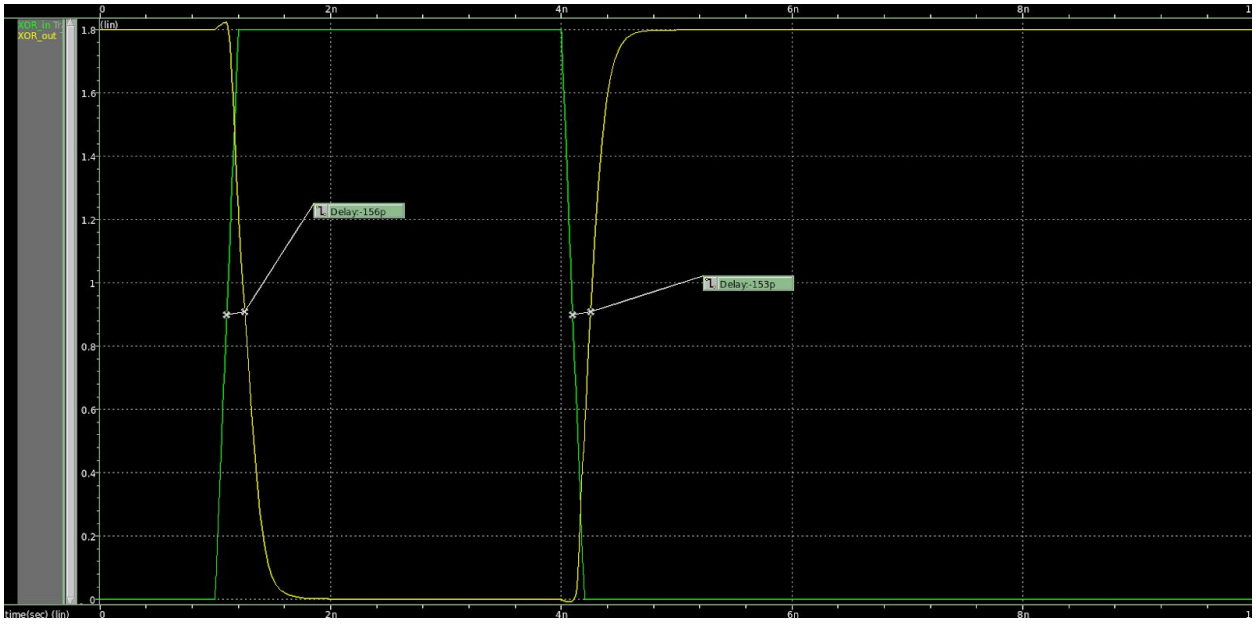
NAND AC Waveform, Sink Capacitance, and Frequency Table



f (MHz)	If (uA)	C (nF)
100	1.49	2.371408652
150	2.23	2.366103487
200	2.98	2.371408652
250	3.74	2.380957949
300	4.47	2.371408652
350	5.22	2.373682294
400	5.97	2.375387526
500	7.45	2.371408652
600	8.95	2.374061234
750	11.2	2.376713817
900	13.4	2.369640264
Mean Cap.		2.373254092

Sink Capacitance: = 2.373254092 nF

XOR Waveform



Rising delay: -156p
Falling delay: -153p
Difference: 3
Error: 1.94%

XOR Simulation File

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/cadence/cellcharacs/model18.spi"
include "~/cadence/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XOR_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR_in vdd XOR_out vdd gnd) XOR wp=8u lp=0.2u wn=2.5u ln=0.2u

R1 (XOR_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR_in XOR_out
```

XOR Delay Table

Capacitance	Rising Delay	Falling Delay	Error (% difference)
1	-53.8	-56.6	5.072463768
10	-64	-66	3.076923077
20	-73.5	-76.4	3.869246164
25	-78.3	-81.8	4.372267333
30	-83.5	-87.1	4.220398593
35	-88.8	-92.3	3.865267808
40	-94.3	-97.4	3.234220136
50	-105	-107	1.886792453
60	-115	-116	0.8658008658
65	-120	-121	0.8298755187
70	-125	-125	0
75	-130	-130	0
80	-136	-135	0.7380073801
90	-146	-144	1.379310345
100	-156	-153	1.941747573

XOR AC Waveform, Sink Capacitance, and Frequency Table

f (MHz)	If (uA)	C (nF)
100	33.8	53.79437077
150	50.8	53.90047406
200	67.4	53.63521582
250	84.6	53.85803274
300	101	53.58216417
350	118	53.65795224
400	135	53.71479329
500	169	53.79437077
600	203	53.84742241
750	253	53.68826747
900	304	53.759003
Mean Cap.		53.74730637

Sink Capacitance: = 53.74730637 nF

cell18.spi File

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV

subckt NAND (A B output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output A VDD VDD parameters wp=0.9u lp=0.2u wn=0.3u ln=0.3u
        M2 output B VDD VDD tsmc18P w=wp l=lp
        M3 output A wire1 wire1 tsmc18N w=wn l=lp
        M4 wire1 B VSS VSS tsmc18N w=wn l=ln
ends NAND

subckt XOR (A B output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 Anot A VDD VDD tsmc18P w=wp l=lp
        M2 Anot A VSS VSS tsmc18N w=wn l=ln
        M3 Bnot B VDD VDD tsmc18P w=wp l=lp
        M4 Bnot B VSS VSS tsmc18N w=wn l=ln
        M5 wire1 B VDD VDD tsmc18P w=wp l=lp
        M6 output Anot wire1 wire1 tsmc18P w=wp l=lp
        M7 wire2 A VDD VDD tsmc18P w=wp l=lp
        M8 output Bnot wire2 wire2 tsmc18P w=wp l=lp
        M9 output Anot wire3 wire3 tsmc18N w=wn l=ln
        M10 wire3 Bnot VSS VSS tsmc18N w=wn l=ln
        M11 output B wire4 wire4 tsmc18N w=wn l=ln
        M12 wire4 A VSS VSS tsmc18N w=wn l=ln
ends XOR
```