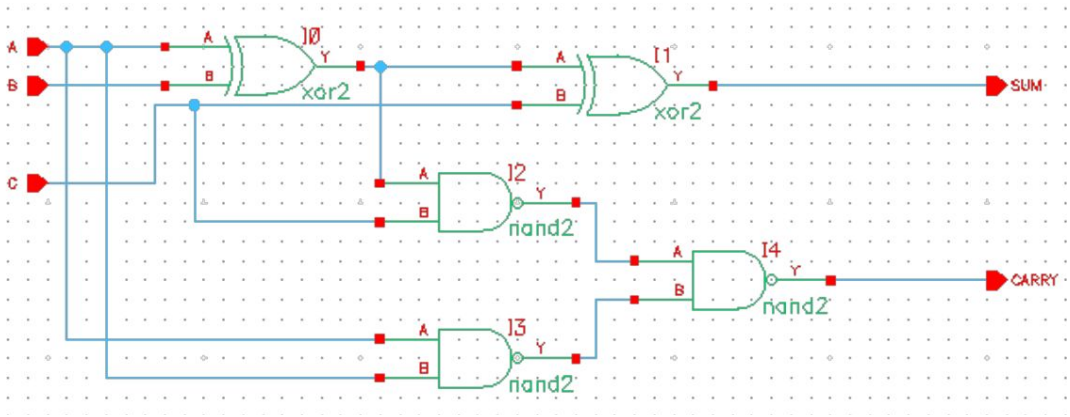
Full Adder

Schematic Design -



Schematic Symbol -

Simulation -

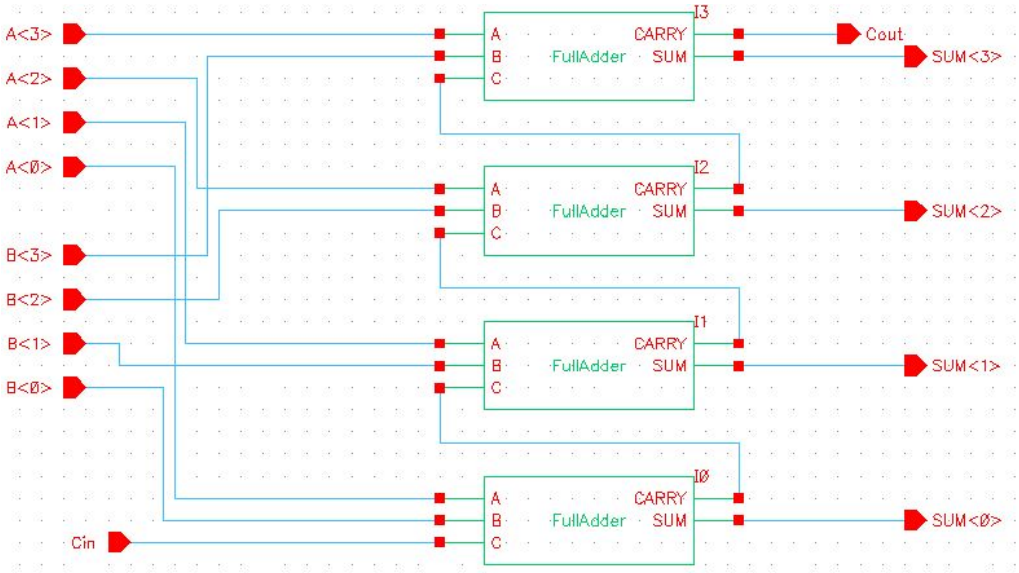
```
-----------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                   0 A=0, B=0, C=0, SUM=0, CARRY=0
                  50 A=0, B=0, C=1, SUM=1, CARRY=0
                 100 A=0, B=1, C=0, SUM=1, CARRY=0
                 150 A=0, B=1, C=1, SUM=0, CARRY=1
                 200 A=1, B=0, C=0, SUM=1, CARRY=1
                 250 A=1, B=0, C=1, SUM=0, CARRY=1
                 300 A=1, B=1, C=0, SUM=0, CARRY=1
                 350 A=1, B=1, C=1, SUM=1, CARRY=1
ncsim> run
ncsim>
```

Verilog -

```
1
2 // Verilog stimulus file.
3 // Please do not create a module in this file.
4
5
6 // Default verilog stimulus.
7
8 initial
9 $monitor ($time," A=%b, B=%b, C=%b, SUM=%b, CARRY=%b", A, B, C, SUM, CARRY);
10
11
12 initial
13 begin
14
15    A = 1'b0;
16    B = 1'b0;
17    C = 1'b0;
18
19 #50 A=1'b0; B=1'b0; C=1'b1;   //ABC=001
20 #50 A=1'b0; B=1'b1; C=1'b0;   //ABC=010
21 #50 A=1'b0; B=1'b1; C=1'b1;   //ABC=011
22 #50 A=1'b1; B=1'b0; C=1'b0;   //ABC=100
23 #50 A=1'b1; B=1'b0; C=1'b1;   //ABC=101
24 #50 A=1'b1; B=1'b1; C=1'b0;   //ABC=110
25 #50 A=1'b1; B=1'b1; C=1'b1;   //ABC=111
26 end
```

4 bit Adder

Schematic Design -



Schematic Symbol -

Simulation -

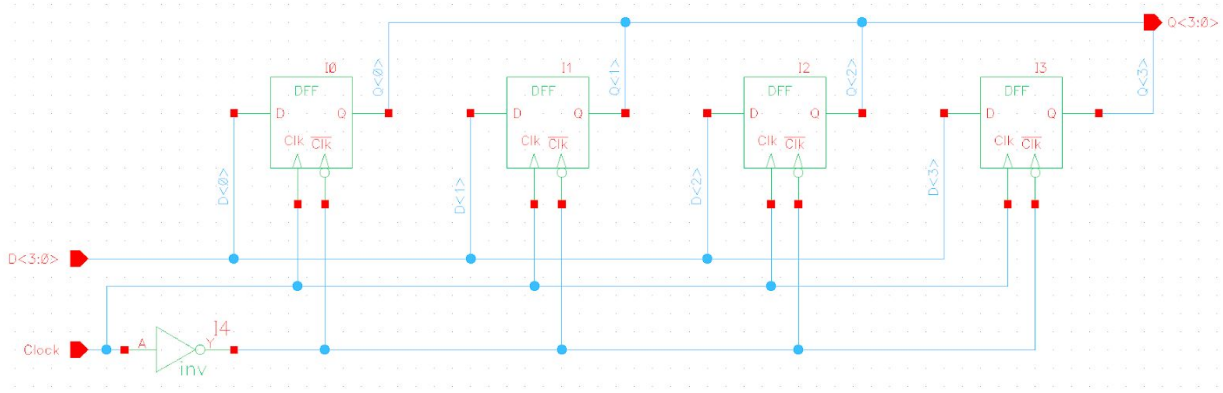
```
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                   0 A=0000, B=0000, Cin=0, Sum=0000, Cout=0
                  50 A=1111, B=1111, Cin=0, Sum=1110, Cout=1
                 100 A=1010, B=1010, Cin=1, Sum=0101, Cout=1
                 150 A=0101, B=0101, Cin=1, Sum=1011, Cout=0
```

Verilog -

```
1
2  // Verilog stimulus file.
3  // Please do not create a module in this file.
4
5
6  // Default verilog stimulus.
7  initial
8  $monitor ($time," A=%b, B=%b, Cin=%b, Sum=%b, Cout=%b", A, B, Cin, Sum, Cout);
9
10
11 initial
12 begin
13
14    A[3:0] = 4'b0000;
15    B[3:0] = 4'b0000;
16    Cin = 1'b0;
17
18 #50 A=4'b1111; B=4'b1111; Cin=1'b0;
19 #50 A=4'b1010; B=4'b1010; Cin=1'b1;
20 #50 A=4'b0101; B=4'b0101; Cin=1'b1;
21 end
22
```

4 bit Register

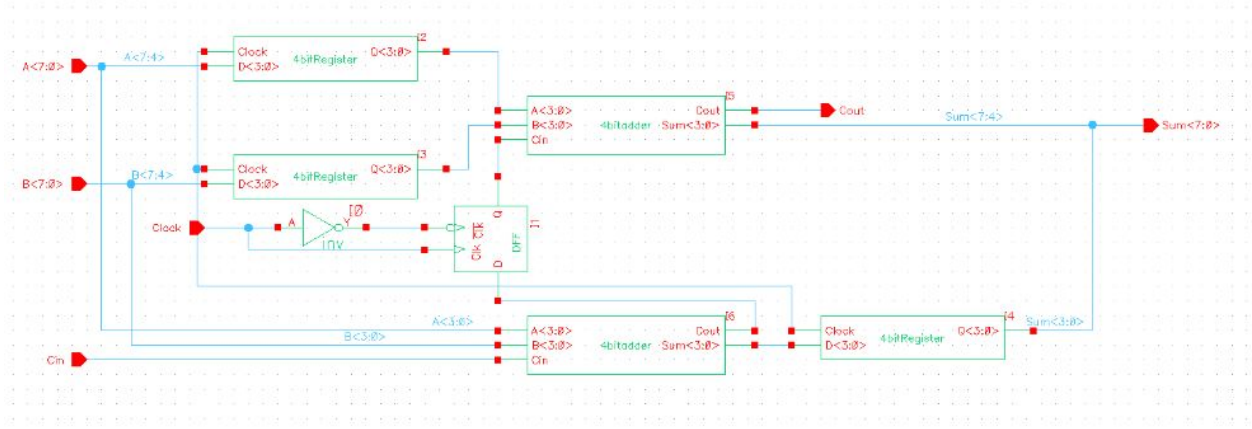
Schematic Design -



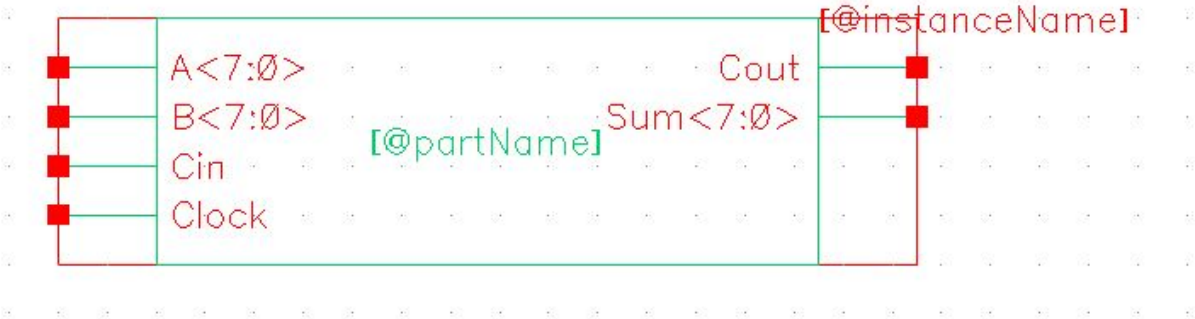
Schematic Symbol -

8 bit Adder

Schematic Design -



Schematic Symbol -



Simulation -

```
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                   0 A=00000000, B=00000000, Cin=0, Sum=xxxxxxxx, Cout=x
                  50 A=01111110, B=11100111, Cin=0, Sum=01100101, Cout=1
                 100 A=11111111, B=00000000, Cin=1, Sum=00000000, Cout=1
                 150 A=10101010, B=01010101, Cin=0, Sum=11111111, Cout=0
                 200 A=10101010, B=01010101, Cin=1, Sum=00000000, Cout=1
                 250 A=11001100, B=00110011, Cin=0, Sum=11111111, Cout=0
                 300 A=11001100, B=00110011, Cin=1, Sum=00000000, Cout=1
```

Verilog -

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.
always
#50 Clock = !Clock;

initial
$monitor ($time," A=%b, B=%b, Cin=%b, Sum=%b, Cout=%b", A, B, Cin, Sum, Cout);

initial
begin
   A[7:0] = 8'b00000000;
   B[7:0] = 8'b00000000;
   Cin = 1'b0;
   Clock = 1'b0;

#50 A=8'b01111110; B=8'b11100111; Cin=1'b0;
#50 A=8'b11111111; B=8'b00000000; Cin=1'b1;
#50 A=8'b10101010; B=8'b01010101; Cin=1'b0;
#50 A=8'b10101010; B=8'b01010101; Cin=1'b1;
#50 A=8'b11001100; B=8'b00110011; Cin=1'b0;
#50 A=8'b11001100; B=8'b00110011; Cin=1'b1;

#50 $finish;
end
```