CS203 LAB 6 REPORT

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Problem Statements of Lab 6

- 8-bit universal shift register with serial as well as parallel input, parallel output.
- 4-bit adder (input two numbers of 4 bits and carry. Output 4-bit sum and carry)
- 8 to 1 multiplexer (input 8 data inputs, 3 control inputs, one output)

Problem Statements of Lab 5

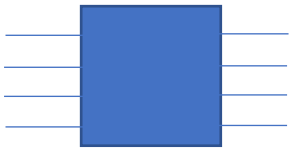
8-bit universal shift register with serial as well as parallel input, parallel output.

LAB 6 CIRCUIT

In Implementing the logics in lab 6:

- 24 Logic Tiles of 5 input 1 output
- 19 Switch Boxes of 4 inputs and 4 outputs

In the following figure



This denotes a switch box

This denotes a logic tile

CS203 LAB 6 IMPLEMENTATION CIRCUIT

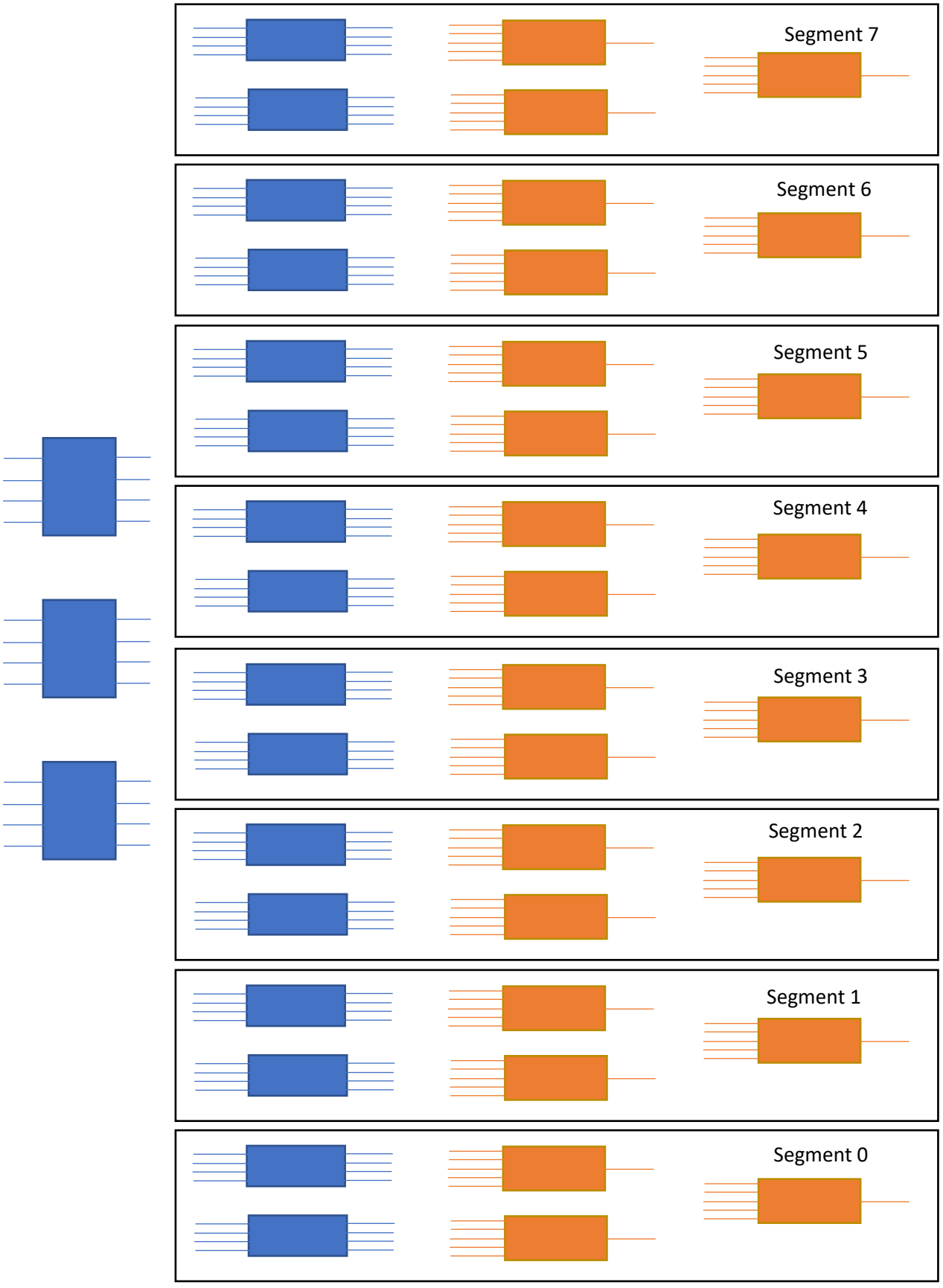
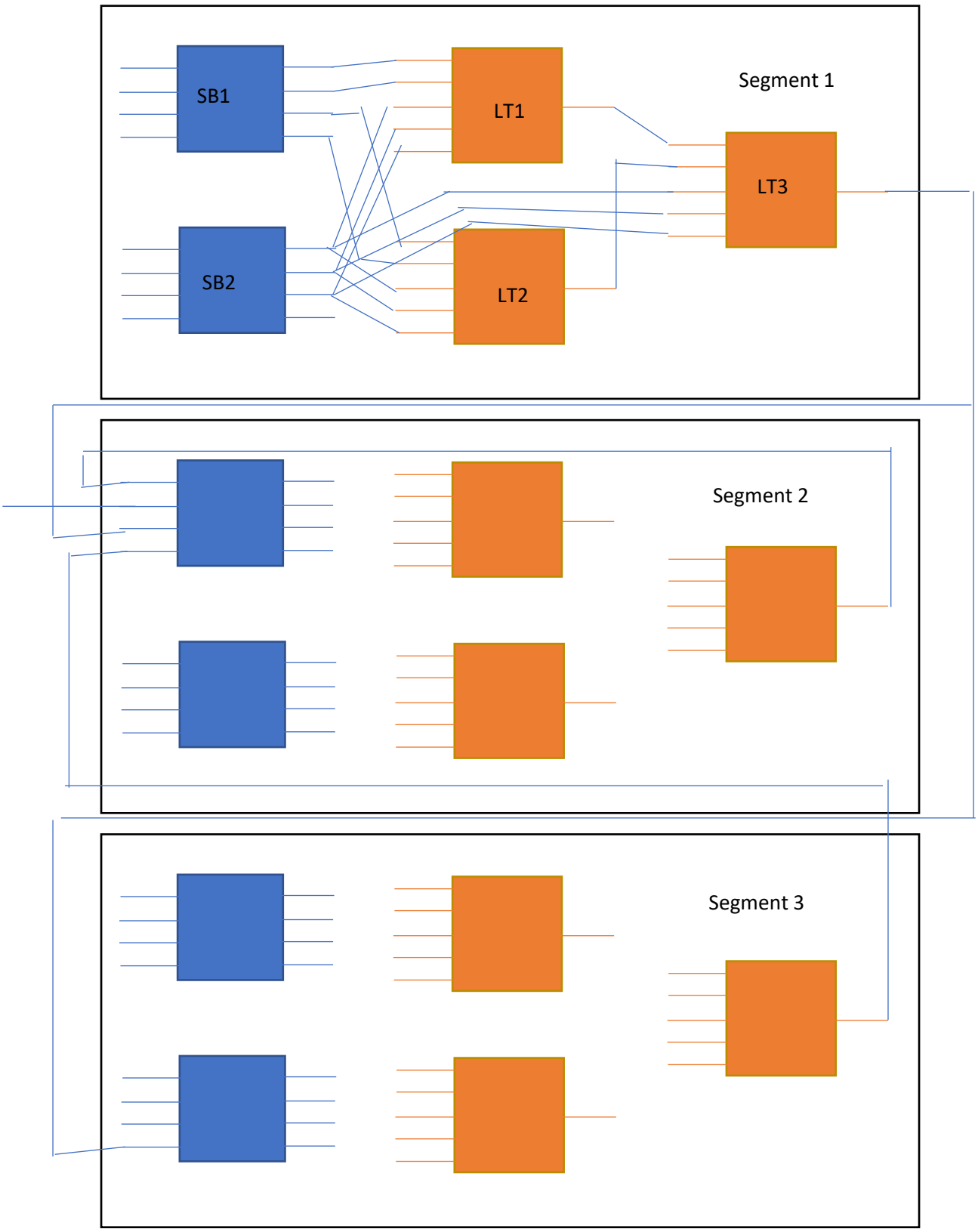


Figure 1

CONNECTIONS

Figure 2



DESCRIPTION OF CONNECTIONS

Figure 2 shows any three consecutive segments of Figure 1(like segment 7, 6, 5 or 4, 3, 2 with segment 1(of Figure 2) referring to segment i (of Figure 1), 2 to i-1 and 3 to i-2).

Intra-segment connections

The internal connections, that is connections within the segments in Fig 1 (that is the 8 segments) are similar to the internal connection displayed in segment 1 in Fig 2.

The outputs of SB1: first two are fed into LT1 and the last 2 into LT2.

The outputs of SB2: the first three outputs are fed into last three inputs of LT1, LT2 and LT3.

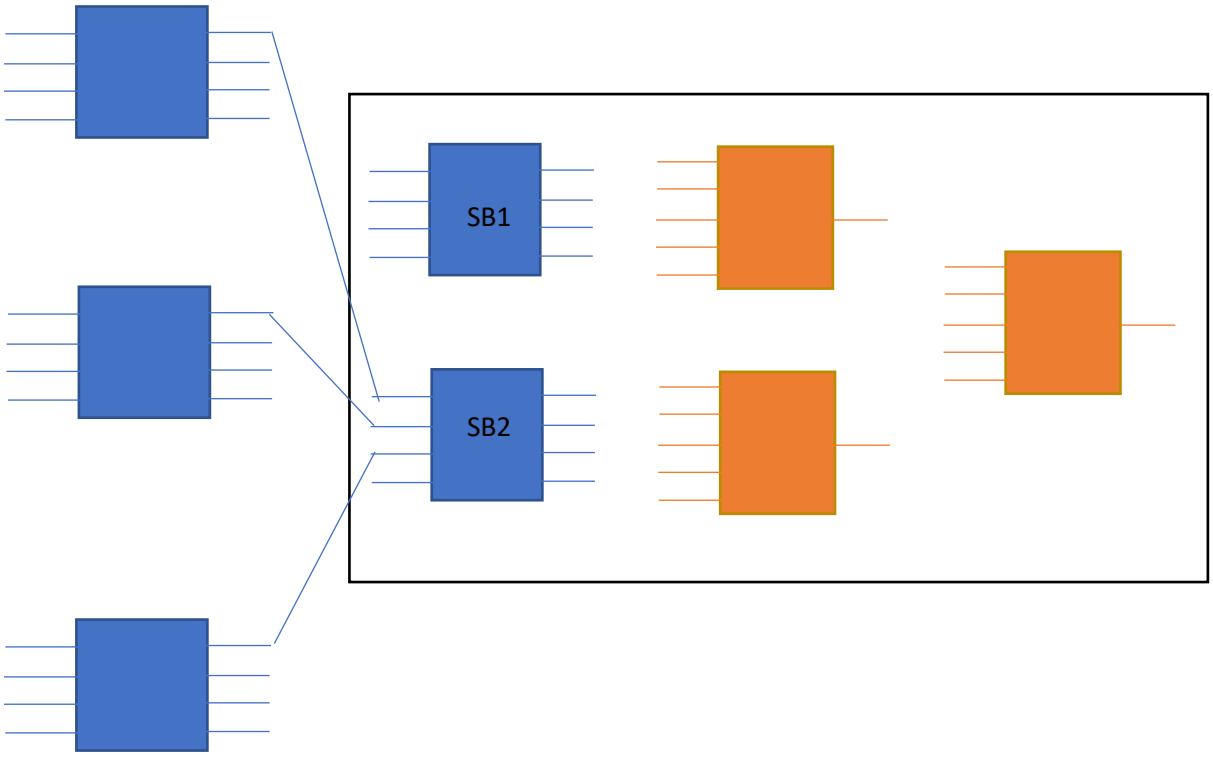
The outputs of LT1 and LT2 are fed into LT3, which produces the output of the segment.

Inter-Segment Connections

The output of segment 1 is fed into SB1 of segment 2 and SB2 of segment 3. The output of segment 1 and output of segment 3 are fed as inputs into SB1 of segment 2. Output of segment 2 is also fed as input into SB1 of segment 2.

1 input of SB1 comes as external input into the configurable fabric.

CONNECTIONS



The first output of the three outer switch boxes (output pin1 of respective exterior switch boxes) are fed as inputs into first three inputs of SB2 of first and segment segments of the 8 segments of Figure 1.

The second inputs of the three outer switch boxes (output pin 2 of the respective exterior switch boxes) are fed as inputs into SB2 of third and forth segments of Figure 1.

Similarly, third inputs into fifth and sixth segments and forth inputs into seventh and eight segments.

IMPLEMENTATION

8-bit universal shift register

3 outer switch boxes

Here and in further explanation, d7, d6, … refer to the load values of the register, input to segment 7, 6, ….

Also, q0, q1, … refer to the final output (output of LT3) produced by segment 0, 1, … respectively.

The outer three switch boxes (outside the 8 segments) take d0, d1, d2, l; d3, d4, d5, shl and d6, d7, si, sh as inputs and the first outer switch box has all 4 outputs connected to l, that is all the four outputs are l, similarly second one has all 4 outputs as shl (out of d3, d4, d5, shl) and third has all outputs as sh.

Switch boxes of any segment

The first and second switch boxes in this case just connect the input and output ports, one to one.

SB1 of any segment (consider segment 7 but can be any other) receive q7, d7, si, q6(in case of segment 6: q6, d6, q7, q5).

SB2 of any segment receives sh, shl, l and the output of the segment previous to previous of the current segment. It just makes the first three outputs as sh, shl and l.

Logic Tiles of any segment

LT1 receives q7 and d7 in segment 7 (likewise q6, d6 in segment 6 or corresponding q and d for any segment) and sh, shl and l. On the basis of sh, shl and l, it chooses q7 or d7.

Likewise, LT2 receives si and q6 in segment 7(q7 and q5 in case of segment 6) and sh, shl and l and on the basis of the latter three values decides the output.

Finally, LT3, receives outputs of LT1 and LT2 and also sh, shl and l and it gives the final output of the segment.

4-bit adder

Let the two input numbers be n1 and n2, and n10 denotes 0^{th} bit of n1, n11 denotes 1^{st} bit of n1, and so on.

Refer to Figure 1 for segment numbering.

Outer three switch boxes

In this case, the outer three switch boxes receive (n10, n11, n12, n13), (n20, n21, n22, n23) and (n10, n11, n12, n13) (the third switch box here is not needed). They just have 8421 configurations, that is, they connect input to output one on one.

Working of the segments

In this case LT2 of any segment does not serve any purpose.

In segment 7, SB1 receives cin (in d7 input port) and SB2 receives the 0^{th} bits of n1 and n2. They are added in LT1 and LT3 simply passes the output of LT1.

In segment 6, same happens, SB1 receives cin and SB2 receives 1^{st} bit of the numbers, but here LT1 calculates the carry produced by the sum (instead of the sum produced in segment 7).

Segment 5 behaves similar to segment 7, except d5 takes output of segment 6 instead of cin and 1^{st} bit of numbers are used.

In segment 4, SB1 becomes redundant and SB2 receives the carry of segment 6, and the 1^{st} bit of the numbers and LT1, using these three inputs, calculates carry.

Similar to segment 5 is segment 3 and segment 1 and similar to segment 4 is segment 2 and segment 0.

Overall

Odd number segments output bits of sum and even numbered segments output carry to be used in the two following segments.

8-bit Multiplexer

Let i0, i1, i2, i3… denote the input bits and c1, c2, c3 denote the control bits.

Outer three Switch Boxes

In this, the outer three switch boxes work similar to the register case, with d0 replaced by i0, d1 by i1, … and sh

by c1, shl by c2 and l by c3. The switch box 1 produces all outputs same as c1, 2nd produces same as c2 and third produces same as c3.

Working of the Segments

In this, all segments work equivalently. SB1 chooses si and d7 in segment 7 (d6 and q7 in segment 6) and sends d6 to LT2 and q7 to LT1. LT1 just outputs whatever is the value of q6 and LT2 calculates minterms from c1, c2, c3 and i6(or d6). LT2 of different segments compute different minterm expressions. LT3 of any segment outputs 1 when either LT1 output is 1 or LT2 output is 1 or both are 1.