Kwame Nkrumah University Of Science And Technology

FACULTY OF COMPUTER ENGINEERING

COE 486 INTRODUCTION TO VLSI

END OF SEMESTER LAB PROJECT

CMOS analog integrated Circuit design & simulation

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Contents

1 Introduction

In the field of VLSI (Very-Large-Scale Integration) design, CMOS (Complementary Metal-Oxide-Semiconductor)[1][2][3][4] technology provides a robust framework for developing efficient and scalable integrated circuits. The inherent advantages of CMOS circuits, such as low power consumption and high noise immunity, make them indispensable across a wide spectrum of applications, ranging from digital processors to analog systems.

The design of CMOS analog circuits begins with a thorough understanding of the basic components, namely NMOS and PMOS transistors. These transistors serve as the fundamental building blocks for more complex circuits, allowing for precise control and amplification of electrical signals. In the initial stages of circuit design, simple configurations like inverters are crucial, especially in digital logic design, as they form the backbone of more intricate circuits.

As circuits grow in complexity, the need for precise current control becomes paramount. This requirement leads to the introduction of current mirrors—essential circuits that replicate a reference current across different branches, ensuring consistent current flow. Current mirrors are integral in analog design, particularly in applications involving constant current sources, biasing, and active loads. Their role in stabilizing and enhancing the performance of amplifiers and other analog devices cannot be overstated.

This lab report focuses on the design and simulation of CMOS inverters, NAND, AND gate and frequency response of analog circuit using Cadence[5], a powerful suite of computer-aided design (CAD) tools. Cadence enables the practical application of theoretical concepts, allowing for the detailed analysis and refinement of circuit designs. By leveraging Cadence's comprehensive simulation capabilities, this report aims to provide a deep understanding of the operation and significance of CMOS inverters and current mirrors in VLSI design, bridging the gap between theoretical knowledge and real-world implementation.

2 Objectives and Learning Outcomes

2.1 Objectives

1. Lab 1: Learn how to login on a Linux[7][8][9] workstation, perform basic Linux tasks, and use the Cadence design system to simulate and layout simple circuits.

2. Lab 2: Design and simulate NAND gate.

3. Lab 3: Design and simulate NAND gate.

4. Lab 4: Perform freaquency analysis on an analog circuit.

3 Equipments

- A computer with Linux Operating system (cent OS[10] in my case). I used a virtual machine installed on windows 11 system using VMWare[11].

- A computer of at least 1GHz dual core CPU, 18GB free disk space and 4GB RAM is necessary to perform the lab.

- Cadence, which is a software suite with:
    1. Schematic editor
    2. Layout editor
    3. Spice simulation[12](Spectre simulation was used in this lab)

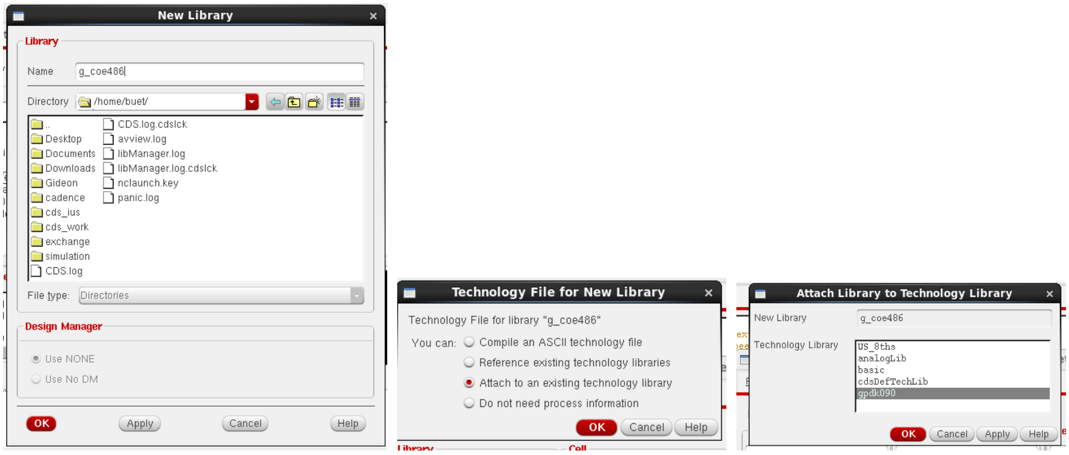
4 METHODOLY AND DESIGN

4.1 LAB 1: INVERTER

4.1.1 Description

In this lab, I got to experiment cadence tools like the schematic editor, layout editor and finally the simulation tool. In particular I designed an inverter as practice.

4.1.2 Design



New Library

Library

Name: g_coe486

Directory: /home/buet/

```
..          CDS.log.cdslck
Desktop     avview.log
Documents   libManager.log
Downloads   libManager.log.cdslck
Gideon      nclaunch.key
cadence     panic.log
cds_ius
cds_work
exchange
simulation
CDS.log
```

File type: Directories

Design Manager

● Use NONE

○ Use No DM

Technology File for New Library

Technology File for library "g_coe486"

You can:
○ Compile an ASCII technology file
○ Reference existing technology libraries
● Attach to an existing technology library
○ Do not need process information

Attach Library to Technology Library

New Library: g_coe486

Technology Library:

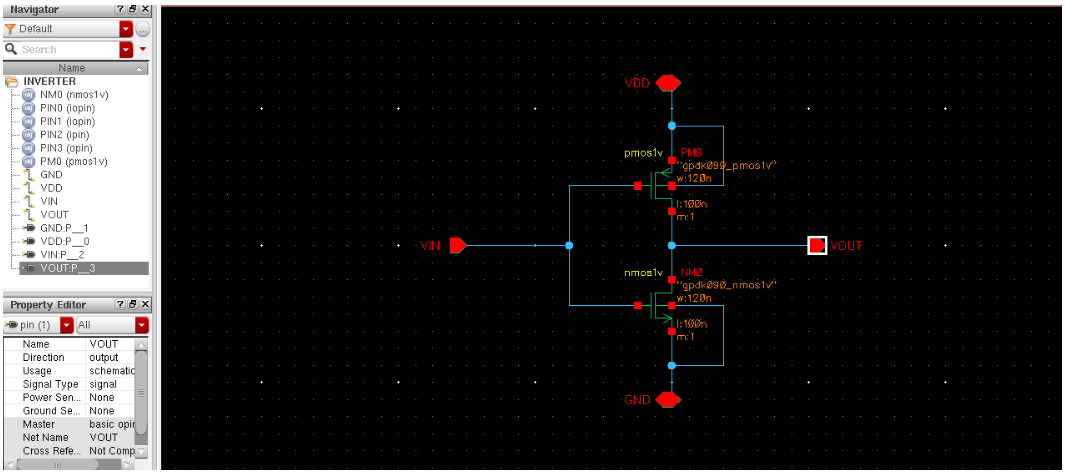
```
US_8ths
analogLib
basic
cdsDefTechLib
gpdk090
```

Figure 1: Creating new library

1. I created a library called g_coe486 as shown in the figure 1 above. I attached an existing technology, *gpdk090*[6].

2. I added a cell called INVERTER in the created library in 1.

3. The figure below shows the inverter schematic I configured in INVERTER schematic.



Navigator

Default

```
INVERTER
  NM0 (nmos1v)
  PIN0 (iopin)
  PIN1 (iopin)
  PIN2 (ipin)
  PIN3 (opin)
  PM0 (pmos1v)
  GND
  VDD
  VIN
  VOUT
  GND:P__1
  VDD:P__0
  VIN:P__2
  VOUT:P__3
```

Property Editor

pin (1) All

Name	VOUT
Direction	output
Usage	schematic
Signal Type	signal
Power Sen...	None
Ground Se...	None
Master	basic opir
Net Name	VOUT
Cross Refe...	Not Comp

Figure 2: schematic

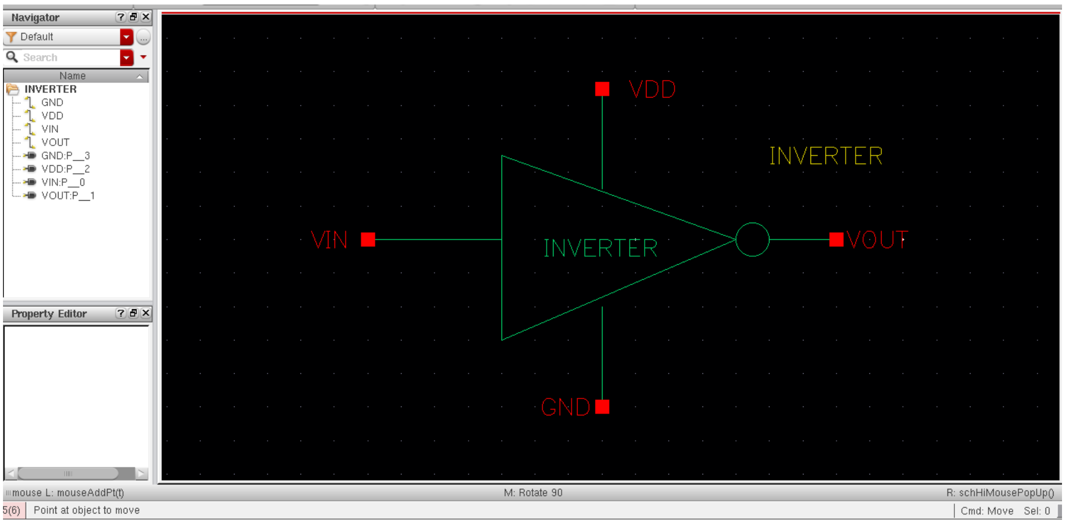


Figure 3: symbol

4. After making sure the schematic is well connected, I created a cellview symbol for the inverter as shown below.

5. After creating the symbol, I created the layout as shown in ¡fig ref¿. The result of both DRC and LVS checks are observed.

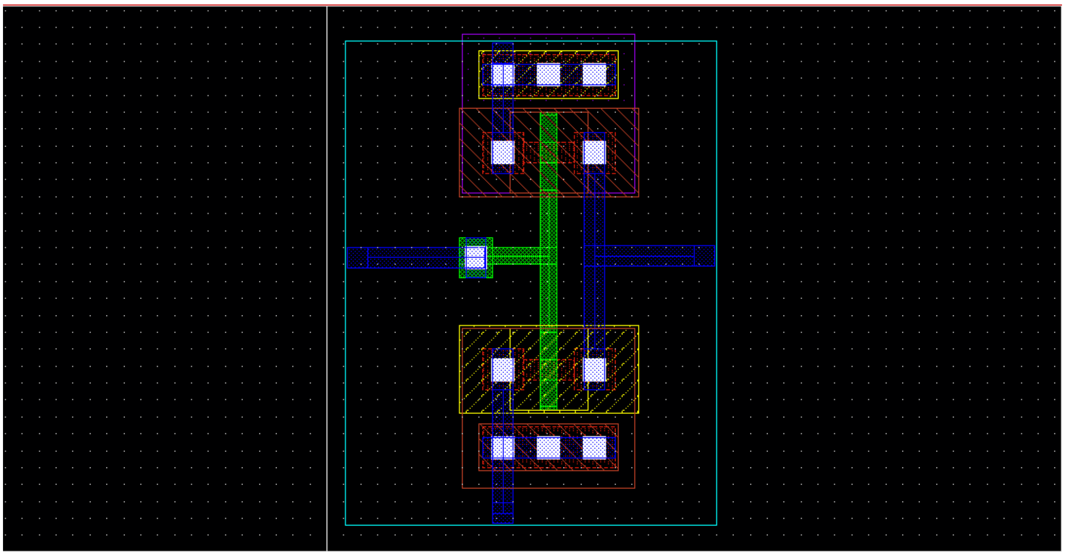


Figure 4: layout

4.2 LAB 2: NAND gate

4.2.1 Description

In this lab, a nand gate was designed, and simulated using cadence.

4.2.2 Design

1. I added a cell called NAND in the g_coe486 library.

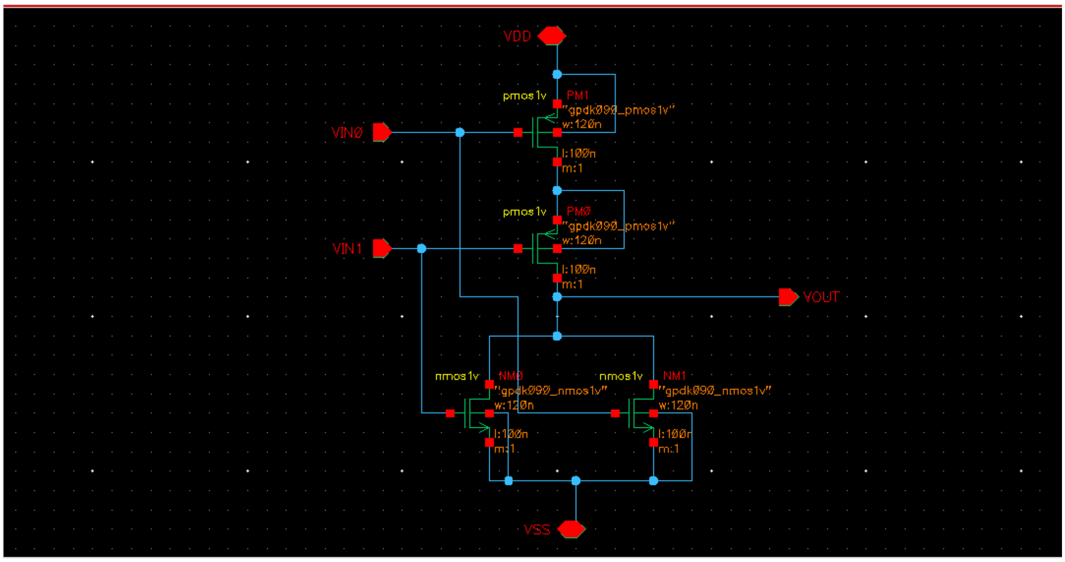


Figure 5: schematic

2. The figure below shows the NAND schematic I configured in NAND schematic.

3. After making sure the schematic is well connected, I created a cellview symbol for the NAND as shown below.

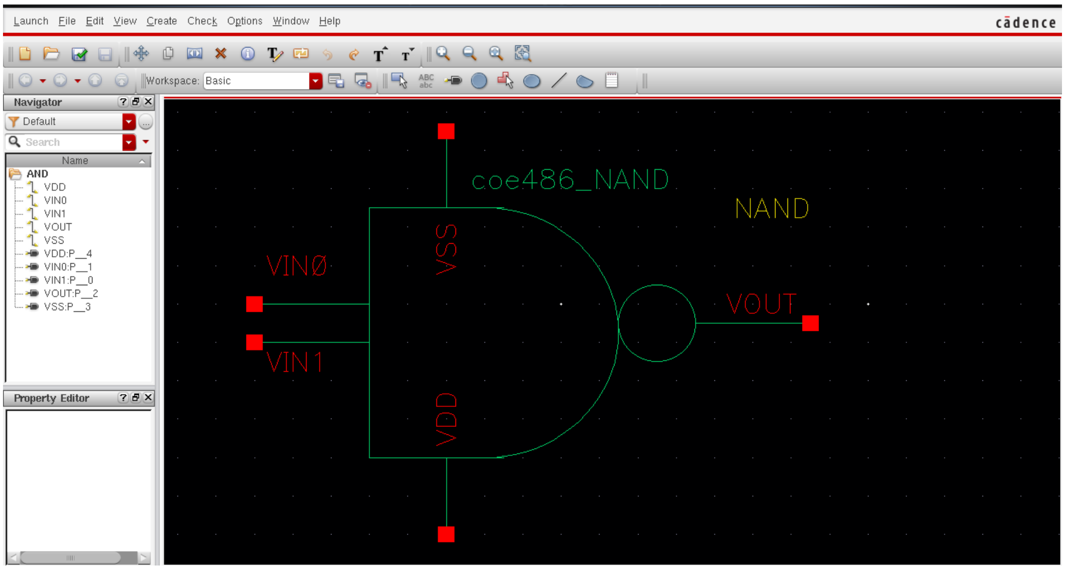
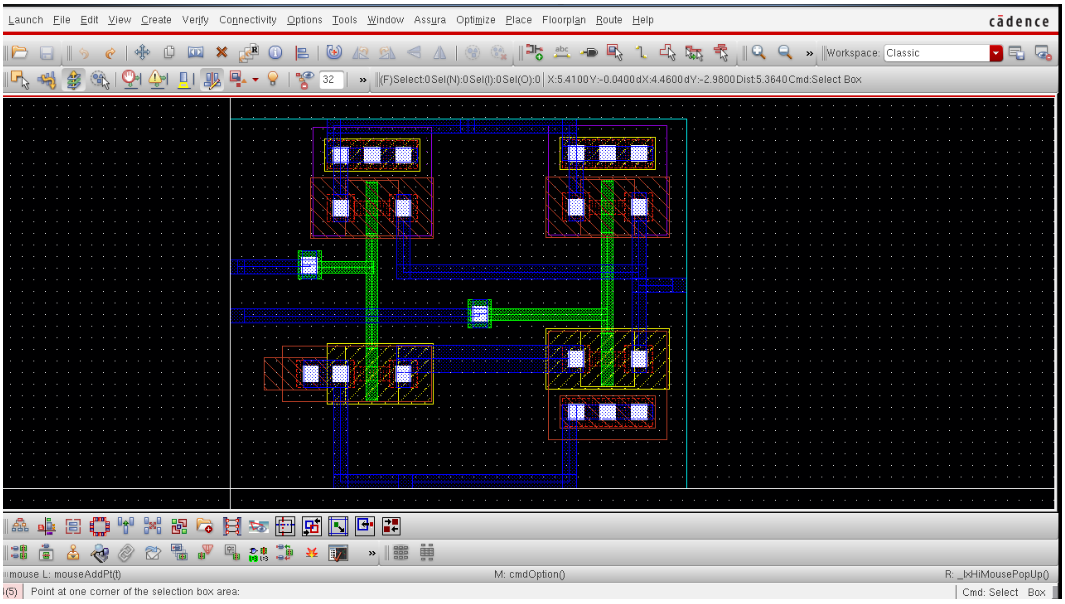


Figure 6: symbol

4. After creating the symbol, I created the layout as shown in ¡fig ref¿. The result of both DRC and LVS checks are observed.

5. From the graph, observing with the vertical marker, a Truth table is obtained to verify the NAND design.


Launch File Edit View Create Verify Connectivity Options Tools Window Assura Optimize Place Floorplan Route Help
cādence
Workspace: Classic
32

(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:5.4100 Y:-0.0400 dX:4.4600 dY:-2.9800 Dist:5.3640 Cmd:Select Box

mouse L: mouseAddPt(t) M: cmdOption() R: _lxHiMousePopUp()

(5) Point at one corner of the selection box area:

Cmd: Select Box

Figure 7: layout

4.3 LAB 3: AND gate

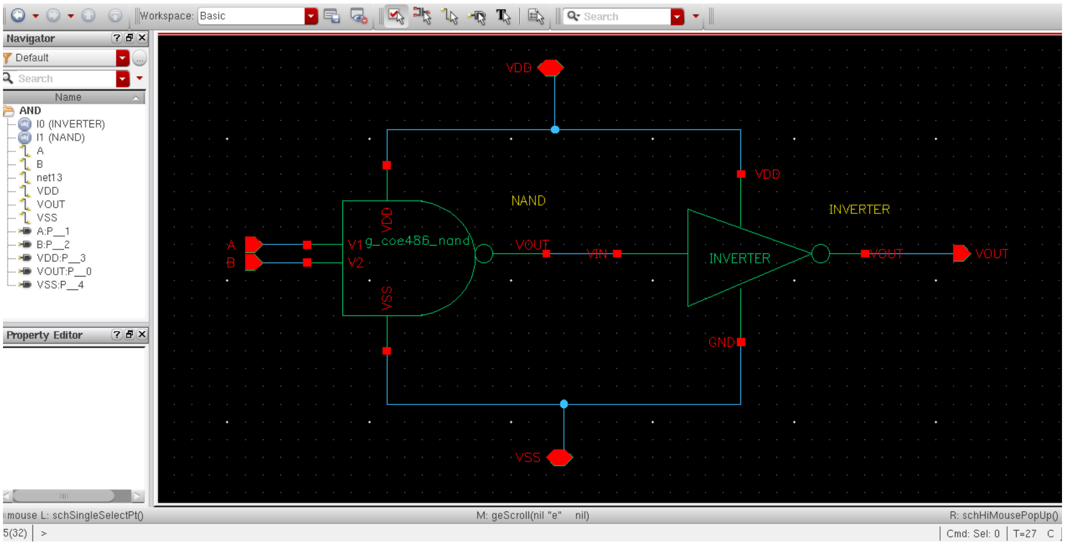
4.3.1 Description

In this lab, an AND gate was designed and simulated using cadence. The simulated result was observed and the truth table verified. I used the created AND and INVERTER created in previous labs.

4.3.2 Design

1. A cell called AND was created in the g_coe486 library.

2. In figure 8 shows the AND schematic configured in the AND schematic using the already created AND and INVERTER.



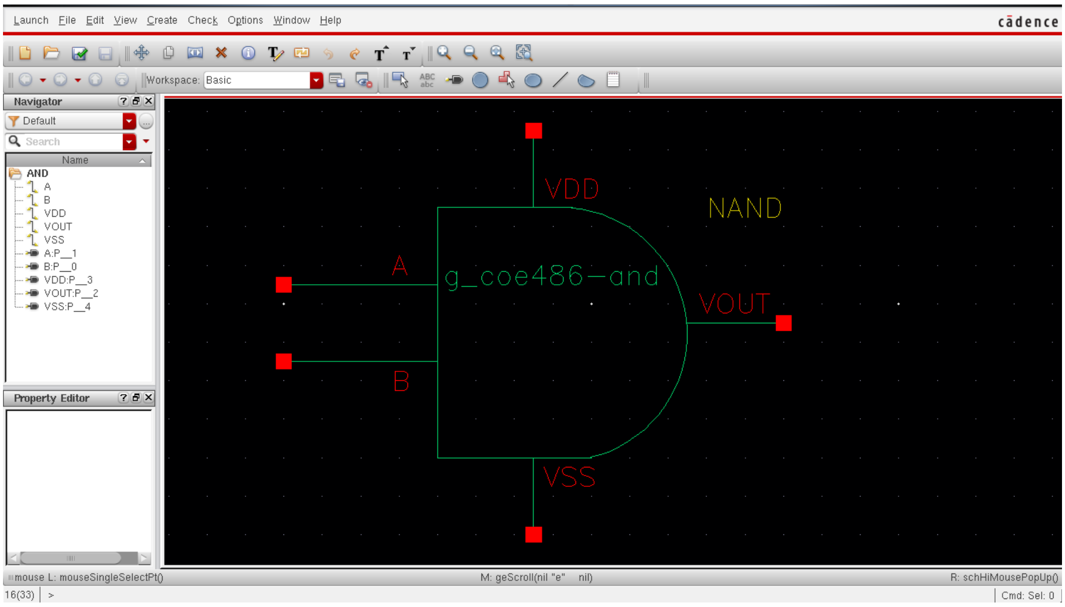
mouse L: schSingleSelectPt() M: geScroll(nil "e" nil) R: schHiMousePopUp()

5(32) >

Cmd: Sel: 0 T=27 C

Figure 8: schematic

3. After making sure the schematic is well connected, I created a cellview symbol for the AND as shown below.

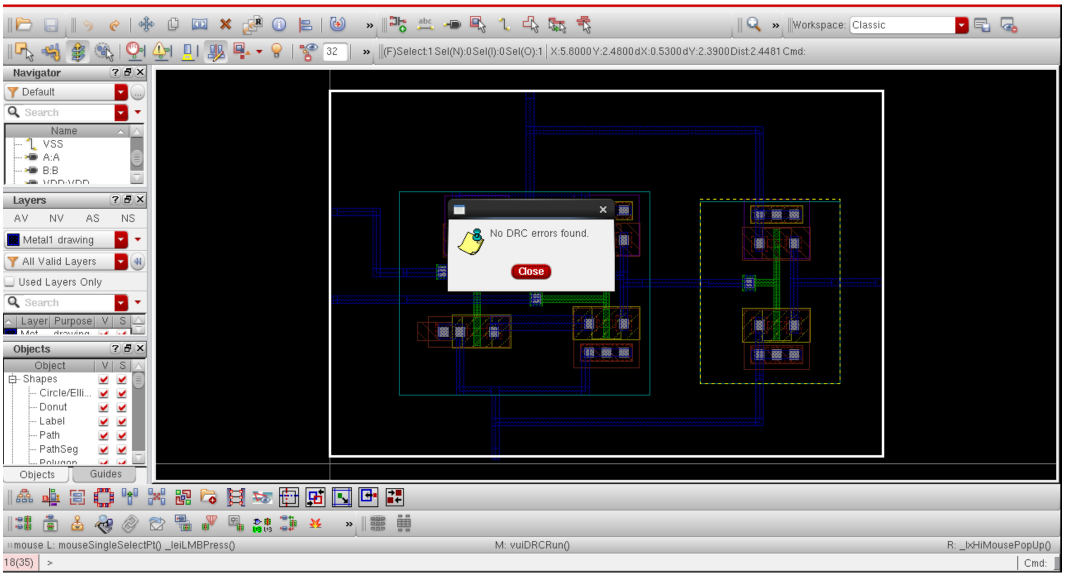


mouse L: mouseSingleSelectPt() M: geScroll(nil "e" nil) R: schHiMousePopUp()

16(33) > Cmd: Sel: 0

Figure 9: symbol

4. After creating the symbol, I created the layout as shown in ¡fig ref¿. The result of both DRC and LVS checks are observed.



(F)Select:1 Sel(N):0 Sel(I):0 Sel(O):1 X:5.8000 Y:2.4800 dX:0.5300 dY:2.3900 Dist:2.4481 Cmd:

No DRC errors found.

mouse L: mouseSingleSelectPt() _leiLMBPress() M: vuiDRCRun() R: _lxHiMousePopUp()

18(35) > Cmd:

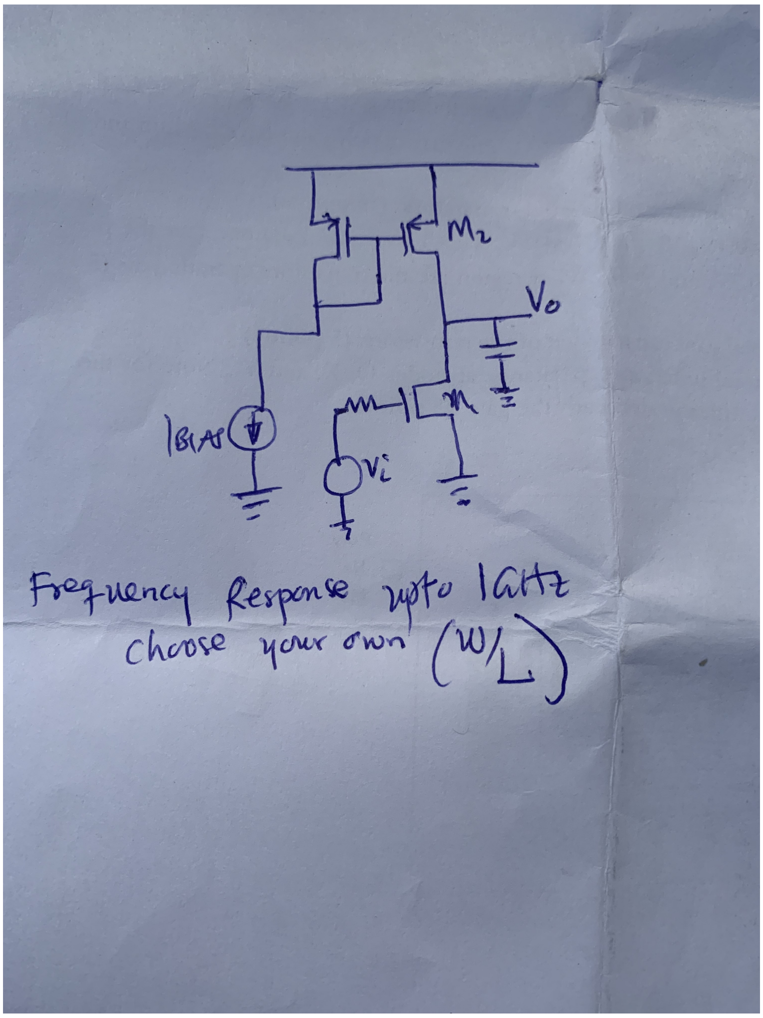
Figure 10: layout

4.4 LAB 4: Frequency Response

4.4.1 Description

In this lab, frequency response analysis was perform. The frequency response for of the circuit below was used in this lab.

v



Frequency Response upto 1GHz
choose your own (W/L)

Figure 11: Circuit diagram

MOSFET Parameter Estimation and Calculations

- 1. Estimating Parameters
  - Channel Length Modulation (λ)

$$\lambda = 0.05\ \mathrm{V}^{-1}$$

  - Mobility (μ)

$$\mu_n \approx 500\ \mathrm{cm}^2/\mathrm{V{\cdot}s}$$

  - Oxide Capacitance (C_{ox})

$$C_{ox} \approx 10\ \mathrm{fF}/\mu\mathrm{m}^2$$

  - Overdrive Voltage (V_{ov})

$$V_{ov} \approx 0.3 \text{ V}$$

- Calculations
  - Transconductance (g_m)

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$$

    where $W = 120$ µm, $L = 0.1$ µm, $I_D = 100$ µA, $\mu = 500$ cm^2/V·s, and $C_{ox} = 10$ fF/µm^2.

  - Output Resistance (r_o)

$$r_o = \frac{1}{\lambda I_D}$$

    where $\lambda = 0.05$ V^{-1} and $I_D = 100$ µA.

  - Effective Output Resistance with Cascode

$$R_{out,\text{eff}} \approx r_{o1} \parallel (g_{m2} \cdot r_{o2} \cdot r_{o1})$$

$$A_v = -g_m \cdot R_{out} \tag{1}$$

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{-g_m \cdot R_{out}}{1 + s \cdot R_{out} \cdot C_{total}} \tag{2}$$

$$\omega_p = \frac{1}{R_{out} \cdot C_{total}} \tag{3}$$

$$s = j\omega \tag{4}$$

4.5 TEST BENCH DESIGN

The test bench schematic is as shown if figure 12.

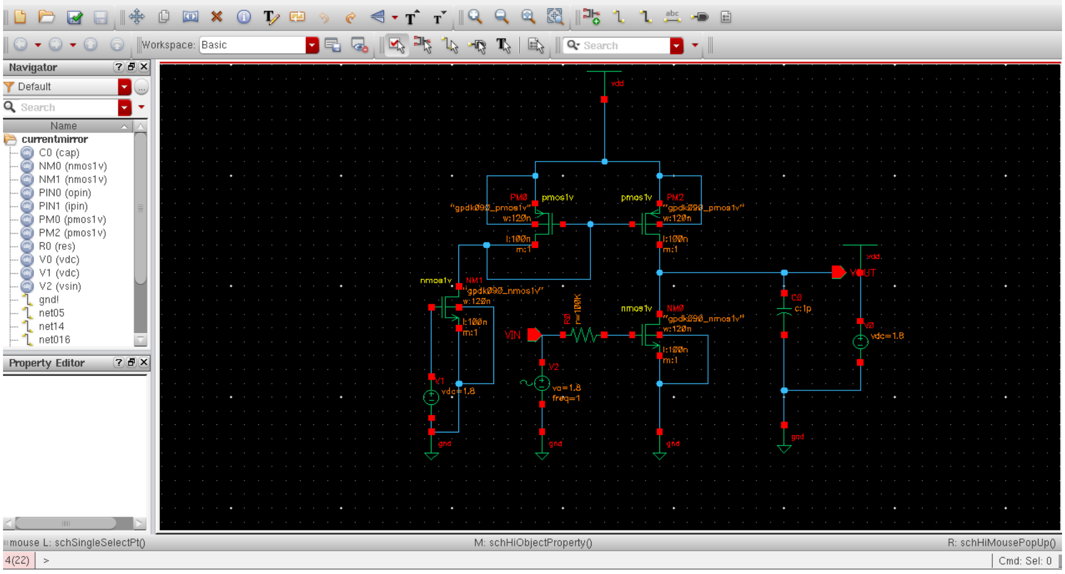
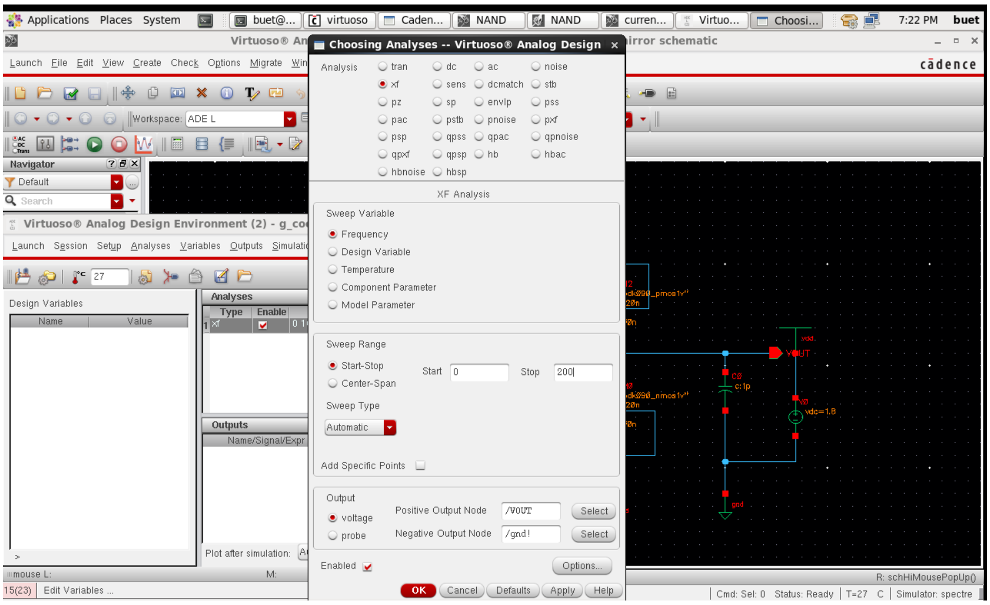


Figure 12: Frequecy Response Test bench schematic

A frequency was performed and the both the magnitude response, phase response, gain were observed. The analysis is as show in figure 13.


Choosing Analyses -- Virtuoso® Analog Design

Analysis: ○ tran ○ dc ○ ac ○ noise ● xf ○ sens ○ dcmatch ○ stb ○ pz ○ sp ○ envlp ○ pss ○ pac ○ pstb ○ pnoise ○ pxf ○ psp ○ qpss ○ qpac ○ qpnoise ○ qpxf ○ qpsp ○ hb ○ hbac ○ hbnoise ○ hbsp

XF Analysis

Sweep Variable: ● Frequency ○ Design Variable ○ Temperature ○ Component Parameter ○ Model Parameter

Sweep Range: ● Start-Stop ○ Center-Span Start 0 Stop 200

Sweep Type: Automatic

Add Specific Points □

Output: ● voltage ○ probe

Positive Output Node /VOUT

Negative Output Node /gnd!

Enabled ☑

Figure 13: Frequecy Response Test bench schematic

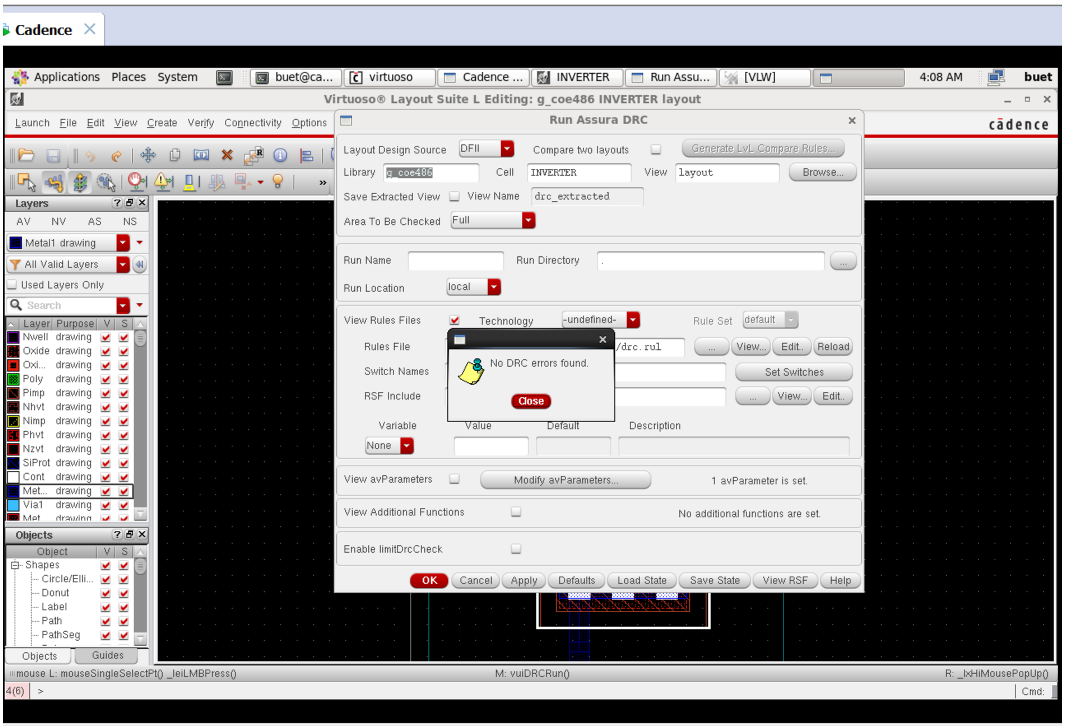
The sweep range 0-1kHz. The resulting graph was observed.

5 Result

5.1 LAB 1: Inverter

5.1.1 DRC and LVS test Results

The following sections shows the results of each tests.



Virtuoso® Layout Suite L Editing: g_coe486 INVERTER layout

Run Assura DRC

Layout Design Source: DFII

Library: g_coe486 Cell: INVERTER View: layout

Save Extracted View □ View Name: drc_extracted

Area To Be Checked: Full

Run Location: local

View Rules Files ☑ Technology: -undefined- Rule Set: default

Rules File: /drc.rul

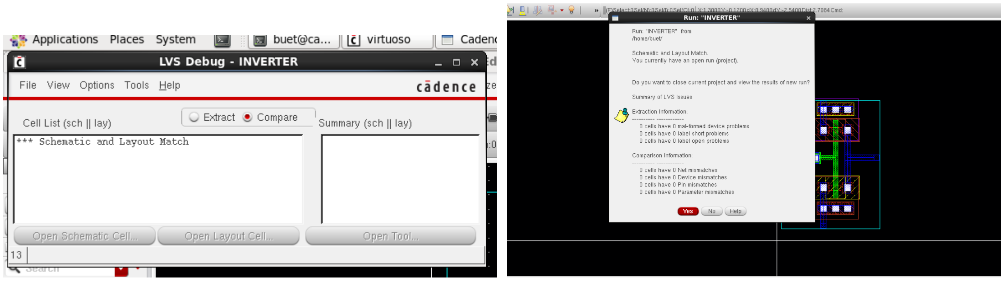
No DRC errors found.

View avParameters □ 1 avParameter is set.

View Additional Functions □ No additional functions are set.

Enable limitDrcCheck □

Figure 14: DRC



LVS Debug - INVERTER

Cell List (sch || lay) ○ Extract ● Compare Summary (sch || lay)

*** Schematic and Layout Match

Run: "INVERTER"

Run: "INVERTER" from
/home/buet/

Schematic and Layout Match.
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:
---------- ------------
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems

Comparison Information:
---------- ------------
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches

Figure 15: LSV

5.1.2 Simulation Results

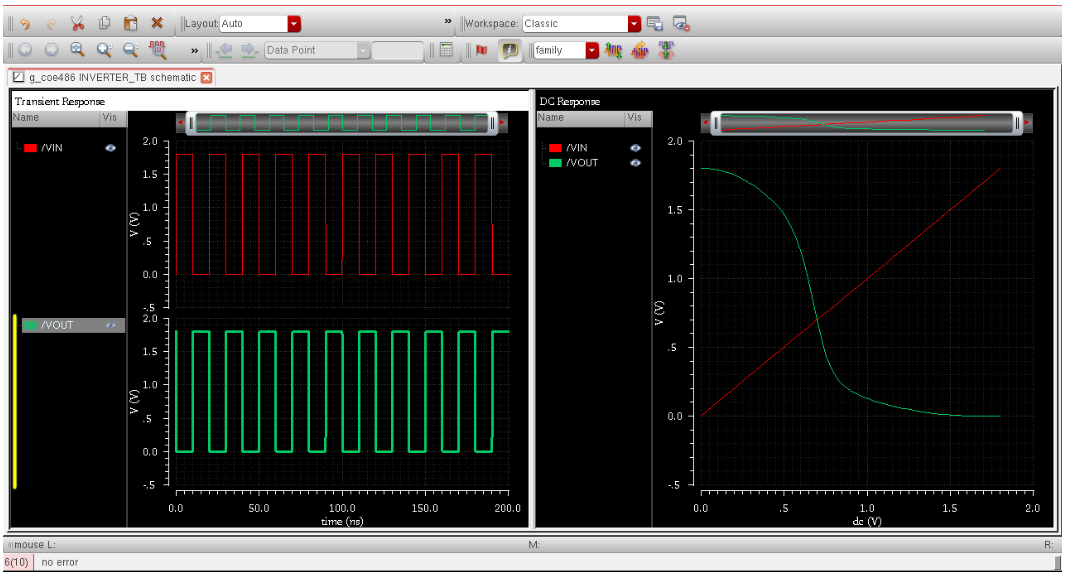
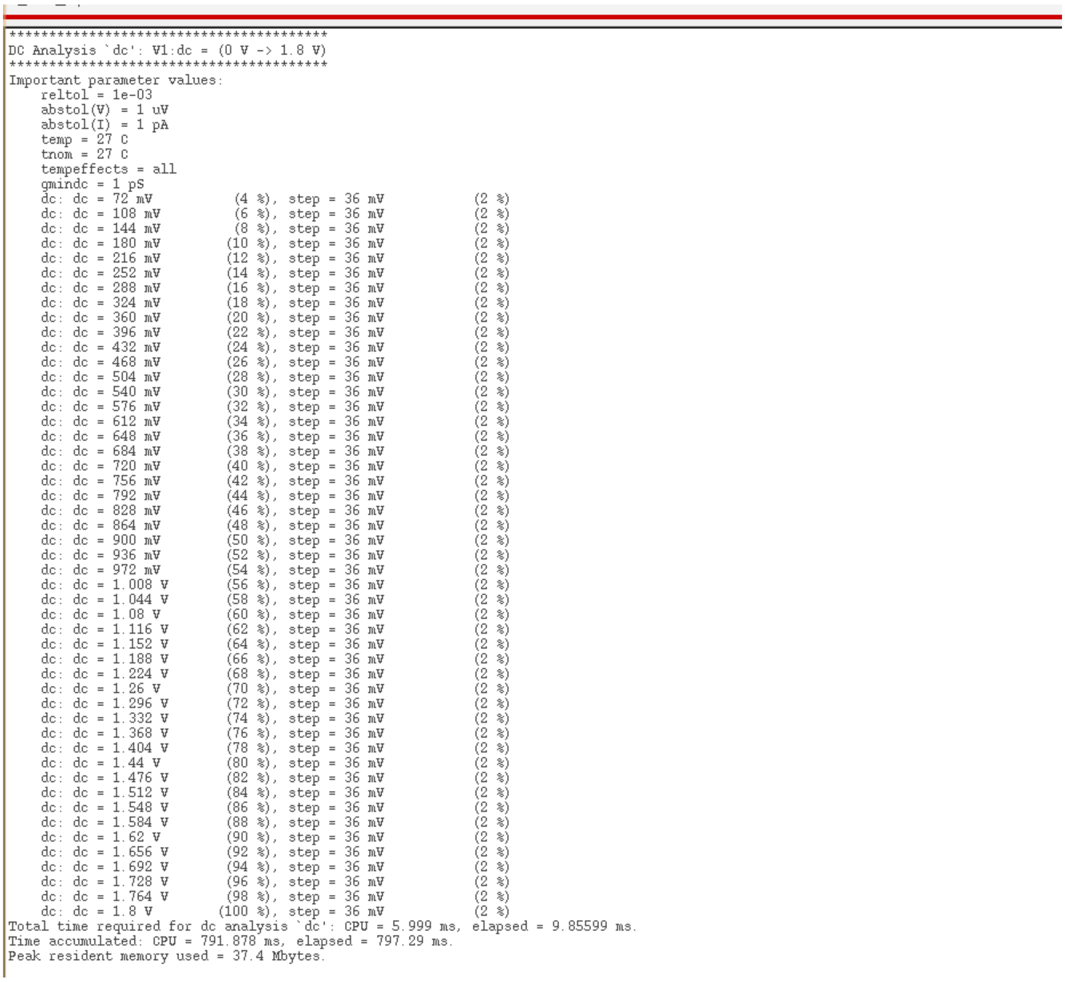
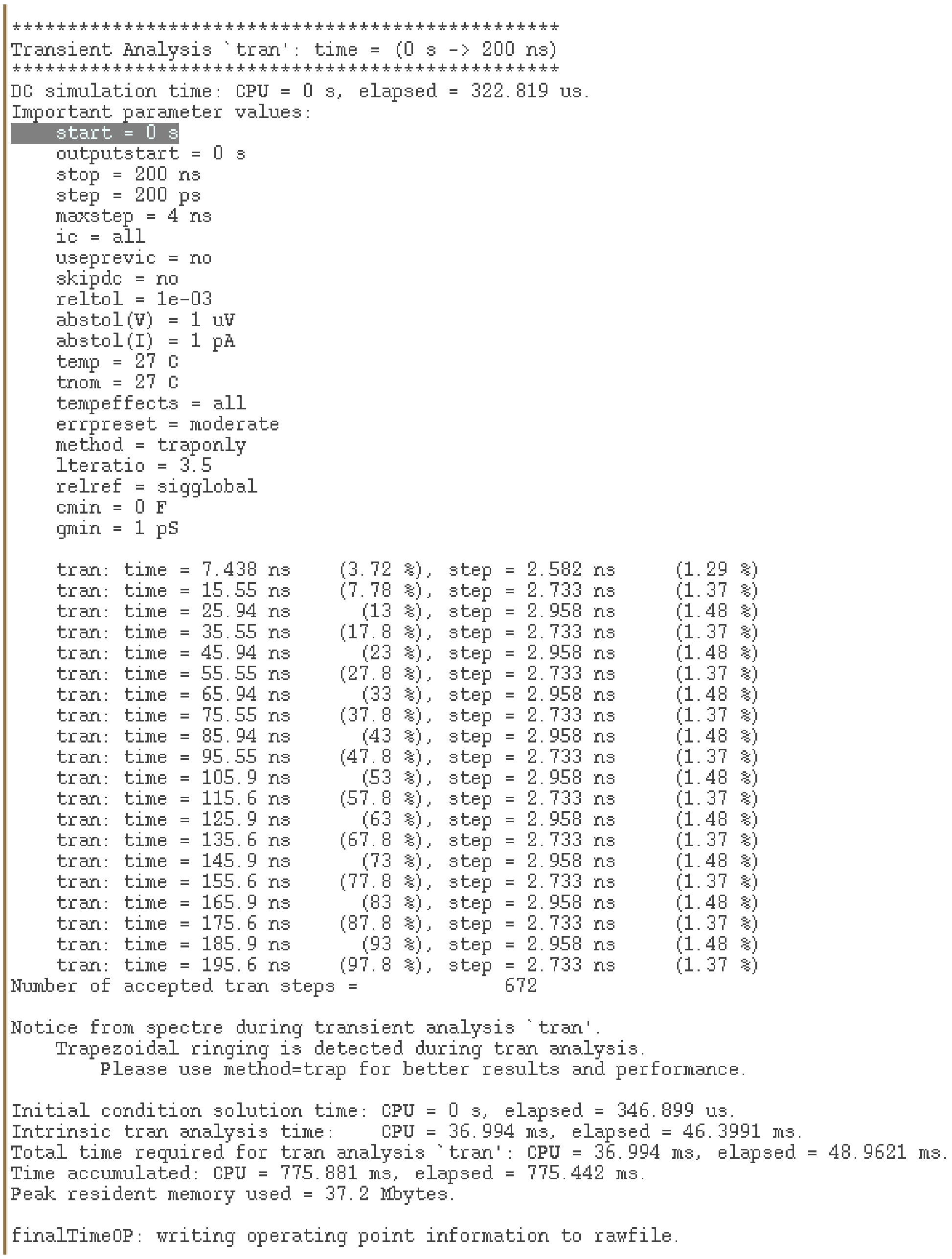


Figure 16: Inverter simulation



```
*******************************************
DC Analysis `dc': V1:dc = (0 V -> 1.8 V)
*******************************************
Important parameter values:
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    gmindc = 1 pS
    dc: dc = 72 mV          (4 %), step = 36 mV           (2 %)
    dc: dc = 108 mV         (6 %), step = 36 mV           (2 %)
    dc: dc = 144 mV         (8 %), step = 36 mV           (2 %)
    dc: dc = 180 mV        (10 %), step = 36 mV           (2 %)
    dc: dc = 216 mV        (12 %), step = 36 mV           (2 %)
    dc: dc = 252 mV        (14 %), step = 36 mV           (2 %)
    dc: dc = 288 mV        (16 %), step = 36 mV           (2 %)
    dc: dc = 324 mV        (18 %), step = 36 mV           (2 %)
    dc: dc = 360 mV        (20 %), step = 36 mV           (2 %)
    dc: dc = 396 mV        (22 %), step = 36 mV           (2 %)
    dc: dc = 432 mV        (24 %), step = 36 mV           (2 %)
    dc: dc = 468 mV        (26 %), step = 36 mV           (2 %)
    dc: dc = 504 mV        (28 %), step = 36 mV           (2 %)
    dc: dc = 540 mV        (30 %), step = 36 mV           (2 %)
    dc: dc = 576 mV        (32 %), step = 36 mV           (2 %)
    dc: dc = 612 mV        (34 %), step = 36 mV           (2 %)
    dc: dc = 648 mV        (36 %), step = 36 mV           (2 %)
    dc: dc = 684 mV        (38 %), step = 36 mV           (2 %)
    dc: dc = 720 mV        (40 %), step = 36 mV           (2 %)
    dc: dc = 756 mV        (42 %), step = 36 mV           (2 %)
    dc: dc = 792 mV        (44 %), step = 36 mV           (2 %)
    dc: dc = 828 mV        (46 %), step = 36 mV           (2 %)
    dc: dc = 864 mV        (48 %), step = 36 mV           (2 %)
    dc: dc = 900 mV        (50 %), step = 36 mV           (2 %)
    dc: dc = 936 mV        (52 %), step = 36 mV           (2 %)
    dc: dc = 972 mV        (54 %), step = 36 mV           (2 %)
    dc: dc = 1.008 V       (56 %), step = 36 mV           (2 %)
    dc: dc = 1.044 V       (58 %), step = 36 mV           (2 %)
    dc: dc = 1.08 V        (60 %), step = 36 mV           (2 %)
    dc: dc = 1.116 V       (62 %), step = 36 mV           (2 %)
    dc: dc = 1.152 V       (64 %), step = 36 mV           (2 %)
    dc: dc = 1.188 V       (66 %), step = 36 mV           (2 %)
    dc: dc = 1.224 V       (68 %), step = 36 mV           (2 %)
    dc: dc = 1.26 V        (70 %), step = 36 mV           (2 %)
    dc: dc = 1.296 V       (72 %), step = 36 mV           (2 %)
    dc: dc = 1.332 V       (74 %), step = 36 mV           (2 %)
    dc: dc = 1.368 V       (76 %), step = 36 mV           (2 %)
    dc: dc = 1.404 V       (78 %), step = 36 mV           (2 %)
    dc: dc = 1.44 V        (80 %), step = 36 mV           (2 %)
    dc: dc = 1.476 V       (82 %), step = 36 mV           (2 %)
    dc: dc = 1.512 V       (84 %), step = 36 mV           (2 %)
    dc: dc = 1.548 V       (86 %), step = 36 mV           (2 %)
    dc: dc = 1.584 V       (88 %), step = 36 mV           (2 %)
    dc: dc = 1.62 V        (90 %), step = 36 mV           (2 %)
    dc: dc = 1.656 V       (92 %), step = 36 mV           (2 %)
    dc: dc = 1.692 V       (94 %), step = 36 mV           (2 %)
    dc: dc = 1.728 V       (96 %), step = 36 mV           (2 %)
    dc: dc = 1.764 V       (98 %), step = 36 mV           (2 %)
    dc: dc = 1.8 V        (100 %), step = 36 mV           (2 %)
Total time required for dc analysis `dc': CPU = 5.999 ms, elapsed = 9.85599 ms.
Time accumulated: CPU = 791.878 ms, elapsed = 797.29 ms.
Peak resident memory used = 37.4 Mbytes.
```

Figure 17: DC

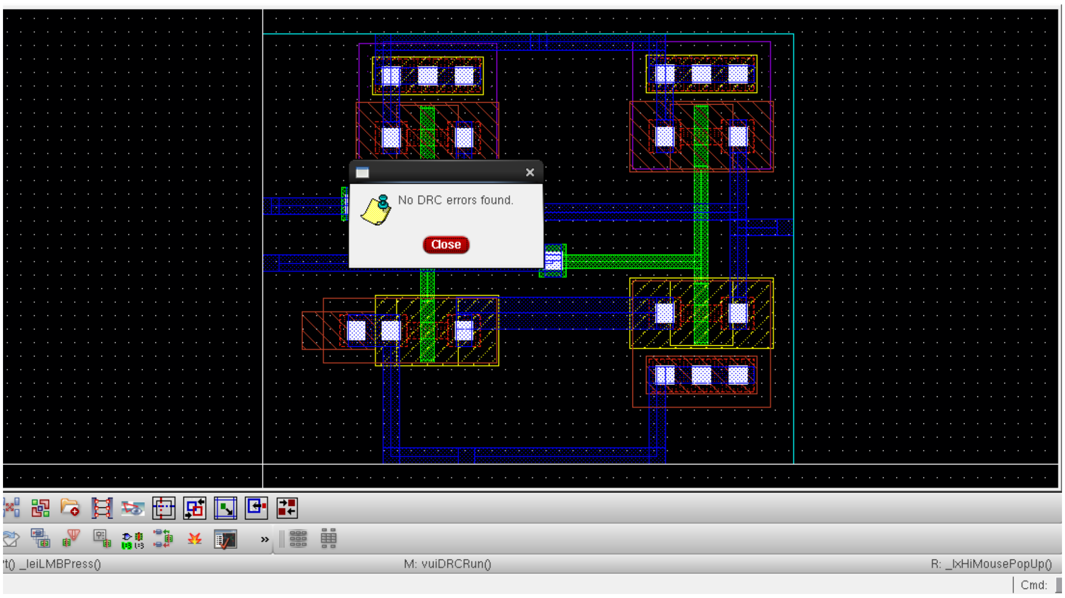


```
*************************************************
Transient Analysis `tran': time = (0 s -> 200 ns)
*************************************************
DC simulation time: CPU = 0 s, elapsed = 322.819 us.
Important parameter values:
    start = 0 s
    outputstart = 0 s
    stop = 200 ns
    step = 200 ps
    maxstep = 4 ns
    ic = all
    useprevic = no
    skipdc = no
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    errpreset = moderate
    method = traponly
    lteratio = 3.5
    relref = sigglobal
    cmin = 0 F
    gmin = 1 pS

    tran: time = 7.438 ns    (3.72 %), step = 2.582 ns     (1.29 %)
    tran: time = 15.55 ns    (7.78 %), step = 2.733 ns     (1.37 %)
    tran: time = 25.94 ns      (13 %), step = 2.958 ns     (1.48 %)
    tran: time = 35.55 ns    (17.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 45.94 ns      (23 %), step = 2.958 ns     (1.48 %)
    tran: time = 55.55 ns    (27.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 65.94 ns      (33 %), step = 2.958 ns     (1.48 %)
    tran: time = 75.55 ns    (37.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 85.94 ns      (43 %), step = 2.958 ns     (1.48 %)
    tran: time = 95.55 ns    (47.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 105.9 ns      (53 %), step = 2.958 ns     (1.48 %)
    tran: time = 115.6 ns    (57.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 125.9 ns      (63 %), step = 2.958 ns     (1.48 %)
    tran: time = 135.6 ns    (67.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 145.9 ns      (73 %), step = 2.958 ns     (1.48 %)
    tran: time = 155.6 ns    (77.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 165.9 ns      (83 %), step = 2.958 ns     (1.48 %)
    tran: time = 175.6 ns    (87.8 %), step = 2.733 ns     (1.37 %)
    tran: time = 185.9 ns      (93 %), step = 2.958 ns     (1.48 %)
    tran: time = 195.6 ns    (97.8 %), step = 2.733 ns     (1.37 %)
Number of accepted tran steps =             672

Notice from spectre during transient analysis `tran'.
    Trapezoidal ringing is detected during tran analysis.
        Please use method=trap for better results and performance.

Initial condition solution time: CPU = 0 s, elapsed = 346.899 us.
Intrinsic tran analysis time:    CPU = 36.994 ms, elapsed = 46.3991 ms.
Total time required for tran analysis `tran': CPU = 36.994 ms, elapsed = 48.9621 ms.
Time accumulated: CPU = 775.881 ms, elapsed = 775.442 ms.
Peak resident memory used = 37.2 Mbytes.

finalTimeOP: writing operating point information to rawfile.
```

Figure 18: Transient

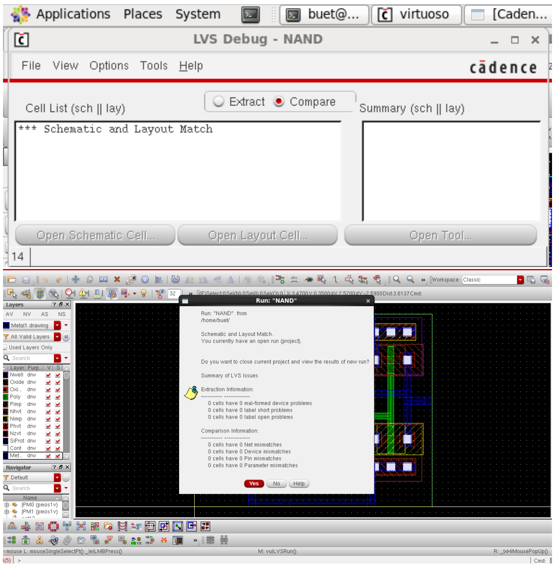
5.2 LAB 2: NAND

5.2.1 DRC and LVS test Results



No DRC errors found.

Figure 19: DRC



```
*** Schematic and Layout Match
```

Run: "NAND" from
/home/buet/

Schematic and Layout Match.
You currently have an open run (project).

Do you want to close current project and view the results of new run?

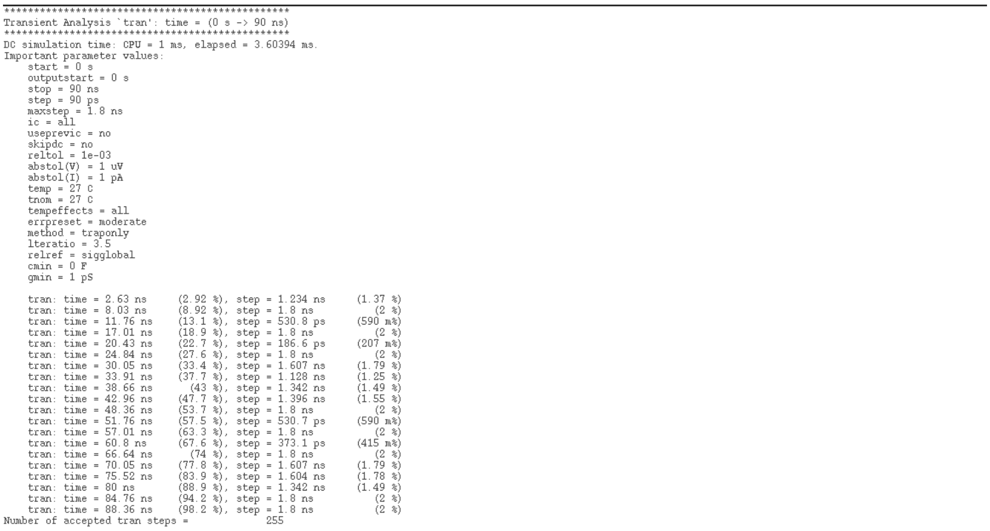
Summary of LVS Issues

Extraction Information:
```
---------- -----------
   0 cells have 0 mal-formed device problems
   0 cells have 0 label short problems
   0 cells have 0 label open problems
```

Comparison Information:
```
---------- -----------
   0 cells have 0 Net mismatches
   0 cells have 0 Device mismatches
   0 cells have 0 Pin mismatches
   0 cells have 0 Parameter mismatches
```

Figure 20: LSV

5.2.2 Simulation Results



```
************************************************
Transient Analysis `tran': time = (0 s -> 90 ns)
************************************************
DC simulation time: CPU = 1 ms, elapsed = 3.60394 ms.
Important parameter values:
    start = 0 s
    outputstart = 0 s
    stop = 90 ns
    step = 90 ps
    maxstep = 1.8 ns
    ic = all
    useprevic = no
    skipdc = no
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    errpreset = moderate
    method = traponly
    lteratio = 3.5
    relref = sigglobal
    cmin = 0 F
    gmin = 1 pS

    tran: time = 2.63 ns     (2.92 %), step = 1.234 ns     (1.37 %)
    tran: time = 8.03 ns     (8.92 %), step = 1.8 ns          (2 %)
    tran: time = 11.76 ns    (13.1 %), step = 530.8 ps     (590 m%)
    tran: time = 17.01 ns    (18.9 %), step = 1.8 ns          (2 %)
    tran: time = 20.43 ns    (22.7 %), step = 186.6 ps     (207 m%)
    tran: time = 24.84 ns    (27.6 %), step = 1.8 ns          (2 %)
    tran: time = 30.05 ns    (33.4 %), step = 1.607 ns     (1.79 %)
    tran: time = 33.91 ns    (37.7 %), step = 1.128 ns     (1.25 %)
    tran: time = 38.66 ns      (43 %), step = 1.342 ns     (1.49 %)
    tran: time = 42.96 ns    (47.7 %), step = 1.396 ns     (1.55 %)
    tran: time = 48.36 ns    (53.7 %), step = 1.8 ns          (2 %)
    tran: time = 51.76 ns    (57.5 %), step = 530.7 ps     (590 m%)
    tran: time = 57.01 ns    (63.3 %), step = 1.8 ns          (2 %)
    tran: time = 60.8 ns     (67.6 %), step = 373.1 ps     (415 m%)
    tran: time = 66.64 ns      (74 %), step = 1.8 ns          (2 %)
    tran: time = 70.05 ns    (77.8 %), step = 1.607 ns     (1.79 %)
    tran: time = 75.52 ns    (83.9 %), step = 1.604 ns     (1.78 %)
    tran: time = 80 ns       (88.9 %), step = 1.342 ns     (1.49 %)
    tran: time = 84.76 ns    (94.2 %), step = 1.8 ns          (2 %)
    tran: time = 88.36 ns    (98.2 %), step = 1.8 ns          (2 %)
Number of accepted tran steps =             255
```

Figure 21: Transient Table of values

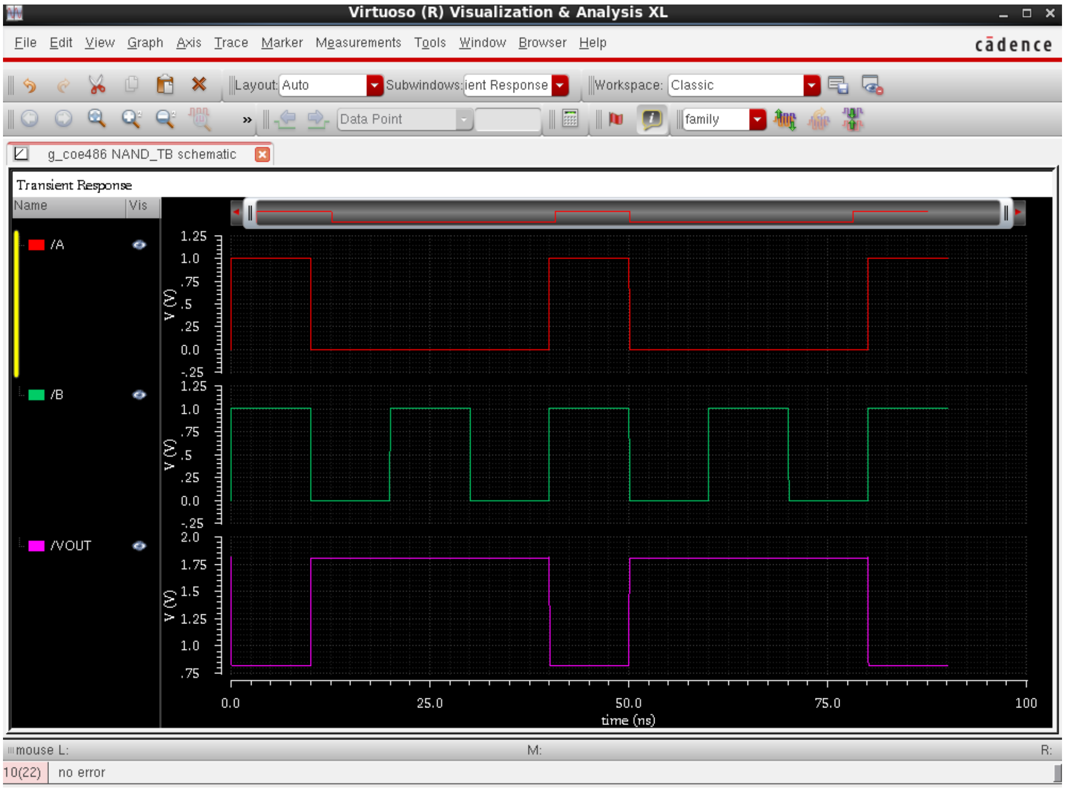


Figure 22: NAND simulation result

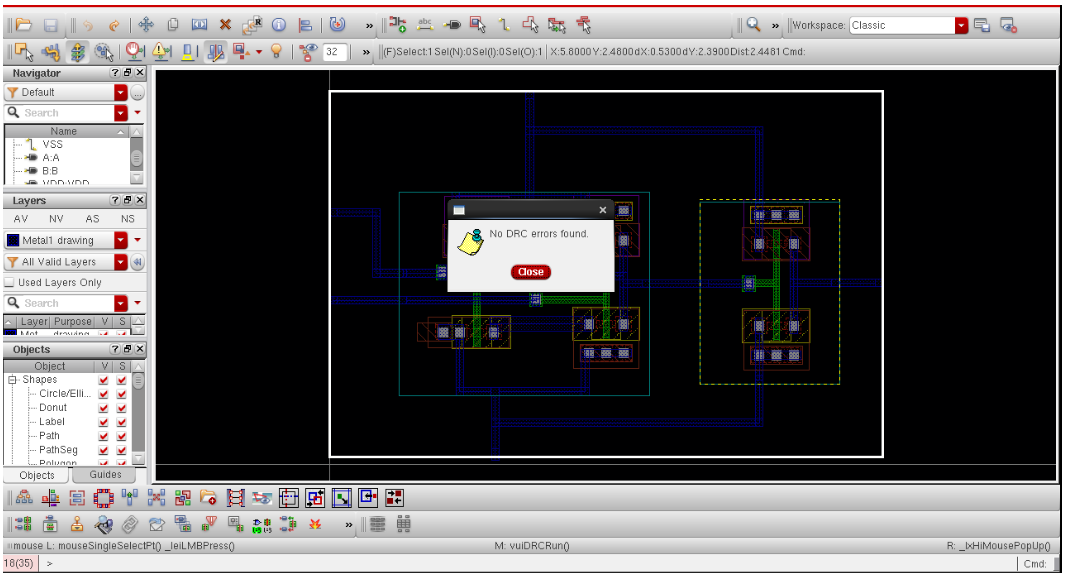
5.2.3 Truth tables

A	B	VOUT
0	1	0.257
0	0	0.300
1	1	0.0017
1	0	0.289

Table 1: NAND truth table observed

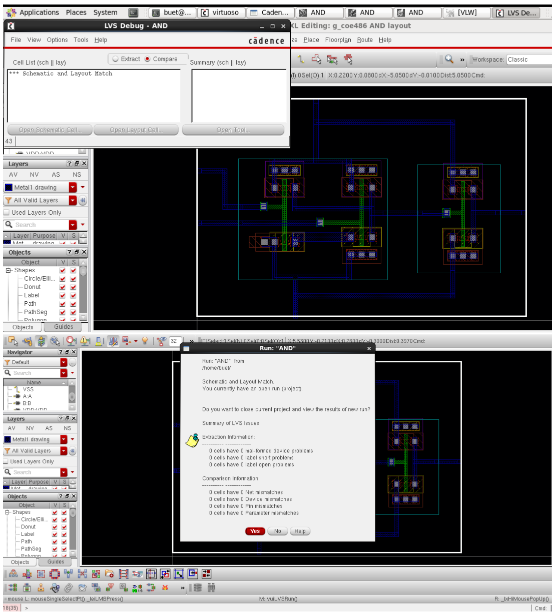
5.3 LAB 3: AND

5.3.1 DRC and LVS test Results



No DRC errors found.

Figure 23: DRC



```
*** Schematic and Layout Match
```

Run: "AND" from
/home/buet/

Schematic and Layout Match.
You currently have an open run (project).

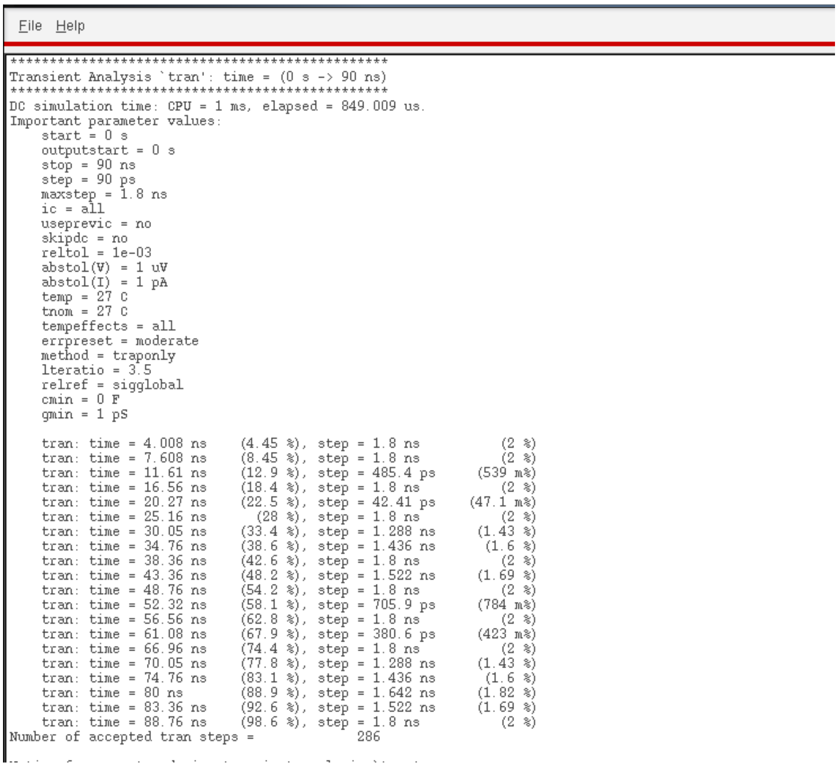
Do you want to close current project and view the results of new run?

Summary of LVS Issues

```
Extraction Information:
---------- -----------
    0 cells have 0 mal-formed device problems
    0 cells have 0 label short problems
    0 cells have 0 label open problems

Comparison Information:
---------- -----------
    0 cells have 0 Net mismatches
    0 cells have 0 Device mismatches
    0 cells have 0 Pin mismatches
    0 cells have 0 Parameter mismatches
```

Figure 24: LSV

5.3.2 Simulation Results



```
************************************************
Transient Analysis `tran': time = (0 s -> 90 ns)
************************************************
DC simulation time: CPU = 1 ms, elapsed = 849.009 us.
Important parameter values:
    start = 0 s
    outputstart = 0 s
    stop = 90 ns
    step = 90 ps
    maxstep = 1.8 ns
    ic = all
    useprevic = no
    skipdc = no
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    errpreset = moderate
    method = traponly
    lteratio = 3.5
    relref = sigglobal
    cmin = 0 F
    gmin = 1 pS

    tran: time = 4.008 ns    (4.45 %), step = 1.8 ns         (2 %)
    tran: time = 7.608 ns    (8.45 %), step = 1.8 ns         (2 %)
    tran: time = 11.61 ns    (12.9 %), step = 485.4 ps     (539 m%)
    tran: time = 16.56 ns    (18.4 %), step = 1.8 ns         (2 %)
    tran: time = 20.27 ns    (22.5 %), step = 42.41 ps    (47.1 m%)
    tran: time = 25.16 ns      (28 %), step = 1.8 ns         (2 %)
    tran: time = 30.05 ns    (33.4 %), step = 1.288 ns     (1.43 %)
    tran: time = 34.76 ns    (38.6 %), step = 1.436 ns      (1.6 %)
    tran: time = 38.36 ns    (42.6 %), step = 1.8 ns         (2 %)
    tran: time = 43.36 ns    (48.2 %), step = 1.522 ns     (1.69 %)
    tran: time = 48.76 ns    (54.2 %), step = 1.8 ns         (2 %)
    tran: time = 52.32 ns    (58.1 %), step = 705.9 ps     (784 m%)
    tran: time = 56.56 ns    (62.8 %), step = 1.8 ns         (2 %)
    tran: time = 61.08 ns    (67.9 %), step = 380.6 ps     (423 m%)
    tran: time = 66.96 ns    (74.4 %), step = 1.8 ns         (2 %)
    tran: time = 70.05 ns    (77.8 %), step = 1.288 ns     (1.43 %)
    tran: time = 74.76 ns    (83.1 %), step = 1.436 ns      (1.6 %)
    tran: time = 80 ns       (88.9 %), step = 1.642 ns     (1.82 %)
    tran: time = 83.36 ns    (92.6 %), step = 1.522 ns     (1.69 %)
    tran: time = 88.76 ns    (98.6 %), step = 1.8 ns         (2 %)
Number of accepted tran steps =             286
```

Figure 25: Transient Table of values

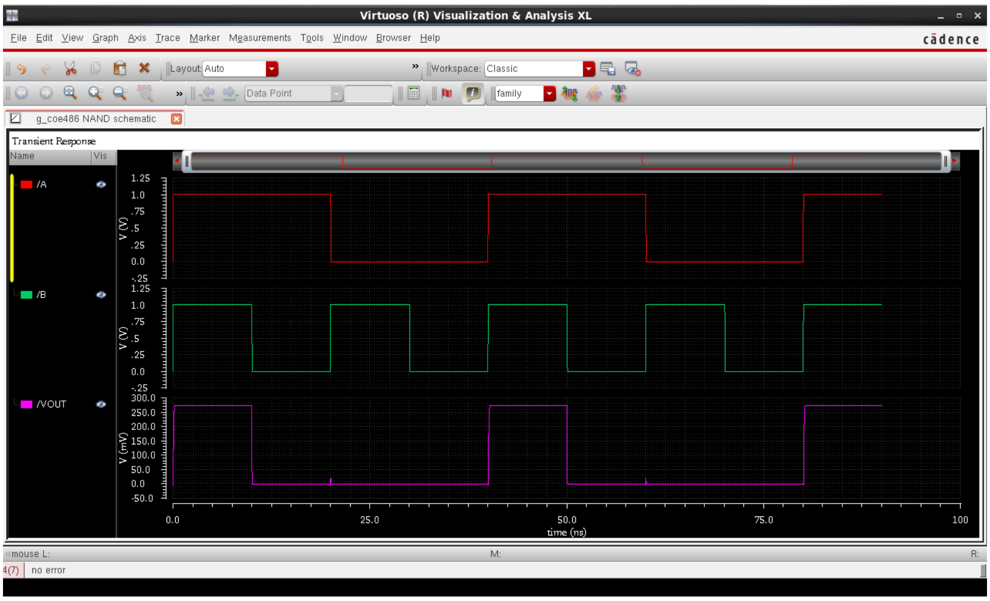


Figure 26: AND simulation result

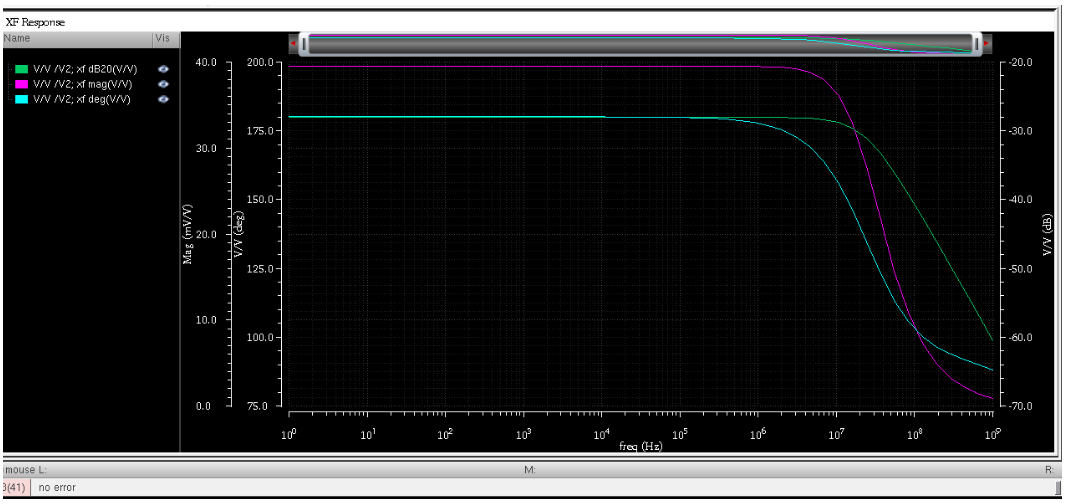
5.3.3 Truth tables

A	B	VOUT
0	1	0.0002
0	0	0.0017
1	1	0.3100
1	0	0.000

Table 2: AND truth table observed

5.4 LAB 4: Frequency Response

5.4.1 Simulation Results



XF Response

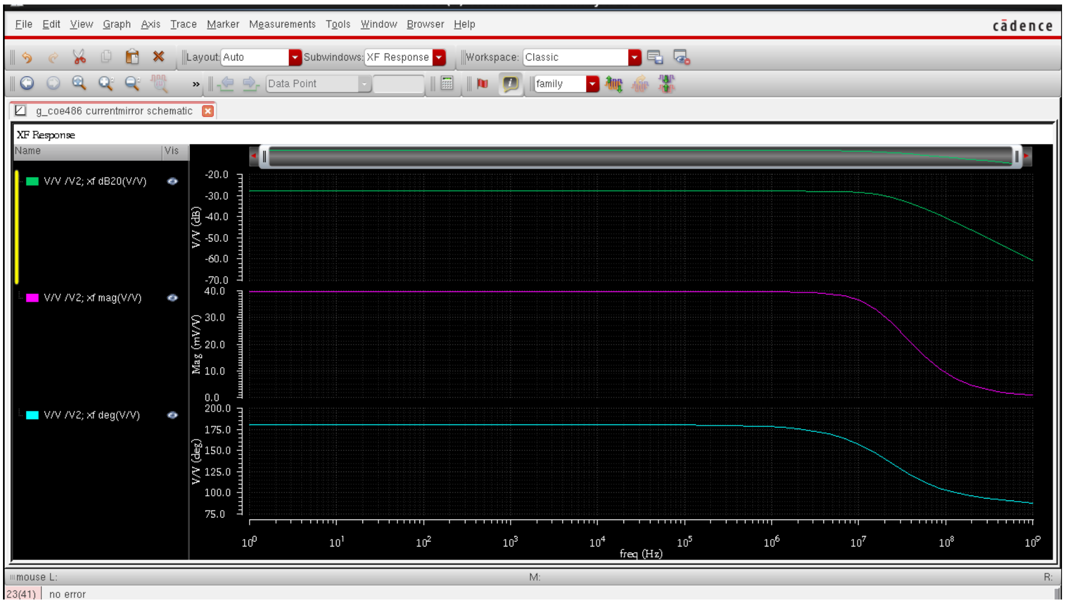
mouse L:

M:

R:

3(41) no error

Figure 27: Frequency Simulation Result



Layout: Auto

Subwindows: XF Response

Workspace: Classic

Data Point

family

g_coe486 currentmirror schematic

XF Response

mouse L:

M:

R:

23(41) no error

Figure 28: Frequency Simulation Result separated

6 Discussion

This section discusses the observations and deduction made in the entire labs.

6.1 LAB 1: Inverter

The result in figure 14 and figure 15 shows that a successful layout which obeys the design rule of the *gpdk090* technology. Also the LSV check guarantees that the layout in figure 4 matches the schematic shown in figure 2

The simulation result shown in figure 16 shows both DC and transient analysis for the inverter. The transient analysis shown verifies that the designed inverter returns a high signal whenever the input signal is low and vice versa. The DC analysis shows how the output signal gradually drops to zero when the input signal is gradually increased from 0 to 1.8(in this case).

6.2 LAB 2: NAND Gate

The result in figure 19 and figure 20 shows that a successful layout which obeys the design rule of the *gpdk090* technology. Also the LSV check guarantees that the layout in figure 7 matches the schematic shown in figure 5

The simulation result shown in figure 22 transient analysis for the NAND gate. The transient analysis shown verifies that the designed NAND gate obeys the NAND logic as shown in the truth table 1. The table shows that, the output signals is not exactly 1 like the input signal. This is due to the dissipation of power the transistor circuit.

6.3 LAB 3: AND Gate

The result in figure 23 and figure 24 shows that a successful layout which obeys the design rule of the *gpdk090* technology. Also the LSV check guarantees that the layout in figure 10 matches the schematic shown in figure 8

The simulation result shown in figure 26 transient analysis for the NAND gate. The transient analysis shown verifies that the designed NAND gate obeys the NAND logic as shown in the truth table 2. The table shows that, the output signals is not exactly 1 like the input signal. This is due to the dissipation of power the transistor circuit.

6.4 LAB 4: Frequency Response

The graph shows that at low frequencies, the signal remains almost constant until it reaches a certain frequency the cut off frequency. The calculation in section 4.4.1 shows how how this frequency can be determined. From the graph shown in figure 27 it can be estimated to approximately 10MHz. This frequency is the cut off frequency of the circuit above.

Since only low frequencies have relatively high gain, it can be concluded that this circuit can filter out high frequency signals. Thus this circuit can function as a low pass filter.

7 Conclusion

Conclusion This lab project provided hands-on experience in CMOS analog circuit design and simulation using Cadence tools. Key outcomes and findings include:

Inverter Design and Simulation: Successfully designed and simulated a CMOS inverter. Verification through DRC and LVS checks ensured the integrity of the design, while simulation results confirmed the functionality of the inverter, showcasing its expected performance in terms of DC and transient behavior.

NAND Gate Implementation: Designed and simulated a NAND gate, verifying its operation through a truth table and simulation results. The design passed DRC and LVS checks, demonstrating correct functionality and adherence to design rules.

AND Gate Design: Developed an AND gate using previously created components. The simulation results and truth table verification confirmed the accuracy of the design, with successful DRC and LVS checks.

Frequency Response Analysis: Performed frequency response analysis on a given circuit, estimating key parameters such as transconductance and output resistance. The frequency response simulations provided insights into the circuit's performance across different frequencies, validating theoretical predictions and enhancing understanding of high-frequency effects.

Overall, the labs effectively bridged theoretical concepts with practical applications, highlighting the importance of accurate design, verification, and simulation in CMOS analog circuit development.

8 References

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