數位邏輯設計-HW1　　鄭凱文　104062223

執行內容：

$$f(x,y) = (x \cup y) \cap \overline{(x \cap y)}$$
$$= (x \cup y) \cap (\bar{x} \cup \bar{y})$$

只有兩個變數，因此 count 為[1:0] 2bit，共有 $2^2 = 4$ 種結果。out = 1，則：

$(x \cup y)$ = 1　→　x, y 不能都為 0

$(\bar{x} \cup \bar{y})$ = 1　→　x ,y 不能都為 1

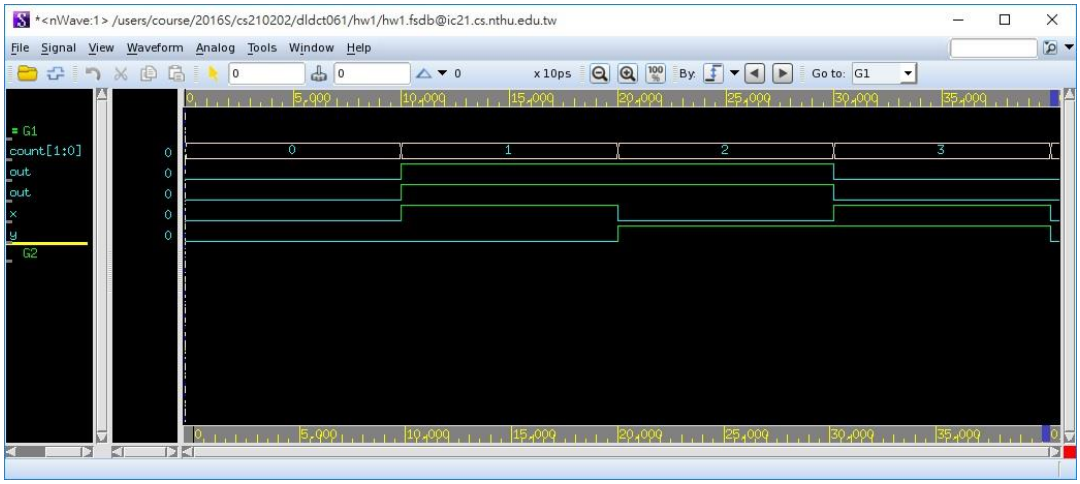
故(x,y) = $(1,0)$ or $(0,1)$，out = 1

Function 寫成程式即為：assign out = (x|y) & ~(x&y)

Simulation：

```
[dldct061@ic21 ~/hw1]$ ncverilog hw1_test.v hw1.v +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Loading snapshot worklib.hw1_test:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file m
ay crash the programs that are using this file.
*Verdi3* : Create FSDB file 'hw1.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
in = 00, out = 0
in = 01, out = 1
in = 10, out = 1
in = 11, out = 0
ncsim: *W,RNQUIE: Simulation is complete.
```

波形圖：



執行心得與問題：

第一次嘗試Verilog這種語言，跟初學C語言的時候一樣充滿著新奇，不過打法都大同小異，加上第一次作業並不難，只是簡單的邏輯運算搭配一個陌生的程式語言，操作上沒有太大的問題。

唯一的小問題是：有時開啟 nWave 時會藍底白字阿(似乎跟電腦的軟體有衝突)