Exercise 01

You do not need to turn in the answer sheet of exercises.

We have a few exercises for you. Please practice them by yourself.

1. Design a 3-input XOR circuit by using exactly one 3:8 decoder and one NOR gate.
2. Design a 16:1 binary-select multiplexer by using 2:1 binary-select MUXes.
3. Design a 3-input function $f(c, b, a)$ by using a 4:1 MUX. The output $f = 1$ only if the 3-bit value $\{c, b, a\} > 4$.
4. Exercise 14.25 (Let's do the simpler part, that is, only considering the `noelectronics` output signal.)
5. Design a 3-bit counter with D flip-flops that repeats the following sequence after reset: 0, 1, 5, 3, 0, 1, 5, 3, …, and so on. Therefore, the state diagram is a loop of 4 states, as shown in the figure below.
   (a) Draw the state table and design the logic diagram with logic optimization using K-map.
   (b) After the logic optimization of the FSM as in (a), draw the resultant state diagram with all the 8 states specifically.