SV/Verilog Testbench

```
1  //'timescale 1ns/1us
2  //at -> a_test, dt -> d_test
3  module dec3to8test();
4
5    reg [2:0]at;
6    wire [7:0]dt;
7    dec3to8 T1(at,dt);
8
9    initial
10     begin
11
12       $dumpfile("dump.vcd");
13       $dumpvars();
14
15       at = 3'b000; #5;
16       at = 3'b001; #5;
17       at = 3'b010; #5;
18       at = 3'b011; #5;
19       at = 3'b100; #5;
20       at = 3'b101; #5;
21       at = 3'b110; #5;
22       at = 3'b111; #5;
23
24     end
25
26 endmodule
```

design.sv

```
1  // 28/7/22 - 2010040027 -> 3 to 8 gate-level decoder modelling
2
3  module dec3to8(input [2:0]a, output [7:0]d);
4
5    wire [2:0] notw;
6
7    not g1(notw[2], a[2]); //a[2]'
8    not g2(notw[1], a[1]); //a[1]'
9    not g3(notw[0], a[0]); //a[0]'
10
11   and g4(d[0], notw[2], notw[1], notw[0]);
12   and g5(d[1], notw[2], notw[1], a[0]);
13   and g6(d[2], notw[2], a[1], notw[0]);
14   and g7(d[3], notw[2], a[1], a[0]);
15   and g8(d[4], a[2], notw[1], notw[0]);
16   and g9(d[5], a[2], notw[1], a[0]);
17   and g10(d[6], a[2], a[1], notw[0]);
18   and g11(d[7], a[2], a[1], a[0]);
19
20 endmodule
```

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