testbench.sv

SV/Verilog Testbench

```
//2010040027
//`timescale 1ns/1ps
module and1test();

  reg A, B;
  wire Y;
  and1 t1(Y, A, B);

  initial

    begin
      $dumpfile("dump.vcd");
      $dumpvars(1);
      A = 1'b0; B = 1'b0; #5;
      A = 1'b0; B = 1'b1; #5;
      A = 1'b1; B = 1'b0; #5;
      A = 1'b1; B = 1'b1; #5;
    end

endmodule
```

design.sv aordesign.sv

SV/Verilog Design

```
// Code your design here
module and1(Y, A, B);

  output Y;
  input A, B;

  and g1(Y, A, B);

endmodule
```