SV/Verilog Testbench

```
//'timescale 1ns/1us
//at -> a_test, dt -> d_test
module dec3to8test();

  reg [2:0]at;
  wire [7:0]dt;
  dec3to8 T1(at,dt);

  initial
    begin

      $dumpfile("dump.vcd");
      $dumpvars();

      at = 3'b000; #5;
      at = 3'b001; #5;
      at = 3'b010; #5;
      at = 3'b011; #5;
      at = 3'b100; #5;
      at = 3'b101; #5;
      at = 3'b110; #5;
      at = 3'b111; #5;

    end

endmodule
```

design.sv

SV/Verilog Design

```
// 28/7/22 - 2010040027 -> 3 to 8 data flow decoder modelling

module dec3to8(input [2:0]a, output [7:0]d);

  assign d[0] = ~a[2] & ~a[1] & ~a[0];
  assign d[1] = ~a[2] & ~a[1] & a[0];
  assign d[2] = ~a[2] & a[1] & ~a[0];
  assign d[3] = ~a[2] & a[1] & a[0];
  assign d[4] = a[2] & ~a[1] & ~a[0];
  assign d[5] = a[2] & ~a[1] & a[0];
  assign d[6] = a[2] & a[1] & ~a[0];
  assign d[7] = a[2] & a[1] & a[0];

endmodule
```

Log Share