```
1  //'timescale 1ns/1us
2  //at -> a_test, dt -> d_test
3  module mux_2_1test();
4
5    reg [1:0]at, st;
6    wire yt;
7    mux_2_1 T1(at,st,yt);
8
9    initial
10     begin
11
12       $dumpfile("dump.vcd");
13       $dumpvars();
14
15       st = 1'b0;
16       at = 2'b00; #5;
17       at = 2'b01; #5;
18       at = 2'b10; #5;
19       at = 2'b11; #5;
20
21       st = 1'b1;
22       at = 2'b00; #5;
23       at = 2'b01; #5;
24       at = 2'b10; #5;
25       at = 2'b11; #5;
26
27     end
28
29 endmodule
```

design.sv

SV/Verilog Design

```
1  // 28/7/22 - 2010040027 -> 2:1 MUX [DataFlow]
2
3  module mux_2_1(input [1:0]a, s,  output y);
4
5    assign y = s ? a[1] : a[0];
6
7  endmodule
```

EPWave