Collaborate

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testbench.sv

```
1  //2010040027
2  //`timescale 1ns/1ps
3  module prog3test();
4
5    reg in1, in2;
6    wire out;
7    prog3 t1(out, in1, in2);
8
9    initial
10
11     begin
12
13       $dumpfile("dump.vcd");
14       $dumpvars(1);
15
16       in1=1'b0; in2=1'b0; #10;
17       in1=1'b0; in2=1'b1; #10;
18       in1=1'b1; in2=1'b0; #10;
19       in1=1'b1; in2=1'b1; #10;
20
21     end
22
23 endmodule
```

design.sv

SV/Verilog Design

```
1  // Code your design here
2  module prog3(out, in1, in2);
3
4    output out;
5    input in1, in2;
6    wire x1;
```

```
7
8     not g1(x1, in2);
9     and g2(out, in1, x1);
10
11  endmodule
```

Log Share

```
[2022-07-21 00:20:15 EDT] iverilog '-Wall' design.sv testb
VCD info: dumpfile dump.vcd opened for output.
Finding VCD file...
./dump.vcd
[2022-07-21 00:20:18 EDT] Opening EPWave...
Done
```