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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Icarus Verilog 0.9.7

Compile Options

-Wall

Run Options

Run Options

- [x] Open **EPWave** after run
- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground) Follow

@edaplayground (https://twitter.com/edaplayground)

testbench.sv

```
1  //2010040027
2  //`timescale 1ns/1ps
3  module aortest();
4
5    reg A, B, C, D;
6    wire Y;
7    aor t1(Y, A, B, C, D);
8
9    initial
10
11     begin
12
13       $dumpfile("dump.vcd");
14       $dumpvars(1);
15
16       A=1'b0; B=1'b0; C=1'b0; D=1'b0; #5;
17       A=1'b0; B=1'b0; C=1'b0; D=1'b1; #5;
18       A=1'b0; B=1'b0; C=1'b1; D=1'b0; #5;
19       A=1'b0; B=1'b0; C=1'b1; D=1'b1; #5;
20       A=1'b0; B=1'b1; C=1'b0; D=1'b0; #5;
```

```
      A=1'b0; B=1'b1; C=1'b0; D=1'b1; #5;
      A=1'b0; B=1'b1; C=1'b1; D=1'b0; #5;
      A=1'b0; B=1'b1; C=1'b1; D=1'b1; #5;
      A=1'b1; B=1'b0; C=1'b0; D=1'b0; #5;
      A=1'b1; B=1'b0; C=1'b0; D=1'b1; #5;
      A=1'b1; B=1'b0; C=1'b1; D=1'b0; #5;
      A=1'b1; B=1'b0; C=1'b1; D=1'b1; #5;
      A=1'b1; B=1'b1; C=1'b0; D=1'b0; #5;
      A=1'b1; B=1'b1; C=1'b0; D=1'b1; #5;
      A=1'b1; B=1'b1; C=1'b1; D=1'b0; #5;
      A=1'b1; B=1'b1; C=1'b1; D=1'b1; #5;

    end

endmodule
```

design.sv

SV/Verilog Design

```
// Code your design here
module aor(Y, A, B, C, D);

  output Y;
  input A, B, C, D;
  wire x1, x2;

  and g1(x1, A, B);
  and g2(x2, C, D);
  or g3(Y, x1, x2);

endmodule
```

Log Share

```
[2022-07-20 23:56:20 EDT] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
Finding VCD file...
./dump.vcd
[2022-07-20 23:56:23 EDT] Opening EPWave...
Done
```