Vivado IP Flow Demo Script

Introduction

This demonstration introduces the IP flow, including:

- Upgrading IP
- Customizing IP
- Generating output products
- Instantiating IP
- Identifying the difference between the out-of-context flow (OOC) flow and global synthesis flow
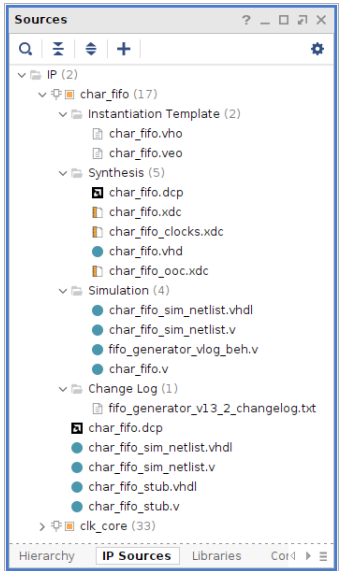
Preparation:

- Required files: `$TRAINING_PATH/IP_Flow/demo/KCU105/verilog`
- Required hardware: None
- Supporting materials: None

Vivado IP Flow

Action with Description	Point of Emphasis and Key Takeaway

• Launch the Vivado™ Design Suite.
• Unzip the project using the Tcl Console:
```exec unzip $::env(TRAINING_PATH)/IP_Flow/demo/KCU105/verilog.zip -d $::env(TRAINING_PATH)/IP_Flow/demo/KCU105/verilog```
	• The Getting Started page provides links to:
	  • Create a new project
	  • Open an existing project
	  • Open example projects
	  • Manage IP
	  • Open the hardware manager
	  • Visit the Vivado Store
	  • View documentation and QuickTake videos for the Vivado Design Suite

• Open the **wave_gen.xpr** project from the following directory: `$TRAINING_PATH/IP_Flow/demo/KCU105/verilog`	• You can easily open an existing Vivado IDE project via the Getting Started page.

Action with Description	Point of Emphasis and Key Takeaway
• Go to **IP Sources** in the Sources window, right-click **clk_core**, and select **Report IP Status**.	• The IP status tab shows the device part of the IP targeted, under *Current Part.* • In this demo, the *clk_core* IP is targeted to a Kintex™ 7 series device and the project is targeted to a Kintex UltraScale™ device. • The change log for the upgraded IP can also be viewed from IP Status tab.
• Right-click **clk_core** from the IP Sources tab and select **Upgrade IP**. • Right-click **clk_core** from the IP Sources tab and select **Generate Output Products.** • Click **Generate** in the dialog box to generate the output products for clk_core. • Click **OK** in the Generate Output Products dialog box.	• The IP Status tab after upgrading the IP shows that the *clk_core* IP is up-to-date. • For this demo, you do not need to enable the core container features for this IP.
• Rerun the IP Status report from **Reports** > **Report IP Status** to notice that the *clk_core* IP is up-to-date now.	
• Select **IP Catalog** from the Flow Navigator.	• The Vivado IP catalog provides consistent, easy access to our IP, including building blocks, wizards, connectivity, DSP, embedded, AXI infrastructure, and video IP from a single common repository regardless of the end application being developed. • Note that only one version of IP (i.e., the latest version of IP) will be available in the IP catalog.

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Action with Description	Point of Emphasis and Key Takeaway
• Search for and select **FIFO Generator** from the IP catalog.	• The IP catalog contains categories of IP that you can filter and search. • You can work with the IP catalog in a variety of ways. You can search using keywords in the search box or browse through the catalog in the various categories. • Selecting IP will list all the details of the selected IP: • Name, version, types of supported interfaces, brief description of IP, IP status, etc.

• Double-click to customize the **FIFO Generator** IP with the following parameters:
   • **Basic** tab > Component Name: **char_fifo**
   • FIFO Implementation: **Independent Clocks Built-in FIFO**
   • **Native ports** tab > Read Mode: **First Word Fall Through**
   • Write width: **8**
   • Write depth: **2048**
	• The selected IP can be customized by right-clicking and selecting **Customize IP** or double -click the IP.
	
	• In the Summary tab of the IP Customization dialog box you can verify that the information is correct and then generate the IP.
	
	• Once the customization is done, the Generate Output Products dialog box opens.

• Click **OK** and click **Generate** in the dialog box to generate the output products with the default settings (OOC flow). • Click **OK** if the Generate Output Products dialog box prompts.	• By default, the **Synthesized Checkpoint (.dcp)** is generated, and an Out-of-Context Module Run for the *char_fifo* IP is added to the Design Runs window. • The new run is created and launched to synthesize the IP. • When the entire design is synthesized, an HDL stub module is provided in the DCP, which causes a black box to be inferred for the IP. • This OOC flow reduces synthesis run times because the IP is synthesized only once. If the top-level design is changed and has to be synthesized, the IP is not re-synthesized. • The synthesis log file can be viewed from the properties window by selecting the created IP run from the Design Runs window.

Action with Description	Point of Emphasis and Key Takeaway
In the Log table tab next to TCL Console tab, select the **char_fifo_synth_1** and see the log file. 	

• Select the **IP Sources** tab to examine the output products that are generated.
 	
	• The IP Sources window shows the generated output products.
	
	 • By default, the IP will generate:
	
	   • Instantiation template
	   • Synthesis files
	     ▪ Constraints files associated with synthesis
	   • Simulation files
	     ▪ Simulation sources associated with IP
	   • Change log
	   • Design checkpoint (*.dcp*)
	     ▪ Synthesizes the IP and generates the DCP file in OOC mode
	   • Simulation netlist and stub files

• View the instantiation template that is generated for *char_fifo*. • Since it is already been instantiated, you can view it in the **Hierarchy** tab under the top-level file (*wave_gen*).	• After the IP is generated, if the IP is not instantiated in the design it will be added at the same level as the top-level wave_gen module in the Hierarchy tab. • The IP has already been instantiated in the design. To view the instantiation, open the *wave_gen.v* file in the text editor and observe lines 338 to 350. • Notice that the Hierarchy, Libraries, and Compile Order tabs are updated to indicate that the IP has been instantiated into the design.

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Action with Description	Point of Emphasis and Key Takeaway

• Observe the directory structure of the generated output products for the IP.
 	
   • Browse to the `$TRAINING_PATH/ IP_Flow/demo/KCU105/verilog/ wave_gen.srcs/sources_1/ip` directory.
   • Notice that there is one directory for each IP.
	• The *clk_core* directory contains the output products for the *clk_core* IP.
	
	 • The *char_fifo* directory contains the output products for the *char_fifo* IP.

• Examine the output products for the *char_fifo* IP in the IP Sources tab of the Sources view.
 	
   • Select the **IP Sources** tab in the Sources window.
   • Expand the **char_fifo** and **clk_core** folders and observe that the outputs products for both IPs are the same.
	• Within the Vivado IDE Sources view, the two IP appear the same, both listing the output products, all of which can be opened for viewing from within the Vivado IDE.

• Generate the output products for *char_fifo* by using the global synthesis flow.
 	
   • Right-click **char_fifo** in the IP Sources window and select **Generate Output Products**.
   • Select the **Global** option in the Synthesis Options section and click **Generate** in the Generate the output products section.
   • Click **OK** if the Generate Output Products dialog box appears.
	• Note that new design run for *char_fifo* is not created as in the OOC flow.
	
	 • Now, the *char_fifo* IP output products will be generated while synthesizing the top-level design.

• Synthesize the design.	• The *char_fifo* IP gets synthesized along with the top-level design.

Action with Description	Point of Emphasis and Key Takeaway

• Right-click the **char_fifo** IP and select **Remove File from Project** to delete the *char_fifo* IP from the IP Sources window.
 	
   • Also, make sure that the IP files are removed from the project directory.
 	
• Run a Tcl script to generate the *char_fifo* IP.
 	
   • Run the Tcl script from the Tcl Console by using the following command:
 	
     `source $::env(TRAINING_PATH)/`
     `IP_Flow/demo/KCU105/verilog/`
     `char_fifo_run.tcl`
 	
   • View the Tcl script and output products generated for *char_fifo*.
	• IP can be created and customized by using Tcl commands such as `create_ip` and `set_property`.
	
	• The `generate_target` command is used to generate output products.

• Select **File** > **Exit** to close the Vivado Design Suite.	

Summary

This demonstration showed you the IP flow, use of the core container feature, and the difference between out-of-context (OOC) and global synthesis flow.

References:

- Supporting materials
  - *Vivado Design Suite User Guide: Design with IP* (UG896)
  - Using Core Containers for IP Quick Take video

    www.xilinx.com/training/vivado/using-core-containers-for-ip.htm

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