Introduction to Vivado Reports Demo Script

Introduction

This demonstration script provides high-level instructions on the timing reports available in the AMD Vivado™ Design Suite that can be used in design timing analysis.

Preparation:

- Required files: `$TRAINING_PATH/Timing_Reports_Intro/demo/ZCU104/verilog`
- Required hardware: None
- Supporting materials: None

Introduction Vivado Timing Reports

Action with Description	Point of Emphasis and Key Takeaway
• Launch the Vivado Design Suite. • Unzip the project using the Tcl Console: `exec unzip $::env(TRAINING_PATH)/Timing_Reports_Intro/demo/ZCU104/verilog.zip -d $::env(TRAINING_PATH)/Timing_Reports_Intro/demo/ZCU104/verilog`	• The Getting Started page provides links to perform various actions.
• Open the **uart_led.xpr** project from the following directory: `$TRAINING_PATH/Timing_Reports_Intro/demo/ZCU104/verilog`	• The Open Project link in the Getting Started helps you to open any existing project.

• Review the **Project Summary** window.	• The Project Summary window provides a quick check for design progress.
	• The Project Summary window provides design information such as:
	  • Targeted device family
	  • Top module name
	  • Synthesis status information
	  • Implementation process status information
	  • DRC violations
	  • Timing
	  • Utilization
	  • Power

Action with Description	Point of Emphasis and Key Takeaway
• Open the synthesized design from the Flow Navigator > Netlist Analysis.	• You can open the synthesized design from the Tcl Console. • Almost all actions that you can perform in the GUI can be done from Tcl Console as well.
• Explore the reports available in the Flow Navigator.	• The Vivado Design Suite provides many design analysis reports, such as the Timing Summary report, Utilization report, Power report, Clock Networks report, etc.

• Click **Report Timing Summary** from the Flow Navigator.
  • Click the **Question Mark** icon (**?**) in the Report Timing Summary dialog box to see information on what is covered in Report Timing Summary report.
  • Click **X** in Quick Help to close the help dialog box.
  • Select the default settings and click **OK** in the Report Timing Summary dialog box.
• Alternatively, you can also open it through the menu **Reports** > **Timing** > **Report Timing Summary** in the Vivado IDE.
• The equivalent Tcl command is `report_timing_summary`.
	• The Report Timing summary dialog box contains three tabs: Options, Advanced, and Timing Settings:
	  • The Options tab allows you to customize the path delay type, number of paths to be displayed in the report, report unconstrained paths, etc.
	  • The Advanced tab allows you to write the report to a text file, customize the report from a cell, show input pins in the path, and report unique pins (eliminates duplication of paths) in the timing report.
	  • The Timer Settings tab allows you to customize the interconnect delay of the paths, speed grade, etc.
	  • At this stage, this report consists of estimated timing numbers since actual place and route details are not available.

• Optional: Generate a Timing Summary report using the Tcl Console command `report_timing_summary -name timing_1`. • **Hint:** Use the `-name` option to view the report graphically. • Notice the difference between the Timing Summary report with and without the `-name timing_1` option.	• The Tcl Console allows you to generate various reports using Tcl commands. • Without the `-name` option the Tcl Console Timing Summary report displays in text. • The comprehensive information contained in the Timing Summary Report is similar to the information provided by several reports available from the Vivado IDE (Report Clock Interaction, Report Pulse Width, Report Timing, Check Timing) and to some of the reports available in Tcl only (report_clocks).

Action with Description	Point of Emphasis and Key Takeaway
• Review the different sections of the Timing Summary report. • Explore the **Show only failing checks** icon.	• The Timing Summary report contains the Design Summary, Check Timing, Intra-Clocks, Inter-Clocks sections, etc. • The Check Timing section provides information on missing timing constraints, such as clock, I/O delay constraints, etc. • After implementation, the Timing Summary report is often used as a sign-off timing report. • Therefore generating the Timing Summary report at implementation is recommended.
• Open the Timing report through the menu **Reports** > **Timing** > **Check Timing** in the Vivado IDE. • Click **OK** in the Check Timing dialog box.	• The Check Timing report contains information about missing timing constraints or paths with constraints issues that need to be reviewed. • For complete timing signoff, all path endpoints must be constrained.
• Open the Timing report through the menu **Reports** > **Timing** > **Report Timing** in the Vivado IDE. • Click the **Question Mark** icon (**?**) in the Report Timing dialog box provides information what is covered in Report Timing report. • Click **X** in Quick Help to close the help dialog box. • Click **OK** in the Report Timing dialog box.	• The Report Timing dialog box lets you generate a timing report for specific paths in the design. • The Report Timing command is similar to the timing summary but it provides more options in the dialog box to customize the timing report.
• Select any timing path from the Timing report and right-click and select Path Properties. • Alternately, double-click the selected timing path. • Review the values for Slack, Requirement, Source, Destination, Logic Levels, clock skew, and path group fields in the Path properties. • Close the report.	• The path properties of the timing path provide more detailed information about the path, such as the number of logic levels, clock skew, clock uncertainty, etc. • The path properties view of the timing path provides detailed information that enables analyzing and debugging the failed timing path (if any).

Action with Description	Point of Emphasis and Key Takeaway
• Click **Report Clock Networks** under Synthesized Design in the Flow Navigator. • You can also generate the report from the Tcl Console. • Expand the **clk_pin_p** tree and observe how the logic is built from the sysClk input pin to the MMCM input.	• The Clock Networks report provides the tree structure of each primary clock and loads clocked by the primary clock in the respective tree.
• Click **Report Clock Interaction** under Synthesized Design in the Flow Navigator.	• The Clock Interaction report analyzes the timing paths that cross from one clock domain to another. • The report displays the analysis in a nice graphical view.
• Open the implemented design. **Note:** Close the synthesized design before opening the implemented design.	
• Explore the other implementation reports available in the Flow Navigator.	• The Vivado Design Suite provides many design analysis reports, such as the Timing Summary report, Utilization report, Power report, Clock Networks report, etc.
• Generate the same Timing reports that you generated on synthesized design.	• The reports generated after implementation are the most accurate.
• Select **File** > **Exit**.	• This option closes the Vivado Design Suite.

Summary

In this demo, you explored various reports for a synthesized and implemented design.