



# Pynq Electrochemical Sensor

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## 1. Linux USB 開機自動掛載

Device	Boot	Start	End	Sectors	Size	Id	Type
/dev/mmcblk0p1	*	2048	206847	204800	100M	c	W95 FAT32 (LBA)
/dev/mmcblk0p2		206848	60735487	60528640	28.9G	83	Linux

Disk /dev/sdb: 29.7 GiB, 31914983424 bytes, 62333952 sectors  
Units: sectors of 1 \* 512 = 512 bytes  
Sector size (logical/physical): 512 bytes / 512 bytes  
I/O size (minimum/optimal): 512 bytes / 512 bytes  
Disklabel type: dos  
Disk identifier: 0xc21055c3

Device	Boot	Start	End	Sectors	Size	Id	Type
/dev/sdb1		8192	62333951	62325760	29.7G	c	W95 FAT32 (LBA)

```
xilinx@pynq:~$ sudo
Display all 1931 possibilities? (y or n)
xilinx@pynq:~$ sudo mount /dev/
Display all 157 possibilities? (y or n)
```

block/	ram12	tty23	tty6
btrfs-control	ram13	tty24	tty60
bus/	ram14	tty25	tty61
char/	ram15	tty26	tty62
console	ram2	tty27	tty63
cpu_dma_latency	ram3	tty28	tty7
disk/	ram4	tty29	tty8
dri/	ram5	tty3	tty9
fd/	ram6	tty30	ttyPS0
fpga0	ram7	tty31	uio0
full	ram8	tty32	urandom
gpiochip0	ram9	tty33	vcs
iio:device0	random	tty34	vcs1
initctl	sdb	tty35	vcs2
kmsg	sdb1	tty36	vcs3
log	sdc	tty37	vcs4
loop0	sg0	tty38	vcs5
loop1	sg1	tty39	vcs6
loop2	shm/	tty4	vcsa
loop3	snd/	tty40	vcsa1
loop4	stderr	tty41	vcsa2
loop5	stdin	tty42	vcsa3
loop6	stdout	tty43	vcsa4
loop7	tty	tty44	vcsa5
loop-control	tty0	tty45	vcsa6
mapper/	tty1	tty46	vcsu
mem	tty10	tty47	vcsu1
mmcblk0	tty11	tty48	vcsu2

loop7	tty	tty44	vcsa5
loop-control	tty0	tty45	vcsa6
mapper/	tty1	tty46	vcsu
mem	tty10	tty47	vcsu1
mmcblk0	tty11	tty48	vcsu2
mmcblk0p1	tty12	tty49	vcsu3
mmcblk0p2	tty13	tty5	vcsu4
mqueue/	tty14	tty50	vcsu5
net/	tty15	tty51	vcsu6
null	tty16	tty52	vga_arbiter
port	tty17	tty53	watchdog
ptmx	tty18	tty54	watchdog0
pts/	tty19	tty55	xlnc
ram0	tty2	tty56	zero
ram1	tty20	tty57	
ram10	tty21	tty58	
ram11	tty22	tty59	

```
xilinx@pynq:~$ sudo mount /dev/sdb
```

```
sdb sdb1
```

```
xilinx@pynq:~$ sudo mount /dev/sdb1 /
```

bin/	lost+found/	sbin/
boot/	media/	sds_trace_data.dat
dev/	mnt/	srv/
etc/	opt/	sys/
home/	proc/	tmp/
lib/	root/	usr/
lib64/	run/	var/

```
xilinx@pynq:~$ sudo mount /dev/sdb1 /home/xilinx/usbstorage
```

```
xilinx@pynq:~$ cd /home/xilinx/usbstorage/
```

```
xilinx@pynq:~/usbstorage$ ls
```

```
'System Volume Information'
```

```
xilinx@pynq:~/usbstorage$
```

# 開機自動mount

```
xilinx
-bash: xilinx: command not found
xilinx@pynq:~$ sudo blkid
[sudo] password for xilinx:
/dev/mmcblk0: PTUUID="33821ab6" PTTY="dos"
/dev/mmcblk0p1: SEC_TYPE="msdos" UUID="D25F-20D1" TYPE="vfat" PARTUUID="33821ab6-01"
/dev/mmcblk0p2: UUID="4573de46-64a6-4219-bcaf-1b50922057e6" TYPE="ext4" PARTUUID="33821ab6-02"
/dev/sda1: UUID="7609-00DA" TYPE="vfat" PARTUUID="c21055c3-01"
xilinx@pynq:~$
```

`$sudo nano /etc/fstab` #進入nano編輯器

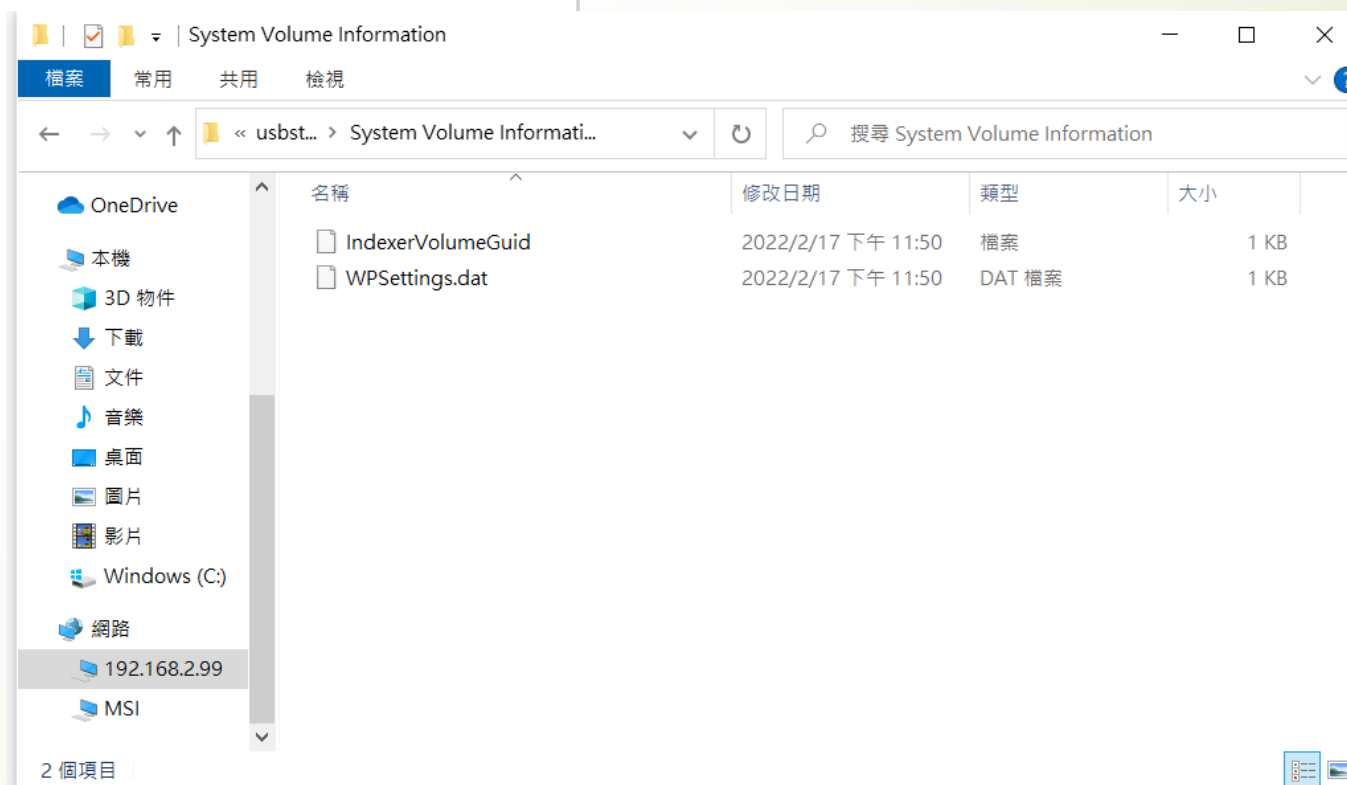
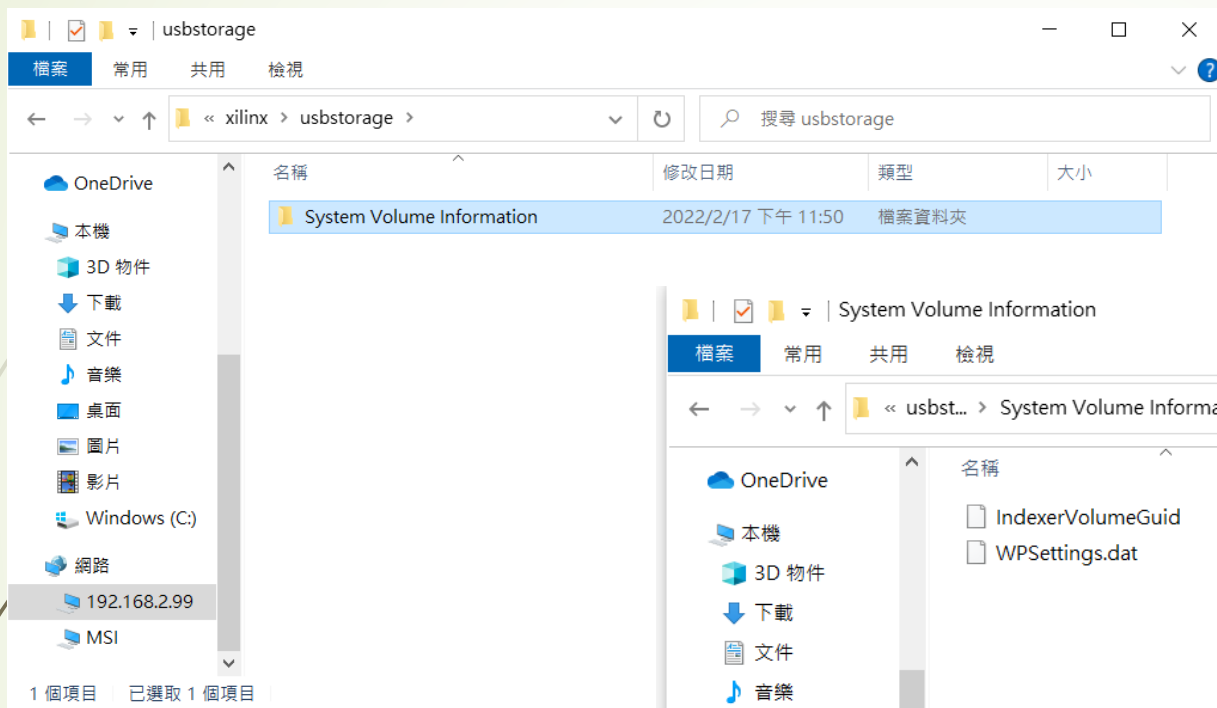
在最後加入這一行：

`UUID="7609-00DA" /home/Xilinx/usbstorage vfat rw,defaults 0 0`

然後下指令測試：

`$ sudo mount -a` #列出mount裝置

# Samba dir.





## 2. Hardware design with pynq(zynq) & python API



# In-House FPGA-Based POCT System

FPGA  
Microcontroller

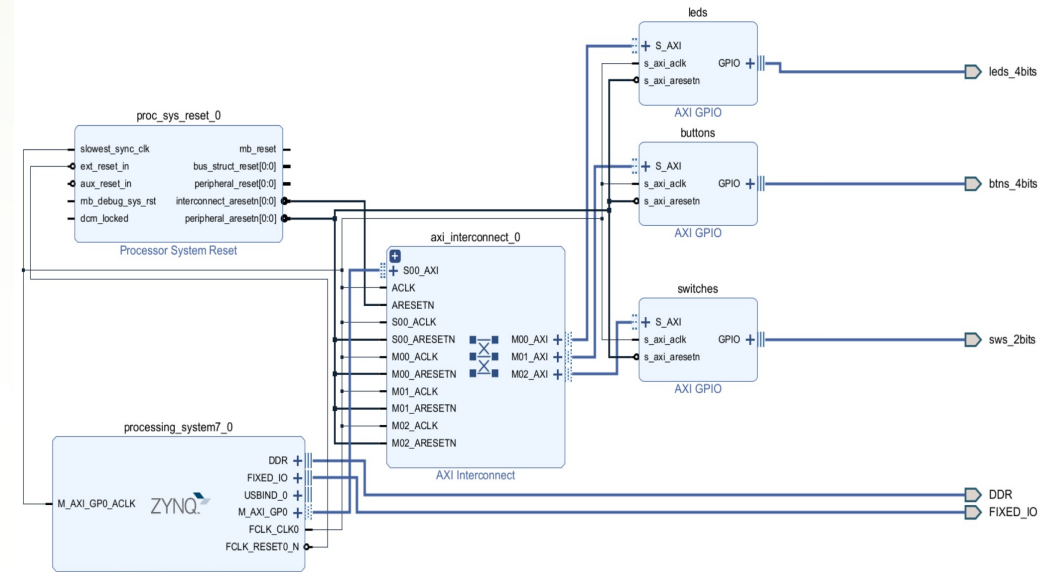
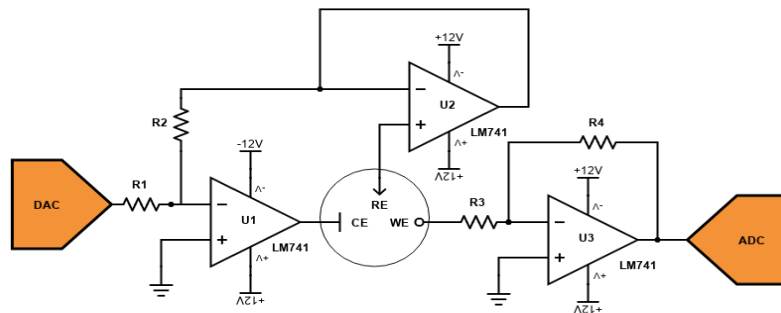
Sensor switch

Power switch

Cyclic  
voltammetry  
circuit

Detection  
module

PYNQ-Z1



ZYNQ7 Processing System

ol = BaseOverlay("base.bit")

dac = Pmod\_DAC(ol.PMODB)

adc = Pmod\_ADC(ol.PMODA)

adc.reset()

time\_fuc = np.linspace(0,40,2000) # 時間

x = 1\*(1-abs(signal.sawtooth( 2 \* np.pi \* 0.025 \* time\_fuc ))) # 產生三角波

V\_value = []

V\_out\_samples = []

sleep\_time = 0.02

tic = time()

# 主執行緒繼續執行自己的工作

for value in x:

dac.write(value)

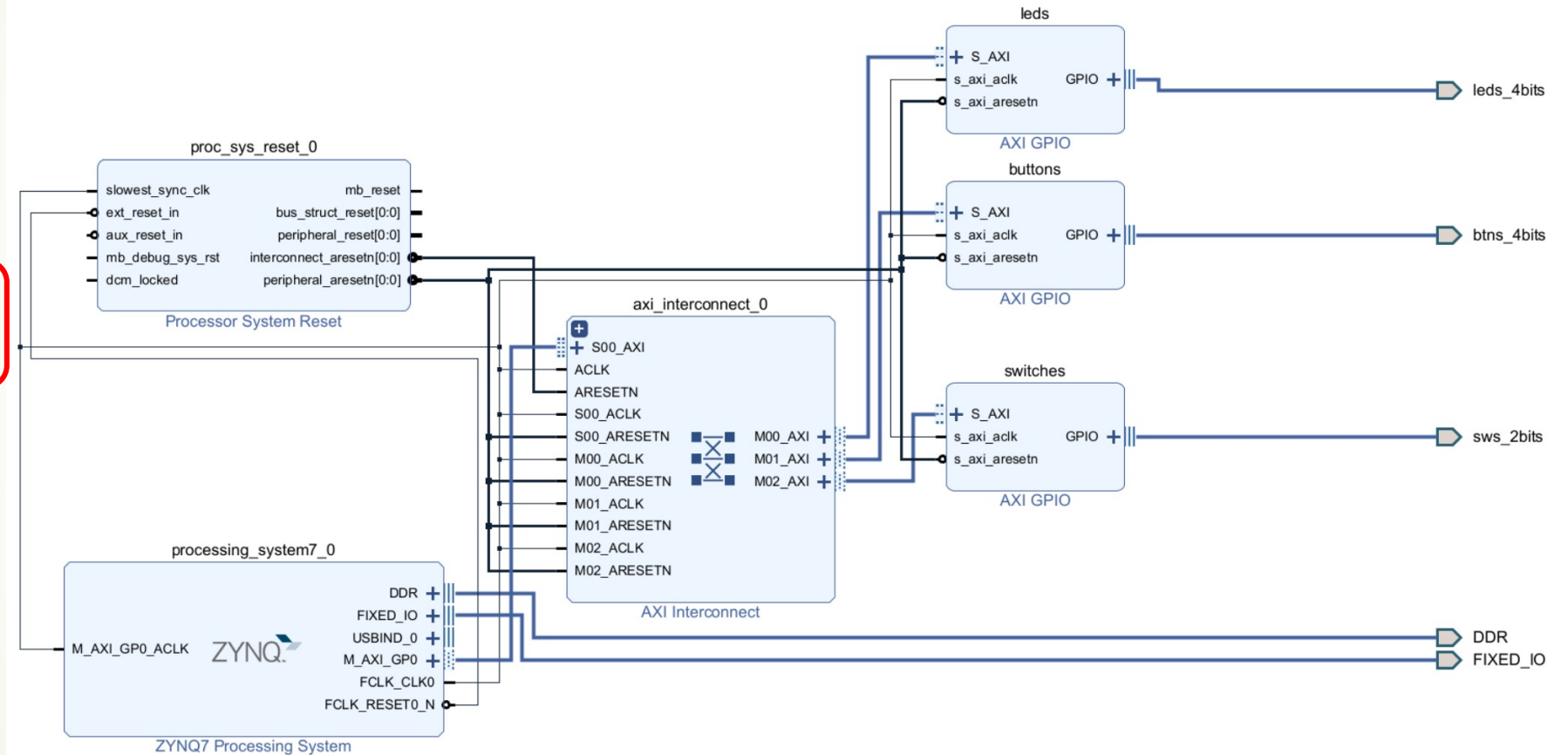
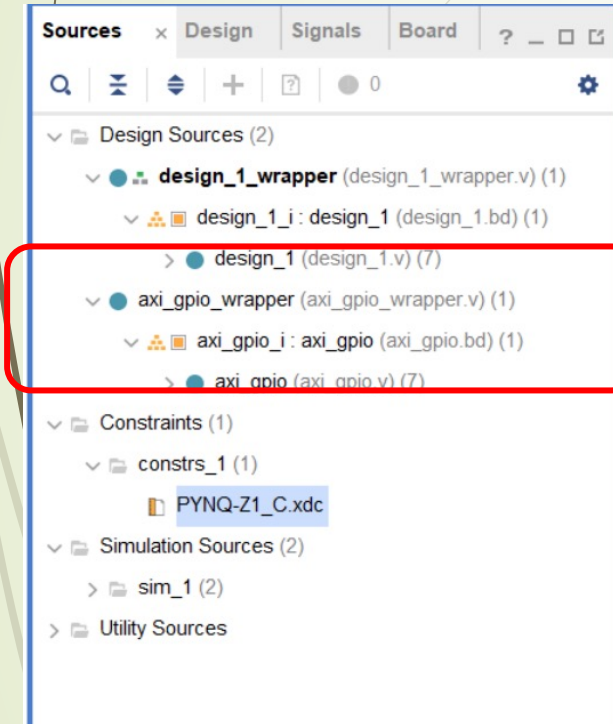
sample = adc.read()

V\_out\_samples.append(sample[0])

sleep(sleep\_time)

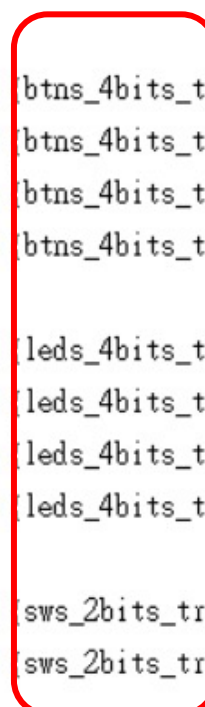

# 等待 t 這個子執行緒結束

# Hardware in vivado





# Constraint



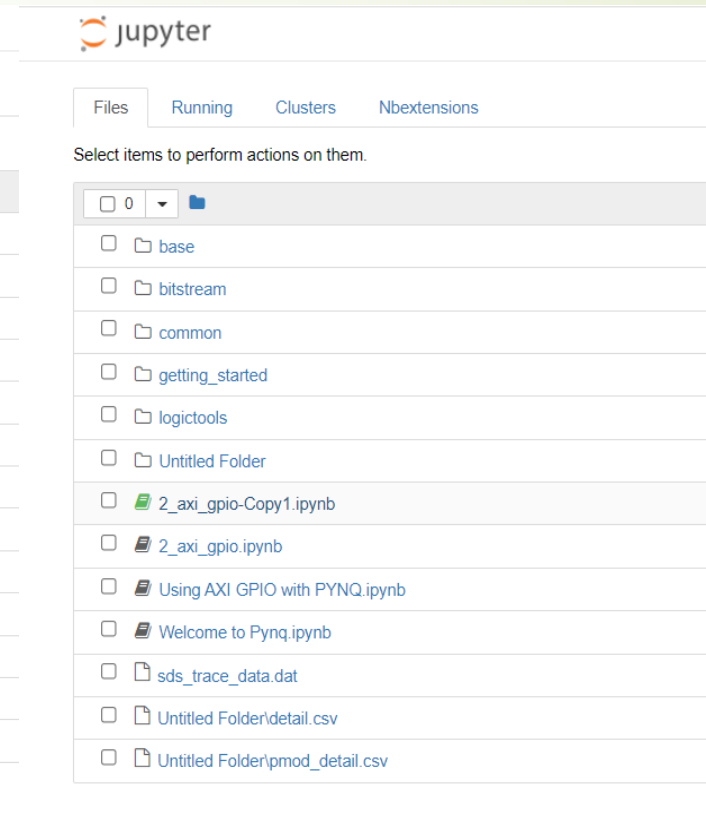
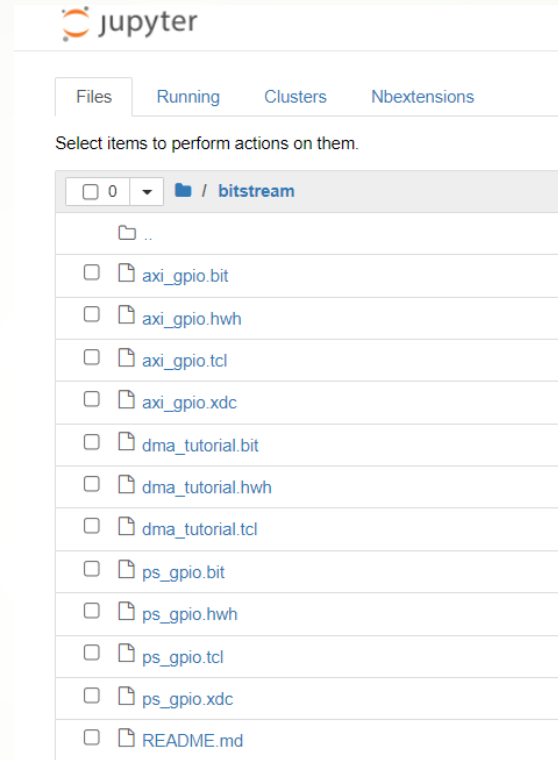
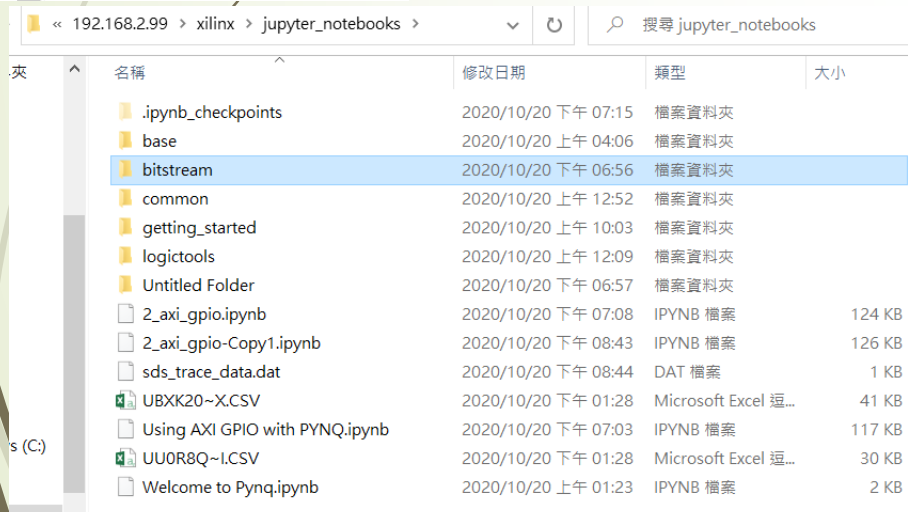
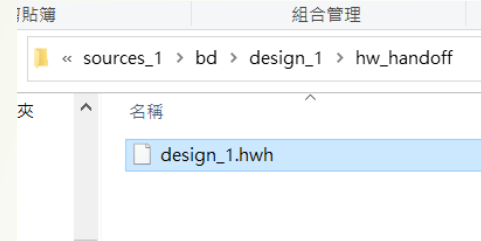
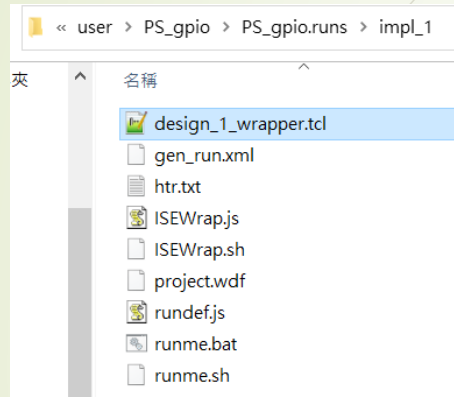
```
Diagram x Address Editor x Address Map x PYNQ-Z1_C.xdc x
C:/Users/user/Desktop/PYNQ/PYNQ-Z1_C.xdc
lines (10 sloc) 919 Bytes
1
2
3 set_property -dict {PACKAGE_PIN D19 IOSTANDARD LVCMOS33} [get_ports btns_4bits_tri_io[0]]
4 set_property -dict {PACKAGE_PIN D20 IOSTANDARD LVCMOS33} [get_ports btns_4bits_tri_io[1]]
5 set_property -dict {PACKAGE_PIN L20 IOSTANDARD LVCMOS33} [get_ports btns_4bits_tri_io[2]]
6 set_property -dict {PACKAGE_PIN L19 IOSTANDARD LVCMOS33} [get_ports btns_4bits_tri_io[3]]
7
8 set_property -dict {PACKAGE_PIN R14 IOSTANDARD LVCMOS33} [get_ports leds_4bits_tri_io[0]]
9 set_property -dict {PACKAGE_PIN P14 IOSTANDARD LVCMOS33} [get_ports leds_4bits_tri_io[1]]
10 set_property -dict {PACKAGE_PIN N16 IOSTANDARD LVCMOS33} [get_ports leds_4bits_tri_io[2]]
11 set_property -dict {PACKAGE_PIN M14 IOSTANDARD LVCMOS33} [get_ports leds_4bits_tri_io[3]]
12
13 set_property -dict {PACKAGE_PIN M20 IOSTANDARD LVCMOS33} [get_ports sws_2bits_tri_io[0]]
14 set_property -dict {PACKAGE_PIN M19 IOSTANDARD LVCMOS33} [get_ports sws_2bits_tri_io[1]]
```

# HWH & Tcl export

The screenshot displays the Xilinx IDE interface. The **Sources** panel on the left shows a project hierarchy under **Design Sources (2)**. The **design\_1\_wrapper** node is expanded, showing **design\_1\_i : design\_1 (design\_1.bd) (1)** and **axi\_gpio\_wrapper (axi\_gpio\_wrapper.v) (1)**. The **axi\_gpio\_wrapper** node is further expanded, showing **axi\_gpio\_i : axi\_gpio (axi\_gpio.bd) (1)** and **axi\_gpio (axi\_gpio.v)**. A context menu is open over the **axi\_gpio\_i** node, with the option **Create HDL Wrapper...** highlighted. The **Address Editor** panel on the right shows the address range **C:/Users/user/Desktop/PYNQ/PYNQ** and the address **lines (10 sloc) 919 Bytes**. The **Flow Navigator** panel on the far right shows the project workflow, including **PROJECT MANAGER**, **IP INTEGRATOR**, **SIMULATION**, **RTL ANALYSIS**, **SYNTHESIS**, **IMPLEMENTATION**, and **PROGRAM AND DEBUG**. The **SYNTHESIS** section is expanded, showing **Run Synthesis** and **Open Synthesized Design**. The **IMPLEMENTATION** section is also expanded, showing **Run Implementation** and **Open Implemented Design**. The **PROGRAM AND DEBUG** section is expanded, showing **Generate Bitstream** and **Open Hardware Manager**. The **Warnings** panel at the bottom shows a warning about the board interface **/switches/GPIO** and a critical warning about two separate IP interfaces **/switches/GPIO** and **/buttons/GPIO** being associated to common resources. The console output shows the following messages:

```
WARNING: [BD 41-1771] Block interface /switches/GPIO has associated board param 'GPIO_BOARD_INTERFACE', which is set to board pa
This is a visual-only issue - this interface /switches/GPIO will be connected to board interface 'btns_4bits'. If desired, please
CRITICAL WARNING: [BD 41-1077] Two separate IP interfaces "/switches/GPIO" and "/buttons/GPIO" should not be associated to common
Wrote : <C:/Users/user/PS_gpio/PS_gpio.srcs/sources_1/bd/design_1/ui/bd_1f5defd0.ui>
Verilog Output written to : c:/Users/user/PS_gpio/PS_gpio.gen/sources_1/bd/design_1/synth/design_1.v
Verilog Output written to : c:/Users/user/PS_gpio/PS_gpio.gen/sources_1/bd/design_1/sim/design_1.v
Verilog Output written to : c:/Users/user/PS_gpio/PS_gpio.gen/sources_1/bd/design_1/hdl/design_1_wrapper.v
Exporting to file c:/Users/user/PS_gpio/PS_gpio.gen/sources_1/bd/design_1/hw_handoff/design_1.hwh
Generated Hardware Definition File c:/Users/user/PS_gpio/PS_gpio.gen/sources_1/bd/design_1/synth/design_1.hwdef
```

# HWH & Tcl to local



```
181     return
182 }
183
184 # Save current instance; Restore later
185 set oldCurInst [current_bd_instance .]
186
187 # Set parent object as current
188 current_bd_instance $parentObj
189
190
191 # Create interface ports
192 set DDR [ create_bd_intf_port -mode Master -vlnv xilinx.com:interface:ddrx_rtl:1.0 DDR ]
193 set FIXED_IO [ create_bd_intf_port -mode Master -vlnv xilinx.com:display_processing_system7:fixedio_rtl:1.0 FIXED_IO ]
194
195 # Create ports
196 set buttons [ create_bd_port -dir I -from 3 -to 0 buttons ]
197 set leds [ create_bd_port -dir O -from 3 -to 0 leds ]
198 set switches [ create_bd_port -dir I -from 1 -to 0 switches ]
199
200 # Create instance: buttons_switches, and set properties
201 set buttons_switches [ create_bd_cell -type ip -vlnv xilinx.com:ip:xlconcat:2.1 buttons_switches ]
202
203 # Create instance: leds, and set properties
204 set leds [ create_bd_cell -type ip -vlnv xilinx.com:ip:xlslice:1.0 leds ]
205 set_property -dict [ list \
206     CONFIG.DIN_FROM {9} \
207     CONFIG.DIN_TO {6} \
208     CONFIG.DIN_WIDTH {64} \
209     CONFIG.DOUT_WIDTH {4} \
210 ] $leds
211
212 # Create instance: processing_system7_0, and set properties
213 set processing_system7_0 [ create_bd_cell -type ip -vlnv xilinx.com:ip:processing_system7:5.5 processing_system7_0 ]
214 set_property -dict [ list \
215     CONFIG.PCW_ACT_APU_PERIPHERAL_FREQMHZ {666.666687} \
216     CONFIG.PCW_ACT_CAN0_PERIPHERAL_FREQMHZ {23.8095} \
217     CONFIG.PCW_ACT_CAN1_PERIPHERAL_FREQMHZ {23.8095} \
218     CONFIG.PCW_ACT_CAN_PERIPHERAL_FREQMHZ {10.000000} \
219     CONFIG.PCW_ACT_DCI_PERIPHERAL_FREQMHZ {10.158730} \
220     CONFIG.PCW_ACT_ENET0_PERIPHERAL_FREQMHZ {10.000000} \
221     CONFIG.PCW_ACT_ENET1_PERIPHERAL_FREQMHZ {10.000000} \
222     CONFIG.PCW_ACT_FPGA0_PERIPHERAL_FREQMHZ {10.000000} \
223     CONFIG.PCW_ACT_FPGA1_PERIPHERAL_FREQMHZ {10.000000} \
```



C:\Users\user\Desktop\PNQ\axi\_gpio.hwh - Notepad++

檔案(F) 編輯(E) 搜尋(S) 檢視(V) 編碼(N) 語言(L) 設定(T) 工具(O) 巨集(M) 執行(R) 外掛(P) 視窗(W) ?



ps\_gpio.tcl x axi\_gpio.hwh x

```
395     </REGISTERS>
396   </ADDRESSBLOCK>
397 </ADDRESSBLOCKS>
398 <PARAMETERS>
399   <PARAMETER NAME="C_FAMILY" VALUE="zynq"/>
400   <PARAMETER NAME="C_S_AXI_ADDR_WIDTH" VALUE="9"/>
401   <PARAMETER NAME="C_S_AXI_DATA_WIDTH" VALUE="32"/>
402   <PARAMETER NAME="C_GPIO_WIDTH" VALUE="4"/>
403   <PARAMETER NAME="C_GPIO2_WIDTH" VALUE="32"/>
404   <PARAMETER NAME="C_ALL_INPUTS" VALUE="0"/>
405   <PARAMETER NAME="C_ALL_INPUTS_2" VALUE="0"/>
406   <PARAMETER NAME="C_ALL_OUTPUTS" VALUE="0"/>
407   <PARAMETER NAME="C_ALL_OUTPUTS_2" VALUE="0"/>
408   <PARAMETER NAME="C_INTERRUPT_PRESENT" VALUE="0"/>
409   <PARAMETER NAME="C_DOUT_DEFAULT" VALUE="0x00000000"/>
410   <PARAMETER NAME="C_TRI_DEFAULT" VALUE="0xFFFFFFFF"/>
411   <PARAMETER NAME="C_IS_DUAL" VALUE="0"/>
412   <PARAMETER NAME="C_DOUT_DEFAULT_2" VALUE="0x00000000"/>
413   <PARAMETER NAME="C_TRI_DEFAULT_2" VALUE="0xFFFFFFFF"/>
414   <PARAMETER NAME="Component_Name" VALUE="axi_gpio_buttons_0"/>
415   <PARAMETER NAME="USE_BOARD_FLOW" VALUE="false"/>
416   <PARAMETER NAME="GPIO_BOARD_INTERFACE" VALUE="Custom"/>
417   <PARAMETER NAME="GPIO2_BOARD_INTERFACE" VALUE="Custom"/>
418   <PARAMETER NAME="EDK_IPTYPE" VALUE="PERIPHERAL"/>
419   <PARAMETER NAME="C_BASEADDR" VALUE="0x41210000"/>
420   <PARAMETER NAME="C_HIGHADDR" VALUE="0x4121FFFF"/>
421 </PARAMETERS>
422 <PORTS>
423   <PORT CLKFREQUENCY="50000000" DIR="I" NAME="s_axi_aclk" SIGIS="clk" SIGNAME="processing_system7_0_FCLK_CLK0">
424     <CONNECTIONS>
425       <CONNECTION INSTANCE="processing_system7_0" PORT="FCLK_CLK0"/>
426     </CONNECTIONS>
427   </PORT>
428   <PORT DIR="I" NAME="s_axi_aresetn" POLARITY="ACTIVE_LOW" SIGIS="rst" SIGNAME="rst_ps7_0_50M_peripheral_aresetn">
429     <CONNECTIONS>
430       <CONNECTION INSTANCE="rst_ps7_0_50M" PORT="peripheral_aresetn"/>
431     </CONNECTIONS>
432   </PORT>
433   <PORT DIR="I" LEFT="8" NAME="s_axi_awaddr" RIGHT="0" SIGIS="undef" SIGNAME="buttons_s_axi_awaddr">
434     <CONNECTIONS>
435       <CONNECTION INSTANCE="ps7_0_axi_periph" PORT="M01_AXI_awaddr"/>
436     </CONNECTIONS>
437   </PORT>
```

```
In [1]: 1 !dir ./bitstream/axi_gpio.*
./bitstream/axi_gpio.bit  ./bitstream/axi_gpio.tcl
./bitstream/axi_gpio.hwh  ./bitstream/axi_gpio.xdc
```

- Download the bitstream

```
In [2]: 1 from pynq import Overlay
2 axi_gpio_design = Overlay("./bitstream/axi_gpio.bit")
```

```
/usr/local/lib/python3.6/dist-packages/pynq/bitstream.py:151: UserWarning: The provided name './bitstream/axi_gpio.bit' resulted in multiple possible matches:
- /home/xilinx/jupyter_notebooks/bitstream/axi_gpio.bit
- /usr/local/lib/python3.6/dist-packages/pynq/overlays/./bitstream/axi_gpio.bit
The first entry of this list, '/home/xilinx/jupyter_notebooks/bitstream/axi_gpio.bit', will be used, please provide the full path in case your target file was a different one in this list.
warnings.warn(msg, UserWarning)
```

Check the IP Dictionary for this design. The IP dictionary lists AXI IP in the design, and for this example will list the AXI GPIO controllers for the buttons, LEDs, and switches. The Physical address, the address range and IP type will be listed. If any interrupts, or GPIO were connected to the PS, they would also be reported.

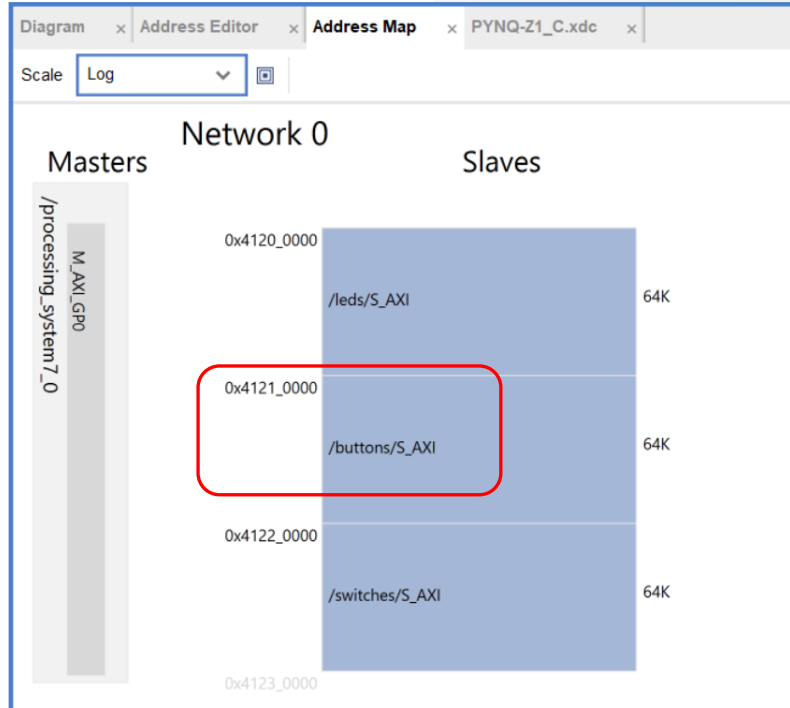
```
In [3]: 1 axi_gpio_design.ip_dict
{'mem_id': 'S_AXI',
 'parameters': {'C_ALL_INPUTS': '0',
 'C_ALL_INPUTS_2': '0',
 'C_ALL_OUTPUTS': '0',
 'C_ALL_OUTPUTS_2': '0',
 'C_BASEADDR': '0x41210000',
 'C_DOUT_DEFAULT': '0x00000000',
 'C_DOUT_DEFAULT_2': '0x00000000',
 'C_FAMILY': 'zynq',
 'C_GPIO2_WIDTH': '32',
 'C_GPIO_WIDTH': '4',
 'C_HIGHADDR': '0x4121FFFF',
 'C_INTERRUPT_PRESENT': '0',
 'C_IS_DUAL': '0',
 'C_S_AXI_ADDR_WIDTH': '9',
 'C_S_AXI_DATA_WIDTH': '32',
 'C_TRI_DEFAULT': '0xFFFFFFFF',
 'C_TRI_DEFAULT_2': '0xFFFFFFFF',
 'Component_Name': 'axi_gpio_buttons_0',
 'EDK_IPTYPE': 'PERIPHERAL',
```

```
In [4]: 1 hex(axi_gpio_design.ip_dict["buttons"]["phys_addr"])
```

```
Out[4]: '0x41210000'
```

測試ip位置

檔案名稱避免重疊





In [23]: `1 from pynq.lib import AxiGPIO` 調用FPGA PL 端之函式

```
2
3 buttons_instance = axi_gpio_design.ip_dict['buttons']
4 buttons = AxiGPIO(buttons_instance).channel1
```

In [24]: `1 switches_instance = axi_gpio_design.ip_dict['switches']`  
`2 switches = AxiGPIO(switches_instance).channel1`

In [25]: `1 led_instance = axi_gpio_design.ip_dict['leds']`  
`2 led = AxiGPIO(led_instance).channel1`

=====

=====

行為測試

In [35]: `1 led[0:4].off()`

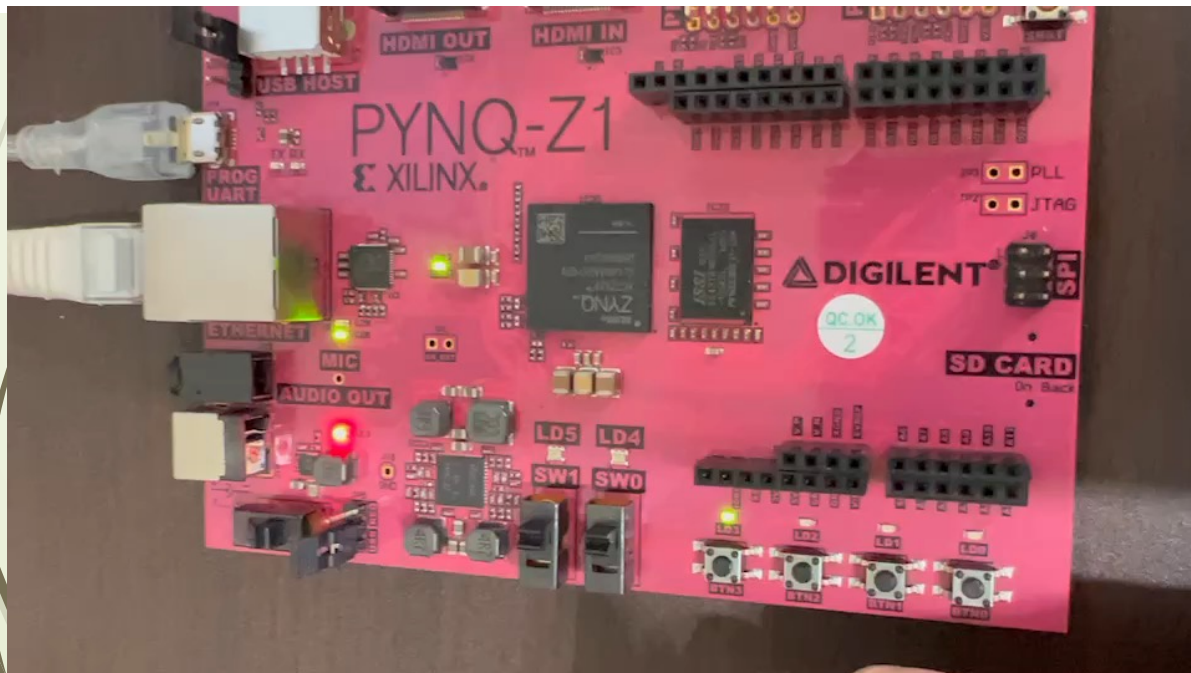
In [26]: `1 buttons.read()`

Out[26]: 0

In [41]:

```
1 print(f"Switches: {switches.read()}")
2 print(f"SW1: {switches.read() & 0x2}")
3 while((switches.read() & 0b10) == 0b10):
4     #總開關 SW1
5
6     if((switches.read() & 0b01) == 0b00):
7         #SW0 模式一
8         led[0:4].write(buttons.read())
9     elif((switches.read() & 0b01) == 0b01):
10        #SW0 模式二
11        led[3].write(switches.read() & 0b01)
12        led[0:4].write(buttons.read())
13
14 print("SW1=0")
15
16
17
```

Switches: 3  
SW1: 2  
SW1=0



# Linux mount usb至指定資料夾

```
sudo mkdir /usbstorage
```

