Unit-5

Semiconductor Devices

Semiconductor devices are nothing but the electronic components that are designed and developed based on the properties of semiconducting materials. All electronic circuits consist of passive components like resistors, capacitors etc. and active components like diodes, transistors etc. p-n junction diode is one of the most important and basic components of electronic circuits. In this chapter, formation of p-n junction, its applications and Transistor- structure and characteristics are discussed.

5.1 Formation of P-N Junction

P-N junction is a basic building block and it is one of the crucial structures in electronics. We know that, when a pure semiconductor like Si or Ge is doped with trivalent impurity, it forms p type semiconductor and if it is doped with pentavalent impurity, then it forms n- type semiconductors. If we try to join two different pieces of p type semiconductor and n type semiconductor to form p-n junction diode, there will be a grain boundary that would scatter the electrons and holes and thus prevent the electrons to move from one side to the other. That means no current will flow through this arrangement. So, it is essential to make the entire p-n junction using a single semiconductor crystal. To form p-n junction, one region of the crystal is initially doped with one type say trivalent impurities which will make it p-type semiconductor and then with pentavalent impurities to form n region. The interface separating p and n region is called as metallurgical junction.

The processes that follow after the formation of a p-n junction are– diffusion and drift. The concentration of holes and electrons at the two sides of a junction are different. Therefore,the holes from the p-side diffuse to the n-side and the electrons from the n-side diffuse to the p-side. Due to diffusion of positive and negative charges, electric field is induced, which also exert force on charges in opposite direction as shown in fig. 5.1 below. This potential barrier is also known as 'built in potential barrier' and is denoted by V_0. In thermal equilibrium, the diffusion force and electric field force balance each other.

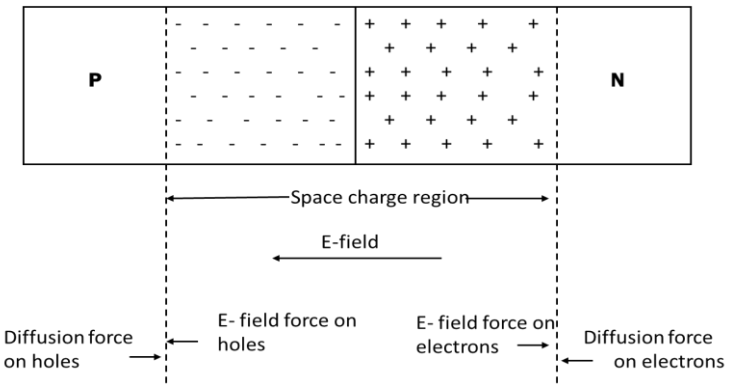


Fig. 5.1. Space charge region and forces acting on charges

Similar to majority charge carriers, minority charge carriers swept across the junction due to drift and some of them recombine with opposite ions and becomes neutral that results into the formation of layer, called depletion layer or potential barrier or junction. The current due to diffusion of majority carriers is called Diffusion current and current due to minority carriers is called as drift current. Due to transport of charge carriers, there is change in energy levels of semiconductor. In equilibrium, Fermi level is equal on both the sides. The energy band diagram of p-n junction in thermal equilibrium is shown in fig. 5.2 below

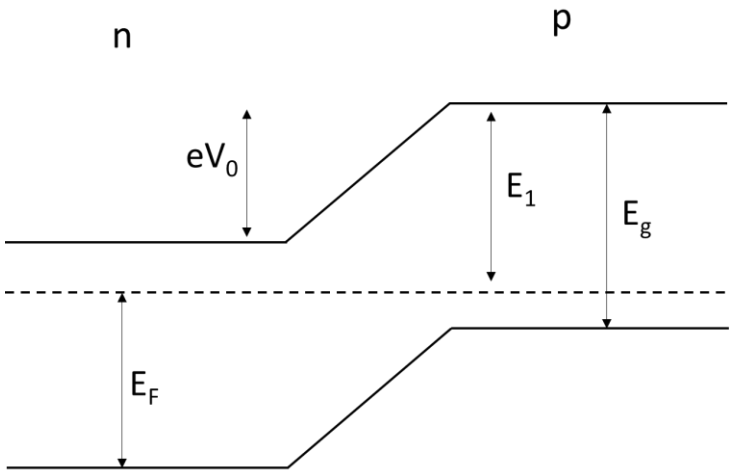


Fig. 5.2. Energy band diagram of p-n junction in thermal equilibrium

Thus, built in potential V_0 is the difference between fermi levels of p and n regions of p-n junction diode. External voltage greater than V_0 has to be applied in order to cross this potential barrier.

Electron concentration in conduction band on n – side,

$$n_n = N_c \exp\left[-\left(E_g - E_F\right)/KT\right] \text{----------(5.1)}$$

Electron concentration in conduction band on p – side,

$$n_p = N_c \exp\left[-\left(E_g + eV_0 - E_F\right)/KT\right] \text{----------(5.2)}$$

Thus

$$\frac{n_n}{n_p} = \exp\left(\frac{eV_0}{KT}\right) \text{----------(5.3)}$$

Taking log on both sides,

$$V_0 = \frac{KT}{e}\ln\left(\frac{n_n}{n_p}\right)$$

$$V_0 = \frac{KT}{e}\ln\left(\frac{n_n p_p}{n_p p_p}\right) \text{ ---------- (5.4)}$$

$n_n=N_D$ and $p_p = N_A$, $p_p n_p=ni^2$ by law of mass action

$$\therefore V_0 = \frac{KT}{e} \ln\left(\frac{N_D N_A}{n_i^2}\right) \text{ ----------(5.5)}$$

Where, N_A is acceptor ion concentration.

$$\therefore V_0 = V_t \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

Where, thermal voltage, $V_t = kT/e$

Diffusion current due to electrons,

$j_e = A \exp [-(E_g - E_F)/KT] \exp(-eV_0/KT)$

$= A \exp [-(E_g - E_F + eV_0)/KT]$

$= A \exp(-E_1/KT) = i_e$

$j_e = i_e$, $j_h = i_h$

Drift current due to minority carriers and diffusion current due to majority carriers are equal and opposite and hence no net current flows across the junction.

5.2 Charge Flow in p-n junction:

As discussed earlier, majority charge carriers inject into junction and reach the other region and continue to diffuse away, called as diffusion. Thus, the current caused by the diffusion of majority charge carriers is called as diffusion current, whereas very few minority carriers are swept across the junction, by the electric field in the depletion region. The current due to drifting of minority carriers is called the drift current. The drift current of minority and diffusion current of majority carriers must balance each other i.e. they are equal and opposite. Thus there is no net current flow across the junction without bias voltage.

In reverse bias, external voltage adds to the barrier potential, thus increases height of barrier. Due to increase in electric field in depletion layer, majority carriers pushed farther and width of the depletion region increases. The increase in potential barrier hinders the diffusion of majority charge carriers and diffusion current drops to zero at higher bias voltage. However, this high barrier potential does not influence the minority charge carriers, instead it increases acceleration of minority carriers. The current through the junction is only due to minority carriers i.e. drift current. It is constant at constant temperature. This drift current is called reverse saturation current and denoted by J_0. If the voltage (V) is given in reverse bias to the p-n junction diode then, total potential is $e(V_0+V)$ i.e. it is greater than V_0. The Energy

band diagram is shown in fig. 5.3 (b). Electron concentration in conduction band on n – side,

$$n_n = N_c \exp\left[-\left(E_g - E_F\right)/KT\right]$$

$$n_n = N_c \exp\left[-\left(E_1 - eV_0\right)/KT\right]$$

The electron diffusion current in reverse bias is,

$$j_e = N_c \exp\left[-\left(E_1 - eV_0\right)/KT\right].\exp\left[-\left(eV_0 + eV\right)/KT\right] \text{ ---------- (5.6)}$$

$$\therefore\ j_e = N_c \exp\left[-\left(E_1 + eV\right)/KT\right]$$

The electron drift current,

$$\therefore i_e = \exp\left[-E_1/KT\right]$$

So, total current density in p-n junction diode,

$J = j_e - i_e = i_e\,[\exp(-eV/KT)-1]$

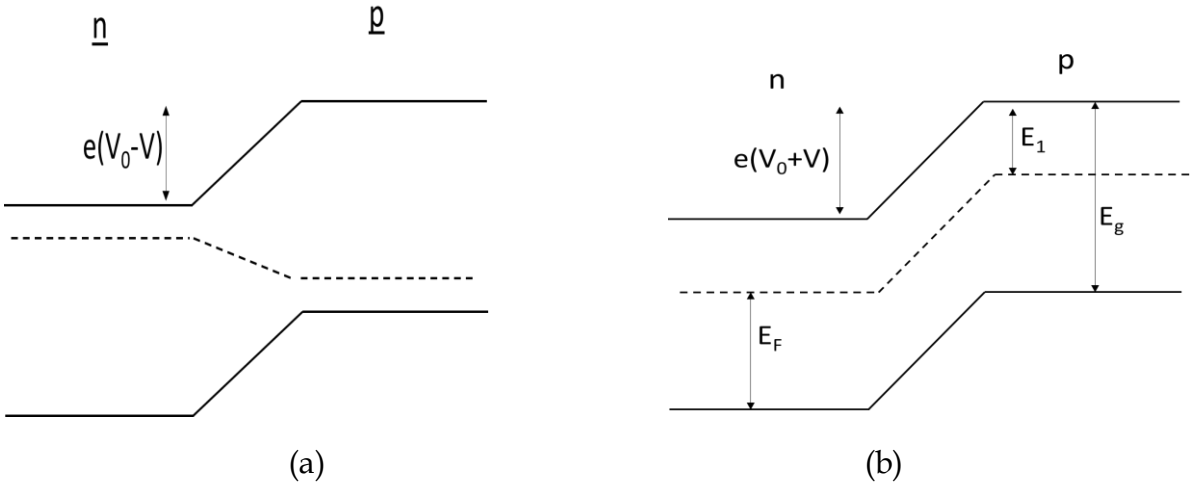
$= J_0\,[\exp(-eV/KT)-1]$ ----------(5.7)

If the voltage is given in forward bias, the total potential is $e(E_0-V)$ i.e. less than that of zero bias (fig. 5.3 (a)). In forward bias, electrons are injected into n region as negative terminal of battery is connected to n side which results in increase in all levels including Fermi level of n region (E_{Fn}) whereas, holes injected into p region resulting in lowering the energy levels. This leads to the lowering of energy difference and hence, barrier potential. Due to reduction of height (potential) of barrier, the movement of majority carriers is promoted. As a result, diffusion current increases. The total current density in forward bias is,

$$J = J_0\left[exp\left(\frac{eV}{kT}\right) - 1\right] \text{ ----------(5.8)}$$

Where, J_0 is called as reverse saturation current

The energy band diagram of p-n junction at thermal equilibrium is shown in fig. 5.2. The change in energy band diagram in forward bias and reverse bias is shown in fig. 5.3 (a) and 5.3 (b).



(a) (b)

Fig. 5.3 Energy band diagram of p-n junction (a) diode in forward bias and (b) in reverse bias

Schottky Diode:

Schottky diode was one of the first practical semiconductor devices formed by the junction of n-type semiconductor with a metal. It is also known as Schottky diode barrier. It is unipolar diode. Compared to p – junction diode, low forward voltage of about 150-450 mV is required to flow the current through it. Due to low voltage, switching is faster.

The junction of semiconductor and metal like gold, tungsten, chromium, platinum, silicides, molybdenum etc forms a Schottky diode. At one end of the diode, there is unilateral junction between metal and lightly doped n-type semiconductor at other end heavily doped semiconductor surface is metalized to give ohmic bilateral contact. This contact is non rectifying and potential is not present.

As doping concentration increases in semiconductor, width of depletion region decreases and below certain width, junction behaves as a ohmic contact. For sufficiently large height (greater than thermal energy KT), junction behaves as a Schottky barrier. Before formation of junction, Fermi level in semiconductor is higher than that in metal. After formation of junction, electrons from semiconductor flow into lower energy states in the metal. Positively charged donor atoms remain in the semiconductor creating a space charge region. Thus electric field is developed across the metal – semiconductor junction causing upward bending of energy bands in semiconductor. The structure is shown in figure below.

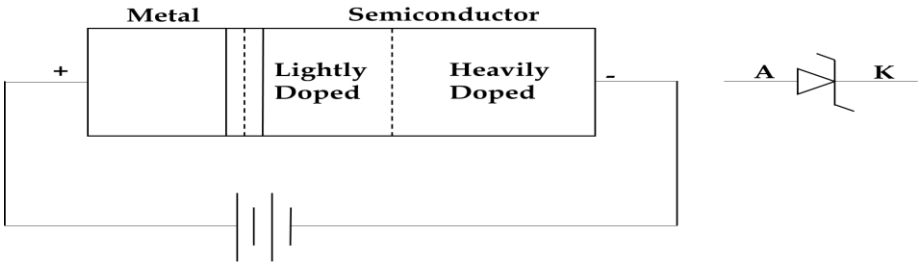
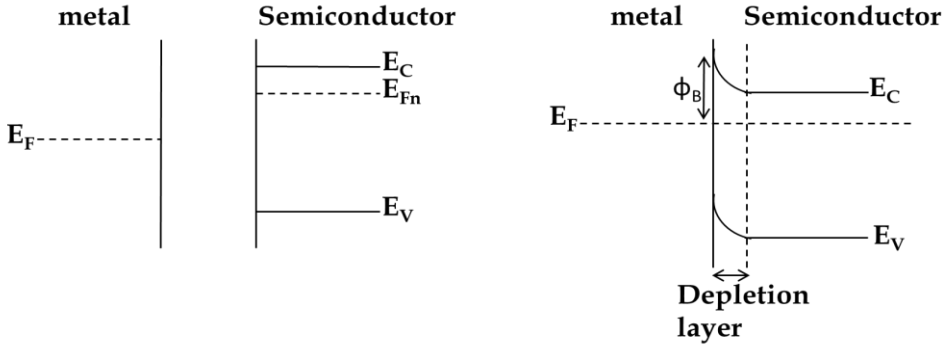


Fig. 1.

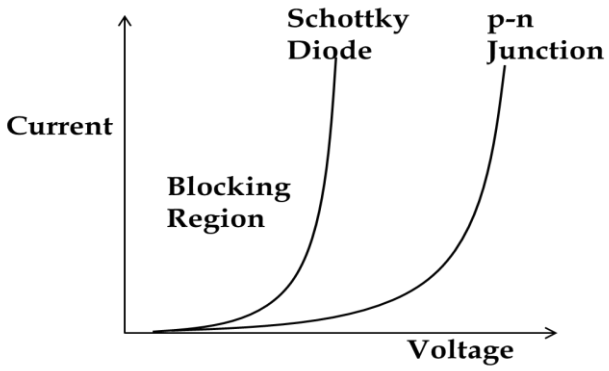
Metal region acts as anode while semiconductor region acts as cathode. Energy level diagram before formation of junction is shown in figure (a) and for Schottky junction is shown in figure (b) below.



(a) (b)

Φ_B – Schottky barrier height.

In forward bias, positive terminal of battery is connected to metal side of junction. Majority carrier electrons in n-type semiconductor cross the junction and current flows through the circuit. Since there is no structure for holes in metal, current due to minority carriers can not flow through the circuit in revere biased condition and the junction is unilateral. Thus in Schotteky diode, there is rapid response to the change in bias. I – V characteristics of Schottky diode is studied in forward bias only.



I – V characteristics of Schottky diode are similar to that of p-n junction diode. But, knee voltage for Schottky diode is much smaller than that of p-n junction diode. Knee voltage for Schottky diode is 0.3 to 0.4 V and that of p-n junction diode is 0.6 to

0.9 V. As voltage is much smaller, power dissipation is very small and Schottky diode can be used in photovoltaic panel. The main limitation of Schottky diode is that it has much lower reverse breakdown voltage and relatively higher reverse leakage current.

Applications of Schottky Diode:

1. Voltage Clamping:

The phenomenon of limiting the output voltage of source is called voltage clamping. Voltage clamping is a feature often found in ac line to protect sensitive electronic equipments from high voltage spikes. When the voltage shoots up, voltage clamper devices like Schottky diode clamps down by increasing its own resistance. For very high voltage that these devices fail to control and open the circuit that leads to stoppage of current flow and thus it protects the equipment. Due to low forward voltage drop and high current density, Schottky diodes are used in voltage clamping.

2. Switching:

As no reverse current is present in Schottky diode, they can be used as switching regulator in switched mode power supply.

Junction Field Effect Transistor (JFET):

The transistor is an active device in electronic circuit while diode is passive device. The basic function of transistor is to control the current using voltage. In bipolar transistor three separately doped regions form p-n and n-p junctions. Since current is due to flow of both electrons and holes, it is called bipolar transistor. In unipolar transistor, current is due to either holes or electrons. Field effect transistor is example of unipolar transistor. Junction field effect transistor (JFET) is one of the simplest type of FET.

JFET consists of three terminals- Source, Drain and Gate. The cross-sectional view is shown in fig. below.

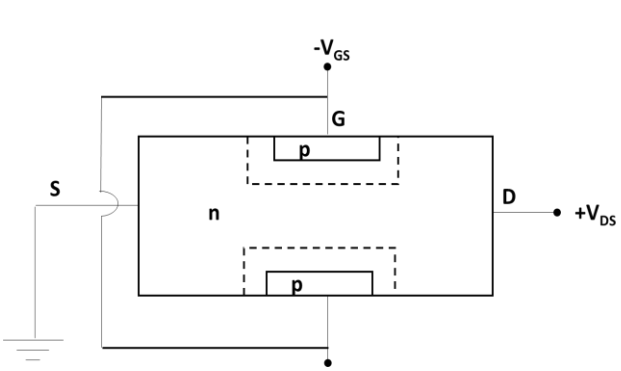


Fig.(a)

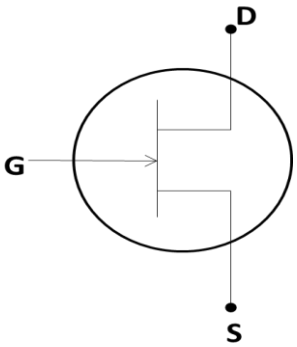


Fig. (b)

There are two types of JFETs: n-channel JFET (fig. a) and p-channel JFET. n-channel JFET is formed as n region is sandwiched between two heavily doped p

regions and p-channel JFET is formed when p region is in between two heavily doped n regions. Two ends of JFET are metalized to draw the Source and Drain terminals. The source is the terminal from which carriers enter the channel and leave from Drain. Gate is used to control the current. Two gate terminals at two p regions are connected to form single gate terminal. In n-channel JFET, majority charge carriers are electrons that flow between Source and Drain. Circuit symbol of JFET is shown in fig. b.

In n – channel JFET in the beginning, gate voltage is zero. If the source is at ground potential and small positive potential is applied to drain terminal, drain current is produced between source and drain terminal. n – channel acts as a resistor and I_D Vs V_{DS} characteristics is linear for small V_{DS}.

If small negative potential is applied to gate terminal, it makes junction reverse biased and it changes conductance of the channel. Depletion region is formed in n-region as shown in figure a. As voltage increases, depletion region increases and channel width decreases thus increasing resistance of channel. It controls diffusion of majority carriers from source to drain and decrease current and hence decreases slope of I_D versus V_{DS} curve for small V_{DS}. If gate voltage is increased, width of space charge region increases and for particular value of VGS, the space charge region completely fills the channel region. This condition is known as pinchoff and drain current at pinchoff is zero. This isolates source and drain terminals. Thus the current in the channel is controlled by gate voltage. The current in the one part of device is controlled by voltage in another part, it is transistor action.

If V_{GS} is constant and V_{DS} is changed, I_D versus V_{DS} is linear for small values of V_{DS}. As drain voltage increases, the gate to channel junction becomes reverse biased near drain terminal and space charge region extends in channel region increasing resistance of channel. Hence slope of I_D versus V_{DS} curve decreases. The effective channel resistance varies along channel length and voltage drop through the channel becomes position dependent. If drain voltage is further increased, the channel is pinchedoff at the drain terminal and drain current remains constant even if V_{DS} is increased. The drain voltage at pinchoff is $V_{DS}(sat)$. If V_{DS} is greater than $V_{DS}(sat)$, the transistor is said to be in saturation region and ideally I_D is independent of V_{DS} but not zero. Device is constant current source.

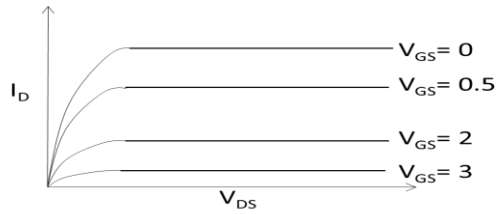


Fig.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET):

MOSFET stands for Metal Oxide Semiconductor FET. It is also called as IGFET (Insulated Gate FET). It is fabricated by the controlled oxidation of a semiconductor. Term metal in MOSFET is sometimes misnomer as it could be a layer of polysilicon also. The structure of MOSFET is shown in figure below.

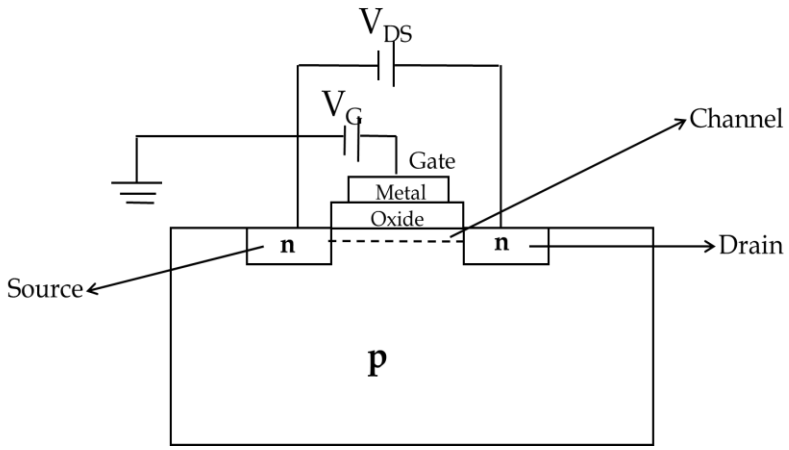


Fig. a

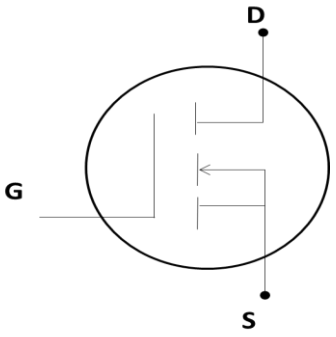


Fig. b

MOSFET is formed by depositing oxide layer on substrate. The substrate is made up of semiconductor. The substrate is a lightly doped semiconductor (e.g. lightly doped p type semiconductor) with diffused heavily doped regions. If lightly doped p type semiconductor is chosen as substrate, it is diffused with heavily doped n type regions as shown in fig. These n regions act as Source and Drain. Such devices are called as NMOS (N gate over P substrate). Similarly, PMOS or (P gate over N substrate) consists of lightly doped n channel semiconductor diffused with heavily doped p type regions. Oxide layer (SiO_2) on substrate acts as insulator. On oxide layer, metal like aluminum or high conductivity silicon is deposited. NMOS is shown in fig. (a) and its circuit symbol is shown in fig.(b). The Fermi level is uniform throughout the system at thermal equilibrium. While forming junction, Fermi level of metal is shifted in downward direction.

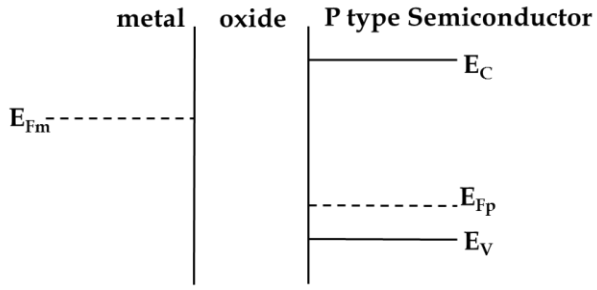


Fig. (a)

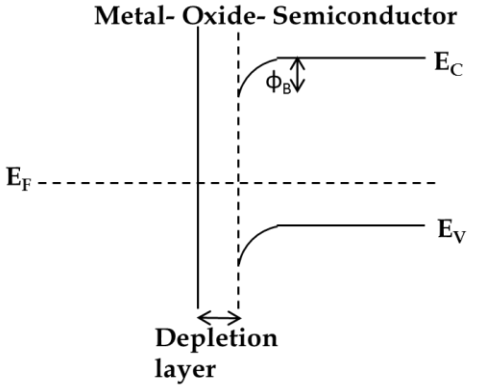


Fig. (b)

MOSFET structure is analogous to parallel plate capacitor. Near the p-type semiconductor and oxide contact, holes get accumulated resulting in bending of valence band and hence conduction band in downward direction.

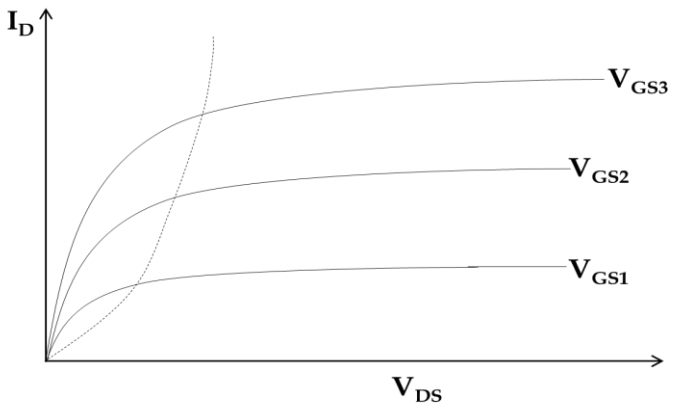
Source is given negative potential and drain terminal is at positive potential. Thus drain terminal is reverse biased. Positive gate voltage produces depletion layer under gate. As voltage V_G increases upto threshold voltage V_T, the inversion region is built up that connects source and drain by conducting channel. If $V_G > V_T$, the induced channel becomes wider and source – drain resistance smaller and it acts as a controlled resistor.

The channel resistance is function of V_G only for small V_{DS}. As V_{DS} increases, the depletion layer at drain p – n junction widens, channel gets narrower and I_D versus V_{DS} curve becomes non linear and number of charge carriers under gate decreases in the direction of drain. Electric field along the channel is non uniform. At certain voltage, channel becomes pinched off and drain current comes to saturation. Saturation current depends on V_G. Higher the V_G, wider is the channel and stronger is the saturation current. V_G controls the I_D – transistor action.

Current – voltage characteristics of MOSFET:

There are three operating regions of MOSFET –

1) Cut off region – $V_G > V_T$, $V_{DS} = 0$, MOSFET is off, it behaves as open switch.
2) Ohmic / linear region – $V_G > V_T$, $V_{DS} < V_G - V_T$, Current increases with value of V_{DS}. In this region, MOSFET acts as amplifier. When V_{DS} is increased, drain side becomes reverse biased and more depletion region towards drain end and channel starts to pinch off.
3) Saturation region – $V_G > V_T$, $V_{DS} > V_G - V_T$, pinch off point moves from drain to source end. Increased voltage gets dropped in depletion region leading to constant current.



Exercise

Q.1. Explain formation of p – n junction and obtain equation for junction potential.

Q.2. Explain formation of p – n junction with energy level diagram.

Q.3. Explain formation of p – n junction and show that no net current flows through the junction in unbiased p-n junction.

Q.4. Explain effect of reverse bias on p-n junction and derive equation for current.

Q.5. Explain effect of reverse bias on p-n junction and derive diode equation.

Q.6. Explain effect of forward bias on p-n junction and derive rectifier equation.

Q.7. Describe structure and operation of Schottky diode.

Q.8. Illustrate structure of junction field effect transistor and discuss effect of gate voltage on I – V characteristics.

Q.9. Discuss construction and working of junction field effect transistor.

Q.10. Discuss construction and working of metal oxide semiconductor field effect transistor.

Q.11. Describe structure and current – voltage characteristics of metal oxide semiconductor field effect transistor.