Learning the Art of Electronics Labs - 4L.2 Emitter Follower Lab

# Test Circuit Description

*Art of Learning Electronics Labs (AoLEL) page 170 Figure 4L.3.*

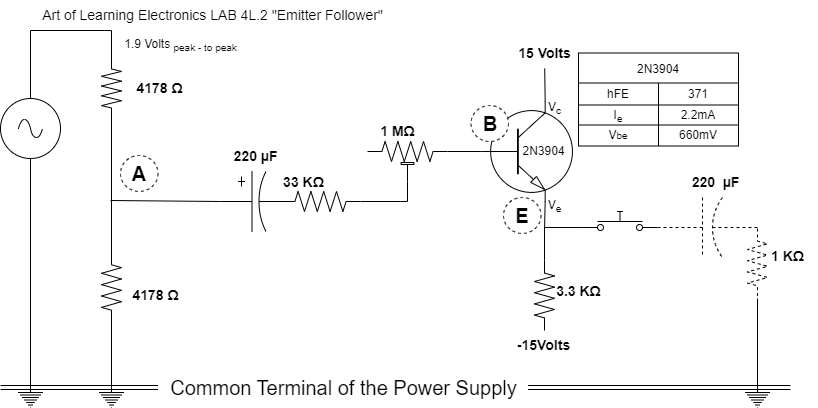
### Circuit modifications

* The 1MΩ potentiometer was added between 33KΩ and VBase for dialing up Z source.  
  *Combined impedance to attenuate VE by 50% was measured to be 1.02 MΩ*
* Larger blocking capacitors 220µF were needed for 50 Hz. The 4.7µF specified were too small. *The 1KΩ load was filtered out @ 4.7µF having no effect on VE.*
* For R out F-Gen signal strength was too strong to meet the recommended 1 Volt p-p .

*1Vp-p and achieved with a voltage divider and using F-Gen’s -20dB Attenuation.*

* The clipping issue was resolved using the -15Vdc on the emitter’s load.  
  *All other ground points, including the scope probes connect to power supply common.*

|  |  |  |
| --- | --- | --- |
| Setting | Value | Comment |
| Frequency | 50 Hz |  |
| DC Offset | OFF |  |
| F-Gen | 1.92 Vp-p | 20 dB attenuation prior to voltage divider |



# Measurements

|  |  |  |  |
| --- | --- | --- | --- |
| Point | Condition | Vp-p | Amplitude |
| A | Baseline | 157 mV | 144 mV |
| V Base | Baseline | 160 mV | 136 mV |
| V Emitter | Baseline | 161 mV | 136 mV |
| *Input Resistance / Impedance Measurements* | | | |
| A | Zin Output 50% Attenuation | 158 mV | 144 mV |
| V Base | Zin Output 50% Attenuation | 80 mV | 50 mV |
| V Emitter | Zin Output 50% Attenuation | 74 mV | 49 mV |
| *Output Resistance / Impedance Measurements* | | | |
| A | Z out 1KΩ Load | 152 mV | 136 mV |
| V Base | Z out 1KΩ Load | 158 mV | 144 mV |

# Calculations & Assumptions

* ΔVin = ΔVout Voltage Gain of 1
* ΔI in << ΔI out Curren Gain much greater than 1
* Vin = Iin Rin (Ohms Law) and Rin = ΔVin / ΔI in
* Vout = I out Rout (Ohms Law) and Rout = ΔVout / ΔI out
* ß is not predictable. ß varies with Ic and temperature.
* ß ≈ 100 is the rule a thumb 2N3904 as safe *underestimation*.
* ΔVin = ΔVbase and ΔVout = ΔV Emitter.

## Calculating Rin and Estimating ß by looking at Rin

* Compare amplitudes on both side of the R base (33 KΩ)  
  *The 1 MΩ potentiometer is dialed down to Zero.  
  144mV drop to 136mV is 5% loss. Keeping 95%.*

Diagram

Description automatically generated***Rin* = (95% / 5%) 33KΩ**  
***Rin* = 627 KΩ**

* *Sample Calculation - Assuming ß = 100  
  Rin = ß\*Re = 100\*3.3KΩ = 330 KΩ.*
* Actual Calculation – Determining ß   
  **ß=Rin /RE**= 627KΩ / 3.3KΩ  
  ***ß = 190***

## Calculating ß using the Hi Source Impedance measurement

* Compare amplitudes on both side of Rsource = 33KΩ + 1 MΩ   
  *144 mV drop to 50 mV is 65% loss, keeping only 35%*Diagram

  Description automatically generated
* **Rin = (35% / 65%) 1020 KΩ**   
  **Rin = 549 KΩ**
* **ß=Rin /RE**= 549KΩ / 3.3KΩ  
  **ß = 165**

## Calculating Rout

* Rout = R source/ß || R Emitter = Rin /ß || R Emitter
* ~~R~~~~out~~ ~~= (549KΩ/166) || 3.3KΩ = 1.65 KΩ~~
* ~~R~~~~out~~ ~~= (627KΩ/190) || 3.3KΩ = 1.65 KΩ~~
* **~~R~~~~out~~ ~~= 1.65 KΩ~~**
* Rout = (33KΩ/190) || 3.3KΩ = 165Ω
* Rout = (33KΩ/166) || 3.3KΩ = 187Ω
* **Rout = 165Ω to 187Ω**

#### 

# High Impedance Source Z Input (50% Attenuation on the Output V Emitter)

Graphical user interface

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## Measuring Output Impedance

#### Output Impedance Zout (Baseline)

#### Graphical user interface, application Description automatically generated

#### Output Impedance Zout (1KΩ load on V Emitter)

## A picture containing diagram Description automatically generated

## Workaround for Negative Side Clipping Vsource / Vinput

The negative side of the input signal is causing the Vbe to go negative and turn off the transistor.

Chart

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Clipping stops when DC Offset shifts the entire signal above +0.62 Vdc.

A picture containing chart

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