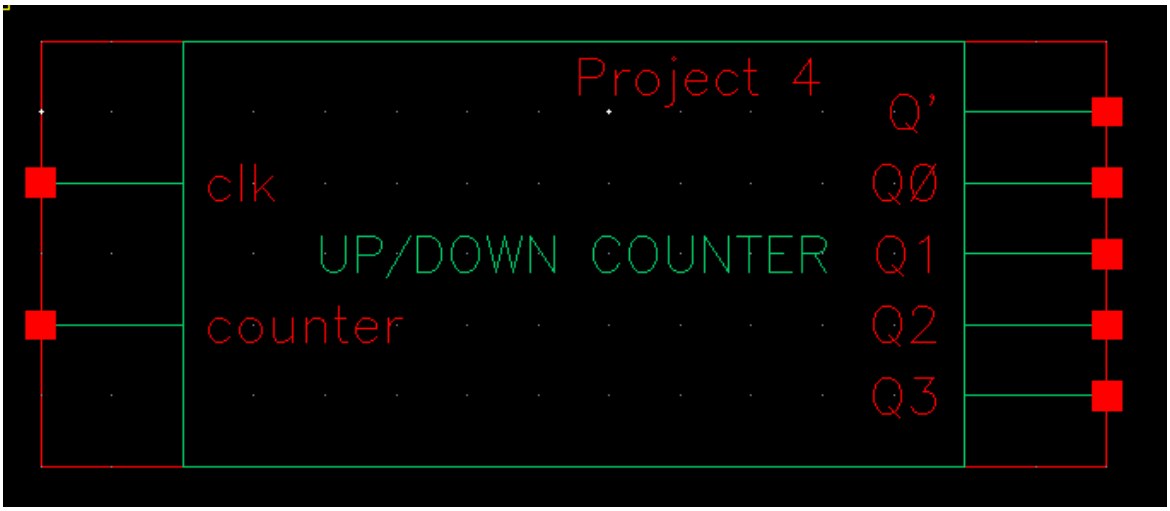
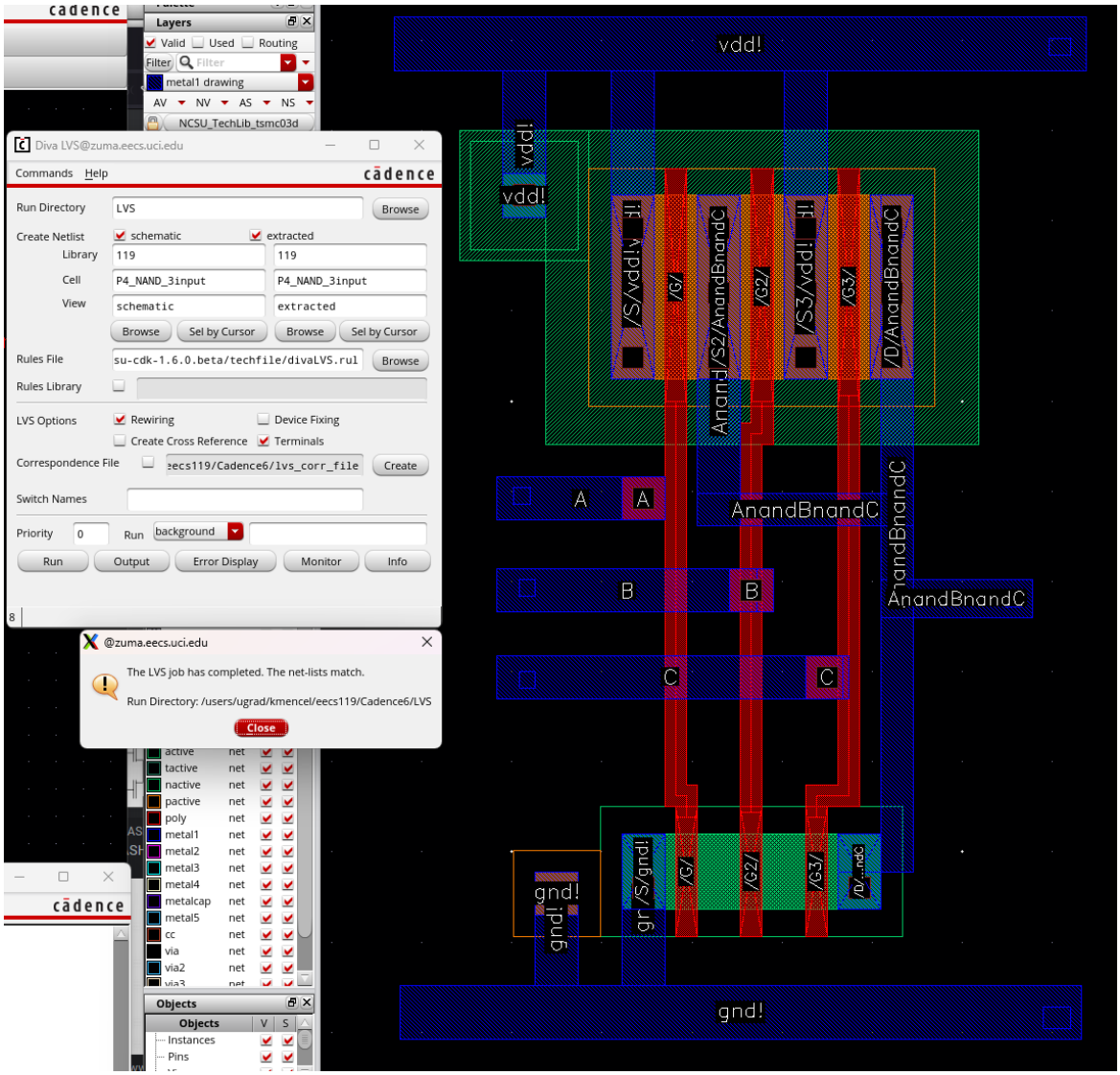
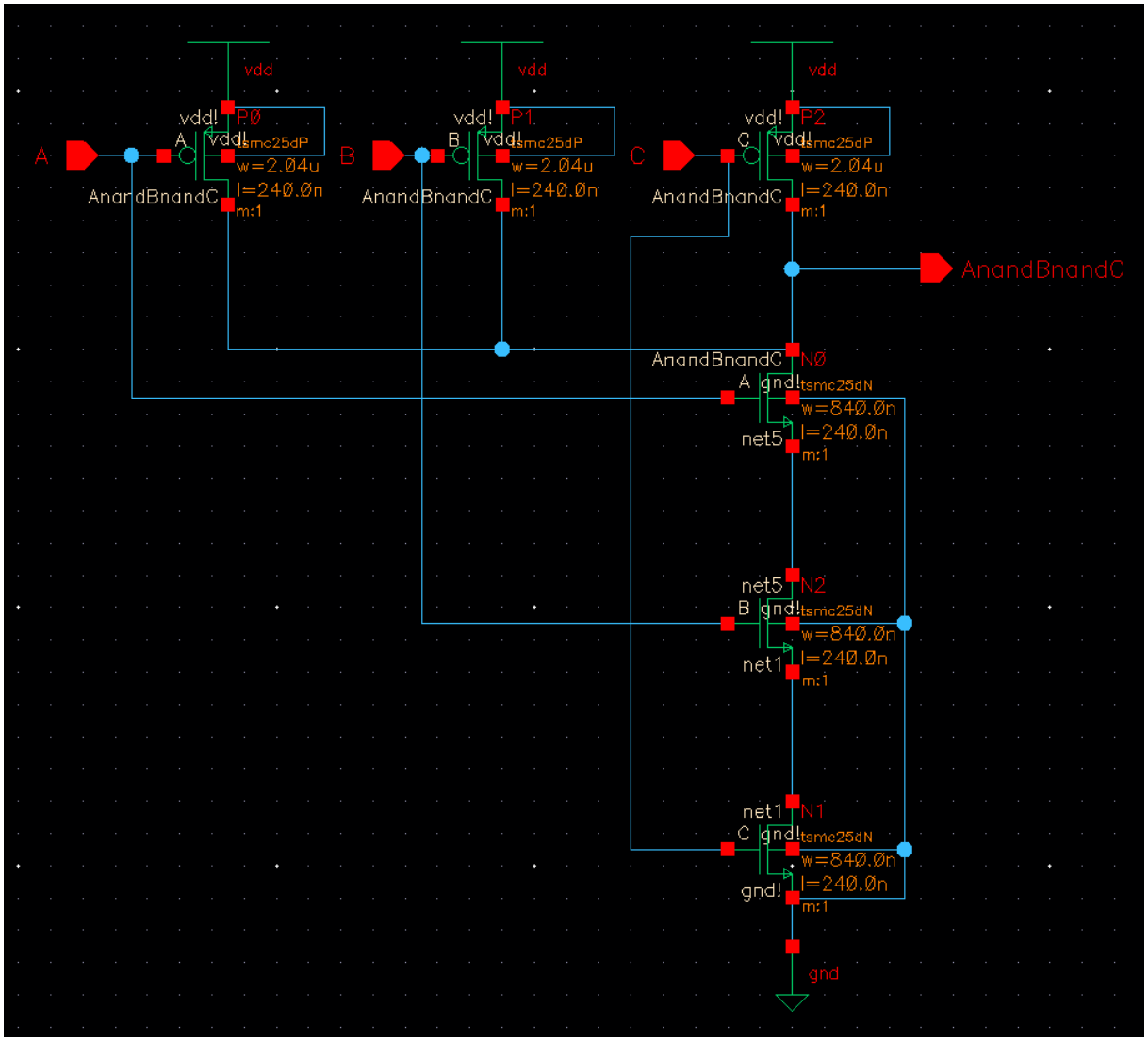
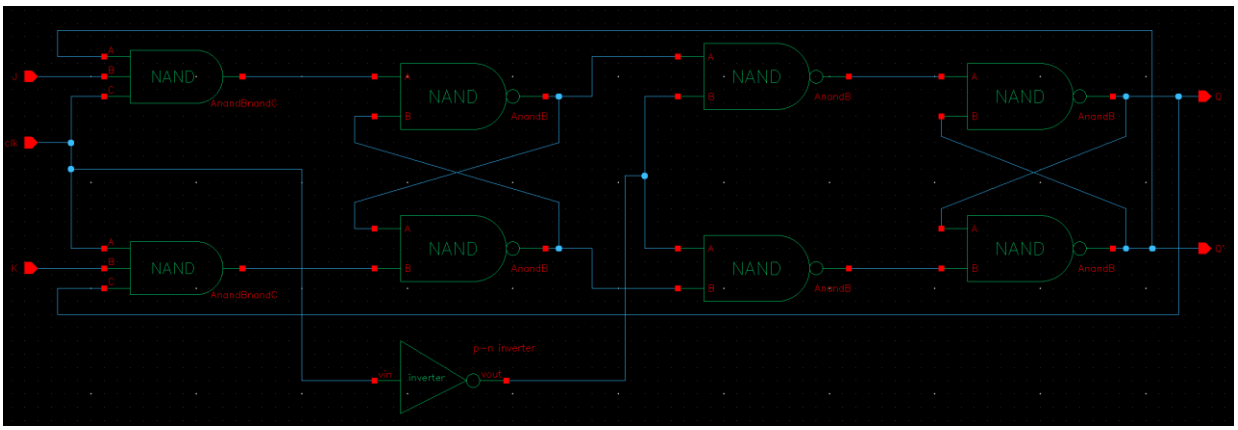

Project 4
clk
UP/DOWN COUNTER
counter
Q'
Q0
Q1
Q2
Q3

NAND 3 – INPUT:

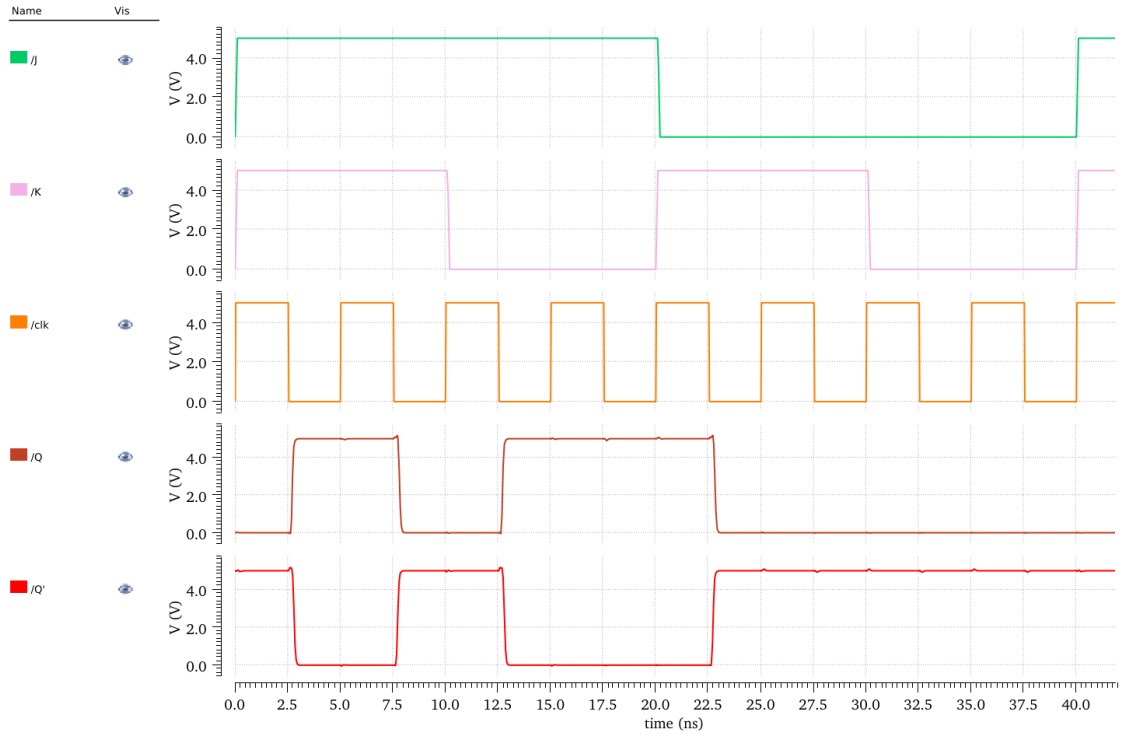

cadence
Layers
Valid
Used
Routing
metal1 drawing
NCSU_TechLib_tsmc03d
Diva LVS@zuma.eecs.uci.edu
Commands
Help
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
119
Cell
P4_NAND_3input
View
schematic
extracted
Sel by Cursor
Rules File
su-cdk-1.6.0.beta/techfile/divaLVS.rul
Rules Library
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
Create
Switch Names
Priority
Run
background
Run
Output
Error Display
Monitor
Info
@zuma.eecs.uci.edu
The LVS job has completed. The net-lists match.
Run Directory: /users/ugrad/kmencel/eecs119/Cadence6/LVS
Close
Objects
Instances
Pins
vdd!
gnd!
A
B
C
AnandBnandC

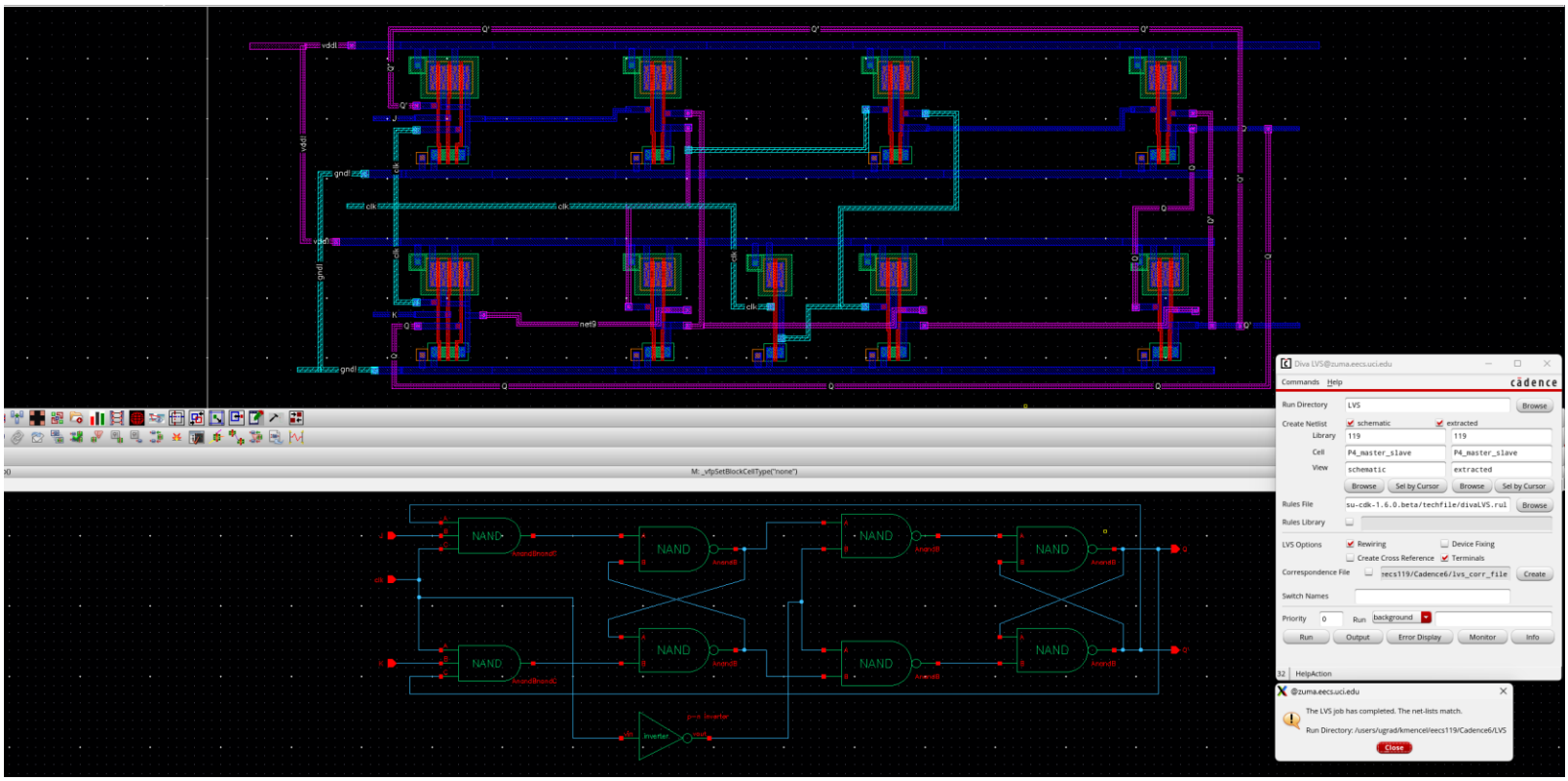


JK master slave flip flop



Transient Response **Wed Nov 22 01:17:12 2023**

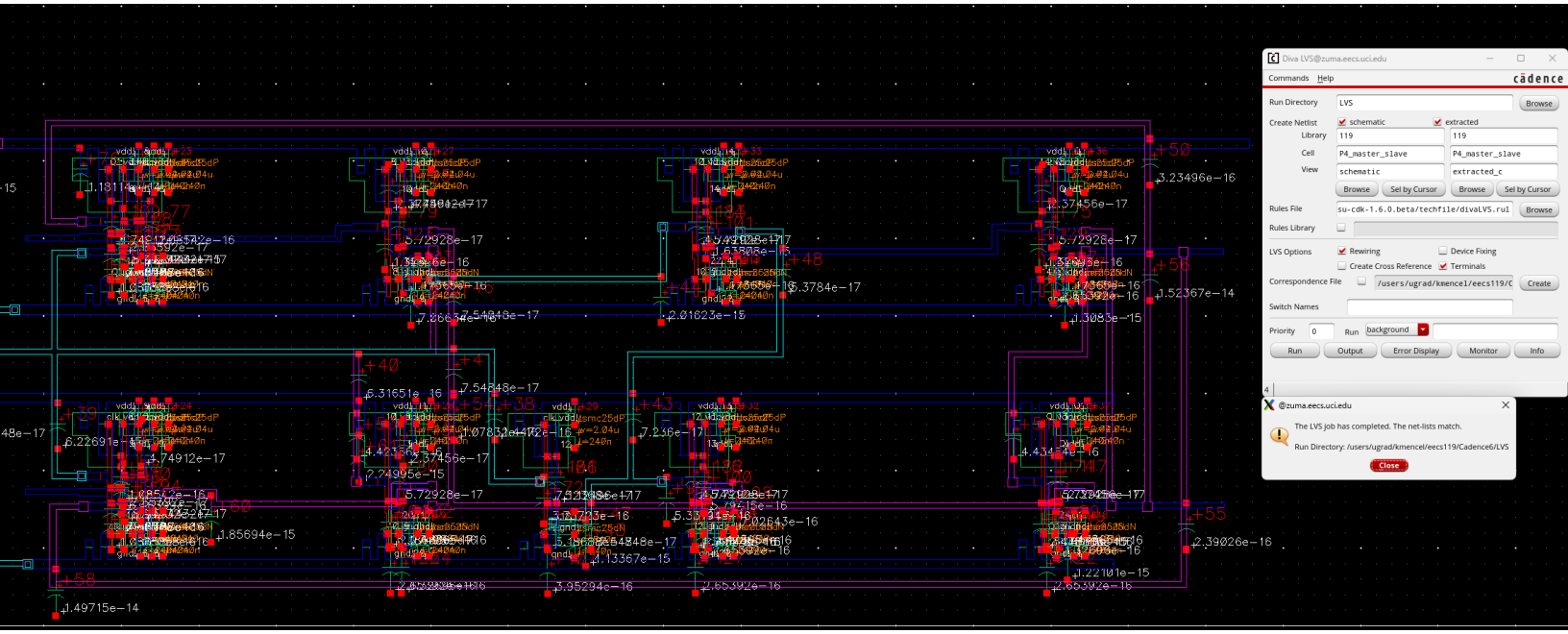




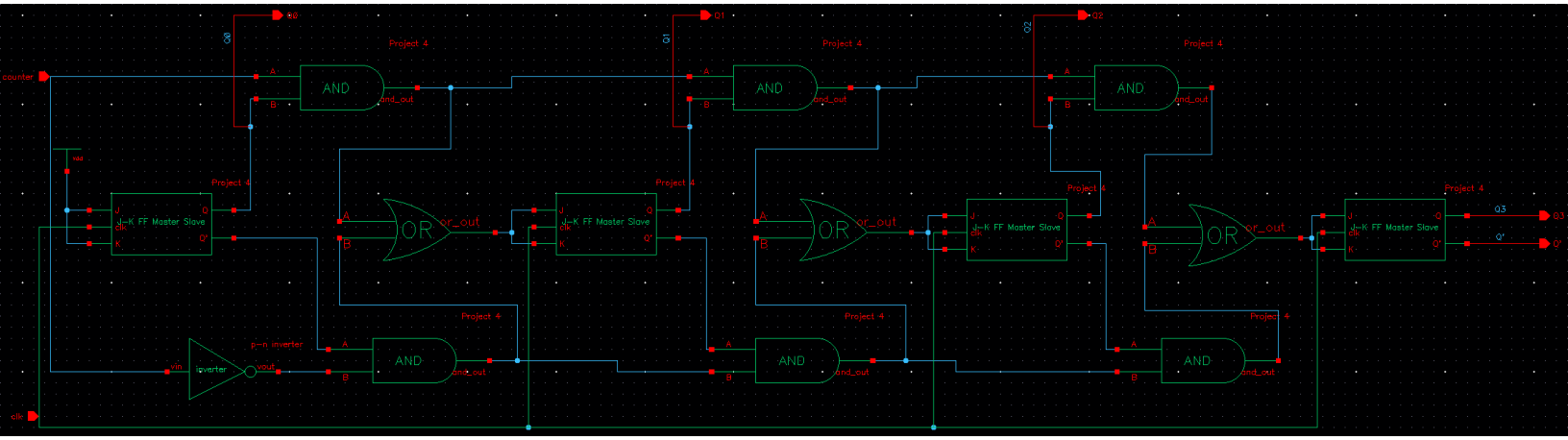
Diva LVS@zuma.eecs.uci.edu
Commands Help
cadence
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
119
119
Cell
P4_master_slave
P4_master_slave
View
schematic
extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Rules File
su-cdk-1.6.0.beta/techfile/divaLVS.rul
Browse
Rules Library
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
eecs119/Cadence6/lvs_corr_file
Create
Switch Names
Priority
0
Run
background
Run
Output
Error Display
Monitor
Info
32
HelpAction
@zuma.eecs.uci.edu
The LVS job has completed. The net-lists match.
Run Directory: /users/ugrad/kmencel/eecs119/Cadence6/LVS
Close

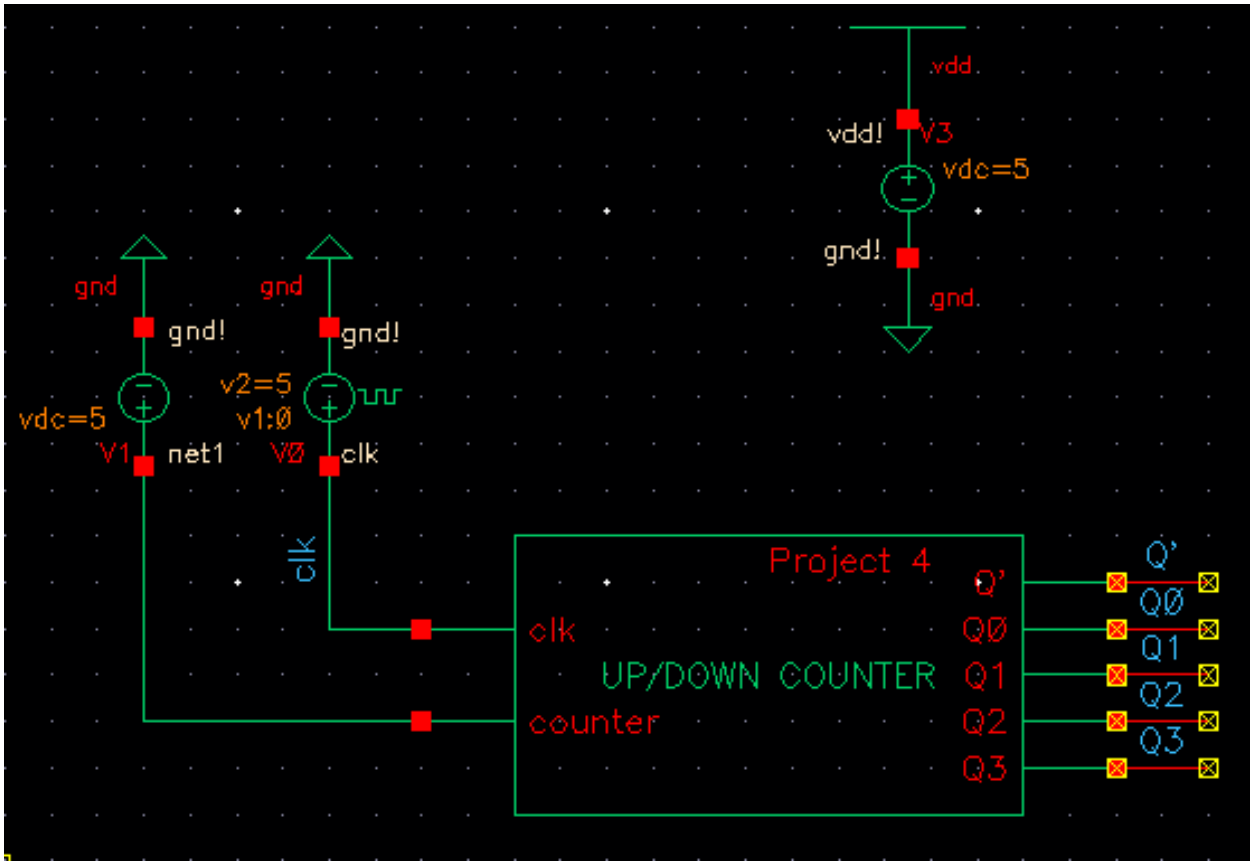
LVS check

Parasitic capacitance:

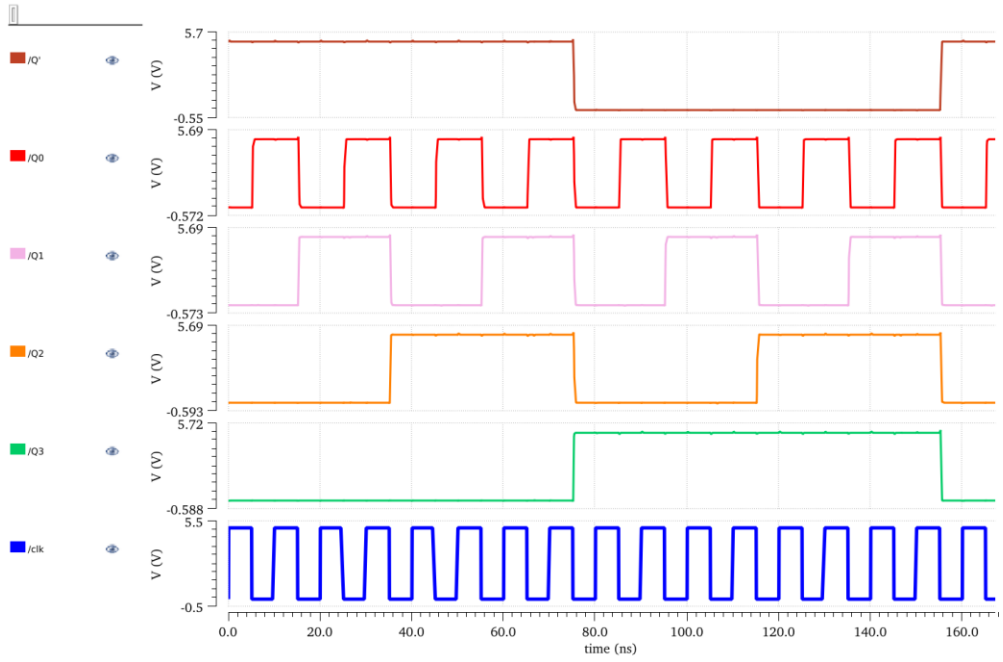


4 bit counter

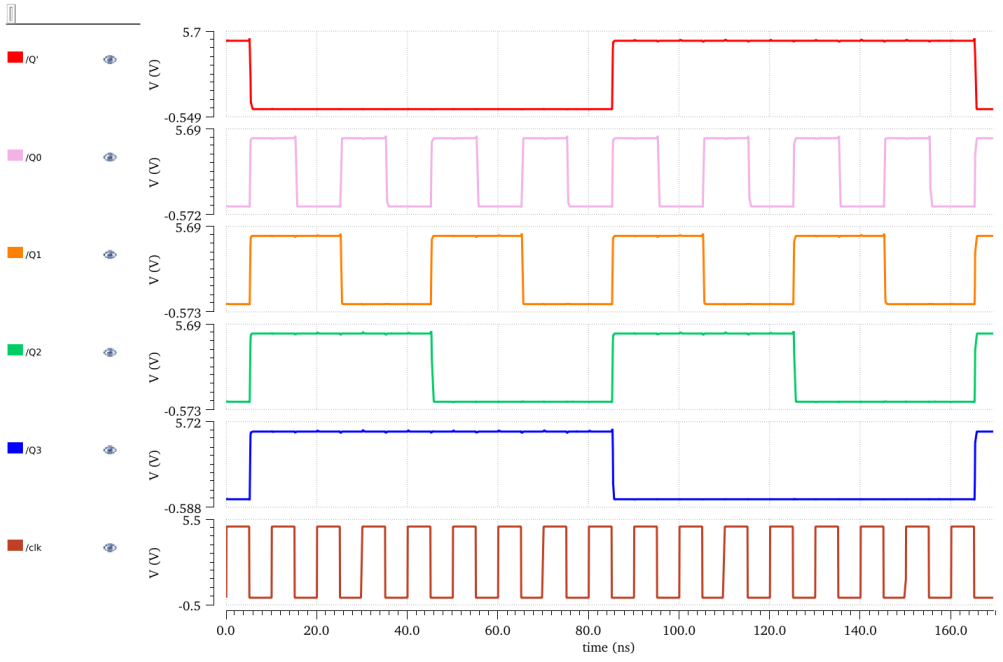
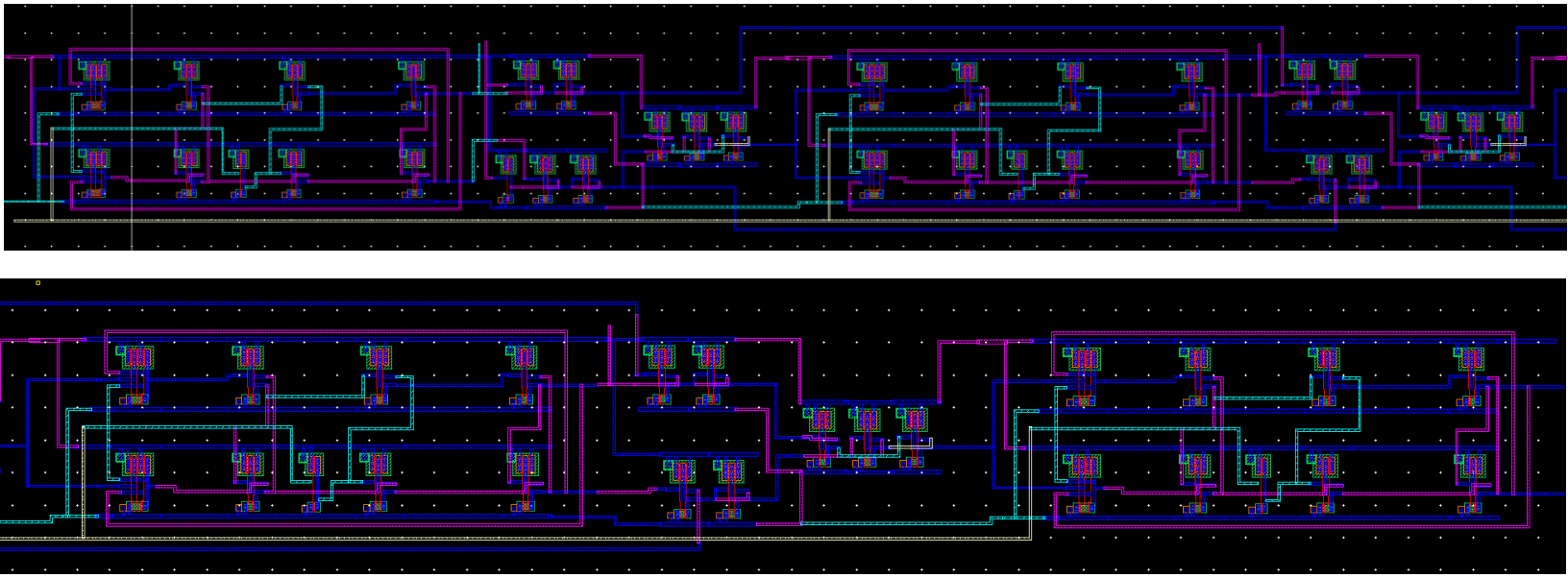



vdd
vdd!
V3
vdc=5
gnd!
gnd
gnd
gnd!
gnd!
v2=5
v1:0
vdc=5
V1
net1
VØ
clk
clk
Project 4
clk
UP/DOWN COUNTER
counter
Q'
QØ
Q1
Q2
Q3
Q'
QØ
Q1
Q2
Q3

Transient Response **Wed Nov 22 01:53:15 2023**



Transient Response **Wed Nov 22 02:03:50 2023**



Layout