Department of Electrical Engineering IIT Ropar EE302 Analog Circuits Lab

Experiment 2: Design and compare different current sources.

Keshav Kishore 2018eeb1158

Submission Date: 08/03/2021

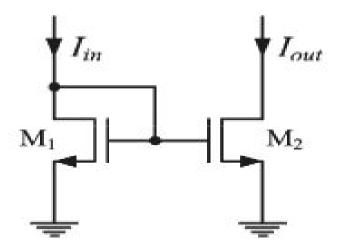
Objectives:

- Design a current source and find its output resistance and the minimum voltage required for its operation.
- Design a cascode current source and find their output resistance and the minimum voltage required for operation.
- Design a low voltage cascode current source and find their output resistance and the minimum voltage required for operation.
- Finally, Compare all the sources

Components/Tools Required: Ltspice, Gdocs

Theory:

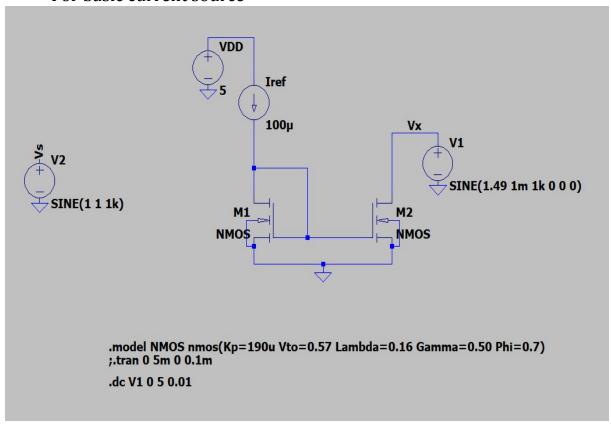
If we apply some input current into M1, then this current will flow through the source of M1 to ground because the gate of M2 has infinite resistance. This current will produce a suitable gate voltage (relative to ground) on M1, to satisfy the I-V square law relationship of the MOSFET. Notice then that the gate voltage of M1 is shared with the gate of M2. Therefore, M2 will have the same Vgs drop, and therefore the same current (if its W/L is the same).



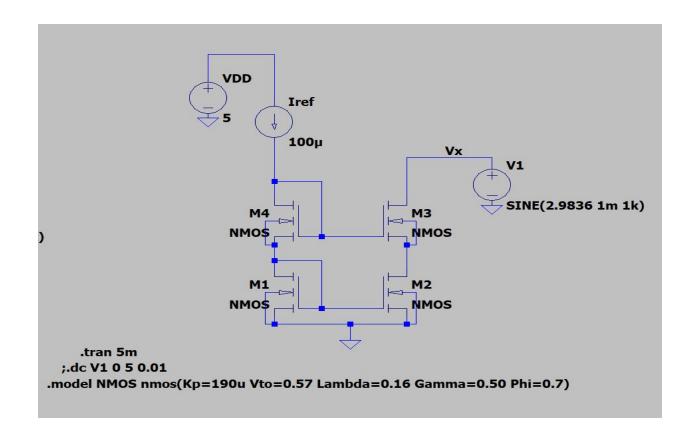
For general Case :
$$\frac{I_{out}}{I_{in}} = \frac{(\frac{W}{L})_{M2}}{(\frac{W}{L})_{M1}}$$

Circuit Diagram:

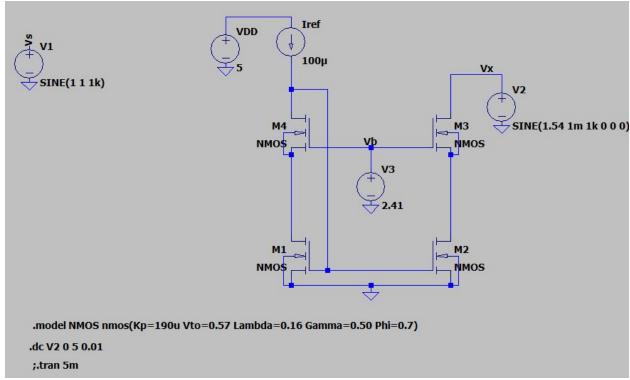
For basic current source



• For cascode current source



• For low voltage cascode current source

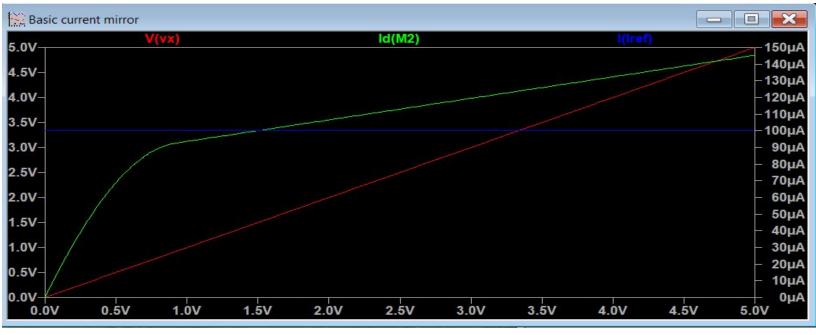


Procedure:

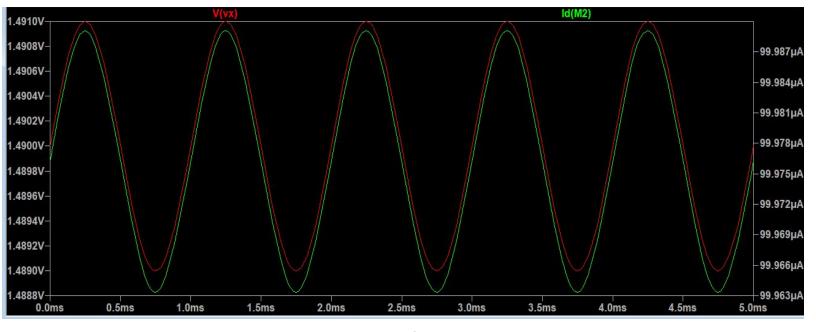
- To design a basic current source of 100uA, a reference current source was applied to M1(see schematic diagram). Further, a mirror ckt was made.
- Then, DC sweep of voltage source V1 was done and Ix was plotted to determine minimum voltage required across the current source to replicate the reference current at output node.
- Now, we applied an external voltage (1mV sinusoid with DC offset equal to the required minimum voltage) and measured peak to peak current at the output node to determine output impedance. (Ro = $\Delta Vx / \Delta Ix$)
- Similar process was done for cascode and low voltage cascode current source.

Waveforms:

Basic Current Source:

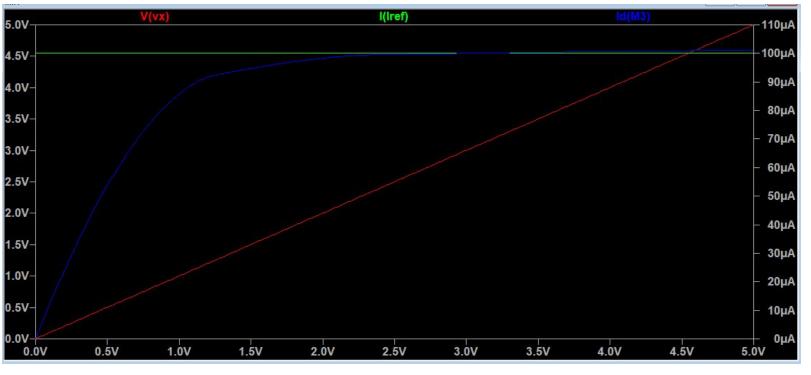


M2(Id vs Vx)

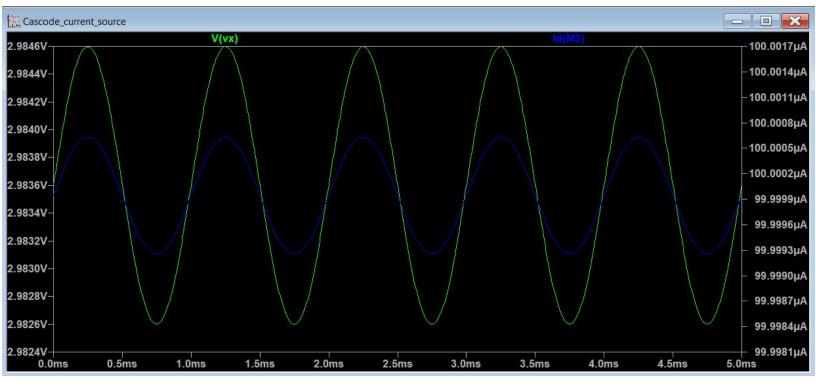


Curve for Ro

Cascode current source:

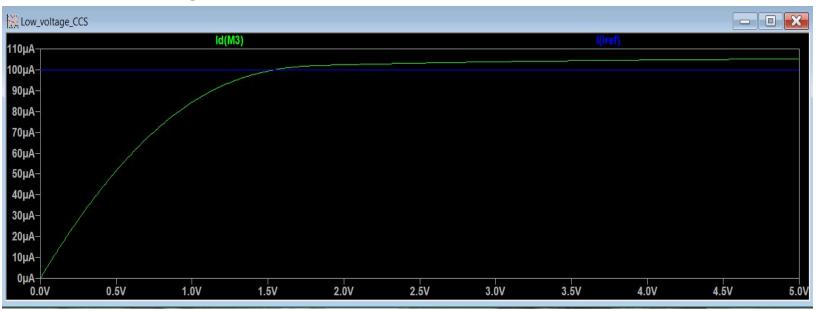


M3(Id vs Vx)

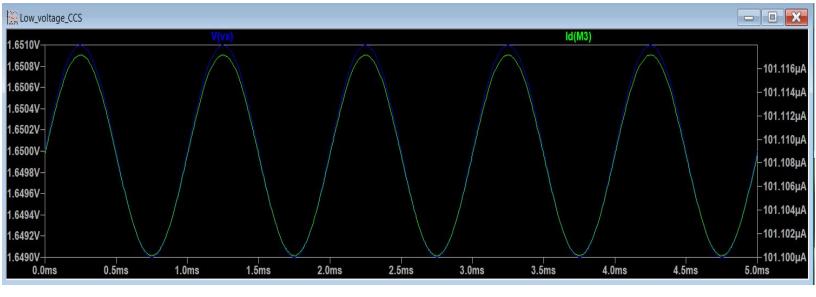


Curve for Ro

Low Voltage Cascode current source:



M3(Id vs Vx)

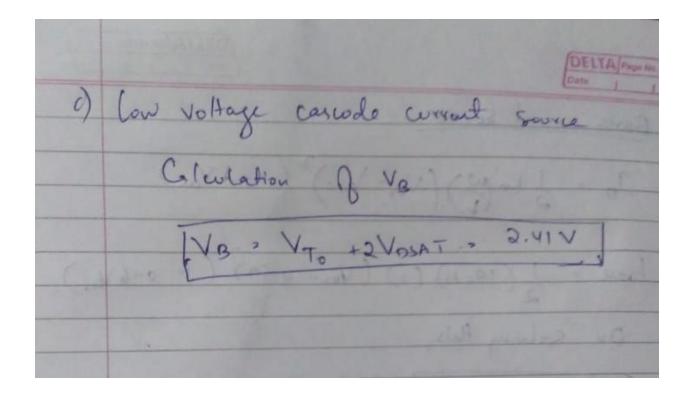


Curve for Ro

Observation Table:

Type	Minimum voltage required(in Volts)	ΔV(in Volts)	ΔI(in nA)	Ro(in $k\Omega$)
Basic current mirror	1.489	0.002	25.8143	77.47
Cascode	2.9836	0.002	1.37477	1453.57
Low voltage Cascode	1.54	0.002	25.9565	77.058

Basic arrent source Io . J King (Vor V10)2 (1-140) 100H = 1 (190H) (D (Vas-0.53) (10 016 Vas) Dr Solving Phis, Vas . 1.49 V Calulation of ro. So, Io . 1 Kn'm) (Var 0.57) "> ID > 80.408 MA » [Y = , 77. 75 Ke Carade wrent source: leut , [1 + 9mg 40 3] 402 + 403 [1+ 2 I D3 . 1] + 1 Ver- Vto A IO,] A IO, A IOS 2 1211.55 KA



Comparison:

Basic Current mirror:

Advantages:

- Low input Voltage to basic current mirror
- low input impedance makes the input current insensitive to the output impedance of the input source
- high output impedance makes the output current insensitive to the impedance of the output load

Disadvantages:

- 1) The mirror adds noise. This gets worse if there are no emitter resistors. With big enough emitter resistors, the noise can be reduced to an insignificant level.
- 2) Channel length modulation error is high.

Cascode current mirror:

Advantages:

- Higher Output resistance results in less error.
- Channel length modulation error gets cancelled.
- Higher minimum output voltage

Low voltage Cascode:

Advantage:

- This configuration makes it possible to use a higher effective gate-source voltage for the mirror transistors, hence reducing the effect of threshold voltage mismatch on the current mirror gain.
- This configuration has the advantage of simplicity combined with a complete elimination of the need for fixed bias voltages or bias currents in the current mirror.

Disadvantage: it requires a higher input voltage to the current mirror.

Results:

- Assumption :
 - All mosfet model ⇒ .model NMOS nmos(Kp=190u Vto=0.57 Lambda=0.16 Gamma=0.50 Phi=0.7)
- In case of Low Voltage Cascode, minimum voltage required is less than the normal cascode.
- Output Resistance in all the cases are very large.