Department of Electrical Engineering
IIT Ropar
EE302 Analog Circuits Lab

Experiment 3
Design and compare different amplifier using resistor and diode-connected loads

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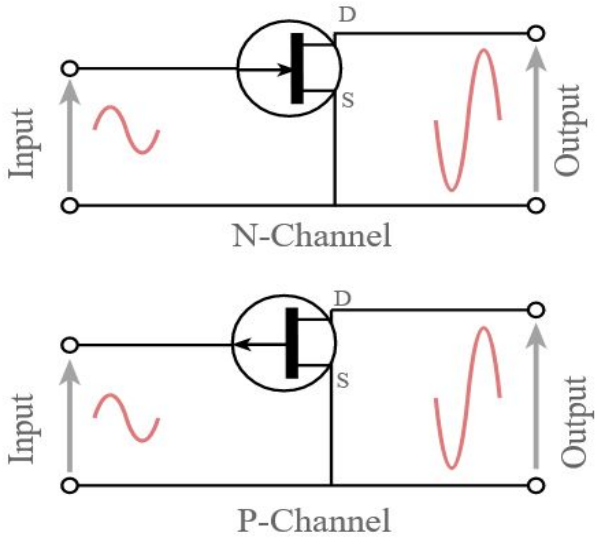
Objectives:

- Design common source, common gate and common drain amplifiers using resistor and diode connected sources
- Specifications:
    a. Common source gain = -15V/V, Common gate gain = 0.8 V/V, Common drain gain = 10 V/V
    b. Maximum Power consumption = 300 uW and load capacitance = 10pF
- Finally, compare all the amplifiers in terms of bandwidth, gain, input and output resistance.

Components/Tools Required: Ltspice, Gdocs

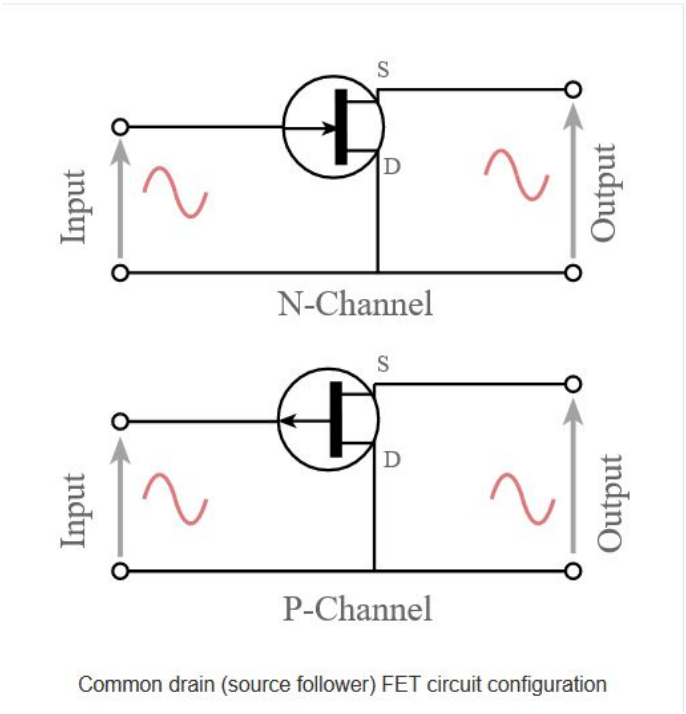
Theory : The three different FET circuit configurations are:

Common source: This FET configuration is probably the most widely used. The common source circuit provides a medium input and output impedance levels. Both current and voltage gain can be described as medium, but the output is the inverse of the input, i.e. 180° phase change. This provides a good overall performance and as such it is often thought of as the most widely used configuration.



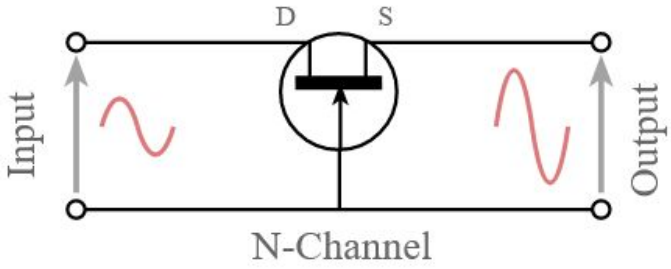
Common source FET circuit configuration

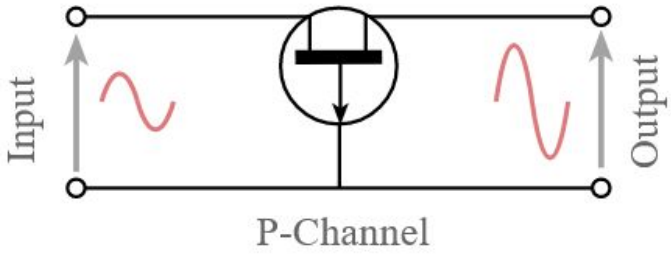
Common drain: This FET configuration is also known as the source follower. The reason for this is that the source voltage follows that of the gate. Offering a high input impedance and a low output impedance it is widely used as a buffer. The voltage gain is close to unity, although current gain is high. The input and output signals are in phase.



Common drain (source follower) FET circuit configuration

Common gate: This transistor configuration provides a low input impedance while offering a high output impedance. Although the voltage is high, the current gain is low and the overall power gain is also low when compared to the other FET circuit configurations available. The other salient feature of this configuration is that the input and output are in phase.

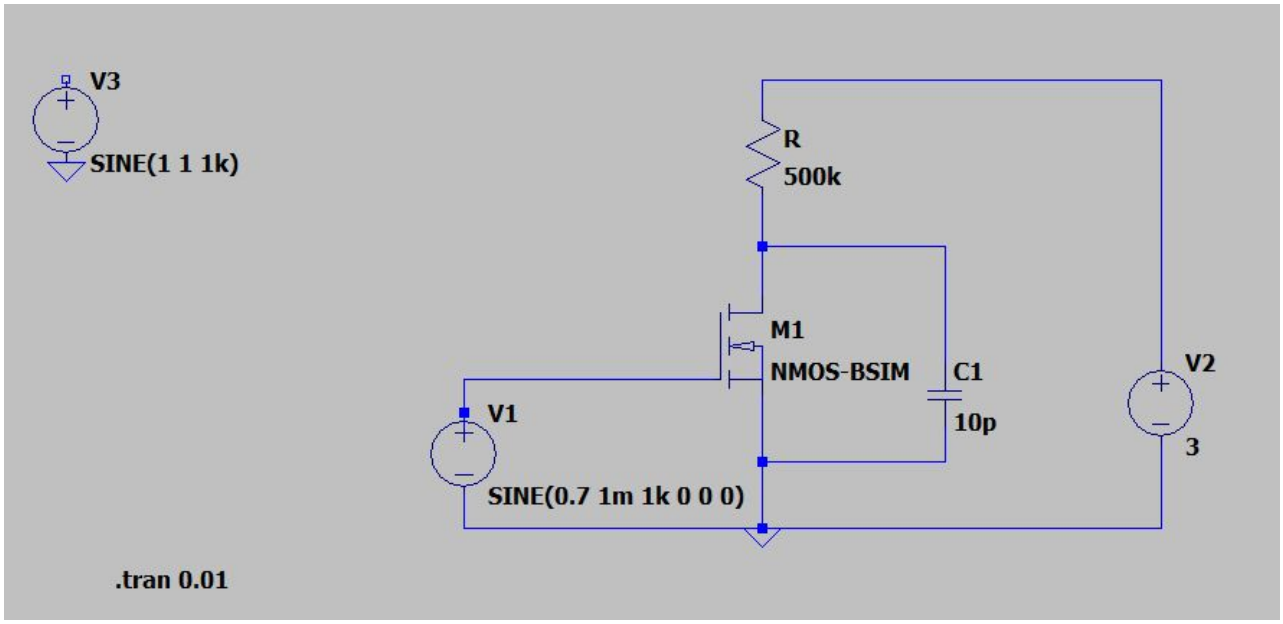




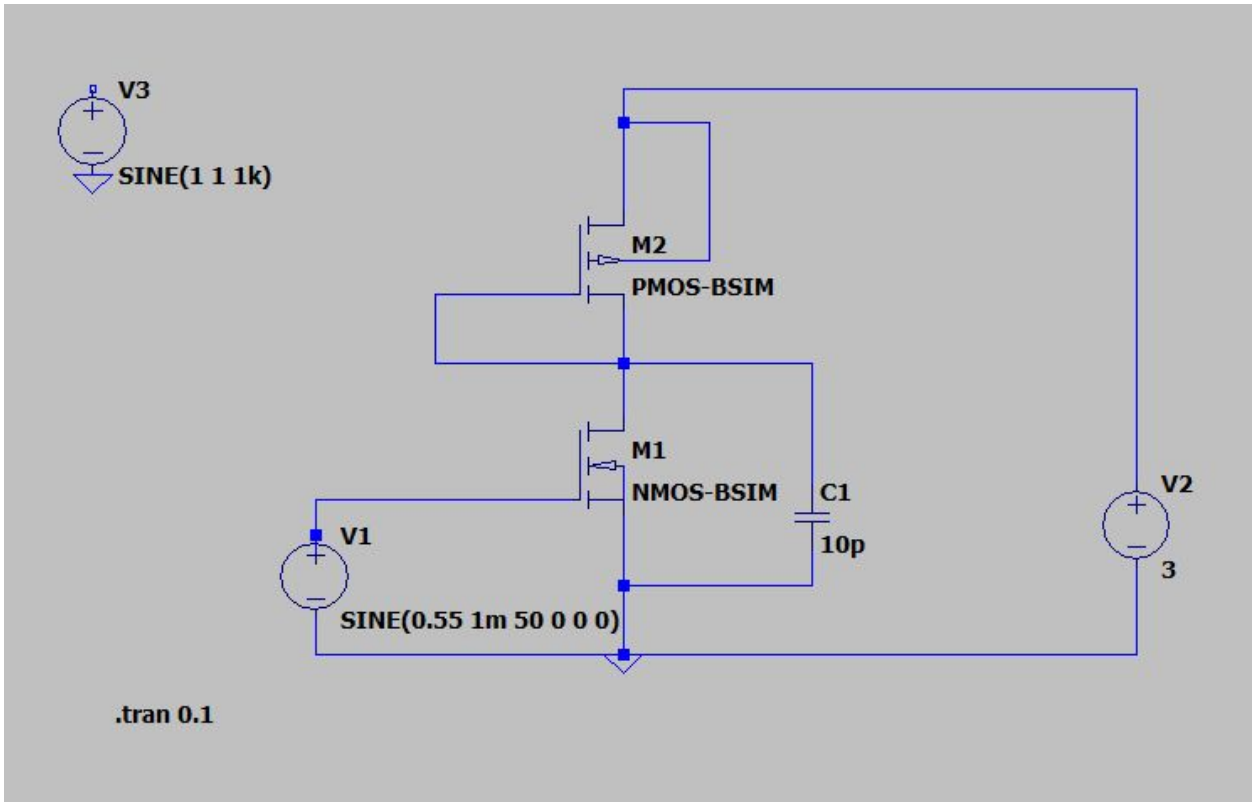
Common gate FET circuit configuration

Circuit Diagram:

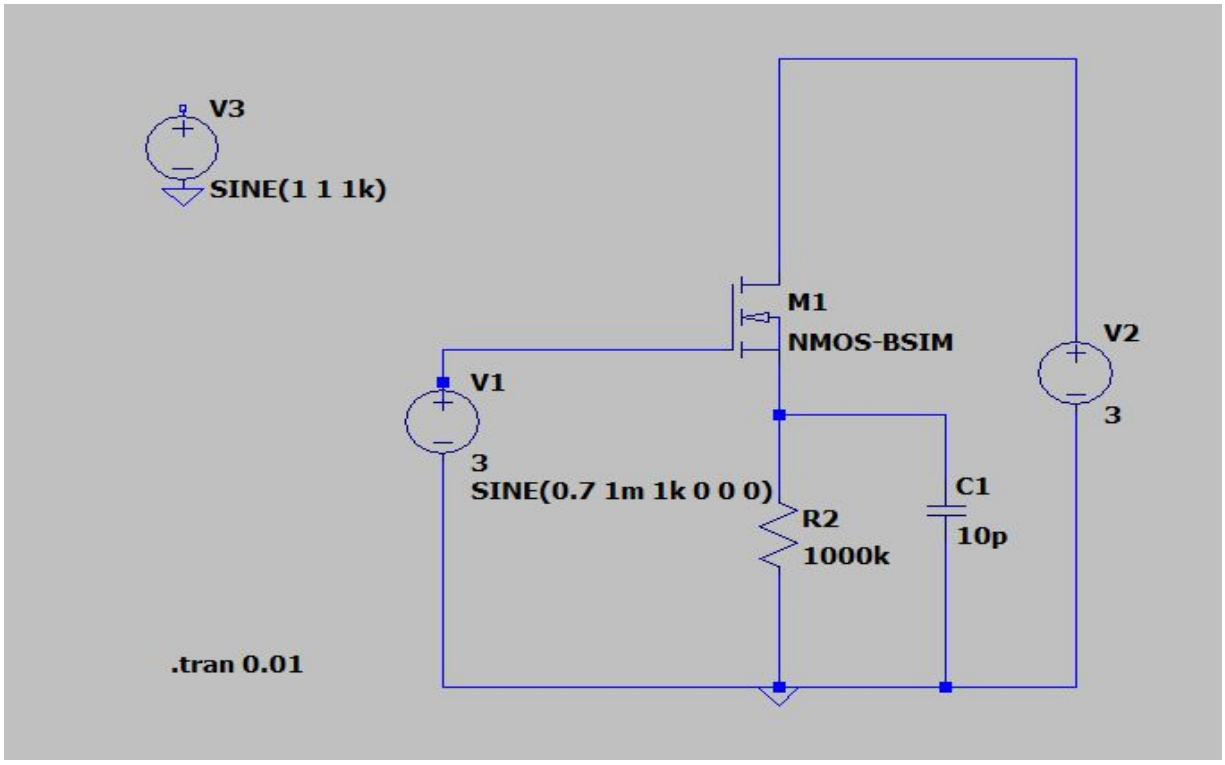
- For Common source - resistor load



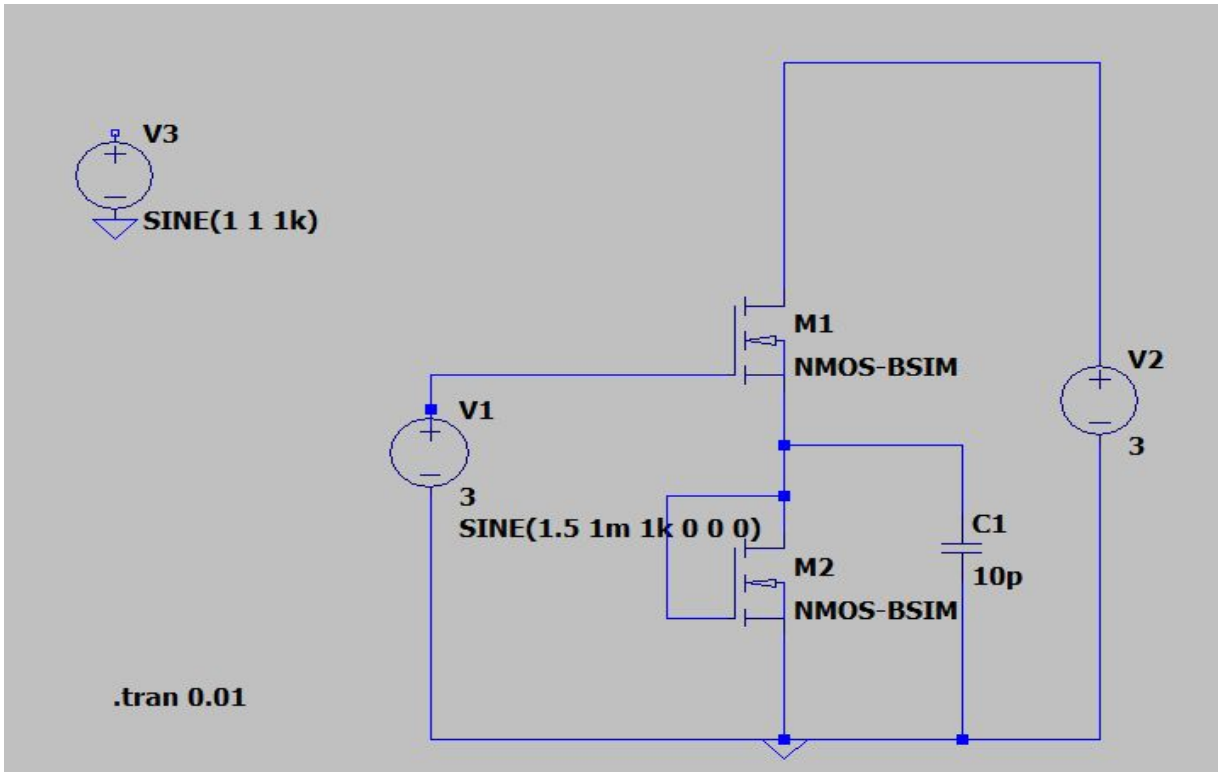
- For Common source - Diode connected



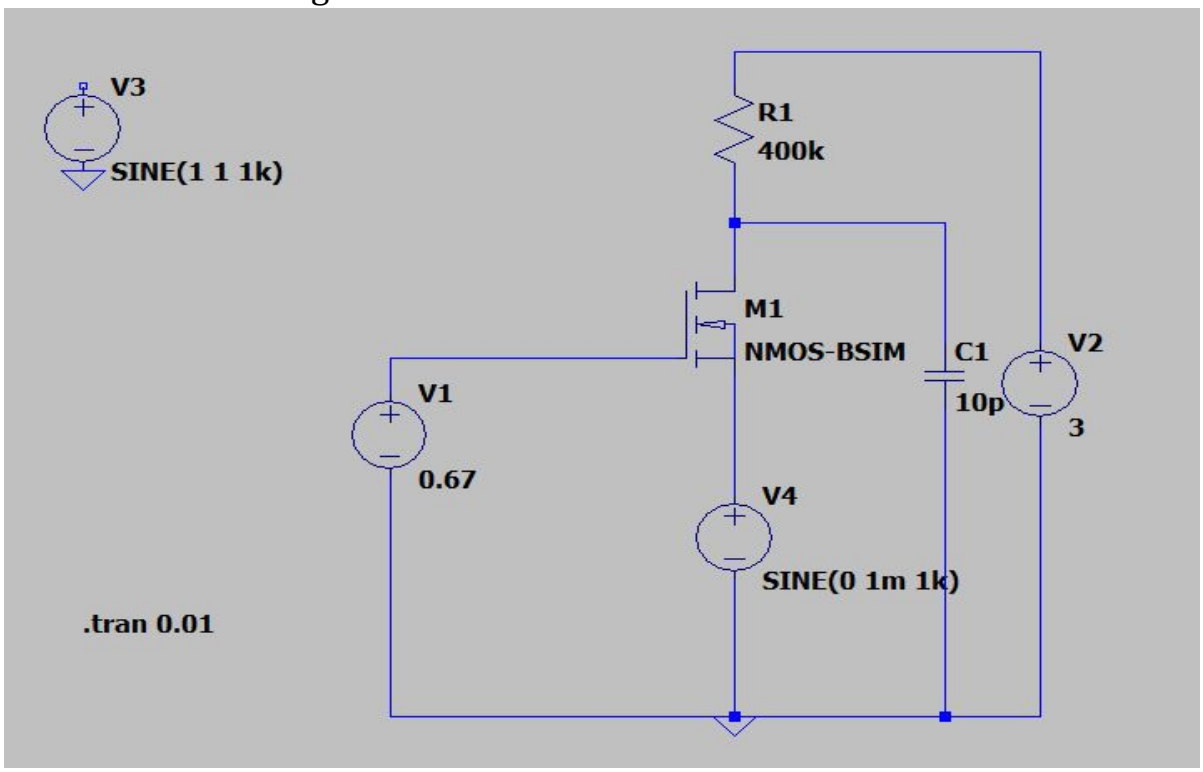
- For Common drain - resistor load



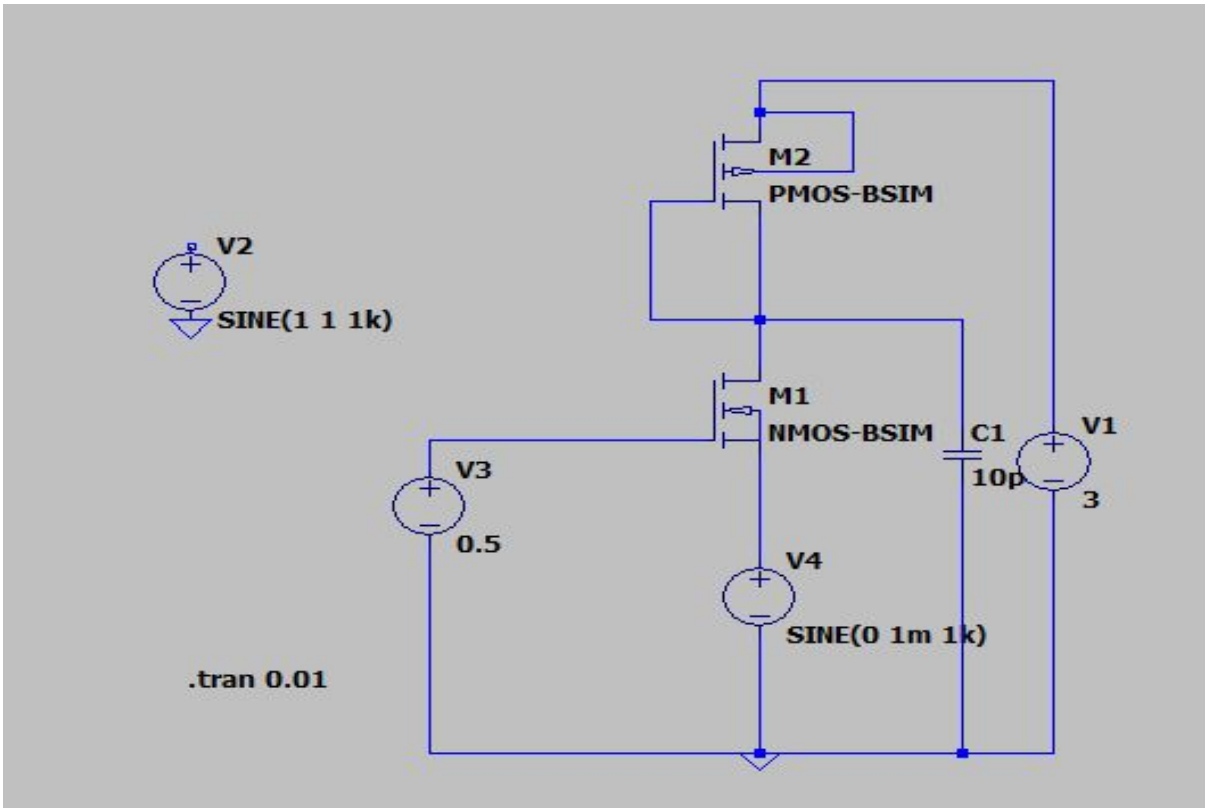
- For Common drain - Diode connected



- For Common gate - resistor load



- For Common gate - Diode connected



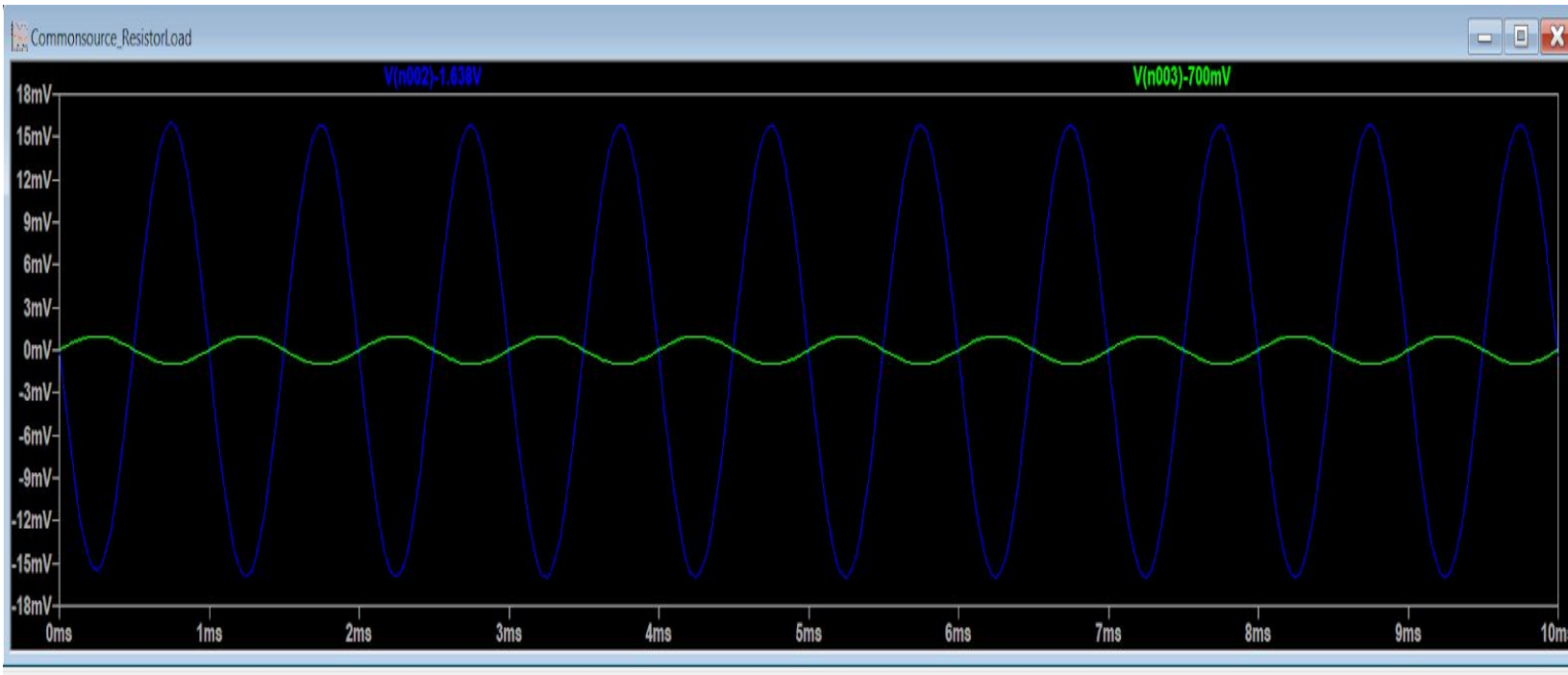
Procedure:

- In a common source amplifier, we give the input at the gate terminal and output is taken from the drain terminal. Then we Implemented the schematic.
- A bias voltage was given to gate and drain, to maintain the transistor in saturation region.
- Then the BSIM 035 model file which defines the values of NMOS & PMOS parameters was included in the schematic using spice directive.
- An AC signal source was applied at the input to do the ac analysis to find the gain and bandwidth.
- Input and output resistance was calculated by adding a small signal voltage source and taking the ratio of voltage applied and current sourced. These simulations were done for resistive load and diode connected load configurations.
- In a common drain amplifier, we give the input at the gate terminal and output is taken from the source terminal. Rest of the procedure is the same.

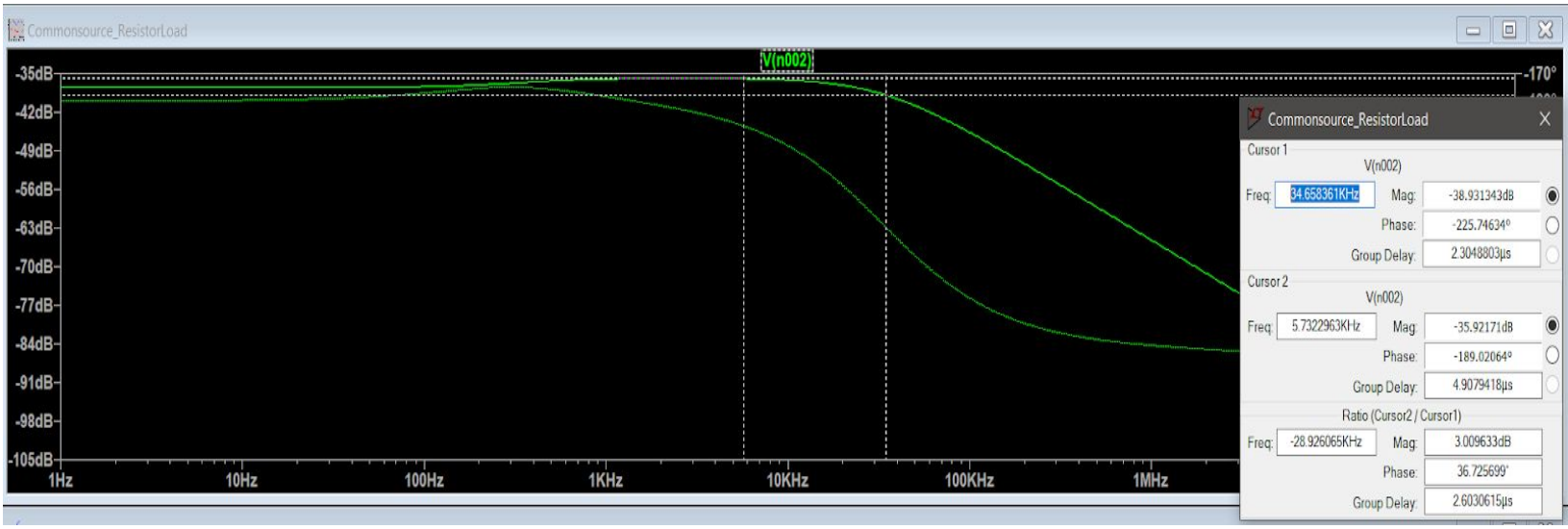
- In a common gate amplifier, we give the input at the source terminal and output is taken from the drain terminal. Rest of the procedure is the same.

Ac and frequency Waveforms:

Common source - Resistor Load:

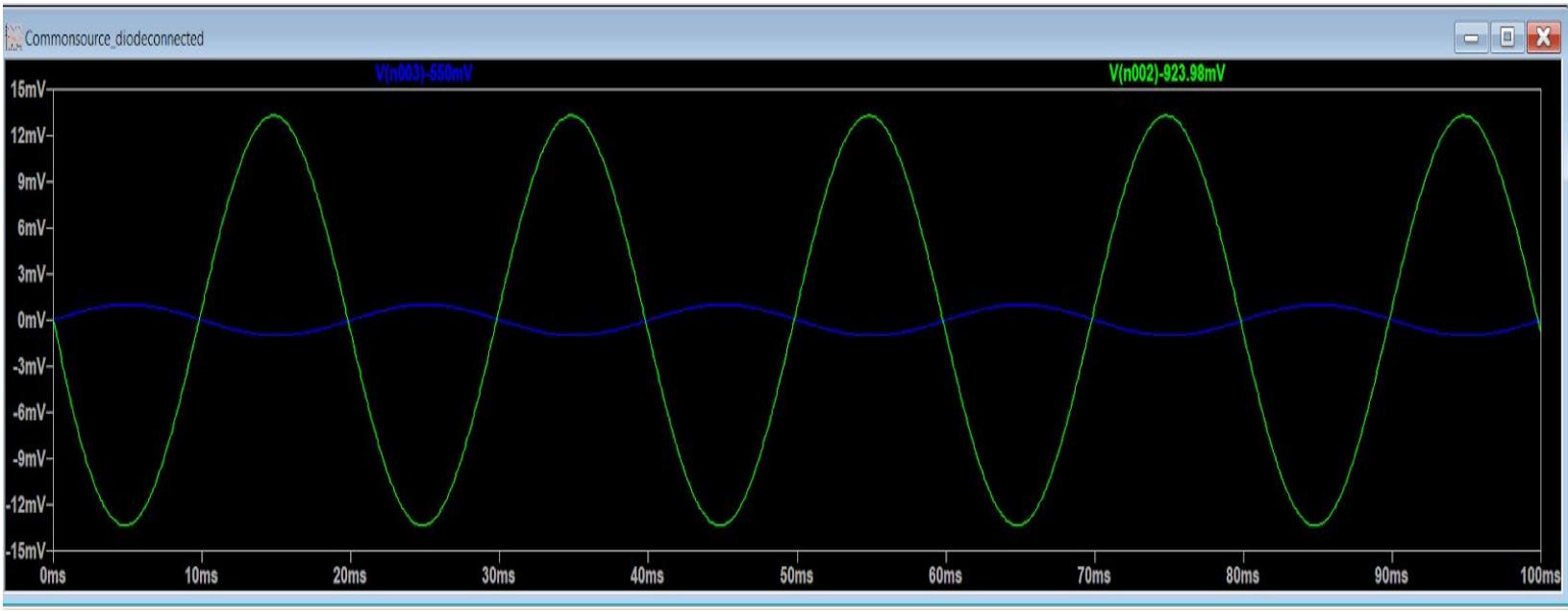


Vi(green) and Vo(blue)

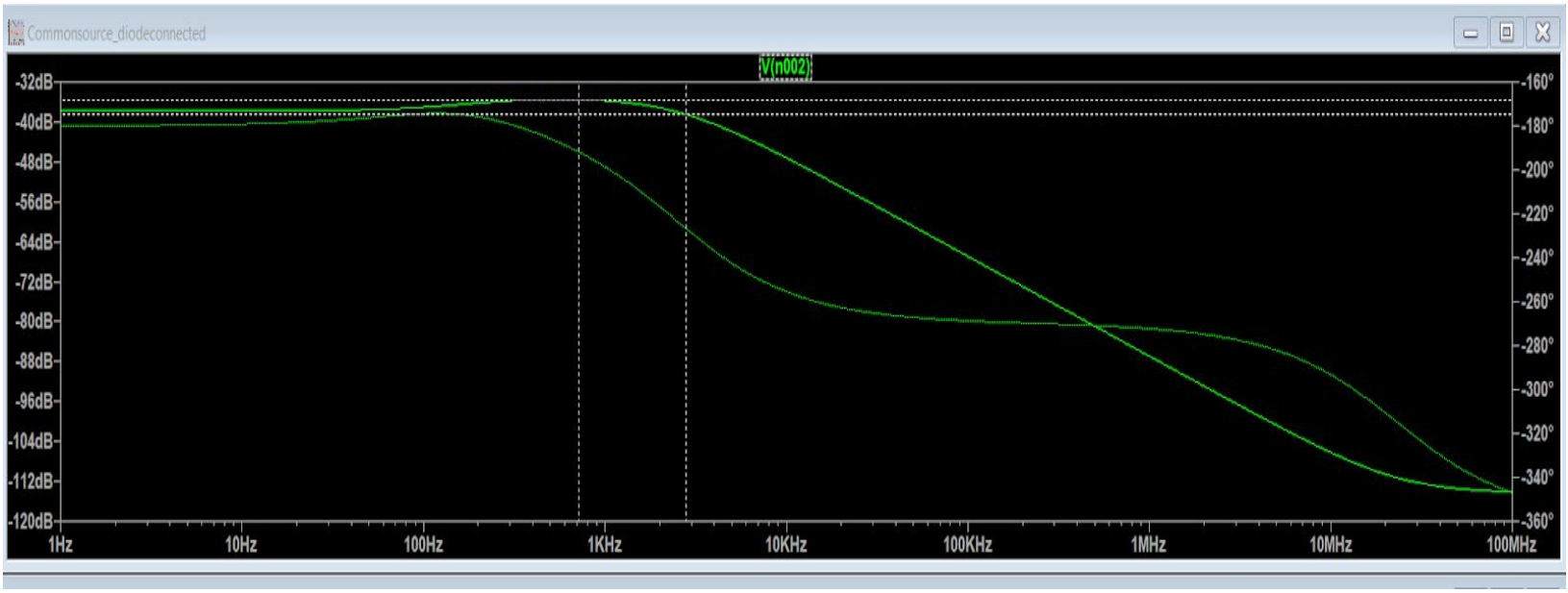


Frequency response

Common source - Diode connected Load:

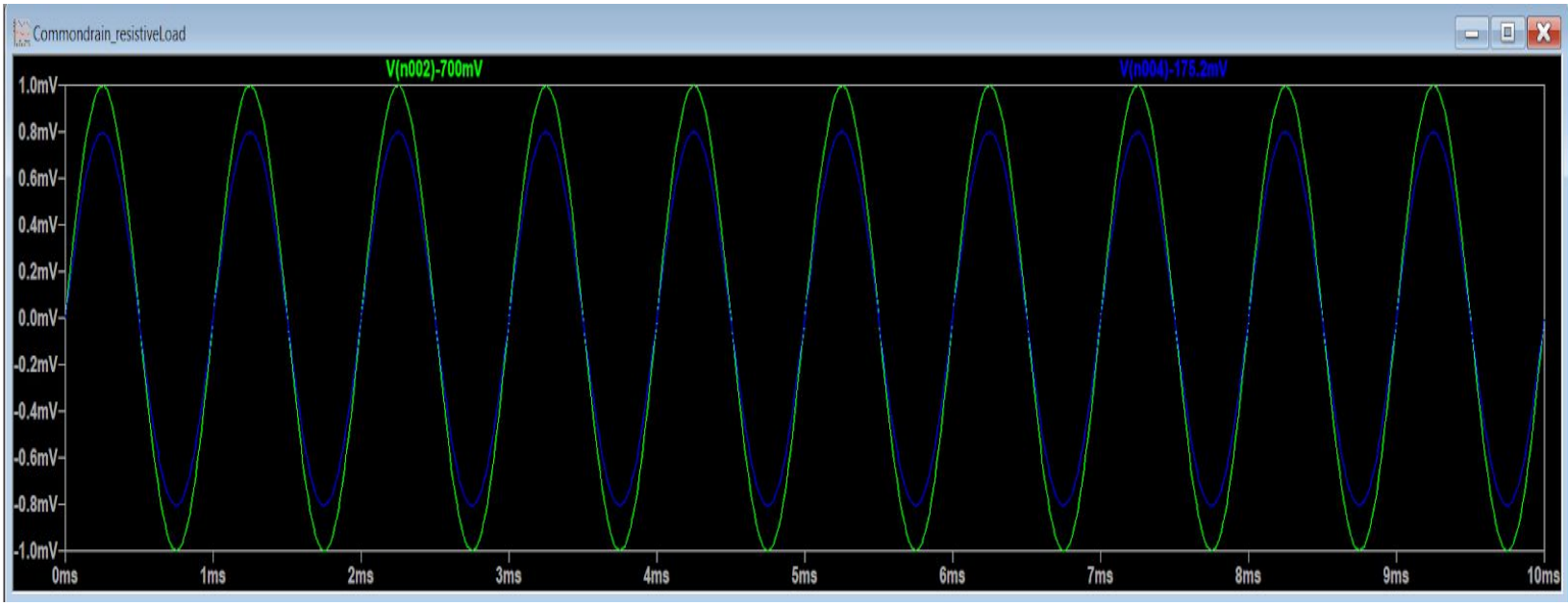


Vi(blue) and Vo(green)

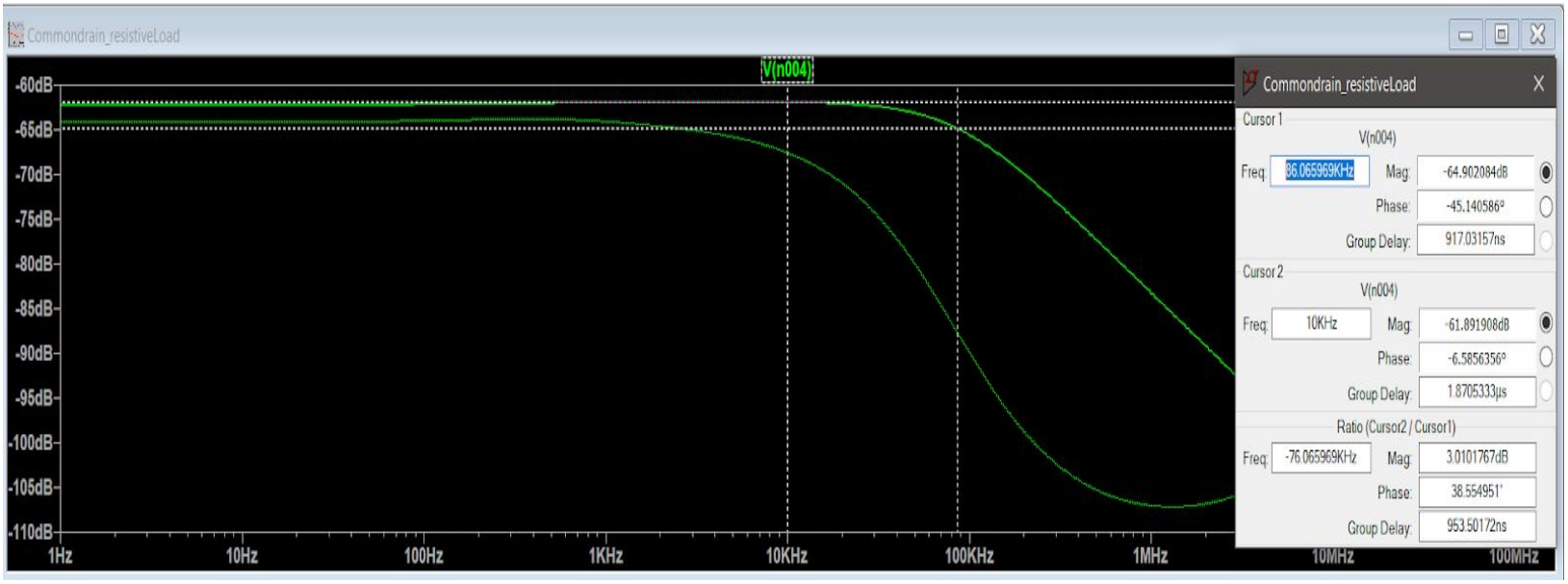


3db Bandwidth

Common Drain - Resistor Load:

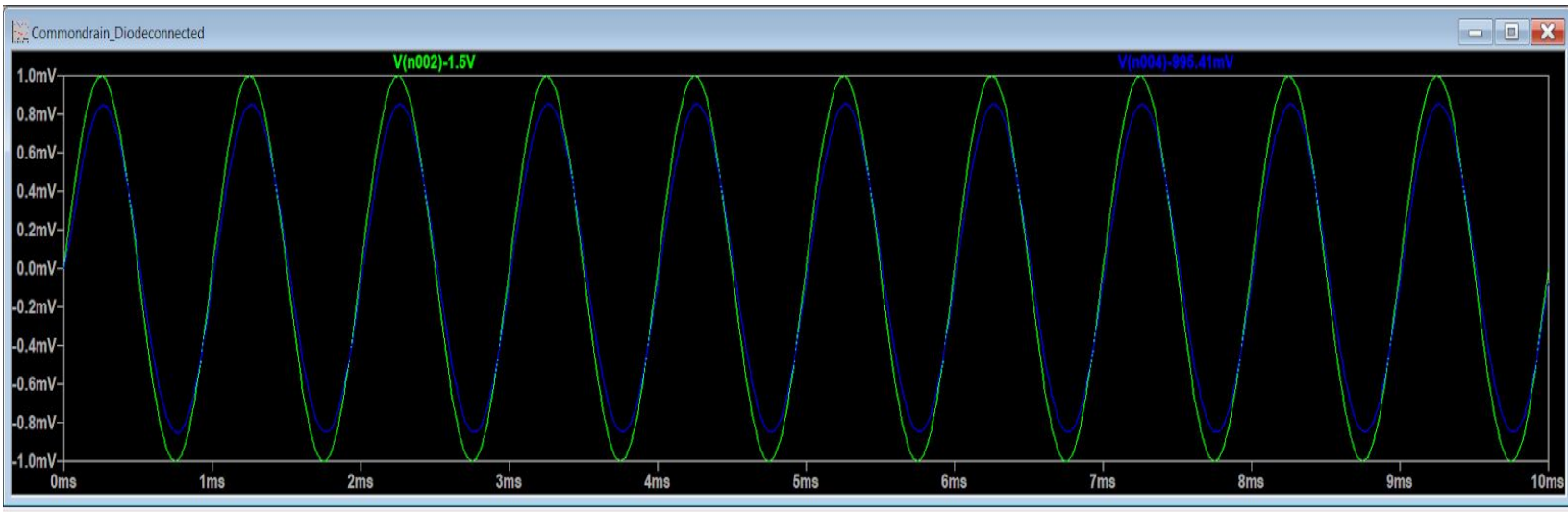


Vi(green) and Vo(blue)

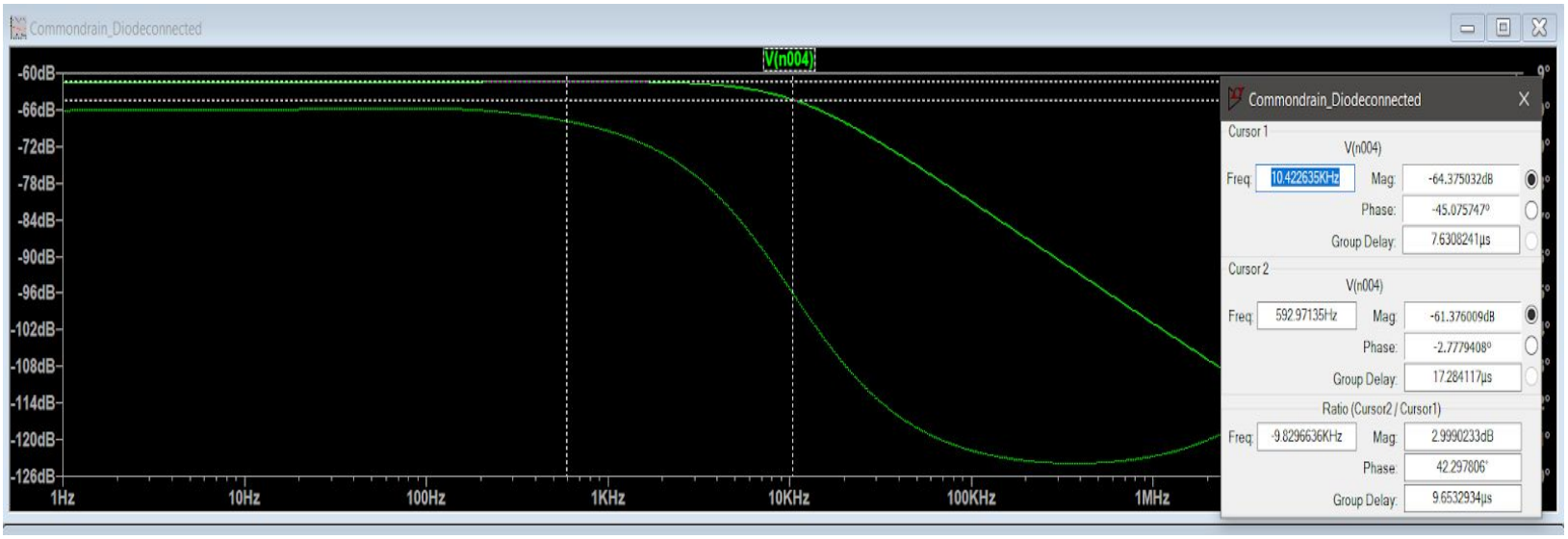


3dB bandwidth

Common Drain - Diode connected Load:

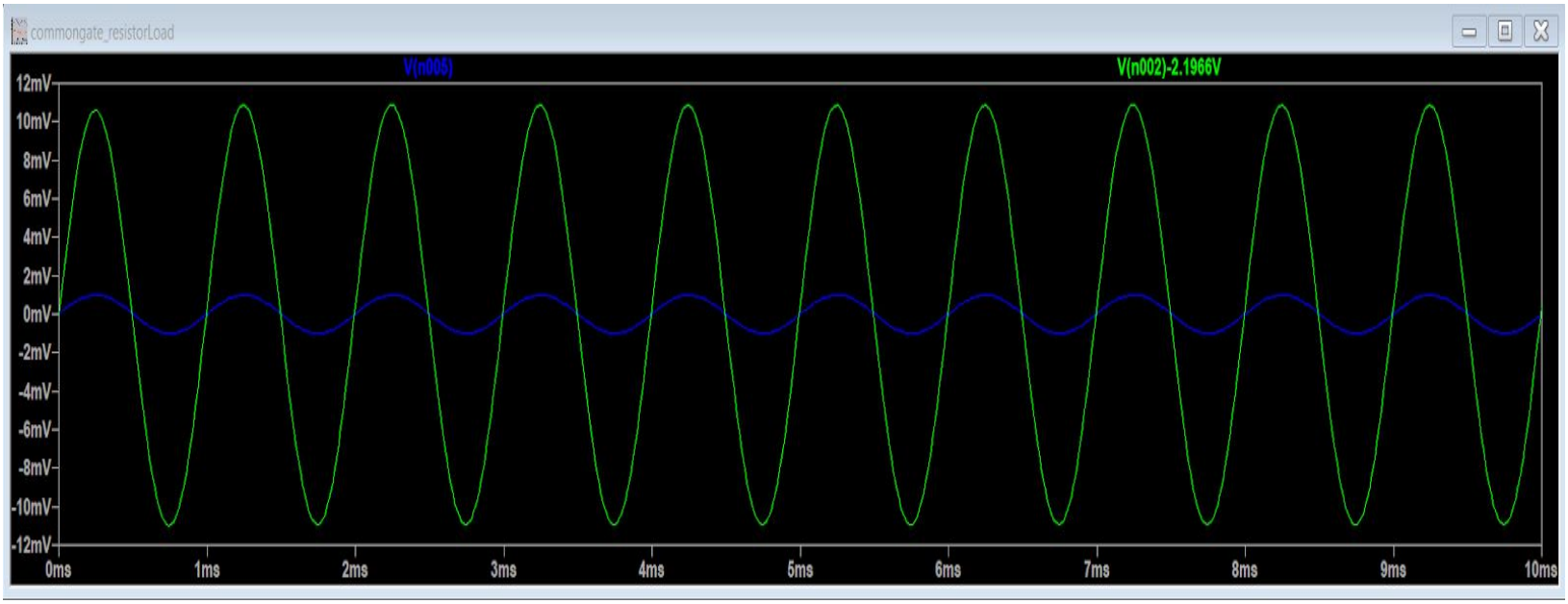


Vin(green) and Vo(blue)

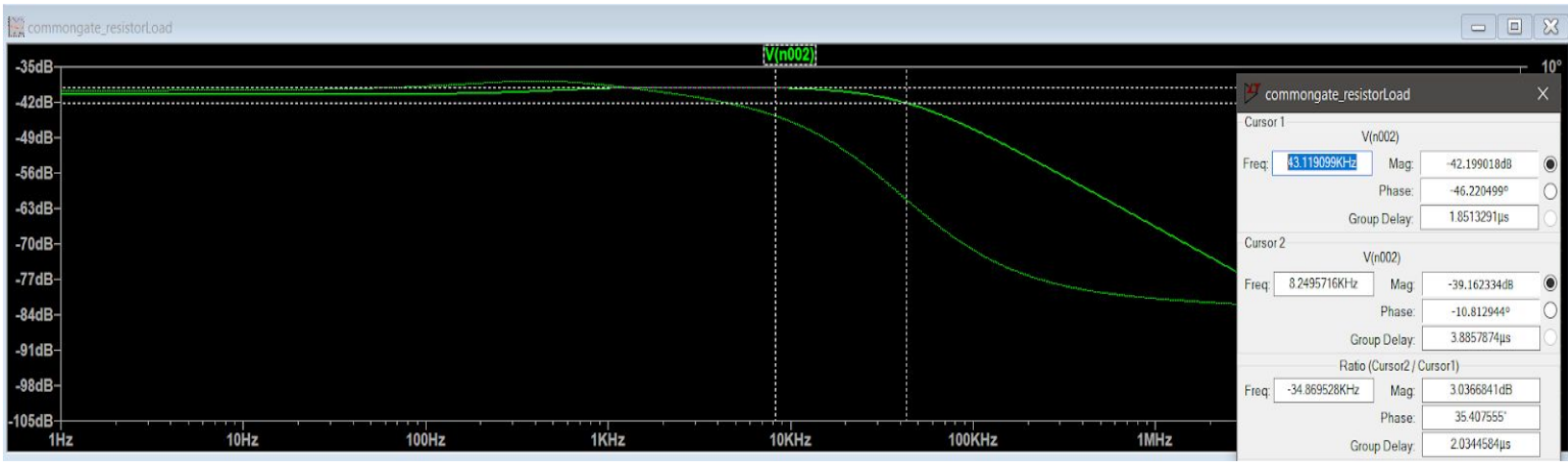


3dB bandwidth

Common gate - Resistor Load:

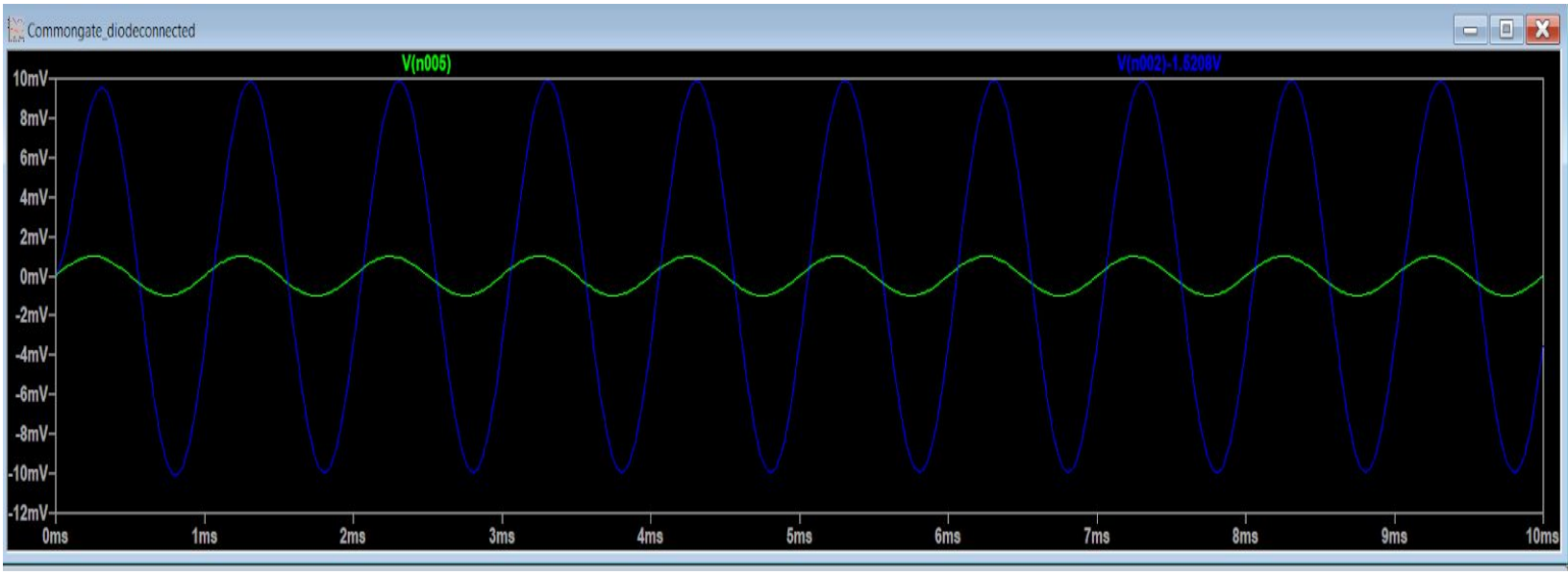


Vi(blue) and Vo(green)

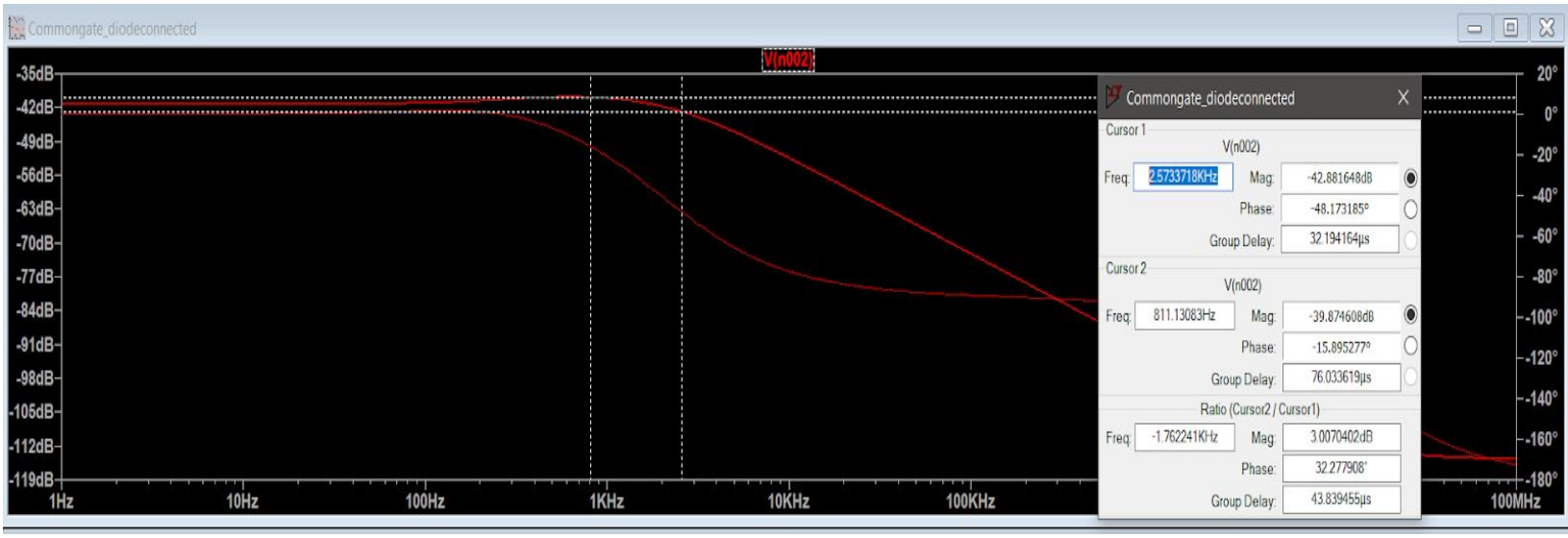


Frequency curve

Common gate - Diode connected Load:



Vi(green) and Vo(blue)



3dB bandwidth

Observation Table:

Type	Load	gain(V/V)	Ro(in $k\Omega$)	Ri(in $k\Omega$)	bandwidth
CS	Resistor	-15	498	infinite	34.6KHz
CS	Diode-connect	-15	23809	infinite	2.79KHz
CD	Resistor	0.8	73.12	infinite	86KHz
CD	Diode-connect	0.8	15922	infinite	10.42KHz
CG	Resistor	10	943.66	93.71	43.11KHz
CG	Diode-connect	9.5	31403	264.33	2.57KHz

Note: infinite resistance means order >= 10

Comparison:

Common source:

- Infinite input resistance
- Bandwidth is lower in diode-connected load
- Voltage gain is high and out of phase.
- High output resistance

Common drain:

- Infinite input resistance
- Bandwidth is lower in diode-connected load
- Voltage gain is low and in phase
- Lower output resistance

Common gate:

- Low input resistance.
- Bandwidth is lower in diode-connected load
- Voltage gain is high and in phase
- High output resistance