Department of Electrical Engineering
IIT Ropar
EE302 Analog Circuits Lab

Experiment 8
Design of Sample and Hold circuits and plotting FFT of output waveforms

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Objectives:

- Design a sample and hold(S/H) circuit using a NMOS switch such that the output of the S/H settles to within 1% of the input within 25ns for a step input of 0.6 V and load capacitor of 20pF.
    - ❖ Find the 1% settling time of the designed S/H for an input of 300mV, 900mV and 1.2V.
    - ❖ Simulate this S/H for an input sine wave of 10K frequency and 100mV amplitude. Plot the fast fourier transform of the sampled output, clock waveform and input signal in matlab.
- Use a NMOS-PMOS complementary switch(pass transistor) to obtain the S/H. Find the 1% settling time of the designed S/H for an input of 300mV, 900mV and 1.2V.

Components/Tools Required: Ltspice, Gdocs

Theory :

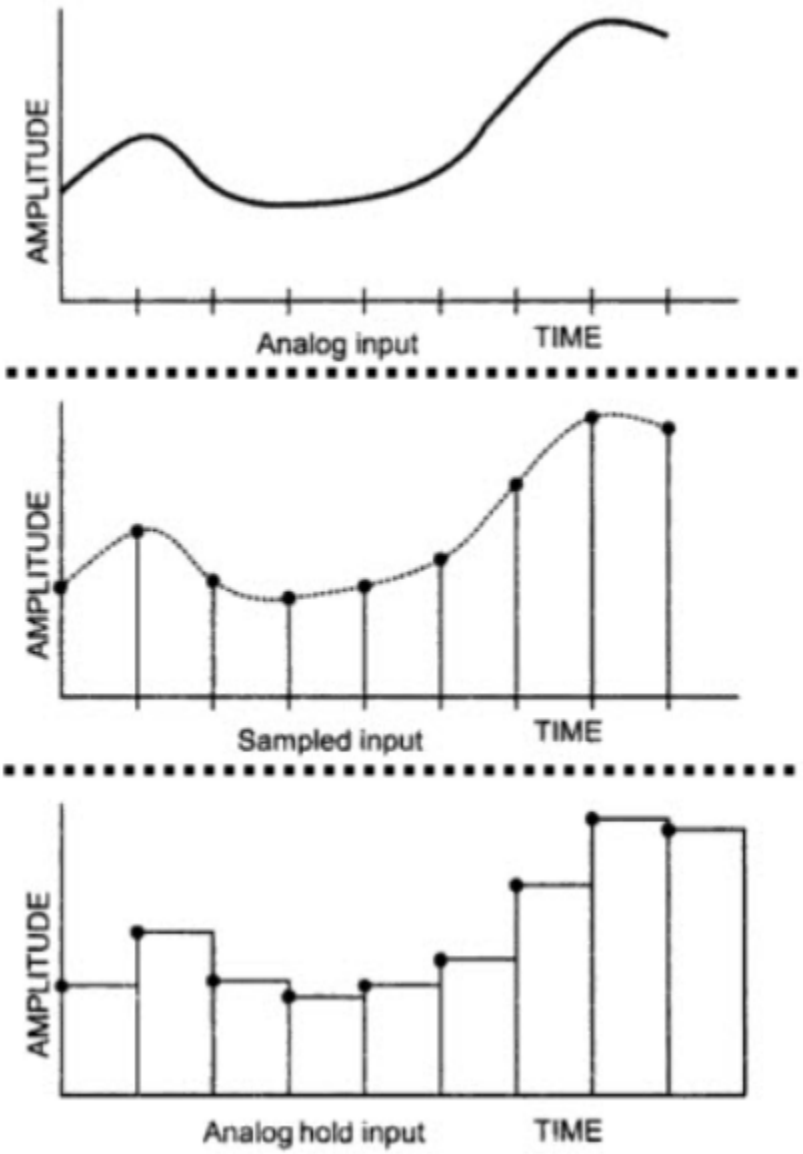
- A Sample and Hold Circuit, sometimes represented as S/H Circuit or S & H Circuit, is usually used with an Analog to Digital Converter to sample the input analog signal and hold the sampled signal.
- In the S/H Circuit, the analog signal is sampled for a short interval of time, usually in the range of 10µS to 1µS. After this, the sampled value is held until the arrival of the next input signal to be sampled. The duration for holding the sample will be usually between few milliseconds to few seconds.

Applications:

- Analog to Digital Converter Circuits (ADC)
- Digital Interface Circuits
- Operational Amplifiers

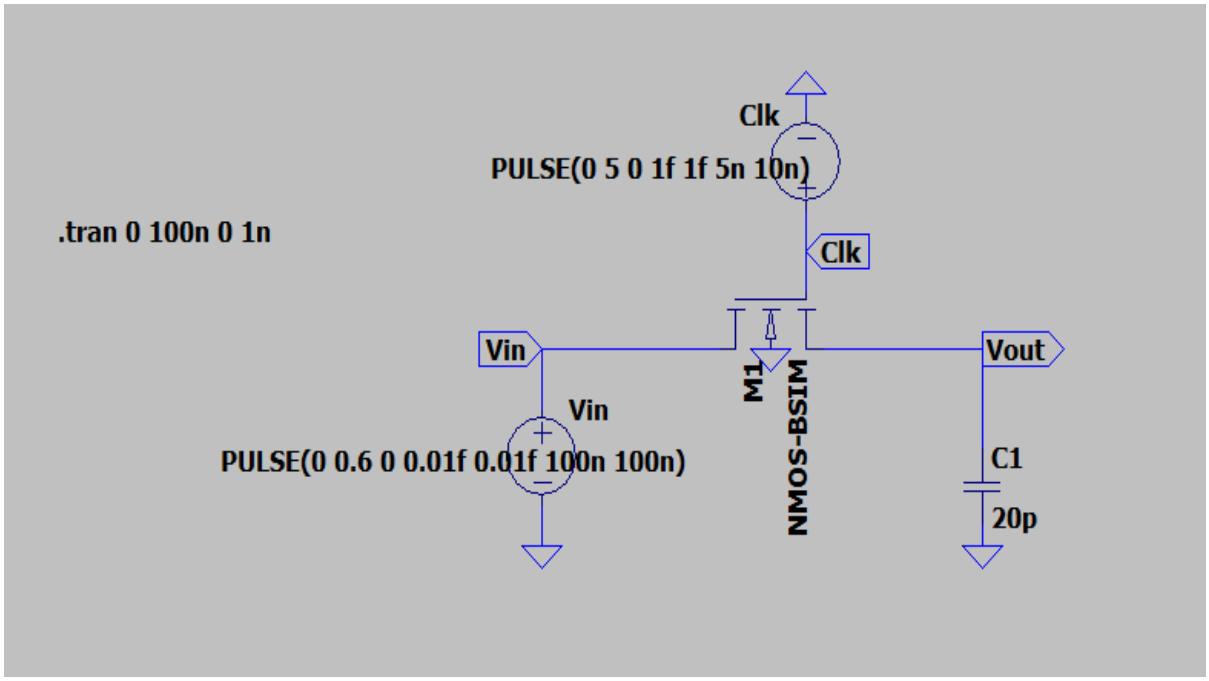
- Analog De-multiplexers
- Data distribution systems
- Storage of outputs of multiplexers
- Pulse Modulation System

Figure below shows the output and input of S/H circuits.

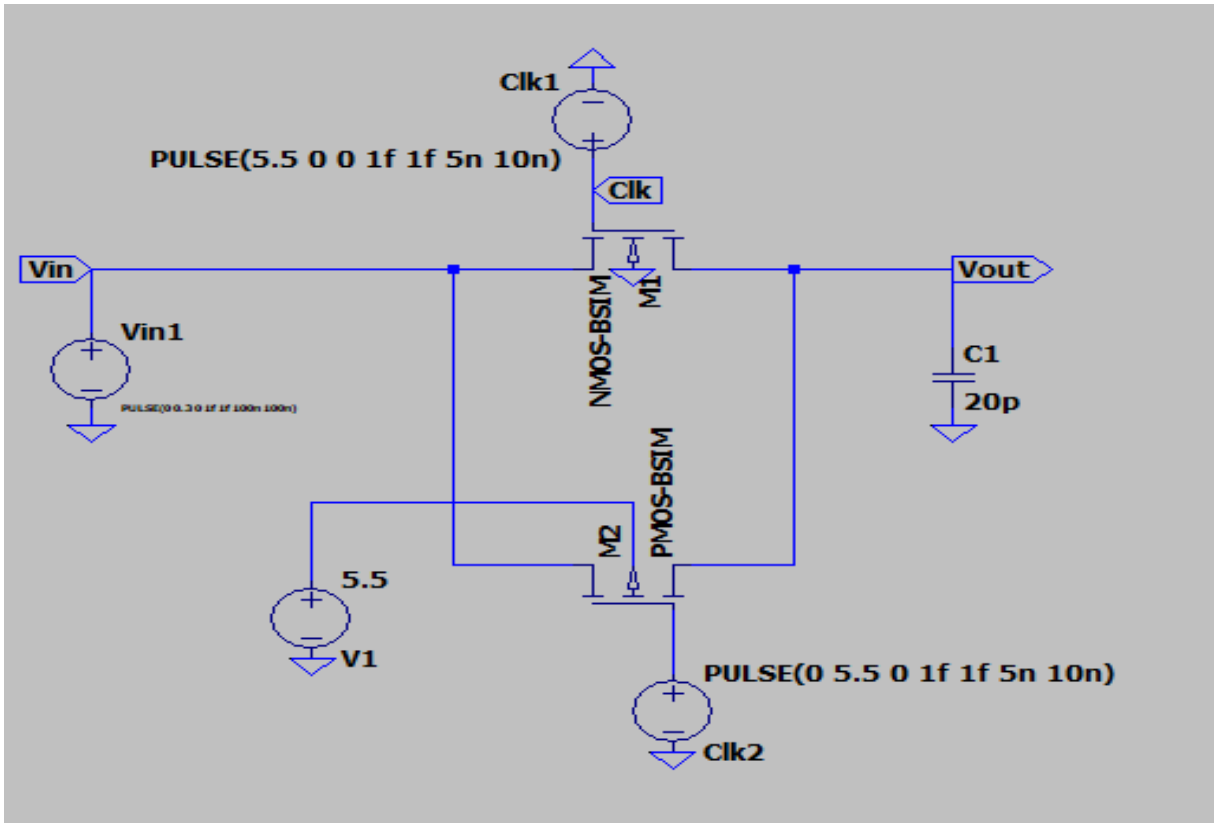


Circuit Diagram:

- S/H circuit using NMOS



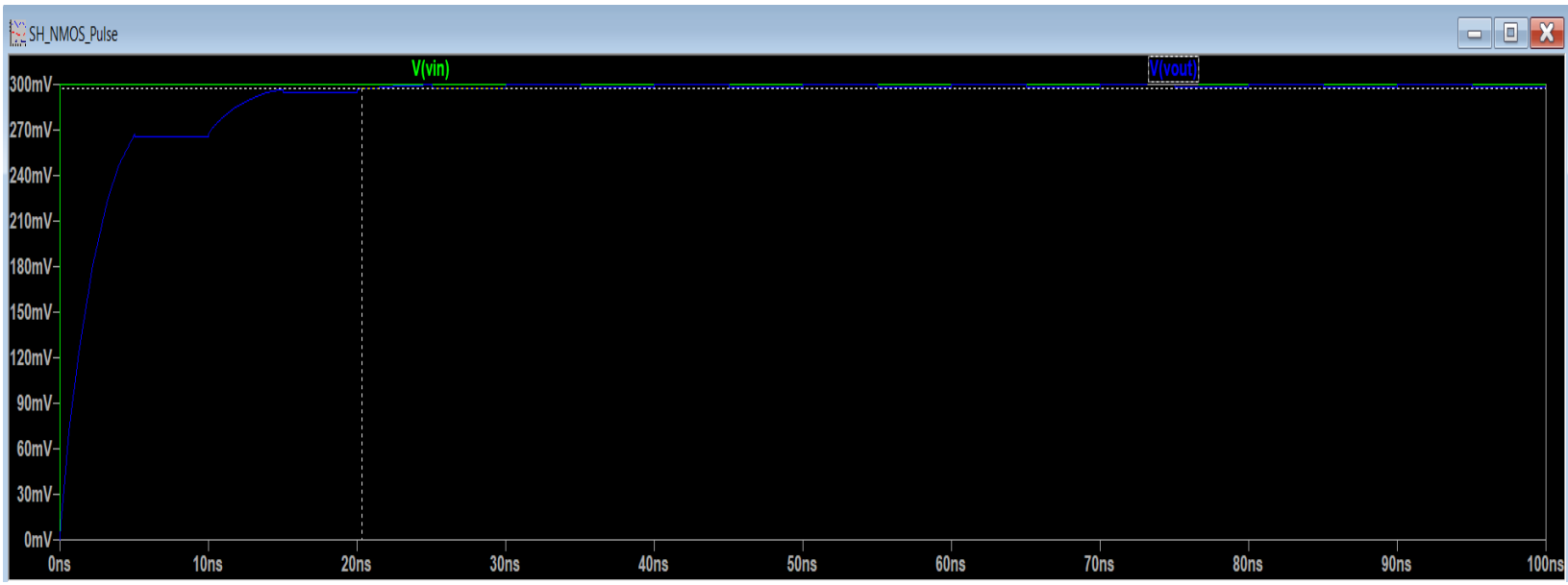
- S/H circuit using Pass Transistor



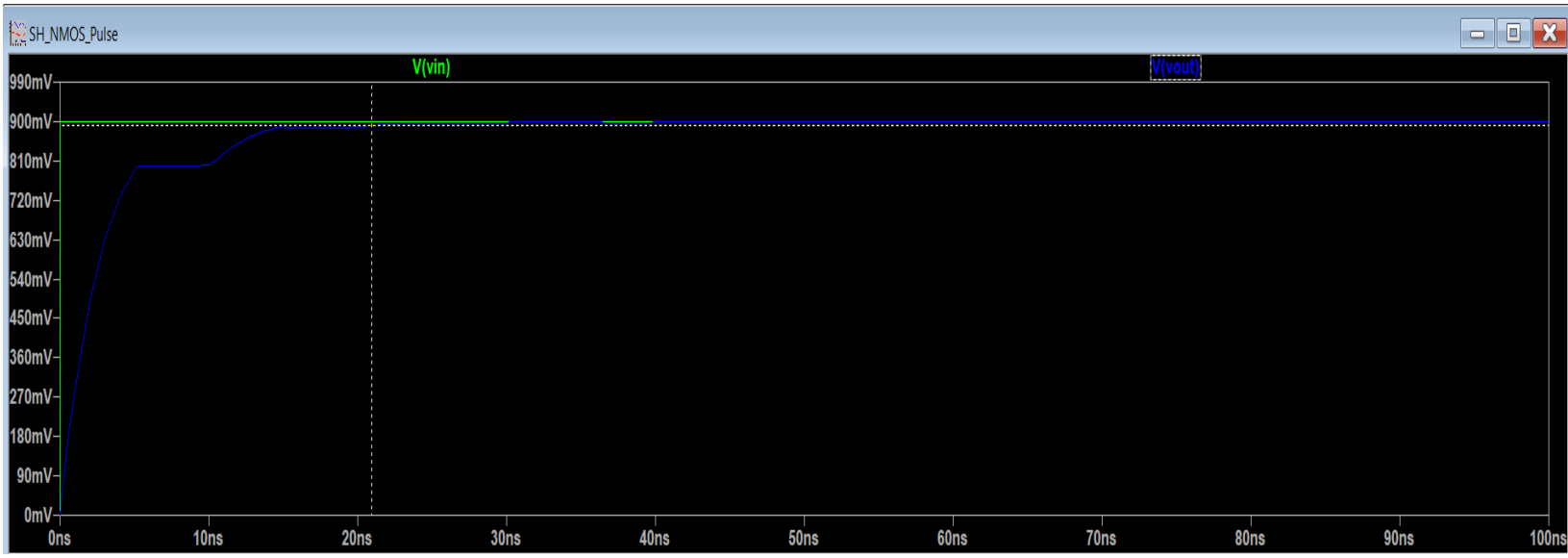
Waveforms:

- S/H using NMOS

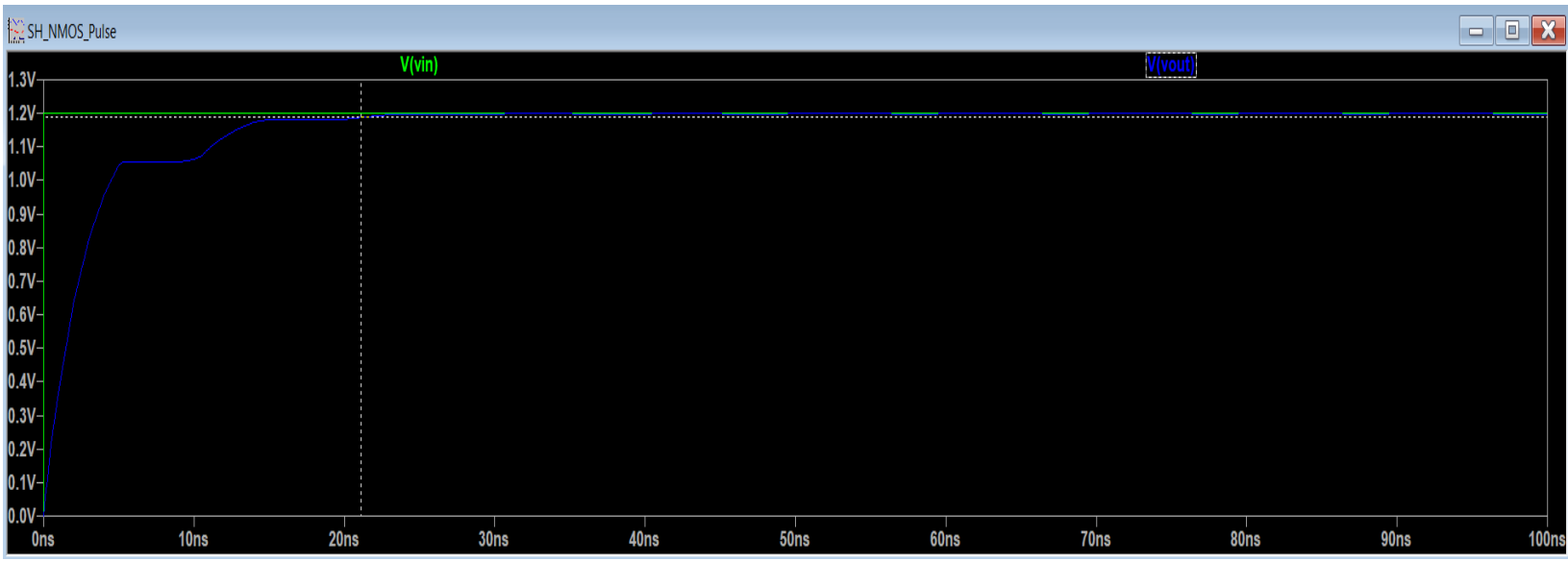
Pulse input : 0.6V & Vout : 1 % settling time = 20.44ns(<25 ns)



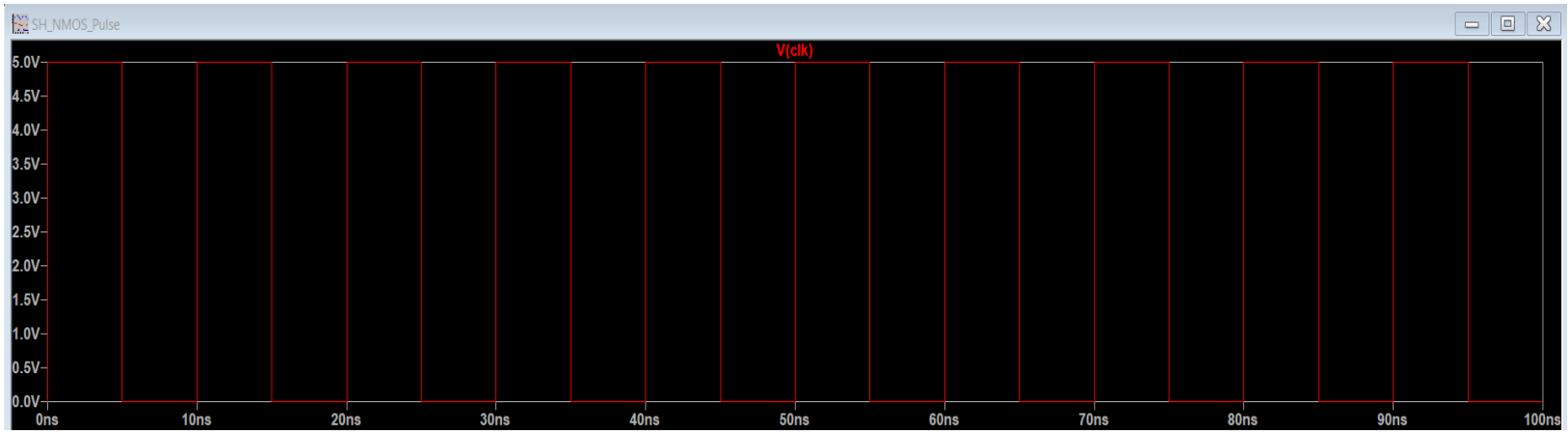
Pulse input : 0.3V & Vout : 1 % settling time = 20.3 ns(<25 ns)



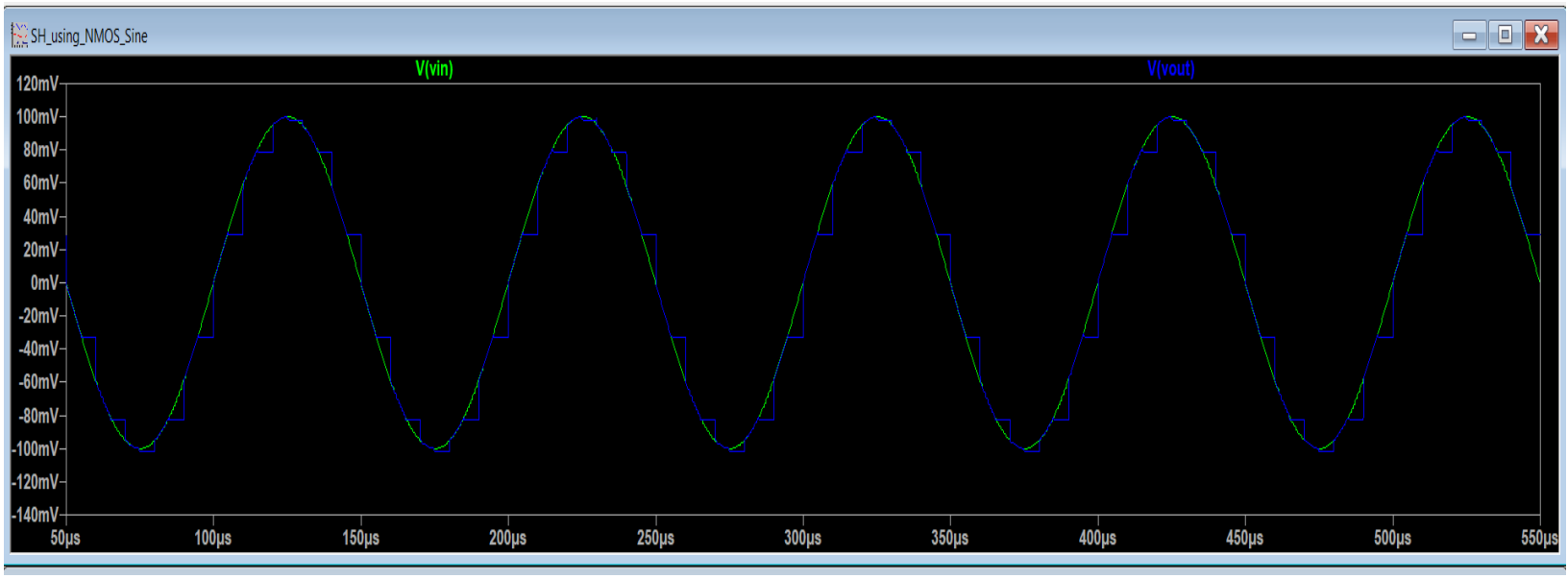
Pulse input : 0.9V & Vout : 1 % settling time = 20.92 ns(<25 ns)



Pulse input : 1.2 V & Vout : 1 % settling time = 21.17 ns(<25 ns)

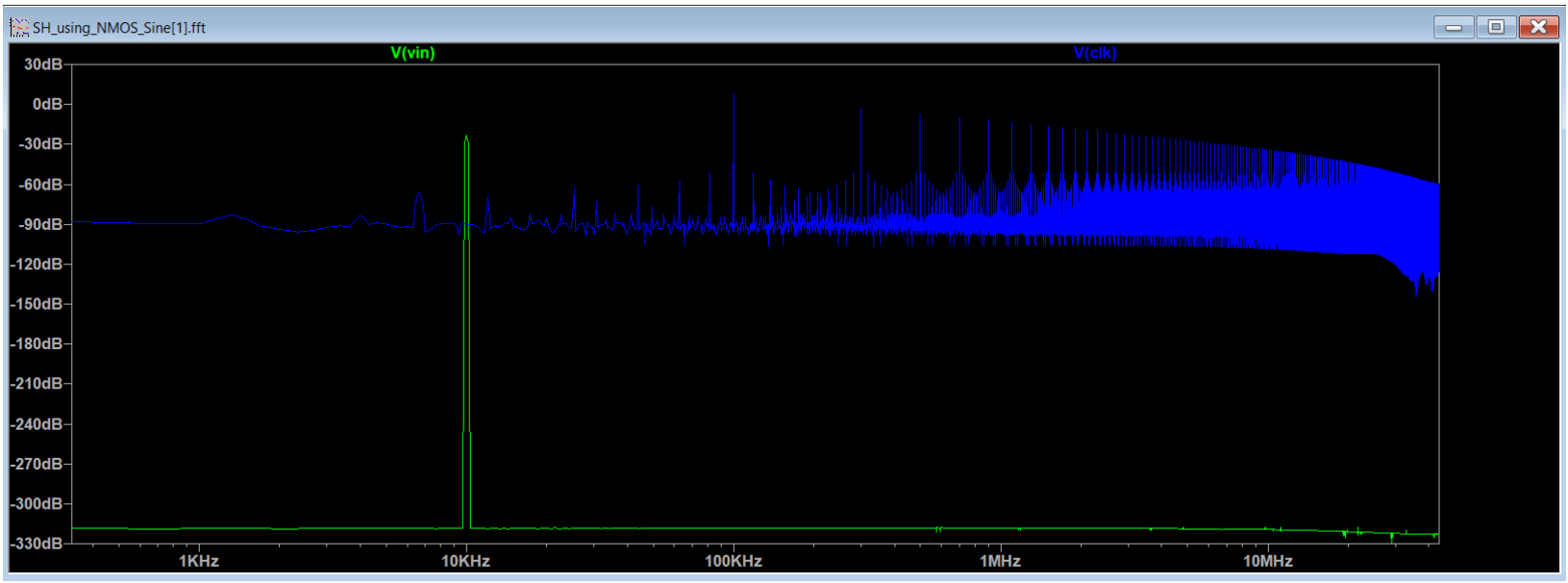


Clock pulse in NMOS

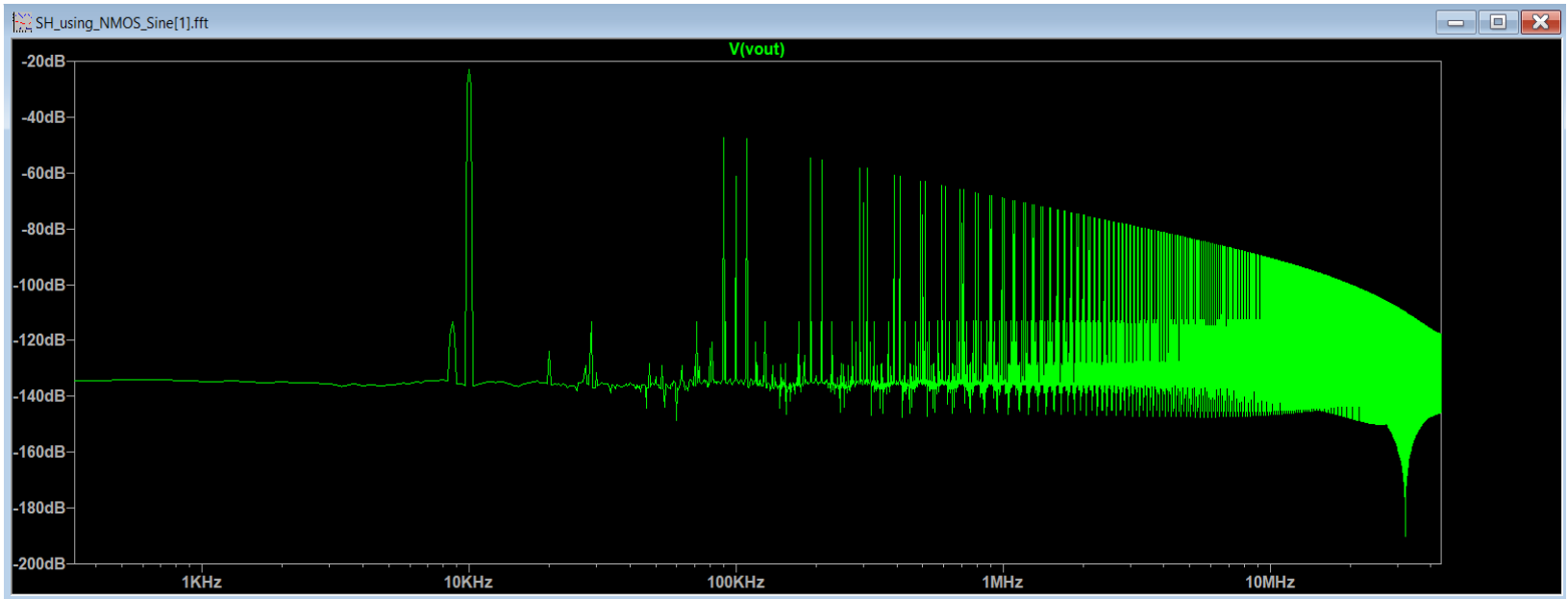


Sine input : 10 KHz and 100mV

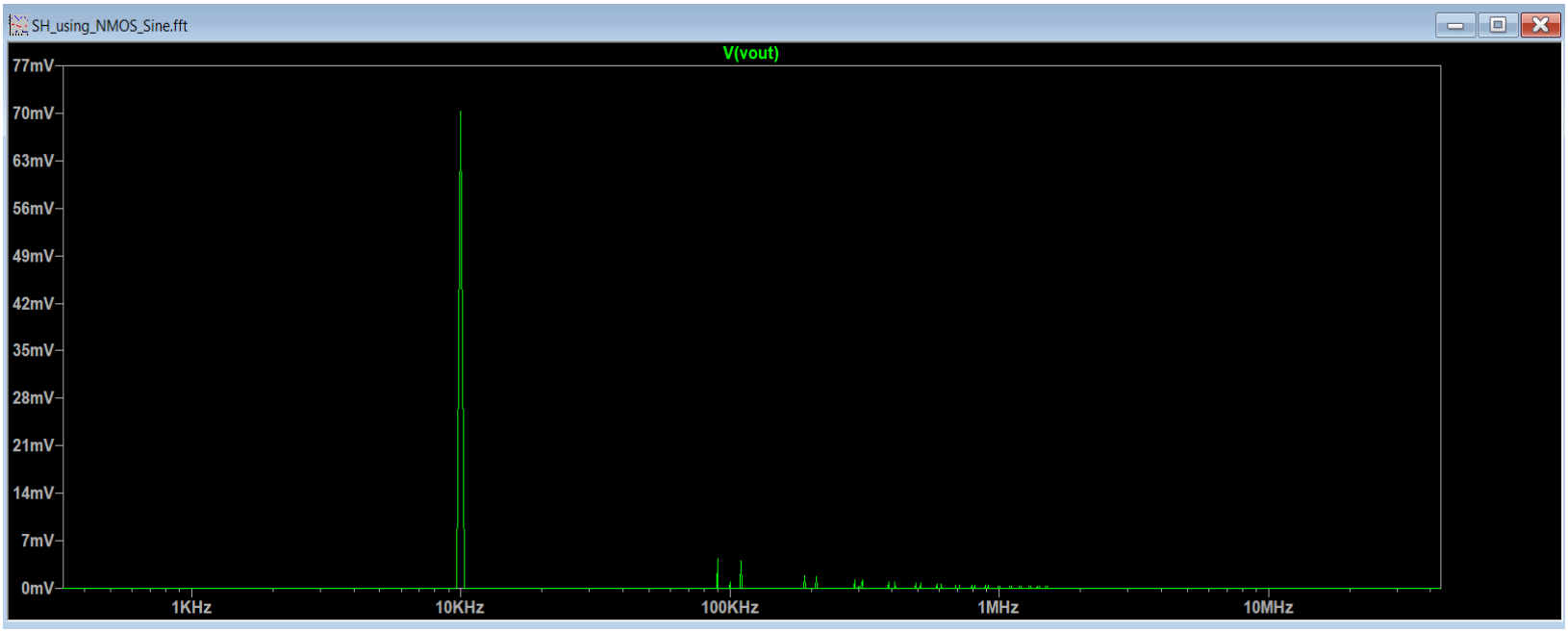
FFT waveforms in NMOS S/H



FFT of input Sine wave and clock pulse



FFT of S/H output in dB scale



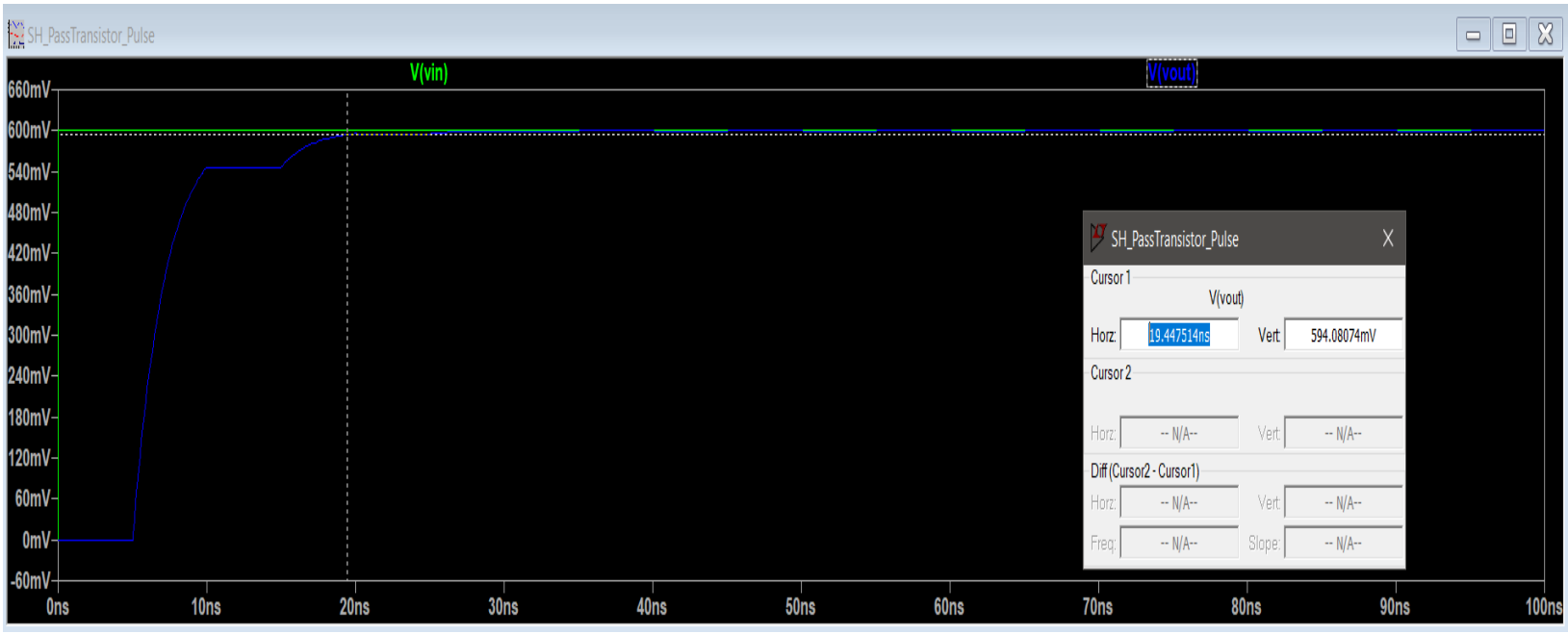
FFT of S/H output in Linear scale

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phas [degr
1	1.000e+04	9.950e-02	1.000e+00	-4
2	2.000e+04	9.008e-07	9.053e-06	176
3	3.000e+04	5.248e-07	5.274e-06	-106
4	4.000e+04	2.166e-07	2.177e-06	-12
5	5.000e+04	1.441e-07	1.448e-06	101
6	6.000e+04	1.702e-07	1.711e-06	-112
7	7.000e+04	5.166e-07	5.192e-06	-22
8	8.000e+04	8.935e-07	8.980e-06	50
9	9.000e+04	6.092e-03	6.123e-02	-26
10	1.000e+05	1.247e-03	1.253e-02	-0

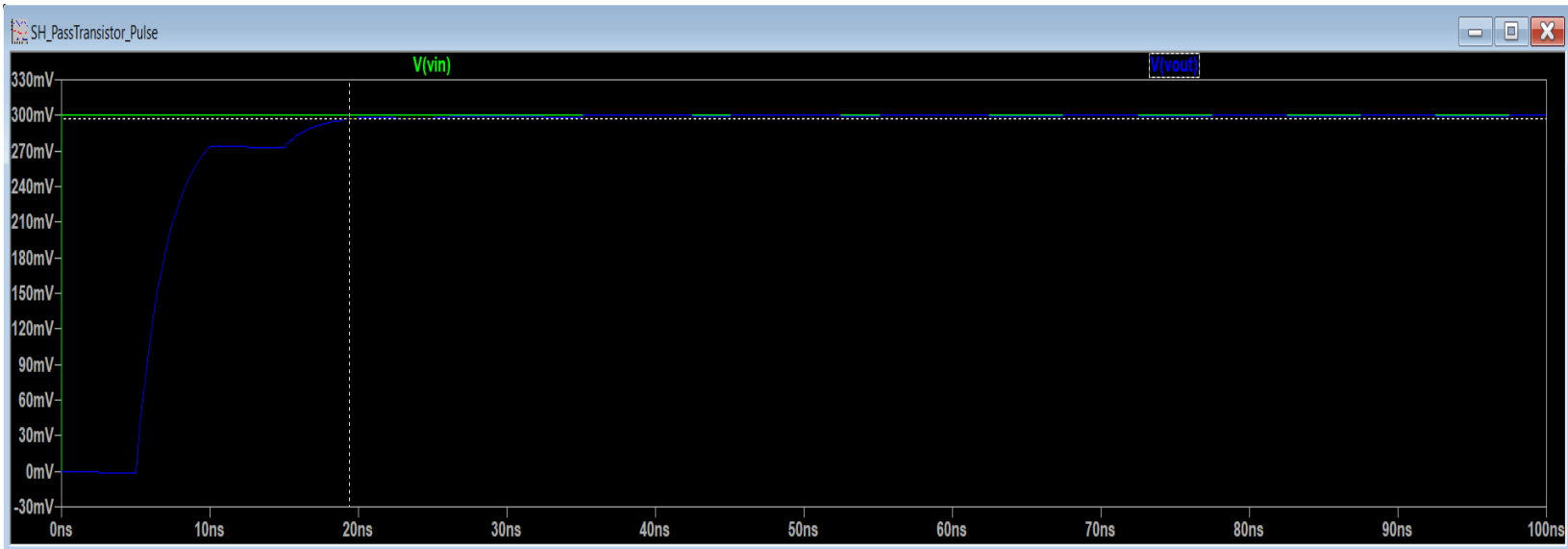
Total Harmonic Distortion: 6.249505%(10.261716%)

We can see from directive : THD = 6.25 %

- S/H using PassTransistor

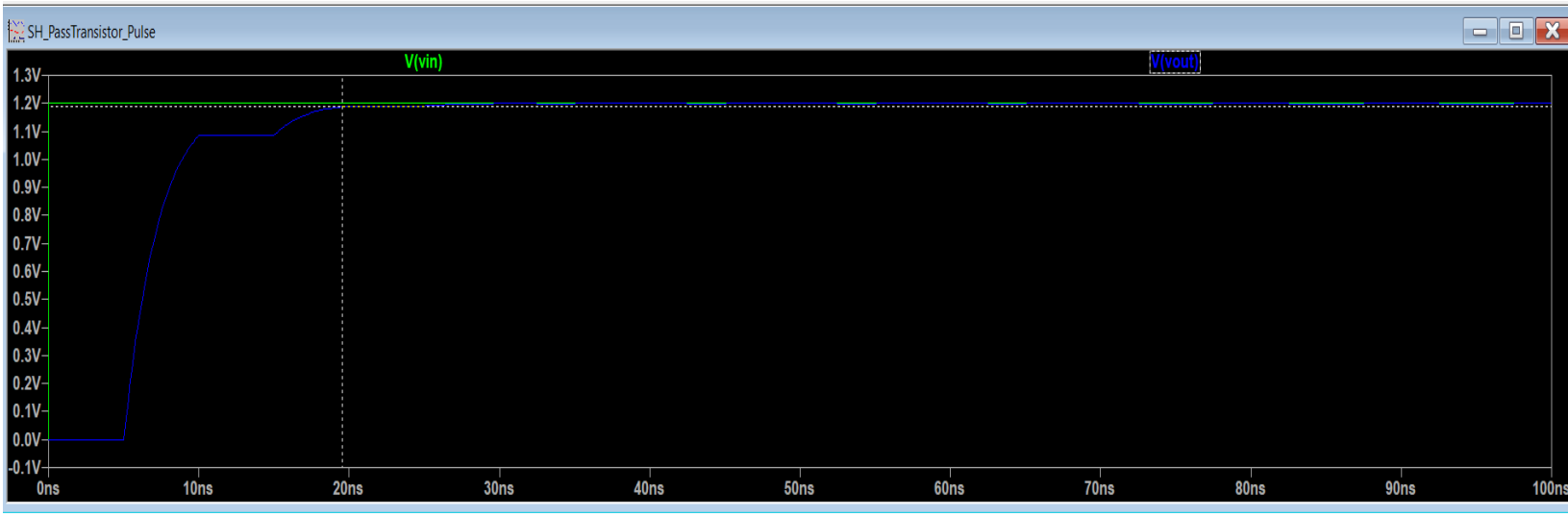


Pulse input : 0.6V & Vout : 1 % settling time = 19.44 ns(<25 ns)

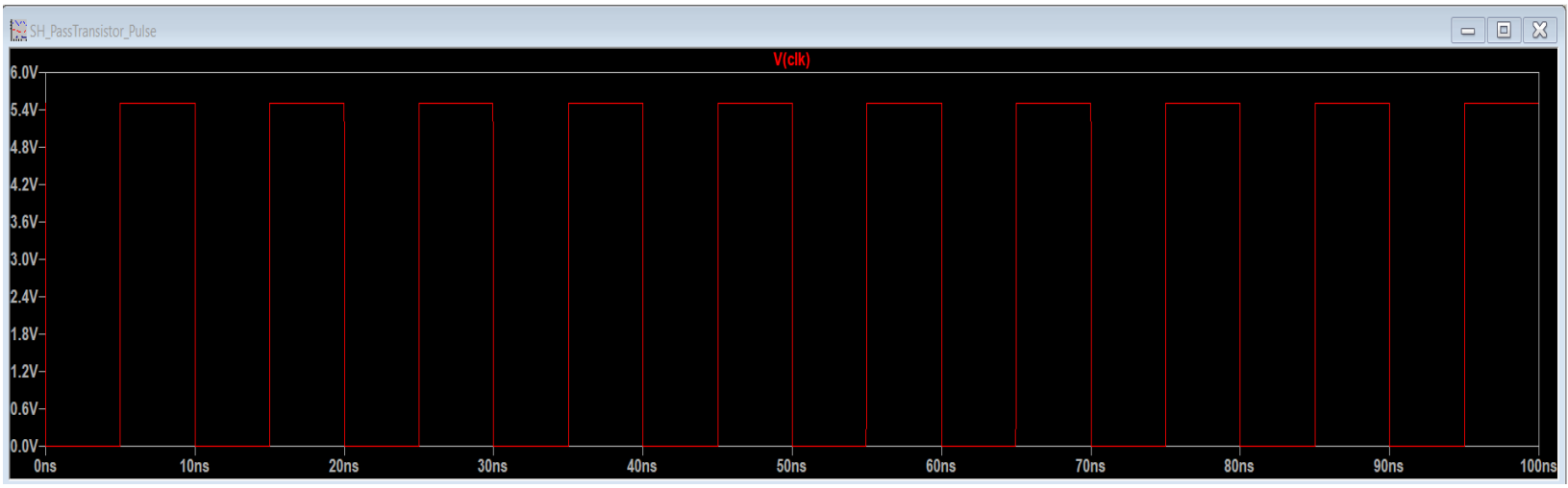


Pulse input : 0.3V & Vout : 1 % settling time = 19.4 ns(<25 ns)

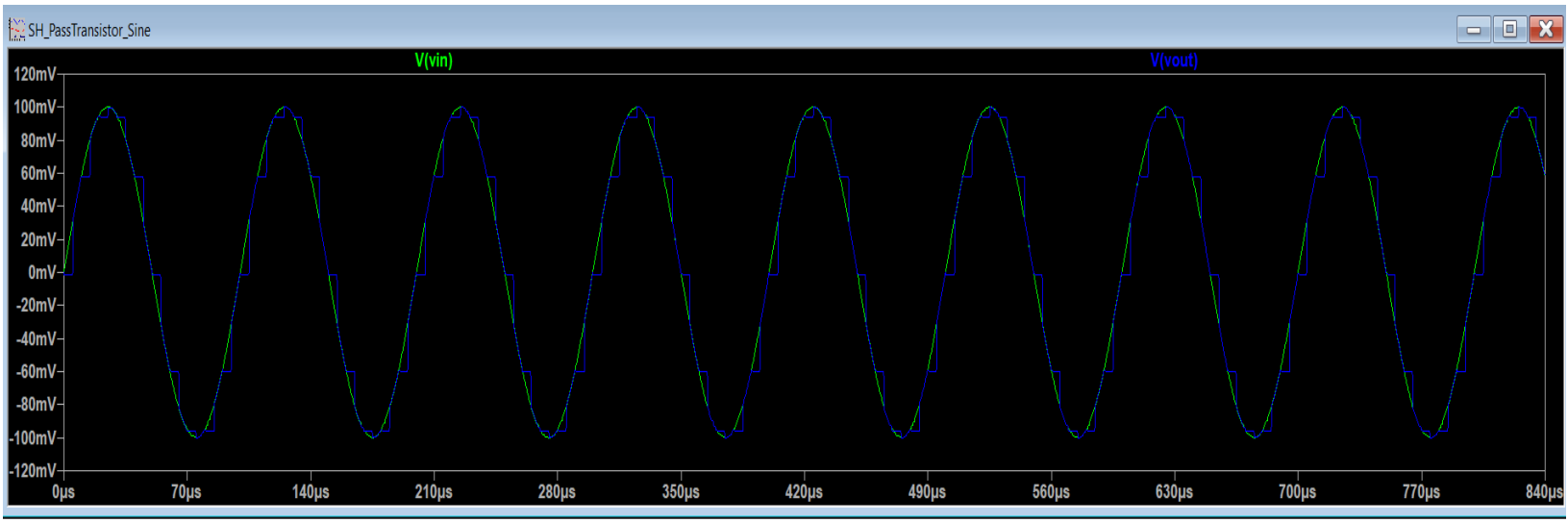
Pulse input : 0.9V & Vout : 1 % settling time = 19.48 ns(<25 ns)



Pulse input : 1.2V & Vout : 1 % settling time = 19.54 ns(<25 ns)

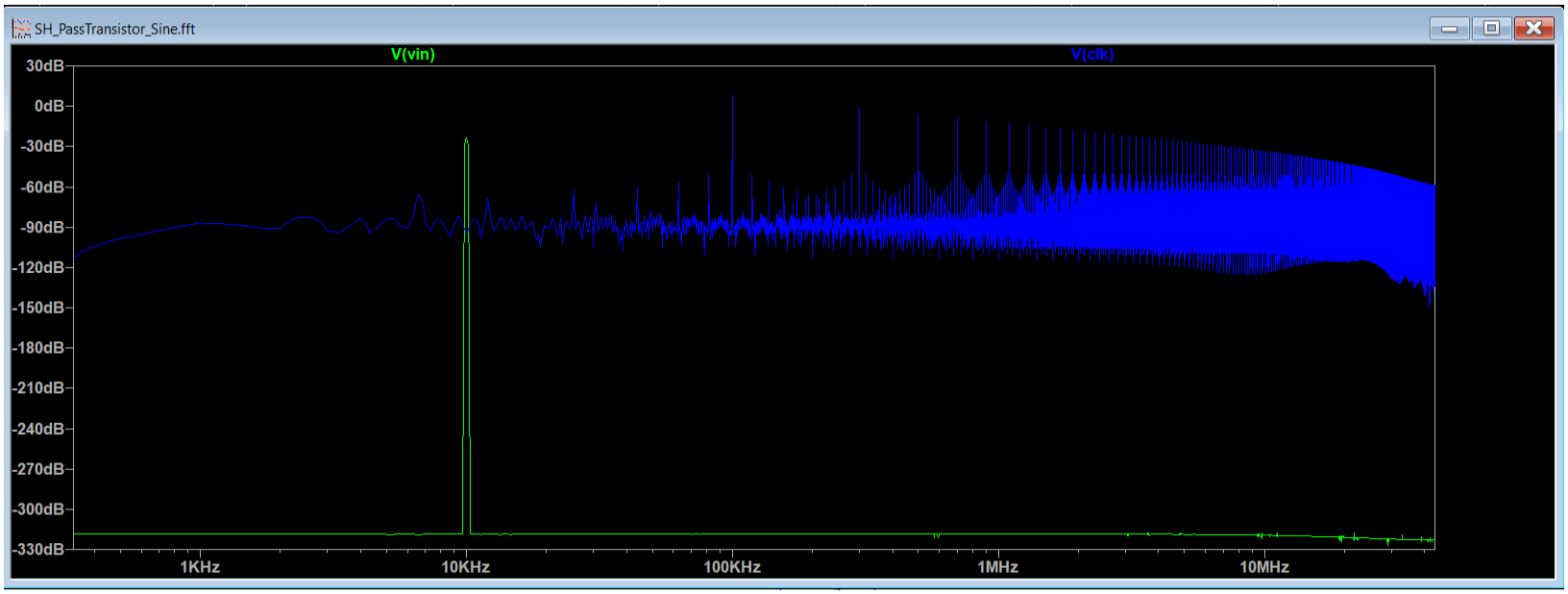


Clock pulse in NMOS

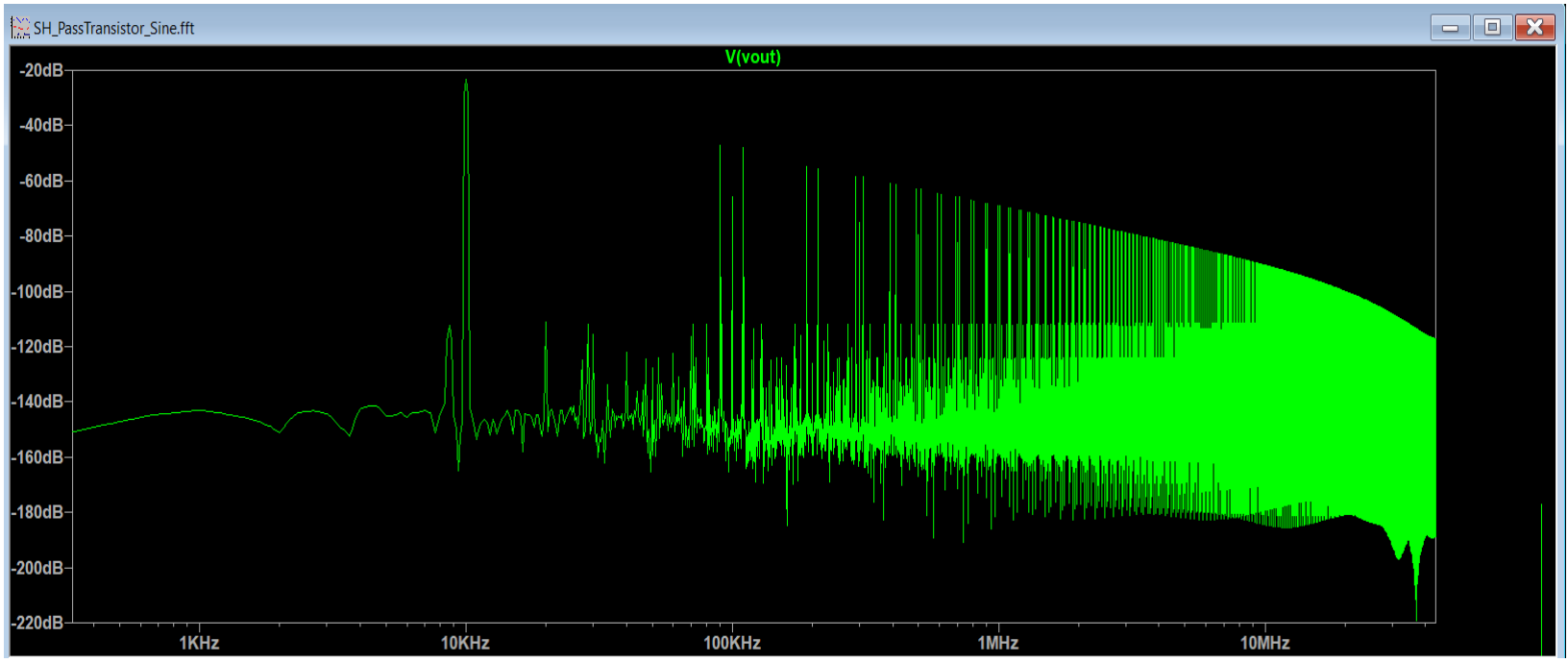


Sine input : 10 KHz and 100mV

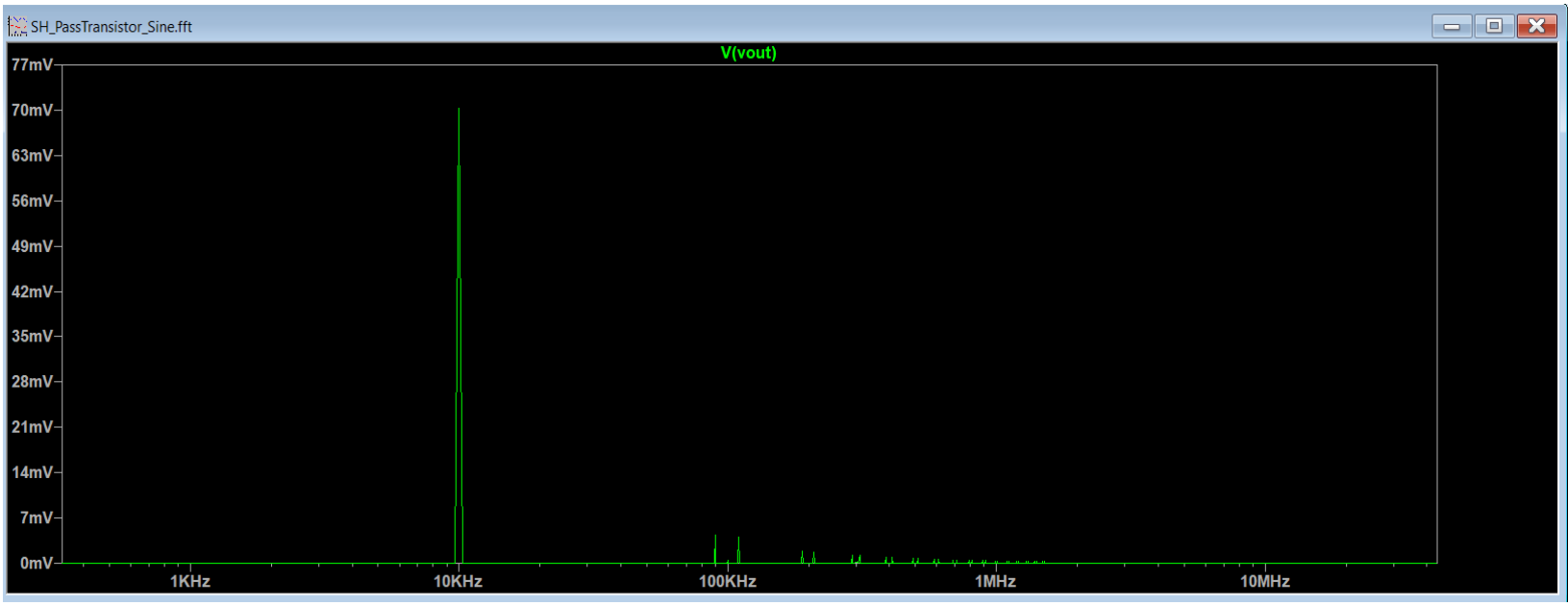
FFT of PassTransistor S/H



FFT of input Sine wave and clock pulse



FFT of S/H output in dB scale



FFT of S/H output in Linear scale

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component
1	1.000e+04	9.950e-02	1.000e+00
2	2.000e+04	3.978e-06	3.998e-05
3	3.000e+04	2.353e-06	2.365e-05
4	4.000e+04	1.084e-06	1.089e-05
5	5.000e+04	6.276e-07	6.308e-06
6	6.000e+04	1.041e-06	1.046e-05
7	7.000e+04	2.162e-06	2.173e-05
8	8.000e+04	3.638e-06	3.656e-05
9	9.000e+04	6.088e-03	6.118e-02
10	1.000e+05	7.457e-04	7.495e-03

Total Harmonic Distortion: 6.164167%(10.196445%)

We can see from directive : THD = 6.16 %

Results:

Table for both the cases

Input Voltage(in V)	1% Settling Time (NMOS)	1% Settling Time (PassTransistor)
0.3	20.3 ns	19.4 ns
0.6	20.41 ns	19.44 ns
0.9	20.92 ns	19.48 ns
1.2	21.17 ns	19.54 ns

Observations :

- Settling time increases in both NMOS and PassTransistor by increasing Voltage.
- Rate of increase of time is less in PassTransistor Logic.
- From FFT data, we can see that there is some distortion in the output signal.