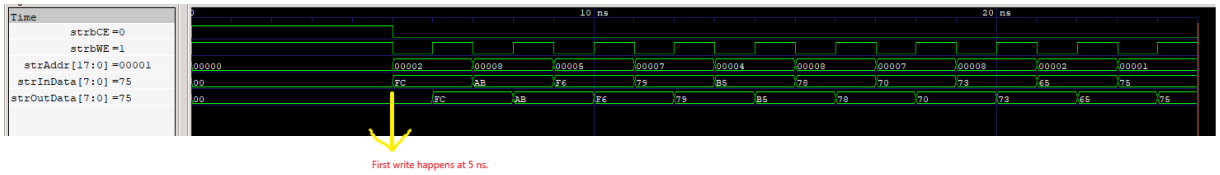
1. Screenshots of the waveform with analysis.

Write happens at time:
5,7,9,11,13,15,17,19,21,23 ns

Read happens at time:
6,8,10,12,14,16,18,20,22,24 ns



2. Screenshots of the simulation output in Terminal.

```
(systemc) bash-4.4$ ./sim.out

        SystemC 3.0.0-Accellera --- Aug 29 2024 18:54:01
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        ALL RIGHTS RESERVED

Info: (I702) default timescale unit used for tracing: 1 ps (VCD_RAM.vcd)
------------------- Beginning of Verification I
Write Address: 2, InData=252 | Read: OutData=252
Write Address: 8, InData=171 | Read: OutData=171
Write Address: 5, InData=246 | Read: OutData=246
Write Address: 7, InData=121 | Read: OutData=121
Write Address: 4, InData=181 | Read: OutData=181
------------------- End of Verification I

------------------- Beginning of Verification II
Write Address: 8, InData=120 | Read: OutData=120
Write Address: 7, InData=112 | Read: OutData=112
Write Address: 8, InData=115 | Read: OutData=115
Write Address: 2, InData=101 | Read: OutData=101
Write Address: 1, InData=117 | Read: OutData=117
------------------- End of Verification II
(systemc) bash-4.4$
```

3. Screenshots of your code in this design with reasonable comments.

Verification1 block:

```
// Verification I
cout << "------------------- Beginning of Verification I" << endl;
for(i=0; i<5; i++){
  // Set writing mode
  // ...
  tbCE = 0;
  tbWE = 0;

  // Generate values of tInData & tAddr using "cPkt"
  // ...
  cPkt.next();
  tAddr.write(static_cast<sc_uint<ADDR_WIDTH>>(*cPkt.sAddr));   //using static cast for type conversion.
  tInData.write(static_cast<sc_uint<DATA_WIDTH>>(*cPkt.sInData));

  //simulate for 1 NS
  sc_start(1, SC_NS);

  // Set reading mode
  // ...
  tbCE = 0;
  tbWE = 1;

  //simulate for 1 NS
  sc_start(1, SC_NS);

  // Data read from tOutData to sOutData
  // ...
  cPkt.sOutData->set(tOutData.read());  //setting sOutData = tOutData

  // Print statistics
  // ...
  cout << "Write Address: ";    //Write and read address is same.
  tAddr.print();
  cout << ", InData=";
  tInData.print();
  cout << " | Read: OutData=";
  tOutData.print();
  cout << endl;
}
cout << "------------------- End of Verification I" << endl << endl;
```

Verification2 block:

```
// Verification II
cout << "------------------- Beginning of Verification II" << endl;
for(i=0; i<5; i++){
  // Set writing mode
  // ...
  tbCE = 0;
  tbWE = 0;

  // Set range distribution
  // ...
  typedef pair <sc_uint<DATA_WIDTH> , sc_uint<DATA_WIDTH>> data_range;
  scv_bag <data_range> data_dist;
  data_dist.add(data_range(0x50 , 0x63) , 5);
  data_dist.add(data_range(0x64 , 0x78) , 95);

  // Generate values of tInData  using "cPkt"
  // ...
  cPkt.sInData->set_mode(data_dist);
  cPkt.next();
  tAddr.write(static_cast<sc_uint<ADDR_WIDTH>>(*cPkt.sAddr));
  tInData.write(static_cast<sc_uint<DATA_WIDTH>>(*cPkt.sInData));

  //simulate for 1 NS
  sc_start(1, SC_NS);

  // Set reading mode
  // ...
  tbCE = 0;
  tbWE = 1;

  //simulate for 1 NS
  sc_start(1, SC_NS);

  // Data read
  // ...
  cPkt.sOutData->set(tOutData.read());

  // Print statistics
  // ...
  cout << "Write Address: ";
  tAddr.print();
  cout << ", InData=";
  tInData.print();
  cout << " | Read: OutData=";
  tOutData.print();
  cout << endl;
}
cout << "------------------- End of Verification II" << endl;
```