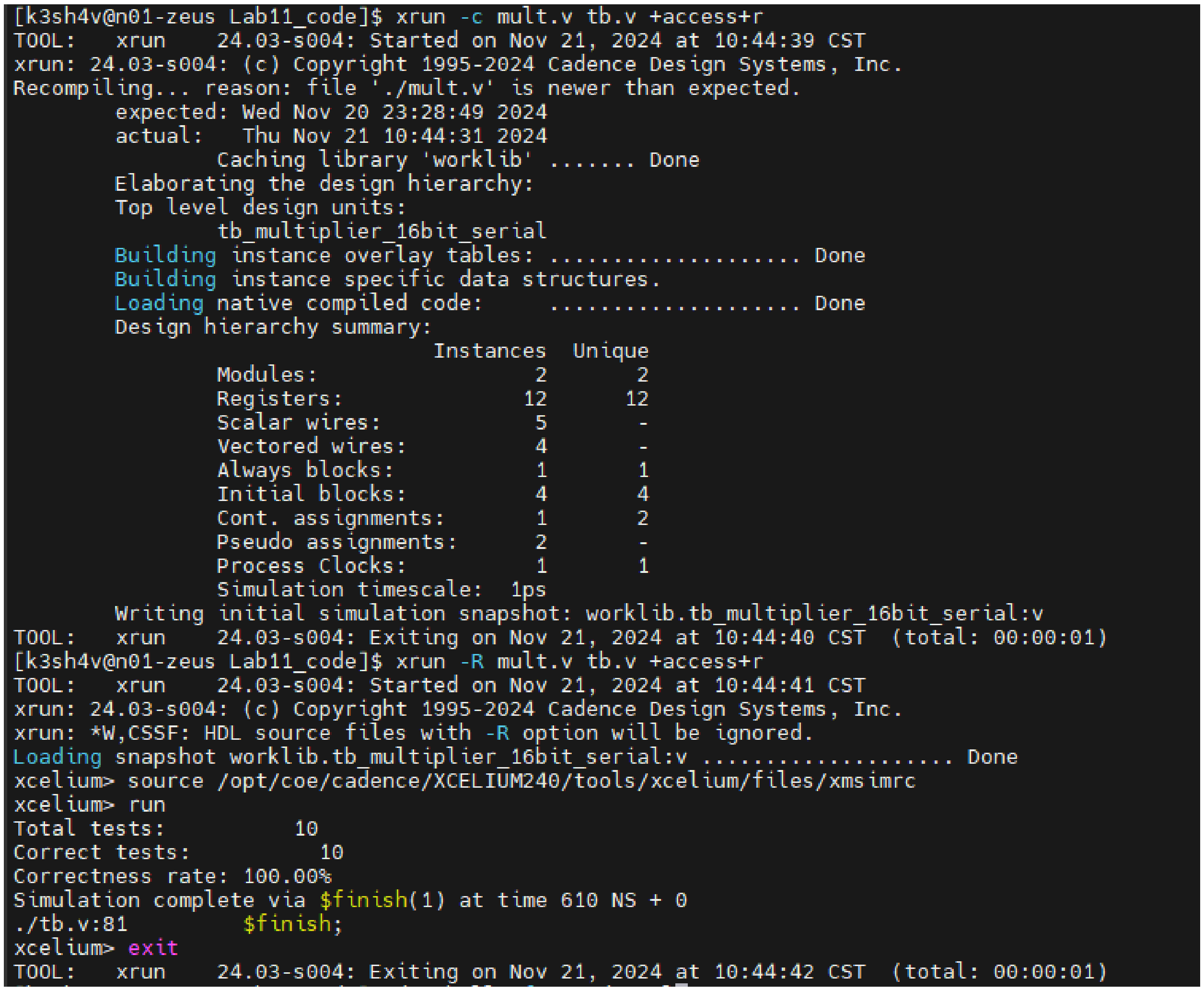
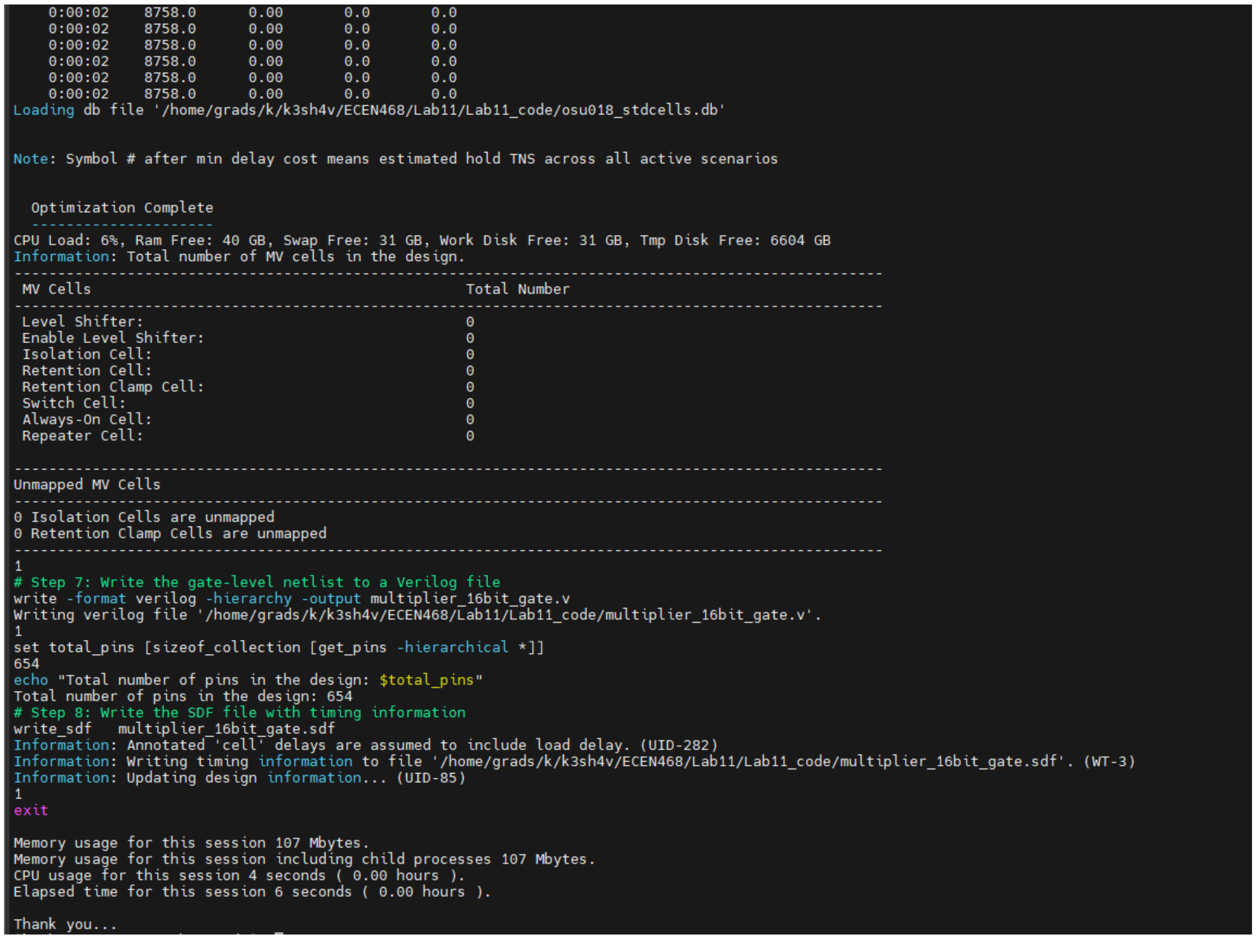
1. Screenshot of terminal output for both functional and gate-level simulation.



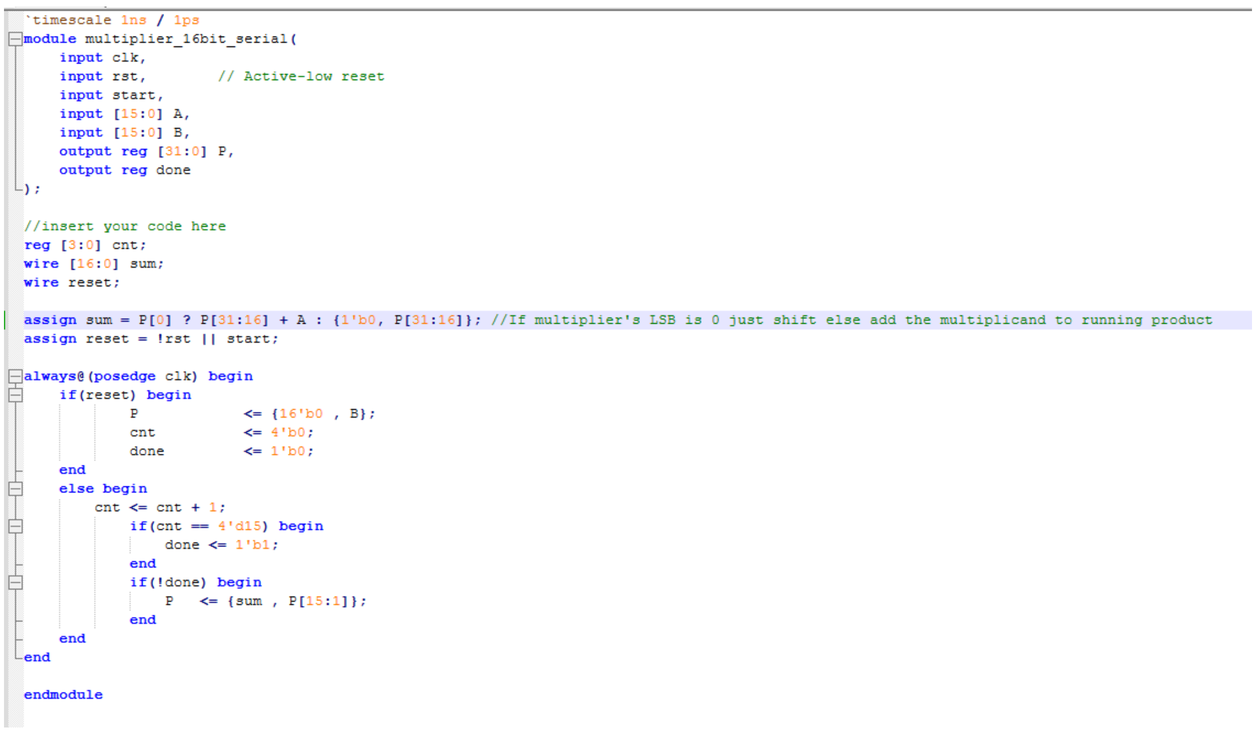
```
[k3sh4v@n01-zeus Lab11_code]$ xrun -c mult.v tb.v +access+r
TOOL:   xrun    24.03-s004: Started on Nov 21, 2024 at 10:44:39 CST
xrun: 24.03-s004: (c) Copyright 1995-2024 Cadence Design Systems, Inc.
Recompiling... reason: file './mult.v' is newer than expected.
        expected: Wed Nov 20 23:28:49 2024
        actual:   Thu Nov 21 10:44:31 2024
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Top level design units:
                tb_multiplier_16bit_serial
        Building instance overlay tables: .................... Done
        Building instance specific data structures.
        Loading native compiled code:     .................... Done
        Design hierarchy summary:
                                 Instances  Unique
                Modules:                 2       2
                Registers:              12      12
                Scalar wires:            5       -
                Vectored wires:          4       -
                Always blocks:           1       1
                Initial blocks:          4       4
                Cont. assignments:       1       2
                Pseudo assignments:      2       -
                Process Clocks:          1       1
                Simulation timescale:  1ps
        Writing initial simulation snapshot: worklib.tb_multiplier_16bit_serial:v
TOOL:   xrun    24.03-s004: Exiting on Nov 21, 2024 at 10:44:40 CST  (total: 00:00:01)
[k3sh4v@n01-zeus Lab11_code]$ xrun -R mult.v tb.v +access+r
TOOL:   xrun    24.03-s004: Started on Nov 21, 2024 at 10:44:41 CST
xrun: 24.03-s004: (c) Copyright 1995-2024 Cadence Design Systems, Inc.
xrun: *W,CSSF: HDL source files with -R option will be ignored.
Loading snapshot worklib.tb_multiplier_16bit_serial:v .................... Done
xcelium> source /opt/coe/cadence/XCELIUM240/tools/xcelium/files/xmsimrc
xcelium> run
Total tests:          10
Correct tests:          10
Correctness rate: 100.00%
Simulation complete via $finish(1) at time 610 NS + 0
./tb.v:81         $finish;
xcelium> exit
TOOL:   xrun    24.03-s004: Exiting on Nov 21, 2024 at 10:44:42 CST  (total: 00:00:01)
```



```
     0:00:02    8758.0      0.00       0.0       0.0
     0:00:02    8758.0      0.00       0.0       0.0
     0:00:02    8758.0      0.00       0.0       0.0
     0:00:02    8758.0      0.00       0.0       0.0
     0:00:02    8758.0      0.00       0.0       0.0
     0:00:02    8758.0      0.00       0.0       0.0
Loading db file '/home/grads/k/k3sh4v/ECEN468/Lab11/Lab11_code/osu018_stdcells.db'


Note: Symbol # after min delay cost means estimated hold TNS across all active scenarios


  Optimization Complete
  ---------------------
CPU Load: 6%, Ram Free: 40 GB, Swap Free: 31 GB, Work Disk Free: 31 GB, Tmp Disk Free: 6604 GB
Information: Total number of MV cells in the design.
----------------------------------------------------------------------------------------------------
 MV Cells                                                   Total Number
----------------------------------------------------------------------------------------------------
 Level Shifter:                                             0
 Enable Level Shifter:                                      0
 Isolation Cell:                                            0
 Retention Cell:                                            0
 Retention Clamp Cell:                                      0
 Switch Cell:                                               0
 Always-On Cell:                                            0
 Repeater Cell:                                             0

----------------------------------------------------------------------------------------------------
Unmapped MV Cells
----------------------------------------------------------------------------------------------------
0 Isolation Cells are unmapped
0 Retention Clamp Cells are unmapped
----------------------------------------------------------------------------------------------------
1
# Step 7: Write the gate-level netlist to a Verilog file
write -format verilog -hierarchy -output multiplier_16bit_gate.v
Writing verilog file '/home/grads/k/k3sh4v/ECEN468/Lab11/Lab11_code/multiplier_16bit_gate.v'.
1
set total_pins [sizeof_collection [get_pins -hierarchical *]]
654
echo "Total number of pins in the design: $total_pins"
Total number of pins in the design: 654
# Step 8: Write the SDF file with timing information
write_sdf   multiplier_16bit_gate.sdf
Information: Annotated 'cell' delays are assumed to include load delay. (UID-282)
Information: Writing timing information to file '/home/grads/k/k3sh4v/ECEN468/Lab11/Lab11_code/multiplier_16bit_gate.sdf'. (WT-3)
Information: Updating design information... (UID-85)
1
exit

Memory usage for this session 107 Mbytes.
Memory usage for this session including child processes 107 Mbytes.
CPU usage for this session 4 seconds ( 0.00 hours ).
Elapsed time for this session 6 seconds ( 0.00 hours ).

Thank you...
```

2. Justification of the correctness of the results.
My multiplier code calculates the product in 16 cycles. The code will assert done signal after 16 cycles indicating that the multiplier has finished its operation. Additionally, the code is also passing the test cases.

3. Screenshots of the code you implemented.



```verilog
`timescale 1ns / 1ps
module multiplier_16bit_serial(
    input clk,
    input rst,         // Active-low reset
    input start,
    input [15:0] A,
    input [15:0] B,
    output reg [31:0] P,
    output reg done
);

//insert your code here
reg [3:0] cnt;
wire [16:0] sum;
wire reset;

assign sum = P[0] ? P[31:16] + A : {1'b0, P[31:16]}; //If multiplier's LSB is 0 just shift else add the multiplicand to running product
assign reset = !rst || start;

always@(posedge clk) begin
    if(reset) begin
            P            <= {16'b0 , B};
            cnt          <= 4'b0;
            done         <= 1'b0;
    end
    else begin
        cnt <= cnt + 1;
            if(cnt == 4'd15) begin
                done <= 1'b1;
            end
            if(!done) begin
                P   <= {sum , P[15:1]};
            end
    end
end

endmodule
```