ECEN 449 - Microprocessor System Design
Test #2

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NAME:

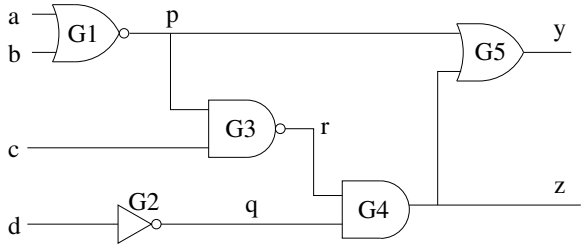
Problem	maximum points	your points
Problem 1	25	
Problem 2	25	
Problem 3	25	
Problem 4	25	
Total	100	

For all your answers which involve Verilog code or C code, you should provide comments in your code for full credit.

For other answers, you must provide comments about *how* you obtained the answer for full credit.

1. (a) Suppose you are implementing a digital design using an FPGA platform. You perform the steps of synthesis, mapping, placement and routing in that order. After each step, you print out the "timing report", which reports the delay of your design after each of the 4 steps as D_s, D_m, D_p and D_r respectively. What can you say about the relative accuracy of these 4 numbers?

   (b) Suppose we have a synthesized circuit as shown below. The worst-case gate delay of an INVerter is 2. The worst-case delay of a NAND2 / NOR2 gate is 4. The worst-case delay of an AND2 / OR2 gates is 5. The circuit has inputs $\{a,\ b,\ c,\ d\}$ and outputs $\{y,\ z\}$. We want to perform Static Timing Analysis (STA) to determine the worst-case delays of all the outputs of the circuit. Assume the signal arrival times of the inputs are $D_a = 1$, $D_b = 2$, $D_c = 3$ and $D_d = 14$.



   i. Write a *general* expression for the worst-case delays D_y, D_z, D_p, D_q, and D_r in terms of delays of any of the signals of the circuit.

   ii. Now *evaluate* these expressions to compute the actual worst-case delays of y, z, p, q and r.

   iii. Write down the *all* the sequences in which you could evaluate the expressions of part i), in order to correctly compute the worst-case delay of the circuit.

   iv. What is the worst-case delay of the circuit shown above?

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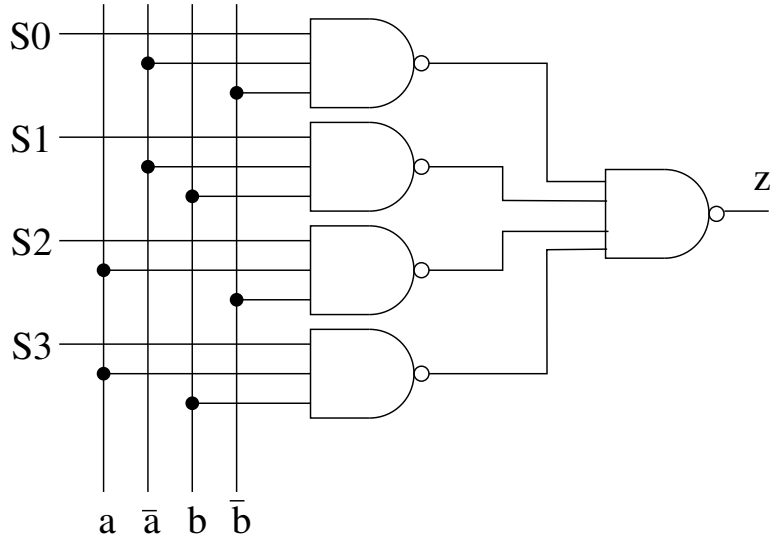
2. (a) Consider the circuit shown below. I claim that it is a 2-input LUT circuit.



i. Write down the logic expression for the output z of the above circuit

ii. Based on the above expression, prove that the circuit behaves as a 2-input LUT.

(b) Consider a signal which has a bandwidth of 50MHz. I would like to transmit it using pulse modulation, over a wire to the receiver. I need help figuring out which type of pulse modulation I should use. Each sample of the signal should have one of 256 discrete values. The fastest that the wire between the sender and the receiver can be switched is 1 GHz.

i. What is the maximum sampling period that I can use, so that the signal can be correctly reconstructed at the receiver?

ii. Now suppose I select PPM to transmit the signal. What is rate that the wire needs to be switched in order to transmit the signal described above?

iii. Now suppose I select PCM to transmit the signal. What is rate that the wire needs to be switched in order to transmit the signal described above?

iv. Now suppose I select PAM-256 to transmit the signal. What is rate that the wire needs to be switched in order to transmit the signal described above?

v. Based on the above, which is the most practical modulation scheme from among PPM, PCM and PAM-256? Given reasons for your choice.

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3. (a) Suppose I am a optic fiber cable operator. My optic fiber connection has a maximum bandwidth of 40 Gbps per wavelength, with a total of 100 wavelengths.

   Suppose I want to sell my bandwidth to a maximum number of customers, and each customer transmits video, 24 hours a day. The video they transmit uses 8 bits for each of the R, G and B pixels, and a screen resolution of 1920 $\times$ 1080 pixels. The screen refresh rate is 120 Hz.

   Suppose the video data was transmitted over the fiber in a compressed manner, so that the compressed video data is C times smaller than the uncompressed video data.

   i. How many customers can my optic fiber cable support assuming no compression?

   ii. Give one benefit of compression, and one downside.

   iii. What is your estimate for the value of C that can be achieved in practice?

   (b) Suppose that I am a internet service provider. It costs me \$1 billion to set up my infrastructure (wiring, cables, equipment etc). Also, it costs me \$1 million in operating costs per month (to maintain the infrastructure, pay employees etc). My total installed bandwidth is 1000 Gbps. At any time, I would like to ensure that no more than 80% of this capacity is utilized, so there is spare capacity in my system. My customers all purchase 10 Mbps connections from me, at a cost of M dollars per month. Demand is extremely high, and I have to turn away several interested customers when I start my company. At any given time, only 5% of the customers are utilizing their internet bandwidth. When a customer uses the internet, they utilize 100% of their purchased bandwidth.

   Suppose that I want to operate my business such that in 12 months, I am able to recover *all* my costs, and become profitable thereafter.

   i. How many customers can I sign up for my service?

   ii. What monthly rate M should I charge these customers?

   iii. What is my monthly profit from the 13th month onwards?

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4. Consider a wire on a printed circuit board (PCB). The wire has a characteristic impedance R_0 of 50 Ω. The wire is driven by a driver with an driving resistance $R_s = 10\ \Omega$ and it is terminated with a termination resistor of value $R = 50\ \Omega$. The driver supply voltage is 2.5V.

   To debug the PCB signals, I connect an oscilloscope probe to the receiver end of the wire. The oscilloscope probe has an impedance (to ground) of $R_{osc} = 200\ \Omega$.

   (a) Given that $R = R_0$, what do you expect the signal at the receiver to look like? Why will the signal at the receiver differ when I check it on the oscilloscope?

   (b) Calculate the value of the source and receiver reflection coefficients while I am debugging the signal at the receiver.

   (c) Plot the voltage at the receiver end of the wire up to $7 \cdot t_d$, where t_d is the time-of-flight through the wire.

   (d) Calculate the voltage at the receiver end of the wire in steady state (when all the reflections have subsided).

   (e) What value of R_{osc} should I use, in order to obtain a perfect reconstruction of the voltage waveform at the receiver end of the wire?

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