EE 449 - Microprocessor System Design
Test #1

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NAME:

Problem	maximum points	your points
Problem 1	20	
Problem 2	25	
Problem 3	30	
Problem 4	25	
Total	100	

For all your answers which involve Verilog code or C code, you should provide comments in your code for full credit.

For other answers, you must provide comments about *how* you obtained the answer for full credit.

1. (a) I write some synthesizable Verilog code, which contains 400 variables of type `reg`. I now synthesize this code. How many flip-flops does the resulting synthesized circuit contain?

   (b) Consider a 2-input XOR gate, where both inputs utilize 4-valued logic. Write down the truth table for this gate below.

   (c) Consider the Verilog code fragment below:

```
always @(posedge clk)
begin
a <= (z|b) & c
b <= (a & c)
end
```

   Assume it was synthesized using D flip-flops with both a `Q` and a `Qbar` output. The synthesis tool utilizes only INV, NAND2 and NOR2 gates. The cost of a gate is the number of inputs it has. Draw a circuit to show the minimum-cost synthesized result.

   (d) Draw the output waveform for signals `a` and `b`, when the code below is simulated. Assume that the `always` block is entered at time 0. Also assume that `a = 1`, `b = 0` and `c = 0` when the `always` block is entered

```
always @(posedge clk)
begin
a <= # 5 (b & c)
b <= # 4 (a | c)
end
```

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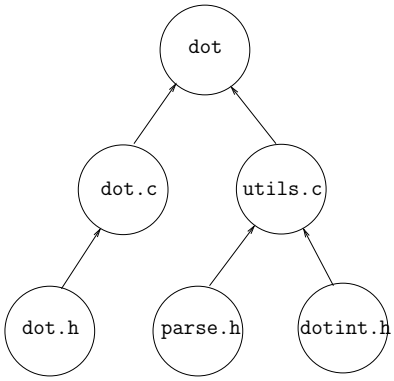
2. (a) Write a C program which accepts two separate strings `string1` and `string2`, and prints out the maximum length common substrings between these two strings. For example if the strings were `stubble` and `bubble`, then your program should output `ubble`.

   (b) I am creating a C project which consists of the files `dot.c`, `utils.c`, `parse.h`, `dot.h` and `dotint.h`. The final compiled binary should be called `dot`.

   The dependencies between these files is shown in the graph below. An arrow from node `x` to node `y` means that the compilation of file `y` depends on file `x`.



   Write the `makefile` for the above project. Typing `make` should result in the generation of the final binary for the project.

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3. Consider a 3-bit Huffman code. In this code, the coding table is as follows:

Symbol	code
P	`0`
O	`10`
S	`110`
T	`111`

Here is how it is used. If the transmitter wants to send a string of symbols (such as TOP for example), they would look up the code for each symbol, and transmit the codes of these symbols, one after the other. In our example the code for T is `111`, the code for O is `10` and the code for P is `0`. Hence the transmitter would transmit `111100`, which can be uniquely decoded by the receiver.

(a) What property do the codes above have, that guarantee that the receiver can unambiguously decode a transmitted message?

(b) Based on the coding table above, draw the STG for the decoding operation done by the receiver

(c) Based on the STG of the previous section, write the Verilog code for the Huffman decoder.

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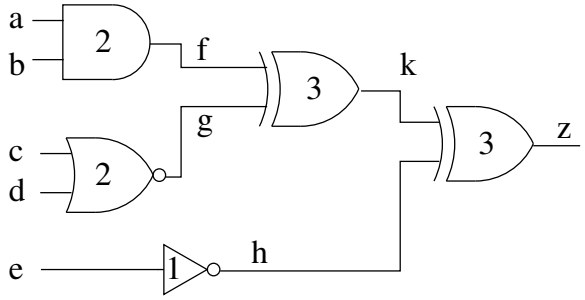
4. (a) Consider the circuit below. For each gate, the corresponding delay is written inside it.



We want to perform event-driven timing simulation of the above circuit, assuming that inputs `b`, `c` and `e` change from 0 to 1 at time 0, and inputs `a` and `d` are statically 0. Write down the event stack generated when the circuit undergoes event driven timing simulation. For each event, you must list, in tabular form,

i. the time of the event,

ii. the circuit node affected by the event

iii. the value of the circuit node in question after the event is processed.

If any event generates additional events, indicate this with arrows.

(b) For the same circuit, perform static timing analysis (STA) to determine its maximum delay.

i. Write the maximum delay of each gate beside it.

ii. In order to perform STA correctly, is there a restriction on the order in which you should visit the gates of the design? Explain your answer.

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