One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

ADF7024 Reference Manual

SCOPE

This user guide provides a detailed description of the ADF7024 functionality and features.

GENERAL INFORMATION

Complete specifications for the ADF7024 device can be found in the ADF7024 data sheet, which is available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the ADF7024.

Additional information about the ADF7024 can be found in the ADF7024 design package, which can be downloaded from the ADF7024 product page.

FUNCTIONAL BLOCK DIAGRAM

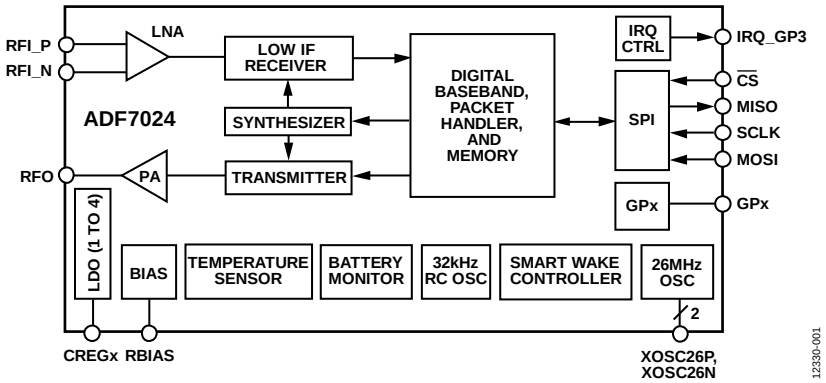


Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

7/14—Revision 0: Initial Version

ABOUT THE ADF7024 REFERENCE MANUAL

NUMBER NOTATIONS

Table 1. Number Notations

Notation	Description
Bit N	Bits are numbered in little endian format, that is, the least significant bit of a number is referred to as Bit 0.
V[X:Y]	Bit field representation covering Bit X to Bit Y of a value or a field (V).
0xNN	Hexadecimal (Base 16) numbers are preceded by the 0x prefix.
0bNN	Binary (Base 2) numbers are preceded by the 0b prefix.
NN	Decimal (Base 10) are represented using no additional prefixes or suffixes.

REGISTER ACCESS CONVENTIONS

Table 2. Register Access Conventions

Mode	Description
R/W	Memory location has read and write access.
R	Memory location is read access only.
W	Memory location is write access only.

Note that register bit combinations that are not documented are reserved and must not be used.

ACRONYMS AND ABBREVIATIONS

Table 3.

Acronym/Abbreviation	Description
ADC	Analog-to-digital converter
AFC	Automatic frequency control
AGC	Automatic gain control
AIN	Analog input pin
BT	Bandwidth time product
CCA	Clear channel assessment
CRC	Cyclic redundancy check
DR	Data rate
2FSK	Two level frequency shift keying
FHSS	Frequency hopping spread spectrum
GFSK	Two level Gaussian frequency shift keying
GMSK	Gaussian minimum shift keying
GPIO	General-purpose input and output
IF	Intermediate frequency
ISM	Industrial, scientific, and medical
LBT	Listen before talk
LO	Local oscillator
LSB	Least significant byte or bit
LNA	Low noise amplifier
MSB	Most significant byte or bit
NOP	No operation
PA	Power amplifier
PFD	Phase frequency detector
PLL	Phase-locked loop
RSSI	Receive signal strength indicator
RF	Radio frequency
Rx	Receive
SAR	Successive approximation register
SPI	Serial peripheral interface
SWD	Sync word detect
SWM	Smart wake mode
Tx	Transmit
VCO	Voltage controlled oscillator
WUC	Wake-up controller
XOSC	Crystal oscillator

Table 4. Related Links and Documents

Resource	Description
ADF7024	ADF7024 product page
ADF7024 Data Sheet	Available from the ADF7024 product page
ADF7024 Design Package	Available from the ADF7024 product page

INTRODUCTION TO THE ADF7024

The ADF7024 is an ultralow power, integrated transceiver for use in the license free ISM bands at 433 MHz, 868 MHz, and 915 MHz. The ease of use and high performance of the ADF7024 make it suitable for a wide variety of wireless applications. The ADF7024 is suitable for operation under the European ETSI EN300-220 regulation, the North American FCC Part 15 regulation, and other similar regulatory standards.

To eliminate many of the RF related design challenges users typically face, Analog Devices has provided a set of radio profiles for the ADF7024. Each radio profile provides a set of optimized register settings for the ADF7024 radio. The radio profile ensures that the RF communication layer works seamlessly, thereby allowing the user to concentrate on the protocol and system level design.

There are six profiles in total for the ADF7024, as shown in Table 5. The register settings for each profile are detailed in Table 11.

Table 5. Radio Profiles

Radio Profile	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	IF Bandwidth (kHz)	Typical Channel Spacing (kHz)	RF Frequency Range (MHz)
A	9.6	FSK/GFSK	9.6	100	200	862 to 928
B	38.4	FSK/GFSK	20	100	200	431 to 435, 862 to 928
C	50	FSK/GFSK	25	100	200	862 to 928
D	100	FSK/GFSK	25	100	200	862 to 928
E	200	FSK/GFSK	50	200	400	862 to 928
F	300	FSK/GFSK	75	300	600	862 to 928

The low IF architecture-based receiver minimizes power consumption and provides excellent sensitivity. The receiver is exceptionally linear and, therefore, is very resilient to the presence of interferers in spectrally noisy environments. The highly efficient transmitter has a programmable output power of up to +13.5 dBm and automatic PA ramping to meet transient spurious specifications. The RF frequency synthesizer comprises a voltage controlled oscillator (VCO), a low noise, fractional-N PLL, and a loop filter, all of which are fully integrated and automatically calibrated. This agile frequency synthesizer facilitates the implementation of FHSS systems.

The ADF7024 simplifies the processing burden of the host processor by integrating the lower layers of a typical communication protocol stack. The host processor configures the ADF7024 over a standard 4-wire SPI interface, using a simple command-based protocol. A single-byte command transitions the radio between states or performs a radio function. A complete wireless solution is built using a small number of external discrete components and a host processor, which is typically a microcontroller.

The smart wake mode (SWM) allows the ADF7024 to wake up autonomously from sleep using the internal wake-up timer without intervention from the host processor. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep, thereby reducing the overall system current consumption.

KEY FEATURES

Ease of Use

- Radio profiles that simplify radio configuration
- Simple command-based SPI protocol for controlling the ADF7024 radio and accessing of memory
- Integrated packet handling, simplifying the host processor firmware design
- Few external components required

RF Performance

- Excellent receiver sensitivity: −111 dBm at 9.6 kbps
- Highly linear receiver: −11.5 dBm input IP3
- Blocking: 76 dB at ±10 MHz offset
- Low power receiver: 12.8 mA in Rx mode
- High efficiency power amplifier (PA): 23.3 mA in Tx mode at 10 dBm
- Output power range: −20 dBm to +13.5 dBm

Packet Handling Features

- 240-byte packet buffer for transmit and receive
- Automatic insertion and detection of preamble, sync word, and CRC
- Optional Manchester and 8-bit/10-bit data encoding and decoding
- Optional data whitening

Low Power Mode Features

- Ultralow power sleep modes for long battery life: 0.33 μA in Deep Sleep Mode 1
- Fast radio state transitions
- Real-time clock capability using integrated RC oscillator and firmware timer
- Autonomous carrier sense for clear channel assessment (CCA) and listen before talk (LBT) applications
- Autonomous packet sniffing and packet reception using smart wake modes

Other Features

- Integrated battery alarm and temperature sensor
- Fully automatic frequency control (AFC) and automatic gain control (AGC)
- Integrated image rejection calibration (patent pending)
- On-chip, 8-bit analog-to-digital converter (ADC)

GETTING STARTED WITH THE ADF7024

DESIGN PACKAGE

The ADF7024 design package contains the necessary resources to perform system design and prototyping with the ADF7024. As the first step in the design process, it is recommended to download and review the design package. The design package is available from the ADF7024 product page.

The design package contains evaluation board schematics, layout files, and bills of materials (BOMs), along with a quick start evaluation guide.

EVALUATION AND DEVELOPMENT PLATFORM

The ADF7024 evaluation and development platform consists of the following:

- RF daughter boards covering different frequency bands and matching topologies (see Table 6). The RF daughter board kit includes a quarter wavelength whip antenna for over the air testing.
- The EVAL-ADF7XXXMB4Z motherboard for evaluation of and development with the ADF7024. The ADF7024 daughter boards plug into the EVAL-ADF7XXXMB4Z motherboard. The EVAL-ADF7XXXMB4Z mother board uses a Renesas RL78 as the host processor to the ADF7024.
- A graphical user interface (GUI) for use with the EVAL-ADF7XXXMB4Z mother board. The GUI can be used for configuring the ADF7024, evaluating the transmit and receive operation, and transmitting and receiving packets.
- Reference C code and IAR Embedded Workbench® projects for the Renesas RL78 low power microcontroller on the EVAL-ADF7XXXMB4Z mother board, with examples on how to configure and to communicate with the ADF7024. This reference C code is available as part of the EVAL-ADF7XXXMB4Z installation.

There are four daughter board models as described in Table 6. Two board layouts are used; one which uses a separate transmit and receive match, and one which uses a combined transmit and receive match. For more information on the difference between these matching topologies, refer to the RF Matching section.

Table 6. ADF7024 Radio Daughter Board Models

Daughter Board Model	Layout Type	RF Frequency Range (MHz)
EVAL-ADF7024DB1Z	Separate Tx/Rx match	862 to 928
EVAL-ADF7024DB2Z	Combined Tx/Rx match	862 to 928
EVAL-ADF7024DB3Z	Separate Tx/Rx match	431 to 435
EVAL-ADF7024DB4Z	Combined Tx/Rx match	431 to 435

ADF7024 MEMORY MAP

The ADF7024 memory map is illustrated in Figure 2.

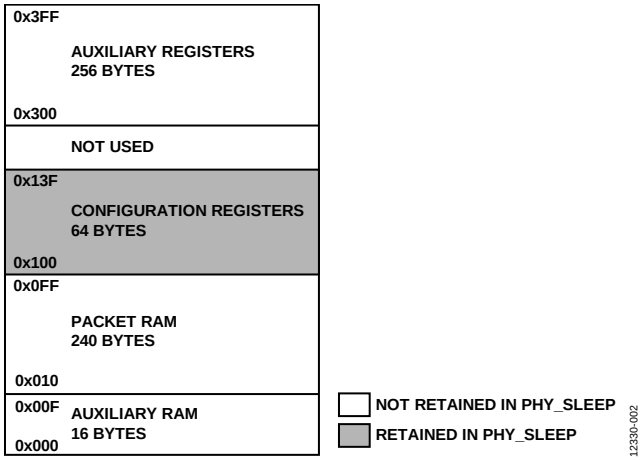


Figure 2. ADF7024 Memory Map

CONFIGURATION REGISTERS

The configuration registers is a 64-byte memory space that contains the registers used to configure the ADF7024. The memory space is made up of registers that configure the radio, packet management, interrupts, and smart wake mode operation. When power is applied (cold start), this memory space is in an unknown state and, therefore, it is necessary for the host processor to write to all of the configuration registers before transitioning from the PHY_OFF state. The registers that form the radio profile are contained within the configuration register memory space. In most applications, the host only writes once to the configuration registers to configure the ADF7024, as the memory is retained in PHY_SLEEP.

AUXILIARY REGISTERS

The auxiliary registers is a 256-byte memory space that contains the registers used for the auxiliary radio functions or for the observation of the radio blocks of the ADF7024. The content of this memory space is not retained in the PHY_SLEEP state. In most applications, it is not necessary to write to this memory space to configure the ADF7024.

AUXILIARY RAM

The auxiliary random access memory (RAM) consists of 16 bytes of memory space that are allocated for use internally by the ADF7024, with the exception of Register VAR_TX_MODE (Address 0x00D), which can be written to by the host processor to configure transmit test modes.

PROGRAM RAM

The program RAM (not shown in Figure 2) consists of 2 kB of volatile memory. This memory space is used for firmware modules, such as the image rejection calibration module, which is available from Analog Devices. The host processor downloads a firmware module to the program RAM memory space over the SPI. See the Downloadable Firmware Modules section for details on loading a firmware module to program RAM.

PACKET RAM

The packet RAM consists of 240 bytes of memory space. This memory space is allocated for the storage of data from valid received packets and packet data to be transmitted. The ADF7024 stores received payload data at the memory location indicated by the value of the PKT_RX_BASE_ADR register (Address 0x125), the receive address pointer. The value of the PKT_TX_BASE_ADR register (Address 0x124), the transmit address pointer, determines the start address of data to be transmitted by the ADF7024. The packet RAM memory can be arbitrarily assigned to store single or multiple transmit or receive packets, with and without overlap, as shown in Figure 3. Choose a PKT_RX_BASE_ADR value that ensures that there is enough allocated packet RAM space for the maximum receive payload length.

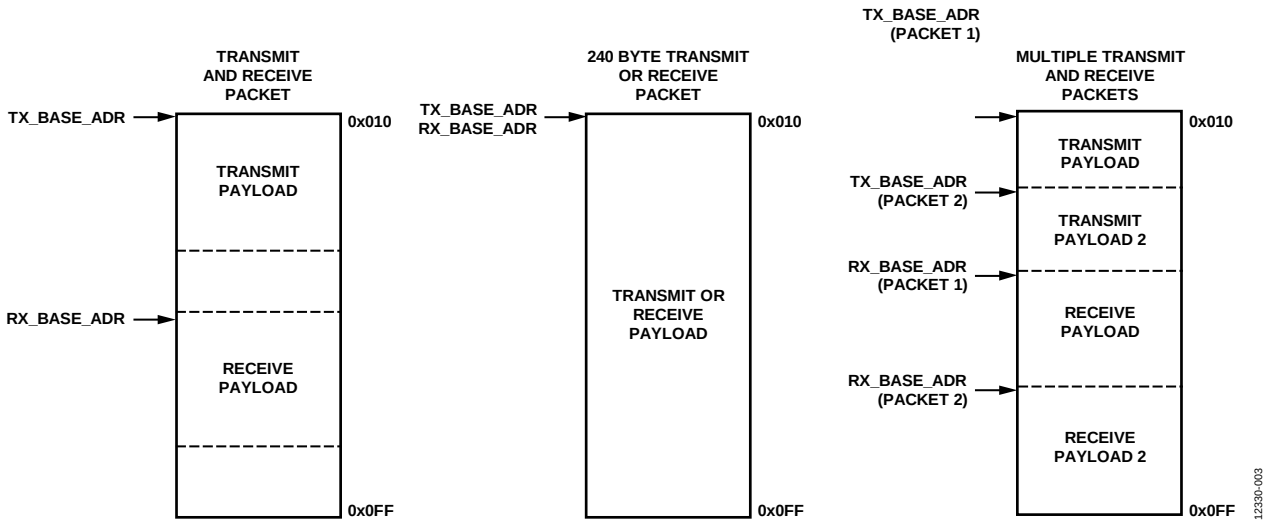


Figure 3. Example Packet RAM Configurations Using the Tx Packet and Rx Packet Address Pointers

HOST PROCESSOR INTERFACE

GENERAL CHARACTERISTICS

The ADF7024 is equipped with a 4-wire SPI interface, using the SCLK, MISO, MOSI, and $\overline{CS}$ pins. The ADF7024 always acts as a slave to the host processor. Figure 4 shows an example connection diagram between the processor and the ADF7024. The diagram in Figure 4 also shows the direction of the signal flow for each pin. The SPI interface is active, and the MISO outputs are enabled, only while the $\overline{CS}$ input is low. The SPI interface uses a word length of eight bits, which is compatible with the SPI hardware of most processors. The data transfer through the SPI interface occurs with the most significant bit first. The MOSI input is sampled at the rising edge of SCLK. As commands or data are shifted in from the MOSI input at the SCLK rising edge, the status word or data is shifted out at the MISO pin synchronous with the SCLK clock falling edge. If $\overline{CS}$ is brought low, the most significant bit of the status word appears on the MISO output, without the need for a rising clock edge on the SCLK input. Refer to the ADF7024 data sheet for SPI timing information. The ADF7024 SPI interface allows control of the ADF7024 via the radio control commands (CMD prefix in the command name) and allows access to the ADF7024 memory spaces via the memory access commands (SPI prefix in the command name).

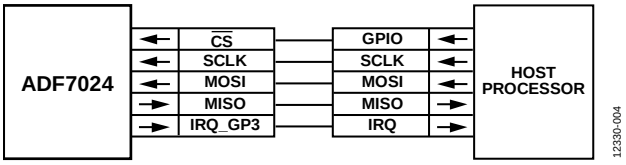


Figure 4. Host Processor Interface Connections

COMMANDS

The ADF7024 is controlled through commands. Command words are single octet instructions that control the state transitions of the radio and provide access to the ADF7024 memory. Commands that have a CMD prefix in the command name control the operation of the ADF7024 radio. Memory access commands have an SPI prefix in the command name and are handled independently of the radio. Therefore, SPI commands can be issued independent of the state of the ADF7024.

A command is initiated by bringing $\overline{CS}$ low and shifting in the command word over the SPI, as shown in Figure 5. All commands are executed on the last positive SCLK edge of the command. The $\overline{CS}$ input must be brought high again after a command has been shifted into the ADF7024 to enable the recognition of successive command words. A single command can be issued only during a $\overline{CS}$ low period (with the exception of a double NOP command).

The complete list of valid commands is provided in the Command Reference section.

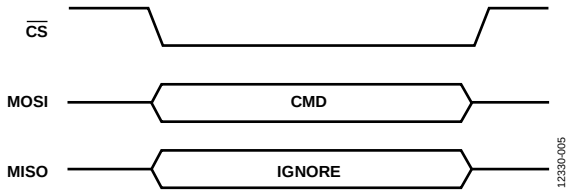


Figure 5. Command Write (No Parameters)

STATUS WORD

The status word of the ADF7024 is automatically returned over the MISO each time a byte is transferred over the MOSI. Shifting in double SPI_NOP commands (see Table 9) causes the status word to be shifted out, as shown in Figure 6. The meaning of the various bit fields in the status word is described in Table 7. The FW_STATE variable is used to read the current state of the ADF7024, as described in Table 8. If the ADF7024 is busy performing an action or state transition, FW_STATE is busy.

The SPI_READY variable is used to indicate when the SPI is ready for access. The CMD_READY variable is used to indicate when the ADF7024 is ready to accept a new command. Poll the status word and examine the CMD_READY bit before issuing a command to ensure that the ADF7024 is ready to accept a new command. It is not necessary to check the CMD_READY bit before issuing a SPI memory access command.

The ADF7024 interrupt handler can be also be configured to generate a hardware interrupt signal on IRQ_GP3 when the ADF7024 is ready to accept a new command (CMD_ READY in the INTERRUPT_SOURCE_1 register [Address 0x337]) or when it has finished processing a command (CMD_FINISHED in the INTERRUPT_SOURCE_1 register [Address 0x337]).

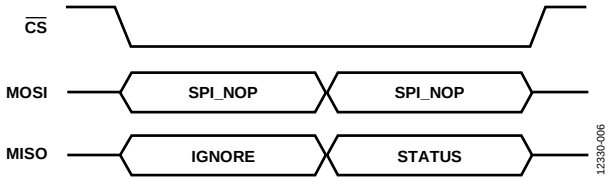


Figure 6. Reading the Status Word Using a Double SPI_NOP Command

Table 7. Status Word

Bit	Name	Description
[7]	SPI_READY	0: SPI is not ready for access. 1: SPI is ready for access.
[6]	IRQ_STATUS	0: no pending interrupt condition. 1: pending interrupt condition (mirrors the IRQ_GP3 pin).
[5]	CMD_READY	0: the ADF7024 is not ready to receive a radio control command. 1: the ADF7024 is ready to receive a radio control command. It is not necessary to check this bit before issuing a SPI memory access command.
[4:0]	FW_STATE	Indicates the ADF7024 state (see Table 8).

Table 8. FW_STATE Description

Value	State
0x0F	Initializing
0x00	Busy, performing a state transition
0x11	PHY_OFF
0x12	PHY_ON
0x13	PHY_RX
0x14	PHY_TX
0x06	PHY_SLEEP
0x05	Performing CMD_GET_RSSI
0x07	Performing CMD_IR_CAL

MEMORY ACCESS

Memory locations are accessed by invoking the relevant SPI command. An 11-bit address is used to identify registers or locations in the memory space. The most significant three bits of the address are incorporated into the SPI command by appending them as the LSBs of the SPI command word. Figure 7 illustrates command, address, and data partitioning. The SPI memory access commands differ depending on the memory location being accessed (see Table 9).

Issue an SPI command only if the SPI_READY bit of the status word is high.

Do not issue an SPI command while the ADF7024 is initializing (FW_STATE = 0x0F). SPI commands can be issued in any other state, including the busy state (FW_STATE = 0x00), which allows the ADF7024 memory to be accessed while the radio is transitioning between states.

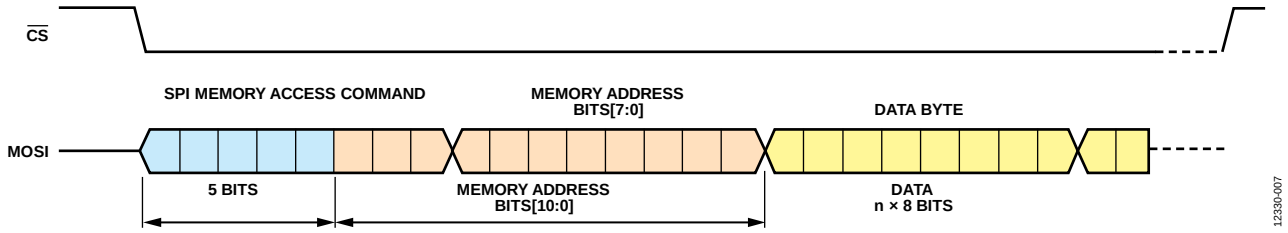


Figure 7. SPI Memory Access Command and Address Format

Table 9. Summary of SPI Memory Access Commands

SPI Command	General Command Format	Command Values	Description
SPI_MEM_WR	0b00011xxx	0x18 (packet RAM), 0x19 (configuration registers), 0x1B (auxiliary registers), and 0x1E (program RAM)	Write data to the ADF7024 sequentially. An 11-bit address is used to identify memory locations. The most significant three bits of the address are incorporated into the command (xxxb). This command is followed by the remaining eight bits of the address.
SPI_MEM_RD	0b00111xxx	0x38 (packet RAM), 0x39 (configuration registers), and 0x3B (auxiliary registers)	Read data from the ADF7024 sequentially. An 11-bit address is used to identify memory locations. The most significant three bits of the address are incorporated into the command (xxxb). This command is followed by the remaining eight bits of the address, which is subsequently followed by the appropriate number of SPI_NOP commands.
SPI_MEMR_WR	0b00001xxx	0x08 (packet RAM), 0x09 (configuration registers), and 0x0B (auxiliary registers)	Write data to the ADF7024 nonsequentially.
SPI_MEMR_RD	0b00101xxx	0x28 (packet RAM), 0x29 (configuration registers), and 0x2B (auxiliary registers)	Read data from the ADF7024 nonsequentially.
SPI_NOP	N/A[1]	0xFF	No operation. Use for dummy writes when polling the status word. Also used as dummy data on the MOSI line when performing a memory read.

[1] Not applicable.

Block Write

All memory locations can be written to in block format using the SPI_MEM_WR command. The SPI_MEM_WR command code is 0b00011xxx, where xxx represent Bits[10:8] of the first 11-bit address. If more than one data byte is written, the write address is automatically incremented for every byte sent until $\overline{CS}$ is set high, which terminates the memory access command (see Figure 8 for more details). The maximum block write for packet RAM is 256 bytes, while the maximum block write for the configuration registers is 64 bytes. These maximum block write lengths must not be exceeded.

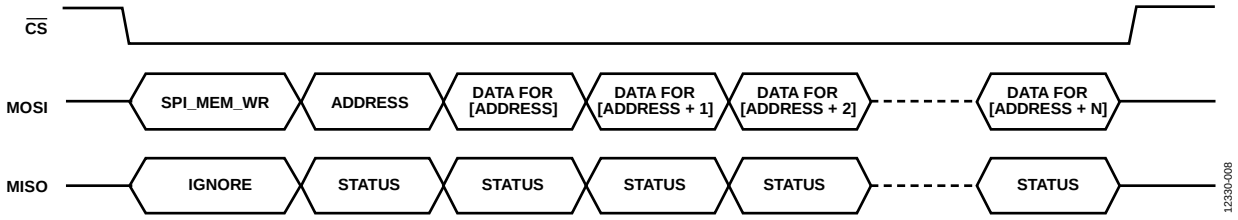


Figure 8. Memory Block Write

Random Address Write

The configuration registers, auxiliary registers, and packet RAM can be written to in a nonsequential manner using the SPI_MEMR_WR command. The SPI_MEMR_WR command code is 0b00001xxx, where xxx represent Bits[10:8] of the 11-bit address. The SPI_MEMR_WR command is followed by the lower eight bits of the address, and then by the data byte to be written to the address. The lower eight bits of the next address are entered, followed by the data byte for that particular address until all required addresses within that block are written, as shown in Figure 9.

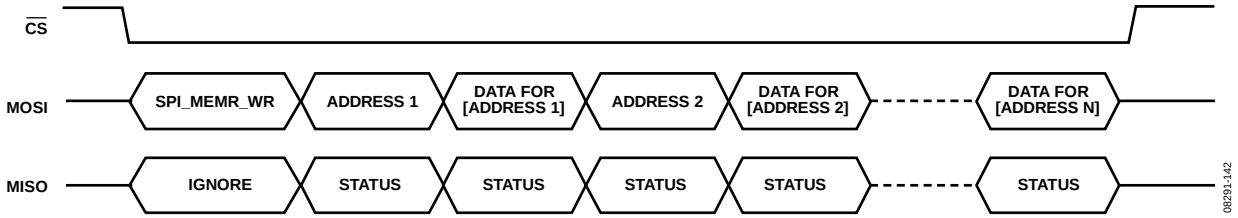


Figure 9. Memory Random Address Write

Block Read

The configuration registers, auxiliary registers, and packet RAM can be read from in block format using the SPI_MEM_RD command. The SPI_MEM_RD command code is 00111xxxb, where xxxb represent Bits[10:8] of the first 11-bit address. The SPI_MEM_RD command is followed by the remaining eight bits of the address to be read, and then by two SPI_NOP commands (dummy bytes). The first byte available after writing the address must be ignored; valid data is available after the second byte. If more than one data byte is to be read, the write address is automatically incremented for the subsequent SPI_NOP commands sent. See Figure 10 for more details.

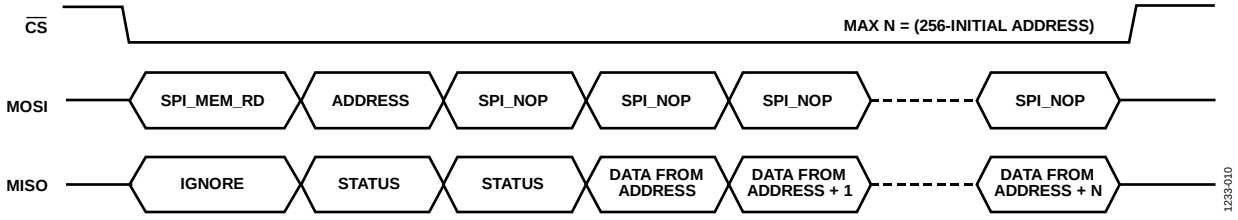


Figure 10. Memory Block Read

Random Address Read

The configuration registers, auxiliary registers, and packet RAM can be read from memory in a nonsequential manner using the SPI_MEMR_RD command. The SPI_MEMR_RD command code is 00101xxxb, where xxxb represent Bits[10:8] of the 11-bit address. The SPI_MEMR_RD command is followed by the remaining eight bits of the address to be written. Each subsequent address byte is then written. The last address byte to be written must be followed by two SPI_NOP commands, as shown in Figure 11. The data bytes from memory, starting at the first address location, are available after the second status byte.

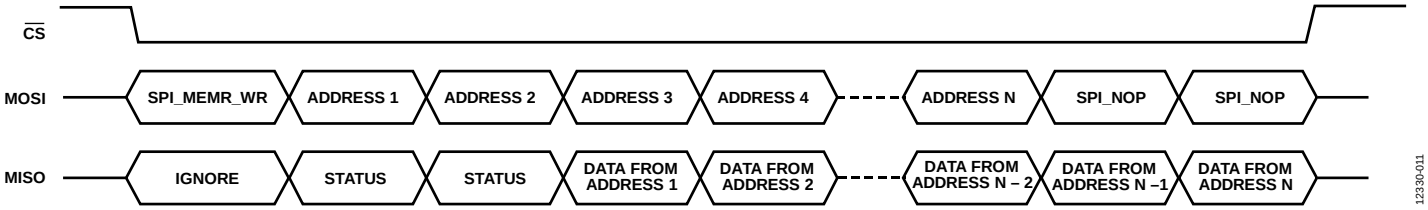


Figure 11. Memory Random Address Read

THE RADIO PROFILE

To eliminate many of the RF related design challenges users typically face, Analog Devices has provided a set of radio profiles for the ADF7024. Each radio profile provides a set of optimized register settings for the ADF7024 radio. There are six profiles in total for the ADF7024, as shown in Table 10.

The radio profile registers form part of the configuration register memory space and use the prefix RADIO_PROFILE_x for their register name. The configuration registers that are not part of the radio profile are open to configuration by the user and are described in the Configuration Registers Description section. The settings for each of the radio profile registers, for Profile A to Profile F, are detailed in Table 11.

Table 10. Radio Profiles

Radio Profile	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	IF Bandwidth (kHz)	Typical Channel Spacing (kHz)	RF Frequency Range (MHz)
A	9.6	FSK/GFSK	9.6	100	200	862 to 928
B	38.4	FSK/GFSK	20	100	200	431 to 435, 862 to 928
C	50	FSK/GFSK	25	100	200	862 to 928
D	100	FSK/GFSK	25	100	200	862 to 928
E	200	FSK/GFSK	50	200	400	862 to 928
F	300	FSK/GFSK	75	300	600	862 to 928

Table 11. Radio Profile Register Settings

Address (Hex)	Register Name	Radio Profile					
		A	B	C	D	E	F
0x10C	RADIO_PROFILE_0	0x60	0x80	0xF4	0xE8	0xD0	0xB8
0x10D	RADIO_PROFILE_1	0x00	0x01	0x01	0x03	0x17	0x2B
0x10E	RADIO_PROFILE_2	0x60	0xC8	0xFA	0xFA	0xF4	0xEE
0x10F	RADIO_PROFILE_3	AFC on: 0x20 AFC off: 0xF4	AFC on: 0x20 AFC off: 0xA3	AFC on: 0x20 AFC off: 0x82	AFC on: 0x20 AFC off: 0x41	0x20	0x16
0x110	RADIO_PROFILE_4	0x04	0x0E	0x13	0x26	0x4B	0x70
0x111	RADIO_PROFILE_5	0x00	0x00	0x00	0x00	0x00	0x00
0x112	RADIO_PROFILE_6	AFC on: 0x00 AFC off: 0x01	0x00	AFC on: 0x00 AFC off: 0x02	AFC on: 0x00 AFC off: 0x02	0x00	0x00
0x115	RADIO_PROFILE_7	FSK: 0x00 GFSK: 0x08	FSK: 0x00 GFSK: 0x08	FSK: 0x00 GFSK: 0x08	FSK: 0x00 GFSK: 0x08	FSK: 0x80 GFSK: 0x88	FSK: 0xC0 GFSK: 0xC8
0x117	RADIO_PROFILE_8	0x37	0x37	0x37	0x37	0x37	0x37
0x128	RADIO_PROFILE_9	0x2B	0x2B	0x2B	0x2B	0x2B	0x2B
0x12B	RADIO_PROFILE_10	0x2F	0x2F	0x2F	0x2F	0x2F	0x2F
0x12C	RADIO_PROFILE_11	0x12	0x12	0x12	0x12	0x12	0x12
0x12D	RADIO_PROFILE_12	0x07	0x07	0x07	0x07	0x07	0x07
0x12F	RADIO_PROFILE_13	0x00	0x00	0x00	0x00	0x00	0x00
0x130	RADIO_PROFILE_14	0x00	0x00	0x00	0x00	0x00	0x00
0x131	RADIO_PROFILE_15	0x00	0x00	0x00	0x00	0x00	0x00
0x132	RADIO_PROFILE_16	0x00	0x00	0x00	0x00	0x00	0x00
0x133	RADIO_PROFILE_17	0x00	0x00	0x00	0x00	0x00	0x00
0x134	RADIO_PROFILE_18	0x00	0x00	0x00	0x00	0x00	0x00
0x135	RADIO_PROFILE_19	0x00	0x00	0x00	0x00	0x00	0x00
0x136	RADIO_PROFILE_20	0x00	0x00	0x00	0x00	0x00	0x00
0x137	RADIO_PROFILE_21	0x00	0x00	0x00	0x00	0x00	0x00
0x138	RADIO_PROFILE_22	0xA7	0xA7	0xA7	0xA7	0xA7	0xA7

RADIO CONTROL

The ADF7024 has five designated radio states; PHY_SLEEP, PHY_OFF, PHY_ON, PHY_TX, and PHY_RX. The host processor can transition the ADF7024 between states by issuing single byte radio control commands over the SPI interface. The various commands and states are illustrated in Figure 12. The ADF7024 simplifies the processing burden of the host processor by handling the sequencing of various radio circuits and critical timing functions.

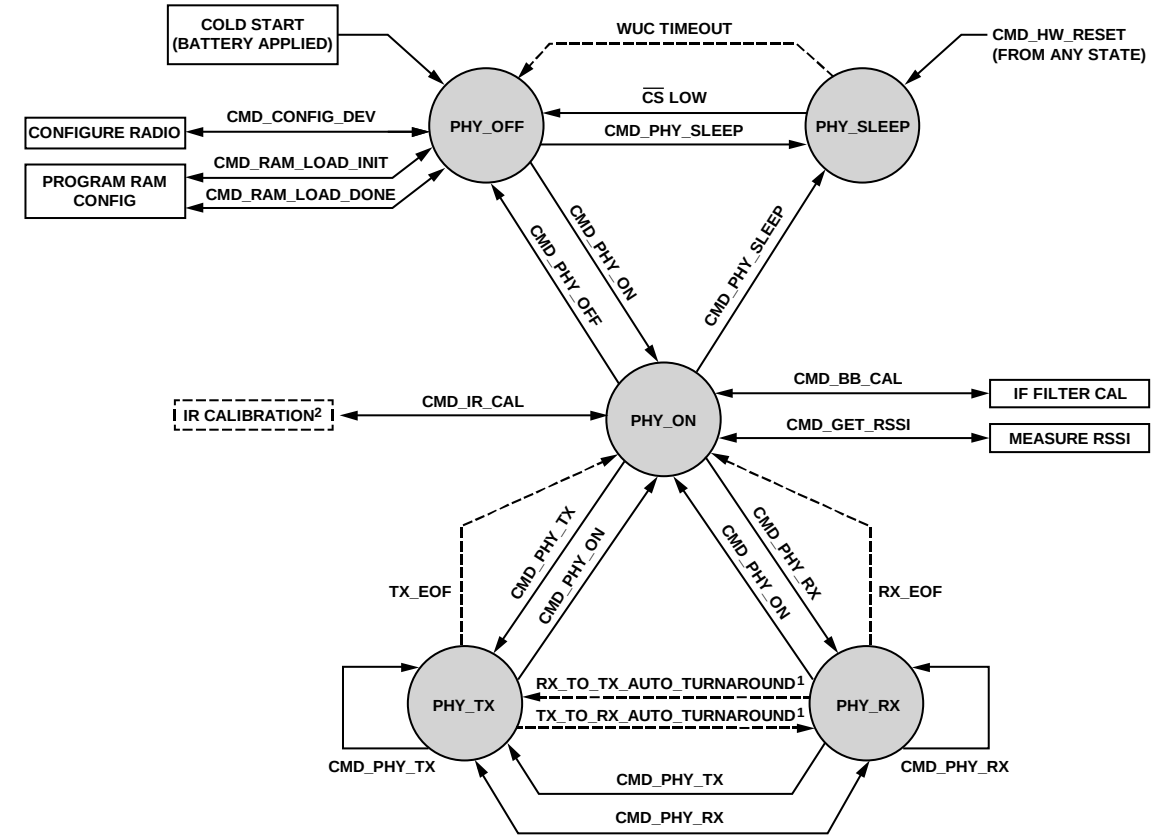


Figure 12. Radio State Diagram

RADIO STATES

PHY_SLEEP

In the PHY_SLEEP state, the device is in a low power sleep mode. To enter the PHY_SLEEP state, issue the CMD_PHY_SLEEP command, either from the PHY_OFF or PHY_ON state. To wake the radio from this state, set the $\overline{CS}$ pin low or use the wake-up controller, in which case, the wake-up timer must be set up before entering the PHY_SLEEP state. If retention of the configuration registers is not required, Deep Sleep Mode 2 can be used to further reduce the PHY_SLEEP state current consumption. Deep Sleep Mode 2 is entered by issuing the CMD_HW_RESET command. The options for the PHY_SLEEP state are detailed in Table 12. When in PHY_SLEEP, the IRQ_GP3 interrupt pin is held at logic low, while the other GPx pins are in a high impedance state.

PHY_OFF

In the PHY_OFF state, the 26 MHz crystal, the digital regulator, and the synthesizer regulator are powered up. All memories are fully accessible. The configuration registers must be valid before exiting this state.

PHY_ON

In the PHY_ON state, the VCO and RF regulators are powered up, in addition to the circuitry already powered up in the PHY_OFF state. The IF filter is calibrated if the BB_CAL bit in the RADIO_CONTROL register (Address 0x11A) was set prior to entering the PHY_ON state from the PHY_OFF state. The device is ready to operate, and the PHY_TX and PHY_RX states can be entered.

PHY_TX

In the PHY_TX state, the synthesizer is enabled and calibrated. The power amplifier is enabled, and the device transmits at the channel frequency defined by the CHANNEL_FREQ[23:0] setting (Address 0x109 to Address 0x10B). The PHY_TX state is entered by issuing the CMD_PHY_TX command. The device ramps up the PA and automatically transmits the transmit packet stored in the packet RAM. After transmission of the packet, the PA ramps down, then disables, and the device automatically returns to the PHY_ON state and can, optionally, generate an interrupt (TX_EOF).

PHY_RX

In the PHY_RX state, the synthesizer is enabled and calibrated. The ADC, RSSI, IF filter, mixer, and LNA are enabled. The radio is in receive mode on the channel frequency defined by the CHANNEL_FREQ[23:0] setting (Address 0x109 to Address 0x10B). After reception of a valid packet, the device returns to the PHY_ON state and can, optionally, generate an interrupt.

Current Consumption

The typical current consumption in each state is detailed in Table 12.

Table 12. Current Consumption in the ADF7024 Radio States

State	Current (Typical)	Test Conditions/Comments
PHY_SLEEP (Deep Sleep Mode 2)	0.18 µA	Wake-up timer off, configuration registers not retained, entered by issuing CMD_HW_RESET
PHY_SLEEP (Deep Sleep Mode 1)	0.33 µA	Wake-up timer off, configuration registers retained
PHY_SLEEP (WUC enabled)	0.75 µA	Wake-up timer on using the 32 kHz RC oscillator, configuration registers retained
PHY_OFF	1.0 mA	
PHY_ON	1.0 mA	
PHY_TX	24.1 mA	10 dBm, 868 MHz
PHY_RX	12.8 mA	

RADIO COMMANDS

The radio commands section details the radio commands that are supported by the ADF7024. The radio commands initiate transitions between radio states or perform tasks as indicated in Figure 12. The execution times for all radio state transitions are detailed in Table 13 and Table 14.

CMD_PHY_OFF (Command 0xB0)

The CMD_PHY_OFF command transitions the ADF7024 to the PHY_OFF state. It is issued in the PHY_ON state and powers down the RF and VCO regulators.

CMD_PHY_ON (Command 0xB1)

The CMD_PHY_ON command transitions the ADF7024 to the PHY_ON state. It can be issued from the PHY_OFF, the PHY_TX, or the PHY_RX state. If the CMD_PHY_ON command is issued in the PHY_OFF state, and if the BB_CAL bit (Bit 6) is set in the RADIO_CONTROL register (Address 0x11A), it performs an IF filter calibration.

CMD_PHY_SLEEP (Command 0xBA)

The CMD_PHY_SLEEP command transitions the ADF7024 to the very low power PHY_SLEEP state, in which, the WUC is operational (if enabled), and the configuration registers are retained. It can be issued from the PHY_OFF or the PHY_ON state.

CMD_PHY_RX (Command 0xB2)

The CMD_PHY_RX command transitions the ADF7024 to the PHY_RX state. It can be issued in the PHY_ON, the PHY_RX, or PHY_TX state. If the CMD_PHY_RX command is issued in the PHY_ON state, the receiver circuitry powers up, the channel frequency sets, based on the CHANNEL_FREQ[23:0] setting, and a VCO and synthesizer calibration performs during the transition to the PHY_RX state.

If the CMD_PHY_RX command is issued in the PHY_RX state, the new channel frequency sets, based on the CHANNEL_FREQ[23:0] setting, and a VCO and synthesizer calibration performs.

If the CMD_PHY_RX command is issued in the PHY_TX state, the PA ramps down, the channel frequency sets, based on the CHANNEL_FREQ[23:0] setting, and a VCO and synthesizer calibration performs during the transition to PHY_RX.

CMD_PHY_TX (Command 0xB5)

The CMD_PHY_TX command transitions the ADF7024 to the PHY_TX state. It can be issued in the PHY_ON, the PHY_TX, or the PHY_RX state. If the CMD_PHY_TX command is issued in the PHY_ON state, the channel frequency sets, based on the CHANNEL_FREQ[23:0] setting, a VCO and synthesizer calibration performs, and the PA ramps up.

If the CMD_PHY_TX command is issued in the PHY_TX state, first the PA ramps down, then the new channel frequency sets, based on the CHANNEL_FREQ[23:0] setting, a VCO and synthesizer calibration performs, and the PA ramps up.

If the CMD_PHY_TX command is issued in the PHY_RX state, the channel frequency sets, based on the CHANNEL_FREQ[23:0] setting, a VCO and synthesizer calibration performs, and the PA ramps up.

CMD_CONFIG_DEV (Command 0xBB)

The CMD_CONFIG_DEV command configures the radio parameters based on the configuration register settings. This command must be issued from the PHY_OFF state only. The only radio parameter that is not configured on this command is the CHANNEL_FREQ[23:0] setting, which is configured as part of a CMD_PHY_TX or CMD_PHY_RX command.

CMD_GET_RSSI (Command 0xBC)

The CMD_GET_RSSI command turns on the receiver, performs an RSSI measurement on the current channel, and returns the ADF7024 to the PHY_ON state. The RSSI result is saved to the RSSI_READBACK register (Address 0x312). This CMD_GET_RSSI command can be issued from the PHY_ON state only.

CMD_BB_CAL (Command 0xBE)

The CMD_BB_CAL command performs an IF filter calibration. This command can be issued from the PHY_ON state only. In many cases, it is not necessary to use the CMD_BB_CAL command, because an IF filter calibration is automatically performed by the ADF7024 on the PHY_OFF to PHY_ON transition, if BB_CAL = 1 in the RADIO_CONTROL register (Address 0x11A).

CMD_HW_RESET (Command 0xC8)

The CMD_HW_RESET command performs a full power-down of all hardware, and the device enters the PHY_SLEEP state, without the configuration register memory retained. The CMD_HW_RESET command can be issued in any state and is independent of the state of the ADF7024. The procedure for initializing the device after a CMD_HW_RESET command is described in detail in the Initialization section.

CMD_RAM_LOAD_INIT (Command 0xBF)

The CMD_RAM_LOAD_INIT command prepares the ADF7024 for the subsequent download of a firmware module. The CMD_RAM_LOAD_INIT command must be issued only before a firmware module is written to the ADF7024 by the host processor.

CMD_RAM_LOAD_DONE (Command 0xC7)

The CMD_RAM_LOAD_DONE command is required only after download of a firmware module to the ADF7024. It confirms to the ADF7024 that a firmware module is loaded by the host processor. The CMD_RAM_LOAD_DONE command is issued in the PHY_OFF state only. The CMD_RAM_LOAD_DONE command resets the ADF7024 and the packet RAM.

CMD_IR_CAL (Command 0xBD)

The CMD_IR_CAL command performs a fully automatic image rejection calibration on the ADF7024 receiver. The CMD_IR_CAL command requires that the IR calibration firmware module is loaded to the ADF7024. The firmware module is available from Analog Devices. For more information, see the Image Rejection Calibration Module section.

AUTOMATIC STATE TRANSITIONS

On certain events, the ADF7024 automatically transitions between states. These automatic transitions are shown as dashed lines in Figure 12 and are explained in this section.

TX_EOF

The ADF7024 automatically transitions the device from the PHY_TX state to the PHY_ON state at the end of a packet transmission.

RX_EOF

The ADF7024 automatically transitions the device from the PHY_RX state to the PHY_ON state at the end of a valid packet reception. A valid packet is one in which the CRC is correct. If CRC detection is disabled, a valid packet is one in which the sync word is detected.

RX_TO_TX_AUTO_TURNAROUND

If the RX_TO_TX_AUTO_TURNAROUND bit in the RADIO_ CONTROL register (Address 0x11A) is enabled, the ADF7024 automatically transitions to the PHY_TX state on the same RF channel frequency at the end of a valid packet reception.

TX_TO_RX_AUTO_TURNAROUND

If the TX_TO_RX_AUTO_TURNAROUND bit in the RADIO_ CONTROL register (Address 0x11A) is enabled, the ADF7024 automatically transitions to the PHY_RX state on the same RF channel frequency at the end of a packet transmission.

WUC Timeout

The ADF7024 uses the WUC to wake from sleep on a timeout of the hardware timer. The device wakes into the PHY_OFF state. See the WUC Mode section for further details.

INITIALIZATION

Initialization After Application of Power

When power is applied to the ADF7024, through the VDDBAT1/VDDBAT2 pins, it registers a power-on reset (POR) event and transitions to the PHY_OFF state. The configuration register memory is unknown, the packet RAM memory clears to 0x00, and the auxiliary register memory resets to its default values. The host processor must take the following steps to complete the initialization sequence:

1. Bring the $\overline{CS}$ pin of the SPI low and wait until the MISO output goes high.
2. Poll the ADF7024 status word by issuing SPI_NOP commands and wait for CMD_READY = 1.
3. Configure the part by writing to all 64 of the configuration registers; an SPI block memory write (SPI_MEM_WR command) is the most efficient way to do this.
4. Issue the CMD_CONFIG_DEV command so that the ADF7024 radio updates using the configuration register values.

The ADF7024 is now configured and ready to transition to the PHY_ON state.

Initialization After Issuing the CMD_HW_RESET Command

The CMD_HW_RESET command performs a full power-down of all hardware and the device enters the PHY_SLEEP state. To complete the hardware reset, the host processor must complete the following steps:

1. Wait for 1 ms.
2. Bring the $\overline{CS}$ pin of the SPI low and wait until the MISO output goes high. The ADF7024 registers a POR and enters the PHY_OFF state.
3. Poll the ADF7024 status word by issuing SPI_NOP commands and wait for CMD_READY = 1.
4. Configure the part by writing to all 64 of the configuration registers; an SPI block memory write (SPI_MEM_WR command) is the most efficient way to do this.
5. Issue the CMD_CONFIG_DEV command so that the ADF7024 radio updates using the configuration register values.

The ADF7024 is now configured and ready to transition to the PHY_ON state.

Initialization on Transitioning from PHY_SLEEP (After $\overline{CS}$ Is Brought Low)

The host processor can bring $\overline{CS}$ low at any time to wake the ADF7024 from the PHY_SLEEP state. This event is not registered as a POR event because the contents of the configuration registers are valid. To initialize the ADF7024 after $\overline{CS}$ is brought low and the ADF7024 is woken from the PHY_SLEEP state, the host processor must complete the following steps:

1. Bring the $\overline{CS}$ line of the SPI low and wait until the MISO output goes high. The ADF7024 enters the PHY_OFF state.
2. Poll the ADF7024 status word by issuing SPI_NOP commands and wait for CMD_READY = 1.
3. Issue the CMD_CONFIG_DEV command so that the ADF7024 radio updates using the configuration register values.

The ADF7024 is now configured and ready to transition to the PHY_ON state.

Initialization After a WUC Timeout

The ADF7024 can autonomously wake from the PHY_SLEEP state using the wake-up controller. If the ADF7024 wakes after a WUC timeout in smart wake mode (SWM), it follows the SWM routine, based on the smart wake mode settings in the register configuration (see the Low Power Modes section). If the ADF7024 wakes after a WUC timeout, with SWM disabled and with the firmware timer disabled, it wakes in the PHY_OFF state. To initialize the ADF7024 after a WUC timeout, the host processor must complete the following steps:

1. Poll the ADF7024 status word by issuing SPI_NOP commands and wait for CMD_READY = 1.
2. Issue the CMD_CONFIG_DEV command so that the ADF7024 radio updates using the configuration register values.

The ADF7024 is now configured and ready to transition to the PHY_ON state.

STATE TRANSITION AND COMMAND TIMING

The execution times for all radio state transitions are detailed in Table 13 and Table 14. Note that these times are typical and can vary, depending on the configuration register settings.

As stated in the Host Processor Interface section, commands are executed on the last positive SCLK edge of the command. For the measured values given in Table 13 and Table 14, there is 200 ns between the last positive SCLK edge and the rising edge of CS.

Table 13. ADF7024 Command Execution Times and State Transition Times not Related to PHY_TX or PHY_RX

Command or Transition	Command Initiated By	Present State	Next State	Transition Time (µs), Typical	Test Conditions/Comments
CMD_HW_RESET	Host	Any	PHY_SLEEP	1	Not applicable
CMD_PHY_SLEEP	Host	PHY_OFF	PHY_SLEEP	22.3	Not applicable
CMD_PHY_SLEEP	Host	PHY_ON	PHY_SLEEP	24.1	Not applicable
CMD_PHY_OFF	Host	PHY_ON	PHY_OFF	24	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt
CMD_PHY_ON	Host	PHY_OFF	PHY_ON	258 or 73	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt, IF filter calibration enabled (258) or disabled (73).
CMD_GET_RSSI	Host	PHY_ON	PHY_ON	631	Not applicable
CMD_CONFIG_DEV	Host	PHY_OFF	PHY_OFF	72	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt
CMD_CONFIG_DEV	Host	PHY_ON	PHY_ON	75.4	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt
CMD_BB_CAL	Host	PHY_ON	PHY_ON	221	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt
Wake-Up From PHY_SLEEP, (WUC Timeout)	ADF7024	PHY_SLEEP	PHY_OFF	304	7 pF load capacitance, T_A = 25°C
Wake-Up From PHY_SLEEP, ($\overline{CS}$ Low)	Host	PHY_SLEEP	PHY_OFF	304	7 pF load capacitance, T_A = 25°C
Cold Start	Application of power	Not applicable	PHY_OFF	304	7 pF load capacitance, T_A = 25°C

Table 14. ADF7024 State Transition Times Related to PHY_TX and PHY_RX

Command/Bit/ Automatic Transition	Present State	Next State	Transition Time (µs)[1, 2] Typical	Test Conditions/Comments
CMD_PHY_ON	PHY_TX	PHY_ON	t_{EOP} + t_{PARAMP_DOWN} + t_{BYTE} + 43	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt.
CMD_PHY_ON	PHY_RX	PHY_ON	t_{BYTE} + 48	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_ON issued during search for preamble.
			50.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_ON issued during preamble qualification.
			50.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_ON issued during sync word qualification.
			t_{EOP} + 62.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_ON issued during Rx data (after a sync word).
CMD_PHY_TX	PHY_ON	PHY_TX	306	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. The PA ramp up starts 3.4 µs after the interrupt. The first bit of user data is transmitted 1.5 × t_{BIT} + 2.3 µs following the interrupt.
CMD_PHY_TX	PHY_RX	PHY_TX	t_{BYTE} + 324.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_TX issued during search for preamble. The PA ramp up starts 3.4 µs after the interrupt. The first bit of user data is transmitted 1.5 × t_{BIT} + 2.3 µs following the interrupt.
			322.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_TX issued during preamble qualification. The PA ramp up starts 3.4 µs after the interrupt. The first bit of user data is transmitted 1.5 × t_{BIT} + 2.3 µs following the interrupt.

Command/Bit/ Automatic Transition	Present State	Next State	Transition Time (µs)[1, 2] Typical	Test Conditions/Comments
			322.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_TX issued during sync word qualification. The PA ramp up starts 3.4 µs after the interrupt. The first bit of user data is transmitted 1.5 × t_{BIT} + 2.3 µs following the interrupt.
			t_{EOP} + 281	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_TX issued during Rx data (after a sync word). The PA ramp up starts 3.4 µs after the interrupt. The first bit of user data is transmitted 1.5 × t_{BIT} + 2.3 µs following the interrupt.
CMD_PHY_TX	PHY_TX	PHY_TX	t_{EOP} + t_{PARAMP_DOWN} + t_{BYTE} + 310	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_TX issued during packet transmission. The PA ramp up starts 3.4 µs after the interrupt. The first bit of user data is transmitted 1.5 × t_{BIT} + 2.3 µs following the interrupt.
RX_TO_TX_AUTO_ TURNAROUND	PHY_RX	PHY_TX	322	From INTERRUPT_CRC_CORRECT to CMD_FINISHED interrupt. The PA ramp up starts 3.4 µs after the interrupt. The first bit of user data is transmitted 1.5 × t_{BIT} + 2.3 µs following the interrupt.
CMD_PHY_RX	PHY_ON	PHY_RX	327	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt.
CMD_PHY_RX	PHY_TX	PHY_RX	t_{EOP} + t_{PARAMP_DOWN} + t_{BYTE} + 336	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_RX issued during packet transmission.
CMD_PHY_RX	PHY_RX	PHY_RX	t_{BYTE} + 341.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_RX issued during search for preamble.
			339.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_RX issued during preamble qualification.
			339.5	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_RX issued during sync word qualification.
			t_{EOP} + 354	From rising edge of $\overline{CS}$ to CMD_FINISHED interrupt. CMD_PHY_RX issued during RX data (after a sync word).
TX_TO_RX_AUTO_ TURNAROUND	PHY_TX	PHY_RX	t_{PARAMP_DOWN} + t_{BYTE} + 322	From TX_EOF interrupt to CMD_FINISHED interrupt.
TX_EOF	PHY_TX	PHY_ON	t_{PARAMP_DOWN} + t_{BYTE} + 25	From TX_EOF interrupt to CMD_FINISHED interrupt.
RX_EOF	PHY_RX	PHY_ON	46	From INTERRUPT_CRC_CORRECT to CMD_FINISHED interrupt.

[1] $t_{PARAMP\_UP} = t_{PARAMP\_DOWN} = \frac{PA\_LEVEL}{Datarate\ (\text{bps}) \times PA\ Ramp\ Rate\ (\text{Codes/ Bits})}$, where PA_LEVEL sets the PA output power (Register RADIO_PA_LEVEL, Address 0x12E).

[2] t_{BYTE} is the one byte period (µs), and t_{EOP} is the time to end of packet (µs).

PACKET MANAGEMENT

The ADF7024 includes comprehensive transmit and receive packet management capabilities and can be configured for use with a wide variety of packet-based radio protocols. The general packet format is shown in Figure 13. 240 bytes of dedicated packet RAM are available to store, transmit, and receive packets. In transmit mode, preamble, sync word, and CRC can be added by the ADF7024 to the payload data that is stored in the packet RAM. In addition, all packet data after the sync word can be optionally whitened, Manchester encoded, or 8b/10b encoded on transmission and can be decoded on reception.

In receive mode, the ADF7024 can be used to qualify received packets based on preamble detection, sync word detection, or CRC validation and to generate an interrupt on the IRQ_GP3 pin. On reception of a valid packet, the received payload data is loaded to the packet RAM memory.

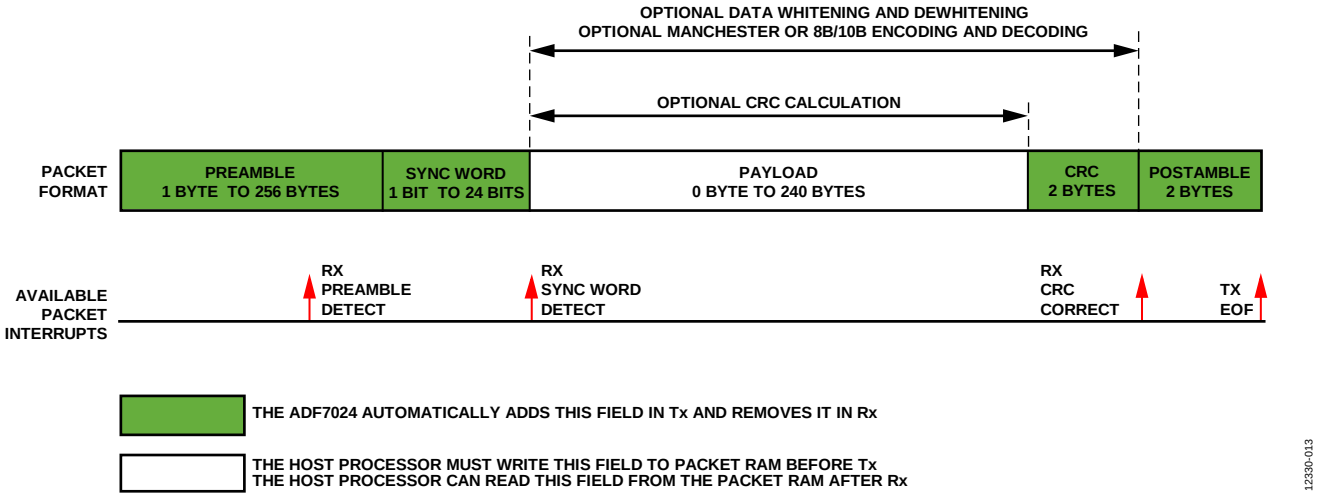


Figure 13.Packet Format and Packet Management Features of the ADF7024

PREAMBLE

The preamble is a mandatory part of the packet that is automatically added by the ADF7024 when transmitting a packet and is removed after receiving a packet. The preamble is a 0x55 sequence, with a programmable length between one byte and 256 bytes, that is set in the PKT_PREAMBLE_LEN register (Address 0x11D). It is necessary to have preamble at the beginning of the packet to allow time for the receiver AGC, AFC, and clock and data recovery circuitry to settle before the start of the sync word.

In receive mode, the ADF7024 can use a preamble qualification circuit to detect preamble and to interrupt the host processor. The preamble qualification circuit tracks the received frame as a sliding window. The window is three bytes in length (12-bit pairs), and the preamble pattern is fixed at 0x55. The preamble bits are examined in 01 pairs. If either bit or both bits are in error, the pair is deemed erroneous. The possible erroneous pairs are 00, 11, and 10. The number of erroneous pairs tolerated in the preamble is set using the PKT_PREAMBLE_MATCH register (Address 0x11B).

When the preamble is detected and the end of preamble is reached, the ADF7024 searches for the sync word. The search for the sync word lasts for a duration equal to the sum of the number of programmed sync word bits, plus the preamble matching tolerance (in bits), plus 16 bits. If the sync word is detected during this search time, the ADF7024 receives the packet, loads the received payload to the packet RAM, and computes the CRC (if enabled). If the sync word is not detected during this search time, the ADF7024 continues searching for the preamble.

Preamble detection is disabled by setting the PKT_PREAMBLE_ MATCH = 0x00. To enable an interrupt when the preamble is detected, the user must set INTERRUPT_PREAMBLE_DETECT = 1 in the INTERRUPT_MASK_0 register (Address 0x100).

Refer to the Recommended Preamble Lengths section for information on preamble length requirements.

SYNC WORD

Sync word is the synchronization word used by the receiver for byte level synchronization. The sync word is automatically added to the packet by the ADF7024 in transmit mode, and it is removed when a packet is received. The ADF7024 also provides an optional interrupt when the sync word is detected.

The value of the sync word is set in the PKT_SYNC_BYTE_0, PKT_SYNC_BYTE_1, and PKT_SYNC_BYTE_2 registers (Address 0x121, Address 0x122, and Address 0x123, respectively). The sync word is transmitted with the most significant bit first, starting with PKT_SYNC_BYTE_0. The sync word matching length at the receiver is set using SYNC_WORD_LENGTH in the PKT_SYNC_CONTROL register (Address 0x120) and can be one bit to 24 bits long. The transmitted sync word is a multiple of eight bits. Therefore, for nonbyte length sync words, the transmitted sync pattern must be appended with the preamble pattern as described in Figure 14 and Table 15.

In receive mode, the ADF7024 can provide an interrupt when the sync word sequence programmed in the PKT_SYNC_BYTE_x registers is received. This feature is used to alert the host processor that a qualified sync word has been received. An error tolerance parameter can also be programmed that accepts a valid match when up to three bits of the sync word sequence are incorrect. The error tolerance value is set using the SYNC_ERROR_TOL setting in the PKT_SYNC_CONTROL register (Address 0x120).

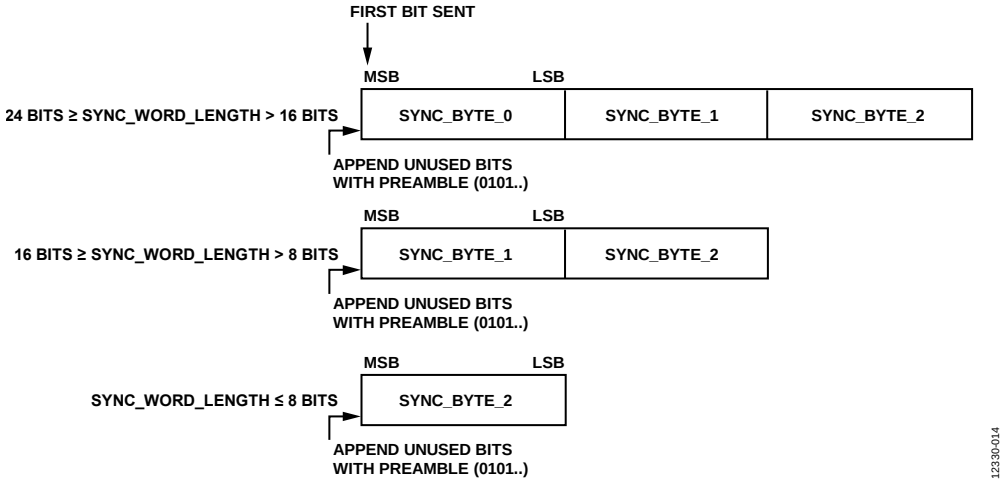


Figure 14. Transmit Sync Word Configuration

Table 15. Sync Word Programming Examples

Required Sync Word (First Bit Being First in Time)	SYNC_WORD_ LENGTH Bits in PKT_SYNC_CONTROL Register (0x120)	PKT_SYNC_ BYTE_0[1]	PKT_SYNC_ BYTE_1[1]	PKT_SYNC_ BYTE_2	Transmitted Sync Word (First Bit Being First in Time)	Receiver Sync Word Match Length (Bits)
0b0001001000110100 01010110	24	0x12	0x34	0x56	0b0001001000110100 01010110	24
0b1110100111001010 00100	21	0x5D	0x39	0x44	0b0101110100111001 01000100	21
0b0001001000110100	16	0xXX	0x12	0x34	0b0001001000110100	16
0b 011100001110	12	0xXX	0x57	0x0E	0b0101011100001110	12
0b 00010010	8	0xXX	0xXX	0x12	0b00010010	8
0b 011100	6	0xXX	0xXX	0x5C	0b01011100	6

[1] X = don't care.

PAYLOAD

The host processor writes the transmit data payload to the packet RAM. The location of the transmit data in the packet RAM is defined by the PKT_TX_BASE_ADR value register (Address 0x124). The PKT_TX_BASE_ADR value is the location of the first byte of the transmit payload data in the packet RAM. On reception of a valid sync word, the ADF7024 automatically loads the receive payload to the packet RAM. The PKT_RX_BASE_ADR register value (Address 0x125) sets the location in the packet RAM of the first byte of the received payload. For more details on packet RAM memory, see the ADF7024 Memory Map section.

Byte Orientation

The over the air arrangement of each transmitted packet RAM byte can be set to MSB first or LSB first using the DATA_BYTE setting in the PKT_LENGTH_CONTROL register (Address 0x126). Use the same orientation setting on the transmit side and the receive side of the RF link.

Packet Length Modes

The ADF7024 can be used in both fixed and variable length packet systems. Fixed or variable length packet mode is set using the PKT_LENGTH_MODE variable setting in the PKT_LENGTH_CONTROL register (Address 0x126).

The payload length is defined as the number of bytes from the end of the sync word to the start of the CRC. In fixed packet length mode, the ADF7024 calculates the length of the transmit and receive payload, based on the PACKET_LENGTH_MAX register (Address 0x127) setting and the LENGTH_OFFSET setting in the PKT_LENGTH_CONTROL register (Address 0x126). In variable packet length mode, the ADF7024 calculates the length of the transmit and receive payload, based on the value of the first payload byte and the LENGTH_OFFSET setting. The LENGTH_OFFSET value allows compatibility with systems in which the length field in the proprietary packet may also include the length of the CRC and/or the sync word. The definition of payload length in fixed and variable length packet modes is shown in Figure 15.

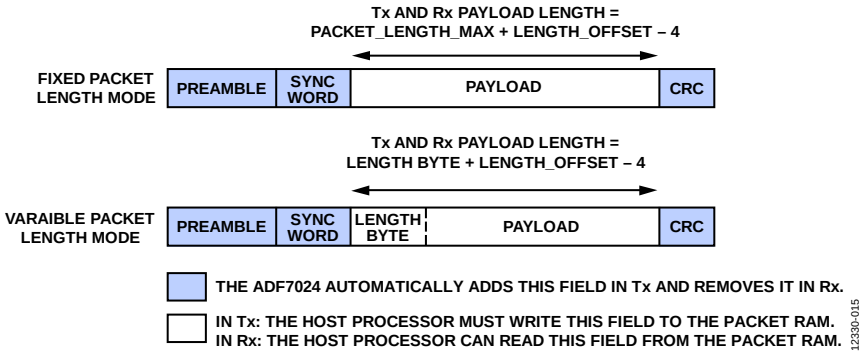


Figure 15. Payload Length in Fixed and Variable Length Packet Modes

CRC

An optional CRC-16 can be appended to the transmit packet by setting CRC_EN = 1 in the PKT_LENGTH_CONTROL register (Address 0x126). In receive mode, this bit enables the CRC validation of the received packet. When a valid CRC is received, if the interrupt is enabled by setting INTERRUPT_CRC_CORRECT = 1 in the INTERRUPT_MASK_0 register (Address 0x100), the interrupt CRC_CORRECT is triggered.

The polynomial is set in PKT_CRC_POLY_0 and PKT_CRC_POLY_1 (Address 0x11E and Address 0x11F, respectively). The CRC calculation is initialized with 0x0000.

To convert a user defined polynomial to the 2-byte value, the polynomial must be written in binary format. The x^{16} coefficient is assumed equal to 1 and is, therefore, discarded. The remaining 16 bits then make up CRC_POLY_0 (most significant byte) and CRC_POLY_1 (least significant byte). Examples of setting common 16-bit CRCs are shown in Table 16.

Table 16. Example Programming of CRC_POLY_0 and CRC_POLY_1

Polynomial	Binary Format (Discarding x^{16})	CRC_POLY_0	CRC_POLY_1
$x^{16} + x^{15} + x^2 + 1$ (CRC-16-IBM)	0b1000000000000101	0x80	0x05
$x^{16} + x^{12} + x^5 + 1$ (CRC-16-CCITT)	0b0001000000100001	0x10	0x21
$x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$ (CRC-16-DNP)	0b0011110101100101	0x3D	0x65

POSTAMBLE

The ADF7024 automatically appends two bytes of postamble to the end of the transmitted packet. Each byte of the postamble is 0x55. The first byte is transmitted immediately after the CRC. The PA ramp down begins immediately after the first postamble byte. The second byte is transmitted while the PA is ramping down.

At the receiver, if the received packet is valid, the RSSI is automatically measured during the first postamble byte, and the result is stored in the RSSI_READBACK register (Address 0x312). The RSSI is measured by the ADF7024 17 µs after the last CRC bit.

DATA WHITENING

Data whitening is employed to avoid long runs of ones or zeros in the transmitted data stream. Data whitening ensures sufficient bit transitions in the packet, which aids in receiver clock and data recovery because the encoding breaks up long runs of ones or zeros in the transmit packet. The data, excluding the preamble and the sync word, is automatically whitened before transmission by XOR'ing the data with an 8-bit pseudorandom sequence. At the receiver, the data is XOR'ed with the same pseudorandom sequence, thereby reversing the whitening. The linear feedback shift register polynomial used is $x^7 + x^1 + 1$. The data whitening is applied to the payload data and the CRC. Data whitening and dewhitening are enabled by setting DATA_WHITENING = 1 in the PKT_SYMBOL_MODE register (Address 0x11C).

MANCHESTER ENCODING

Manchester encoding is used to ensure a dc free transmission of the data bits. The encoded over the air bit rate (chip rate) is double the data rate defined by the chosen radio profile. A Binary 0 is mapped to 10, and a Binary 1 is mapped to 01. Manchester encoding and decoding are applied to the payload data and the CRC. Manchester encoding and decoding are enabled by setting MANCHESTER_ENC = 1 in the PKT_SYMBOL_MODE register (Address 0x11C).

8b/10b ENCODING

8b/10b encoding is a byte orientated encoding scheme that maps an 8-bit byte to a 10-bit data block. It ensures that the maximum number of consecutive ones or zeros (run length) in any 10-bit transmitted symbol is five. The advantage of this encoding scheme is that dc balancing is employed without the efficiency loss of Manchester encoding. The rate loss for 8b/10b encoding is 0.8, whereas for Manchester encoding, it is 0.5. Encoding and decoding are applied to the payload data and the CRC. The 8b/10b encoding and decoding are enabled by setting EIGHT_TEN_ENC = 1 and by setting SYMBOL_LENGTH = 1 in the PKT_SYMBOL_MODE register (Address 0x11C).

INTERRUPT GENERATION

The ADF7024 uses a flexible interrupt system with support for MAC level interrupts and PHY level interrupts.

The MAC interrupt sources are enabled by writing a Logic 1 to the relevant bits of the INTERRUPT_MASK_0 register (Address 0x100). The interrupt source is read from the INTERRUPT_SOURCE_0 register (Address 0x336).

For the PHY interrupts to be available on the IRQ_GP3 pin, the relevant bit of the INTERRUPT_MASK_1 register (Address 0x101) must be set to Logic 1. The interrupt source is read from the INTERRUPT_SOURCE_1 register (Address 0x337).

When a masked interrupt occurs, the IRQ_GP3 pin goes high, and the interrupt bit of the status word is set to Logic 1. The host processor can use either the IRQ_GP3 pin or the status word to check for an interrupt. After an interrupt is asserted, the ADF7024 continues operations unaffected, unless it is directed to do otherwise by the host processor. An outline of the interrupt source and mask system is shown in Figure 16 and described in Table 17 and Table 18.

Following an interrupt condition, the host processor must clear the relevant interrupt flag so that further interrupts assert the IRQ_GP3 pin. The host processor can clear the flag by writing a Logic 1 to the bit that is high in either the INTERRUPT_SOURCE_0 or the INTERRUPT_SOURCE_1 register. If multiple bits in the interrupt source registers are high, they can be cleared individually or together by writing Logic 1. The IRQ_GP3 pin goes low when all the masked interrupt source bits are cleared.

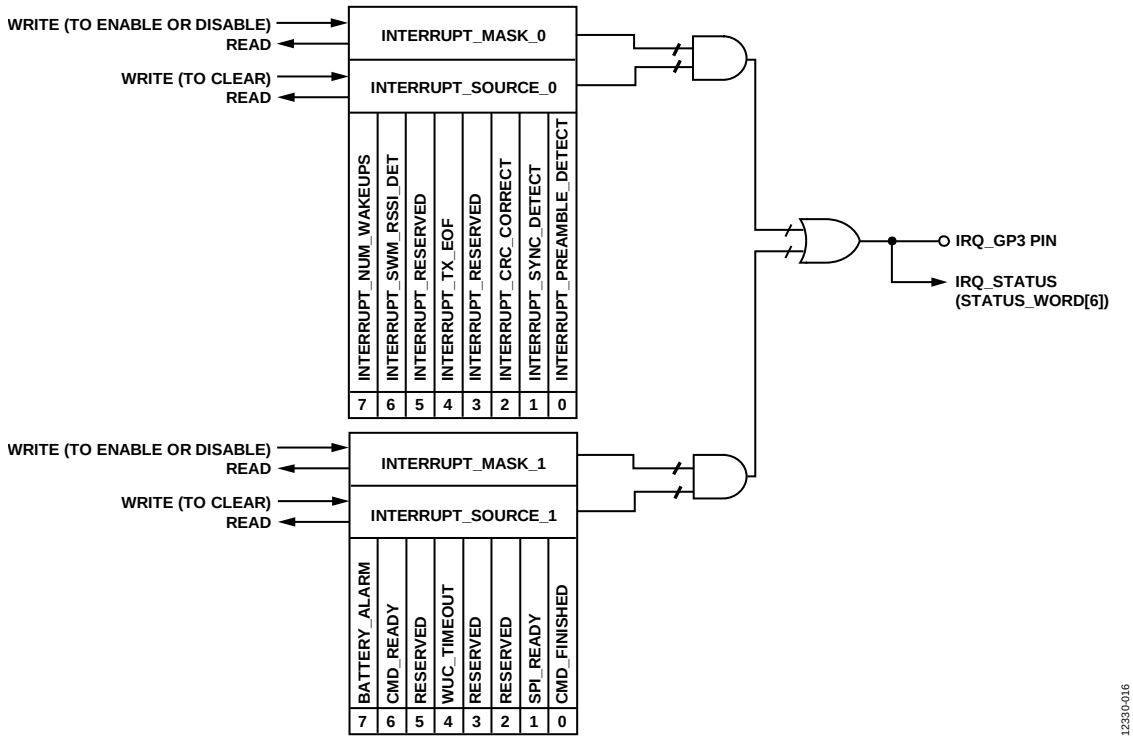


Figure 16. ADF7024 Interrupt System

Table 17. MAC Interrupts

Register	Bit	Interrupt Name	Description
INTERRUPT_MASK_0, Address 0x100 and INTERRUPT_SOURCE_0, Address 0x336	7	INTERRUPT_NUM_WAKEUPS	Asserted when the number of WUC wakeups (NUMBER_OF_WAKEUPS[15:0]) reaches the threshold (NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[15:0]). To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	6	INTERRUPT_SWM_RSSI_DET	Asserted when the measured RSSI during smart wake mode exceeds the RSSI threshold value (SWM_RSSI_THRESH, Address 0x108). To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	5	Reserved	Reserved.
	4	INTERRUPT_TX_EOF	Asserted when a packet has finished transmitting. To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	3	Reserved	Reserved.
	2	INTERRUPT_CRC_CORRECT	Asserted when a received packet has the correct CRC. To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	1	INTERRUPT_SYNC_DETECT	Asserted when a qualified sync word has been detected in the received packet. To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	0	INTERRUPT_PREAMBLE_DETECT	Asserted when a qualified preamble has been detected in the received packet. To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.

Table 18. PHY Interrupts

Register	Bit	Name	Description
INTERRUPT_MASK_1, Address 0x101 and INTERRUPT_SOURCE_1, Address 0x337	7	BATTERY_ALARM	Asserted when the battery voltage drops below the threshold value (BATTERY_MONITOR_THRESHOLD_VOLTAGE, Address 0x32D). To mirror this interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	6	CMD_READY	Asserted when the ADF7024 is ready to load a new command; mirrors the CMD_READY bit of the status word. To mirror this interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	5	Reserved	Reserved.
	4	WUC_TIMEOUT	Asserted when the WUC has timed out. To mirror this interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	3	Reserved	Reserved.
	2	Reserved	Reserved.
	1	SPI_READY	Asserted when the SPI is ready for access. To mirror this interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	0	CMD_FINISHED	Asserted when the ADF7024 has finished performing a command. To mirror this interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.

RADIO BLOCKS

FREQUENCY SYNTHESIZER

A fully integrated RF frequency synthesizer is used to generate both the transmit signal and the receiver local oscillator (LO) signal. A high speed, fully automatic calibration scheme is used to ensure that the frequency and amplitude characteristics of the VCO are maintained over temperature, supply voltage, and process variations. The calibration is automatically performed when the CMD_PHY_RX or the CMD_PHY_TX command is issued.

The ADF7024 automatically sets the bandwidth of the synthesizer when the device enters the PHY_TX or the PHY_RX state. When the ADF7024 enters the PHY_TX state, it automatically chooses the bandwidth, based on the radio profile, which ensures optimum modulation quality for each data rate. When the ADF7024 enters the PHY_RX state, it sets a narrow bandwidth to ensure best interference rejection. Each synthesizer bandwidth setting is described in Table 19.

Table 19. Automatic Synthesizer Bandwidth Selections

Description	Profile	Data Rate (kbps)	Closed-Loop Synthesizer Bandwidth (kHz)
Rx	All	All	92
Tx	A	9.6	130
Tx	B	38.4	130
Tx	C	50	174
Tx	D	100	174
Tx	E	200	305
Tx	F	300	382

CRYSTAL OSCILLATOR

A 26 MHz crystal oscillator, operating in parallel mode, must be connected between the XOSC26P and the XOSC26N pins to provide a reference for the ADF7024. It is also possible to use a single-ended reference (TCXO), which can be ac-coupled to the XOSC26N pin, with the XOSC26P pin left unconnected.

When using a 26 MHz crystal oscillator, two parallel loading capacitors are required for oscillation at the correct frequency. Their values are dependent on the crystal specification. Choose capacitors to ensure that the shunt value of the capacitance added to the PCB track capacitance and the input pin capacitance of the ADF7024 equates to the specified load capacitance of the crystal, usually 10 pF to 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on the board layout. The total load capacitance is described by

$$C_{LOAD} = \frac{1}{\frac{1}{C1}+\frac{1}{C2}} + \frac{C_{PIN}}{2} + C_{PCB}$$

where:
C_{LOAD} is the total load capacitance.
$C1$ and $C2$ are the external crystal load capacitors.
C_{PIN} is the ADF7024 input capacitance of the XOSC26P and the XOSC26N pins and is equal to 2.1 pF.
C_{PCB} is the PCB track capacitance.

When possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

The crystal frequency error can be corrected by means of an integrated digital tuning varactor. For a typical crystal load capacitance of 10 pF, a tuning range of 0 ppm to 15 ppm is available via programming of a 3-bit DAC, as shown in Table 20. Write the 3-bit value to the XOSC_CAP_DAC bits in the OSC_CONFIG register (Address 0x3D2).

Alternatively, any error in the RF frequency due to crystal error can be adjusted by offsetting the RF channel frequency, using the RF channel frequency setting in the configuration register memory. The AFC feature can also correct frequency errors by automatically adjusting the receiver LO frequency to match the RF transmit frequency. See the AFC section for further details.

Table 20. Crystal Frequency Pulling Programming

XOSC_CAP_DAC	Pulling (ppm)
000	+15
001	+11.25
010	+7.5
011	+3.75
100	0

MODULATION

The ADF7024 supports binary frequency shift keying (2FSK) and binary level Gaussian filtered 2FSK (GFSK) modulation. For GFSK modulation, the Gaussian filter uses a fixed BT of 0.5. The modulation type is set by configuring the RADIO_PROFILE_7 register (Address 0x115) for the desired radio profile register, as described in Table 11.

RF OUTPUT STAGE

Power Amplifier (PA)

The ADF7024 PA has a single-ended output that can deliver up to 13.5 dBm output power. The output power is set with a typical resolution of 0.5 dB, using the PA_LEVEL setting in the RADIO_PA_LEVEL register (Address 0x12E).

Automatic PA Ramp

The ADF7024 has built-in up and down PA ramping that reduces spectral splatter. The PA ramps at a rate defined by the PA_RAMP setting in the RADIO_PA_RAMP register (Address 0x114) and ramps to the level set by the PA_LEVEL in the RADIO_PA_LEVEL register (Address 0x12E). The ramp rate is configured as a certain number of PA level codes per data bit period. To ensure optimum performance, an adequately long PA ramp rate is required, based on the data rate and the PA output power setting. Therefore, the PA_RAMP setting must be set so that

$$Ramp\ Rate\ \left(\text{Codes/Bit}\right) < 10^6 \times \frac{PA\_LEVEL}{Datarate\ \left(\text{bps}\right)}$$

The PA ramp up and down timing in relation to the transmit packet data is described in Figure 17. For a long PA ramp time, the end of the PA ramp can occur after the start of the preamble data. In this case, the PA ramp rate should be increased to ensure the PA ramp has finished before the start of the preamble data. In applications where a long PA ramp time is required, increase the transmit preamble length by one byte to allow extra time for the PA to finish ramping before the start of the actual preamble.

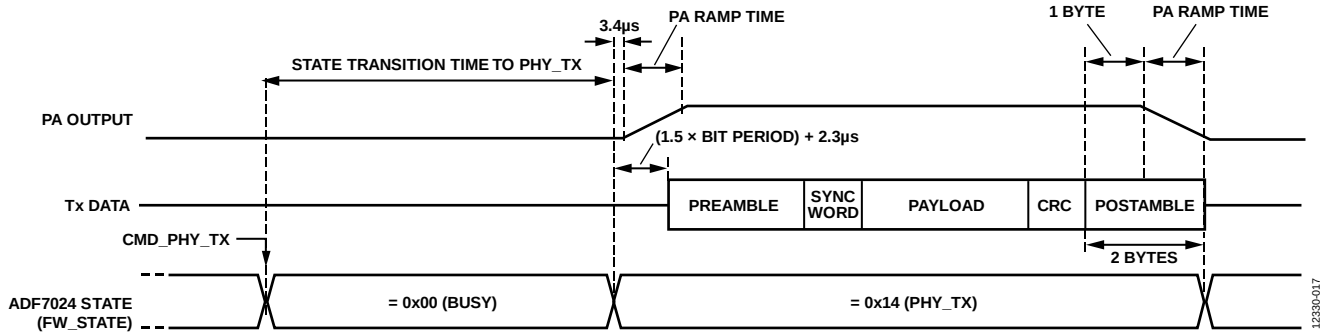


Figure 17. Transmit Packet Timing

RECEIVE CHANNEL FILTER

The receive channel filter of the ADF7024 provides excellent interference suppression of adjacent and neighboring channels. The center frequency and bandwidth of the filter is configured based on the radio profile, as described in Table 21. The bandwidth and center frequency of the IF filter are calibrated automatically after entering the PHY_ON state, if the BB_CAL bit is set in the RADIO_CONTROL register (Address 0x11A).

Table 21. Receive Channel Filter Configuration for Each Radio Profile

Radio Profile	IF Frequency (kHz)	Receive Channel Filter Bandwidth (kHz)
A	200	100
B	200	100
C	200	100
D	200	100
E	200	200
F	300	300

IMAGE CHANNEL REJECTION

The ADF7024 can provide improved receiver image rejection performance by the use of a fully integrated image rejection calibration system. To operate the calibration system, a firmware module is downloaded to the on-chip program RAM. The firmware download is supplied by Analog Devices and is described in the Downloadable Firmware Module section.

To achieve the typical uncalibrated image attenuation values given in the ADF7024 data sheet, use the recommended default values for IMAGE_REJECT_CAL_PHASE (Address 0x118) and IMAGE_REJECT_CAL_AMPLITUDE (Address 0x119). These recommended defaults, at 868 MHz or 915 MHz, are IMAGE_REJECT_CAL_AMPLITUDE = 0x07 and IMAGE_REJECT_CAL_PHASE = 0x16. The recommended defaults, at 433 MHz, are IMAGE_REJECT_CAL_AMPLITUDE = 0x03 and IMAGE_REJECT_CAL_PHASE = 0x08.

However, writing a nonzero value to the IMAGE_REJECT_CAL_PHASE or IMAGE_REJECT_CAL_AMPLITUDE registers can degrade the receiver sensitivity by up to 1 dB.

AUTOMATIC GAIN CONTROL (AGC)

The AGC is enabled by default and keeps the receiver gain at the correct level by selecting the LNA, mixer, and receive channel filter gain settings, based on the measured RSSI level. In total, there are six AGC stages, which are defined in Table 22.

Table 22. AGC Gain Modes

Gain Mode	LNA Gain	Mixer Gain	Filter Gain
1	High	High	High
2	High	Low	High
3	Medium	Low	High
4	Low	Low	High
5	Low	Low	Medium
6	Low	Low	Low

The AGC can be configured to lock on detection of the qualified preamble or on detection of the qualified sync word. To lock the AGC on detection of the qualified preamble, set AGC_LOCK_ MODE = 3 (Address 0x113) and ensure that preamble detection is enabled in the PKT_PREAMBLE_MATCH register (Address 0x11B). The AGC lock is released if the sync word is not detected after the end of the preamble. If the qualified preamble is followed by a qualified sync word, the AGC lock is maintained for the duration of the packet. To lock the AGC on detection of the qualified sync word, set AFC_LOCK_MODE = 3 and ensure that preamble detection is disabled in the PREAMBLE_MATCH register (Address 0x11B).

The LNA, filter, and mixer gains can be read back through the AGC_GAIN_STATUS register (Address 0x360).

RSSI

The ADF7024 provides an accurate measurement of the received signal strength. The ADF7024 has three RSSI measurement methods that support a wide range of applications. These functions can be used to implement carrier sense (CS) or clear channel assessment (CCA). The RSSI is automatically recorded in the auxiliary memory register RSSI_READBACK (Address 0x312) after receiving a packet. The three RSSI measurement methods are described in the following sections and are summarized in Table 24.

RSSI Method 1

When a valid packet is received, the RSSI level during postamble is automatically loaded to the RSSI_READBACK register (Address 0x312). The RSSI_READBACK register contains a twos complement value and can be converted to input power in dBm using the following formula:

$$RSSI(dBm) = RSSI\_READBACK - 107$$

RSSI Method 2

The CMD_GET_RSSI command can be used from the PHY_ON state to read the RSSI. This RSSI measurement method uses additional low-pass filtering, resulting in a more accurate RSSI reading. The RSSI result is loaded to the RSSI_READBACK register (Address 0x312). The CMD_GET_RSSI execution time is specified in Table 13. The RSSI_READBACK register contains a twos complement value and can be converted to input power in dBm using the following formula:

$$RSSI(dBm) = RSSI\_READBACK - 107$$

RSSI Method 3

This method supports the measurement of the RSSI by the host processor while in the PHY_RX state. The receiver input power can be calculated using the following procedure:

1. Lock the AGC by setting the AGC_MODE register (Address 0x35D) = 0x40. This step can be skipped if the AGC was already automatically locked after preamble or sync word detection.
2. Read back the AGC gain settings (AGC_GAIN_STATUS register, Address 0x360).
3. Read the ADC_READBACK[7:0] bit values (Address 0x327 and Address 0x328; see the Analog-to-Digital Converter section).
4. Unlock the AGC by setting the AGC_MODE register (Address 0x35D) = 0x00. This step can be skipped if the AGC was already automatically locked after preamble or sync word detection.
5. Calculate the RSSI in dBm as follows:

$$RSSI(dBm) = \left(ADC\_READBACK[7:0] \times \frac{1}{7} + Gain\_Correction \right) - 109$$

where *Gain_Correction* is determined by the value of the AGC_GAIN_STATUS register (Address 0x360), as shown in Table 23.

Table 23. Gain Mode Correction RSSI

AGC_GAIN_STATUS (Address 0x360)	GAIN_CORRECTION
0x00	44
0x01	35
0x02	26
0x0A	17
0x12	10
0x16	0

To simplify the RSSI calculation, the host processor uses the following approximation:

$$\frac{1}{7} \approx \frac{1}{8}\left(1+\frac{1}{8}+\frac{1}{64}\right)$$

Table 24. Summary of RSSI Measurement Methods

RSSI Method	RSSI Type	Description
1	Automatic end of packet RSSI	Automatic RSSI measurement during reception of the postamble in packet mode. The RSSI result is available in the RSSI_READBACK register (Address 0x312).
2	CMD_GET_RSSI command from PHY_ON	Automatic RSSI measurement from PHY_ON using CMD_GET_RSSI. The RSSI result is available in the RSSI_READBACK register (Address 0x312).
3	RSSI via ADC and AGC readback	RSSI measurement based on the ADC and AGC gain readbacks. The host processor calculates RSSI in dBm.

DEMODULATION

A correlator demodulator is used for demodulation. The quadrature outputs of the IF filter are first limited and then fed to a digital frequency correlator that performs filtering and frequency discrimination of the 2FSK/GFSK spectrum. Data is recovered by comparing the output levels from two correlators. The performance of this frequency discriminator approximates that of a matched filter detector, which is known to provide optimum detection in the presence of additive white Gaussian noise (AWGN). This method of demodulation provides approximately 3 dB to 4 dB better sensitivity than a linear frequency discriminator.

AFC

The ADF7024 features an internal, real-time, automatic frequency control loop. In receive mode, with AFC enabled, the control loop automatically monitors the frequency error during the packet preamble sequence and adjusts the receiver synthesizer local oscillator using proportional integral (PI) control. The AFC frequency error measurement bandwidth is targeted specifically at the packet preamble sequence.

The AFC can be configured to lock when the qualified preamble or when the qualified sync word is detected. To lock the AFC when the qualified preamble is detected, set AFC_LOCK_ MODE = 3 (Address 0x116) and ensure that preamble detection is enabled in the PKT_PREAMBLE_MATCH register (Address 0x11B). The AFC lock is released if the sync word is not detected immediately after the end of the preamble. If the qualified preamble is followed by a qualified sync word, the AFC lock is maintained for the duration of the packet.

To lock the AFC when the qualified sync word is detected, set AFC_LOCK_MODE = 3 and ensure that preamble detection is disabled in the PREAMBLE_MATCH register (Address 0x11B). If this mode is selected, consideration must be given to the selection of the sync word.

The sync word must be dc free, have short run lengths, and low correlation with the preamble sequence. When the AFC locks after detecting the qualified sync word, the AFC lock is maintained for the duration of the packet.

AFC and Preamble Length

The AFC requires a certain number of the received preamble bits to correct the frequency error between the transmitter and the receiver. The number of preamble bits required depends on the radio profile and on whether the AFC is locked after detecting the qualified preamble or locked after detecting the qualified sync word. For more information, see the Recommended Preamble Length section.

AFC Readback

The frequency error between the received carrier and the receiver channel frequency is measured when AFC is enabled. The error value is read from the FREQUENCY_ERROR_READBACK register (Address 0x372), where each LSB equals 1 kHz. The value is a twos complement number. The FREQUENCY_ERROR_ READBACK value is valid in the PHY_RX state after the AFC is locked. The value is retained in the FREQUENCY_ ERROR_READBACK register after recovering a valid packet (CRC is correct) and transitioning back to the PHY_ON state.

CLOCK RECOVERY

An oversampled digital clock and data recovery (CDR) PLL is used to resynchronize the received bit stream to a local clock in all modulation modes. The maximum symbol rate tolerance of the CDR PLL is determined by the number of bit transitions in the transmitted bit stream. For example, during reception of a 010101 preamble, the CDR achieves a maximum data rate tolerance of ±3.0%. However, during recovery of the remainder of the payload, where symbol transitions may not be guaranteed to occur at regular intervals, the data rate tolerance is reduced. To maximize data rate tolerance of the receiver CDR, 8b/10b encoding or Manchester encoding must be enabled, which guarantees a maximum number of contiguous bits in the transmitted bit stream. Data whitening can also be enabled on the ADF7024 to break up long sequences of contiguous data bit patterns.

The ADF7024 can tolerate uncoded payload data fields and payload data fields with long run length coding constraints, if the data rate tolerance and packet length are both constrained. More details of CDR operation using uncoded packet formats are discussed in the AN-915 Application Note.

RECOMMENDED PREAMBLE LENGTHS

To ensure optimal performance of the ADF7024 receiver, a sufficient number of preamble bytes is required in the packet. The required preamble length and typical receiver frequency tolerances for various radio profiles and receiver configurations are summarized in Table 25.

Table 25. Minimum Preamble Length Requirements and Typical Receiver Frequency Tolerances

Radio Profile	AFC	Preamble Detection	Minimum Recommended Preamble Length (Bytes)	Typical Receiver Frequency Tolerance (kHz)	Recommended Sync Word Error Tolerance (bits)	DC Balanced Sync Word Required?
F	Enabled	Enabled	8	±46	0	No
F	Disabled	Enabled	5	±10	0	No
F	Enabled	Disabled	8	±46	1	Yes
F	Disabled	Disabled	4	±10	0	No
E	Enabled	Enabled	7	±46	0	No
E	Disabled	Enabled	4	±6.2	0	No
E	Enabled	Disabled	7	±46	1	Yes
E	Disabled	Disabled	4	±6.2	0	No
D	Enabled	Enabled	6	±46	0	No
D	Enabled	Disabled	4	±46	1	Yes
C	Enabled	Enabled	6	±46	0	No
C	Enabled	Disabled	3	±46	0	Yes
B	Enabled	Enabled	7	±46	0	No
B	Enabled	Disabled	2	±46	0	Yes
A	Enabled	Enabled	5	±46	0	No
A	Enabled	Disabled	2	±46	0	Yes

AFC Enabled, Preamble Detection Enabled

With the AFC and preamble detection enabled, the AFC and AGC lock when the qualified preamble is detected. In this configuration, a sufficient number of preamble bytes are required by the receiver for frequency acquisition of the AFC loop, for receiver AGC and CDR acquisition, and for preamble qualification. This is the recommended receiver configuration, unless a shorter preamble length is required.

AFC Enabled, Preamble Detection Disabled

With preamble detection disabled, the AFC and AGC lock when the sync word is detected; therefore, preamble qualification is not required, which reduces the minimum preamble requirement. However, in this configuration, the format of the sync word is important and needs to be dc balanced to ensure that the AFC frequency acquisition is accurate during reception of the sync word. As well as having the sync word dc balanced, it is recommended to set the last nibble of the sync word to 0b1010 or 0b0101. For some radio profiles, it is recommended to allow one bit error in the sync word by setting SYNC_ERROR_TOL = 1 in the PKT_SYNC_CONTROL register (Address 0x120). This setting allows a single bit error to occur in the sync word without preventing qualification of the sync word. However, increasing the sync word error tolerance increases the probability of false sync word detections.

AFC Disabled

With the AFC disabled, the preamble length requirement is reduced, because the receiver no longer requires preamble for frequency acquisition of the AFC loop. Therefore, this receiver configuration has the shortest minimum preamble requirement. However, because there is no correction of the RF frequency error with AFC disabled, the tolerance of the receiver to RF frequency errors is greatly reduced, as shown in Table 25. Therefore, this mode is only recommended for applications that use a high accuracy crystal or TCXO as the reference for the ADF7024, or for applications where some form of frequency correction is implemented on the transmit and receive devices.

LOW POWER MODES

The ADF7024 can be configured to operate in a broad range of energy sensitive applications where battery lifetime is critical. This range includes support for applications in which the ADF7024 is required to operate in a fully autonomous mode, or applications in which the host processor controls the transceiver during low power mode operation. These low power modes are implemented using a hardware wake-up controller (WUC), a firmware timer, and the smart wake mode functionality. The hardware WUC is a low power WUC that comprises a 16-bit wake-up timer with a programmable prescaler. The 32.768 kHz RC oscillator (RC OSC) provides the clock source for the timer.

The firmware timer is a software timer residing on the ADF7024. The firmware timer is used to count the number of WUC timeouts and can be used to count the number of ADF7024 wakeups. Therefore, the WUC and the firmware timer provide a real-time clock (RTC) capability.

The combination of the low power WUC, the firmware timer, and the smart wake modes (SWM) allows the ADF7024 to wake up autonomously from sleep without intervention from the host processor. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep, thereby dramatically reducing the overall system current consumption. The SWM can then wake the host processor on an interrupt condition. An overview of the various low power mode configurations is described in the following sections and as shown in Figure 18.

LOW POWER MODE DESCRIPTION

Deep Sleep Mode 2

Deep Sleep Mode 2 is suitable for applications in which the host processor controls the low power mode timing and the lowest possible ADF7024 sleep current is required.

In Deep Sleep Mode 2, the ADF7024 is in the PHY_SLEEP state. The contents of the configuration registers are not retained. Deep Sleep Mode 2 is entered by issuing the CMD_HW_RESET command from any radio state. To wake the device from the PHY_SLEEP state, the $\overline{CS}$ pin must be set low. After a CMD_HW_RESET command, the initialization routine must be followed, as detailed in the Radio Control section.

Deep Sleep Mode 1

Deep Sleep Mode 1 is suitable for applications in which the host processor controls the low power mode timing and the ADF7024 configuration is retained during the PHY_SLEEP state.

In Deep Sleep Mode 1, the ADF7024 is in the PHY_SLEEP state with the configuration registers retained. Before entering the PHY_SLEEP state, the WUC_RETAIN_CONFIGREG_EN bit (Address 0x30D) must be set to 1 to ensure that the configuration registers are retained. Deep sleep mode 1 is entered by issuing the CMD_PHY_SLEEP command from either the PHY_OFF or the PHY_ON state. To exit the PHY_SLEEP state, set the $\overline{CS}$ pin low and then follow the $\overline{CS}$ low initialization routine, as detailed in the Initialization section.

WUC Mode

In WUC low power mode, the hardware WUC is used to wake the ADF7024 from the PHY_SLEEP state after a user defined duration. At the end of this period, the ADF7024 provides an interrupt to the host processor. While the ADF7024 is in the PHY_SLEEP state, the host processor can optionally be in a deep sleep state to save power.

Before issuing the CMD_PHY_SLEEP command, the host processor must configure the WUC and set the firmware timer threshold to zero (SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_x = 0, Address 0x104 and Address 0x105). The WUC_RETAIN_CONFIGREG_EN (Address 0x30D, Bit 3) must be set to 1 to ensure that the configuration registers are retained. When the CMD_PHY_ SLEEP command is issued, the device goes to sleep for a period until the hardware timer times out. At this point, the device wakes up, and, if the WUC_TIMEOUT bit (Address 0x101, Bit 4) or the INTERRUPT_NUM_WAKEUPS bit (Address 0x100, Bit 7) interrupts are enabled, the device asserts the IRQ_GP3 pin.

The operation of the WUC low power mode is illustrated in Figure 18 and the timing is illustrated in Figure 19.

WUC Mode with Firmware Timer

In WUC mode with firmware timer, the WUC is used to periodically wake the ADF7024 from the PHY_SLEEP state, and the firmware timer is used to count the number of wakeups. The combination of the WUC and the firmware timer provides an RTC capability.

The host processor must set up the WUC and the firmware timer before entering the PHY_SLEEP state. The WUC_RETAIN_CONFIGREG_EN bit (Address 0x30D, Bit 3) must be set to 1 to ensure that the configuration register memory is retained. The WUC can be configured to time out at a specific time interval (for example, 1 sec, 60 sec). When the CMD_PHY_SLEEP command is issued, the device enters the PHY_SLEEP state for a period until the hardware timer times out. At this point, the device wakes up, increments the 16-bit firmware timer (NUMBER_OF_WAKEUPS_x, Address 0x102 and Address 0x103) and, if the WUC_TIMEOUT bit (Address 0x101, Bit 4) is enabled, the device asserts the IRQ_GP3 pin. If the 16-bit firmware count is less than or equal to the user set threshold (NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_x, Address 0x104 and Address 0x105), the device returns to the PHY_SLEEP state. With this method, the firmware count (NUMBER_OF_WAKEUPS_x) equates to a real-time interval.

When the firmware count exceeds the user set threshold (NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_x), if the INTERRUPT_NUM_WAKEUPS bit (Address 0x100, Bit 7) is set, the ADF7024 asserts the IRQ_GP3 pin and enters the PHY_OFF state. The operation of WUC mode with firmware timer is illustrated in Figure 18 and the timing is illustrated in Figure 20.

Smart Wake Mode with Autonomous Carrier Sense

In smart wake mode with autonomous carrier sense, the WUC, firmware timer, and smart wake mode are used to implement periodic RSSI measurements on a particular channel (carrier sense). To enable this low power mode, the WUC and firmware timer must be configured before entering the PHY_SLEEP state. The WUC_RETAIN_CONFIGREG_EN bit (Address 0x30D) must be set to 1 to ensure that the configuration register memory is retained. The RSSI measurement is enabled by setting the SWM_RSSI_QUAL bit = 1 and the SWM_EN bit = 1 (Address 0x11A). The INTERRUPT_SWM_RSSI_DET bit (Address 0x100) must also be enabled. If the measured RSSI value is below the user defined threshold set in the SWM_RSSI_THRESH register (Address 0x108), the device returns to the PHY_SLEEP state. If the RSSI measurement is greater than the SWM_RSSI_THRESH value, the device sets the INTERRUPT_SWM_RSSI_DET interrupt to alert the host processor and remains in the PHY_RX state looking for the preamble or waiting for a host command. The operation of smart wake mode with autonomous carrier sense is illustrated in Figure 18 and the timing is illustrated in Figure 21.

Smart Wake Mode with Autonomous Packet Reception

In smart wake mode with autonomous packet reception, the WUC, firmware timer, and smart wake mode are employed to periodically listen for packets. To enable this low power mode, the WUC and firmware timer must be configured and the smart wake mode (SWM) enabled (the SWM_EN bit [Bit 7], Address 0x11A) before entering the PHY_SLEEP state. The WUC_RETAIN_CONFIGREG_EN bit (Address 0x30D, Bit 3) must be set to 1 to ensure that the configuration register memory is retained. RSSI prequalification can be optionally enabled (SWM_RSSI_QUAL = 1, Address 0x11A, Bit 5). When RSSI prequalification is enabled, the ADF7024 begins searching for the preamble only if the RSSI measurement is greater than the user defined threshold.

The ADF7024 is in the PHY_RX state for a duration determined by the SWM_RX_DWELL_TIME setting (Address 0x106). If the ADF7024 detects the preamble during the receive dwell time, it searches for the sync word. If the sync word routine is detected, the ADF7024 loads the received data to the packet RAM and checks for a CRC, if enabled. If any of the receive packet interrupts is set, the ADF7024 returns to the PHY_ON state and waits for a host command.

If the ADF7024 receives preamble detection during the receive dwell time, but the remainder of the received packet extends beyond the dwell time, the ADF7024 extends the dwell time until all of the packet is received or the packet is recognized as invalid (for example, there is an incorrect sync word).

Smart wake mode with autonomous packet reception terminates when a valid packet interrupt is received. Alternatively, this low power mode can be terminated via a firmware timer timeout. The firmware timeout can be useful if certain radio tasks (for example, IR calibration) or processor tasks must be run periodically while in the low power mode.

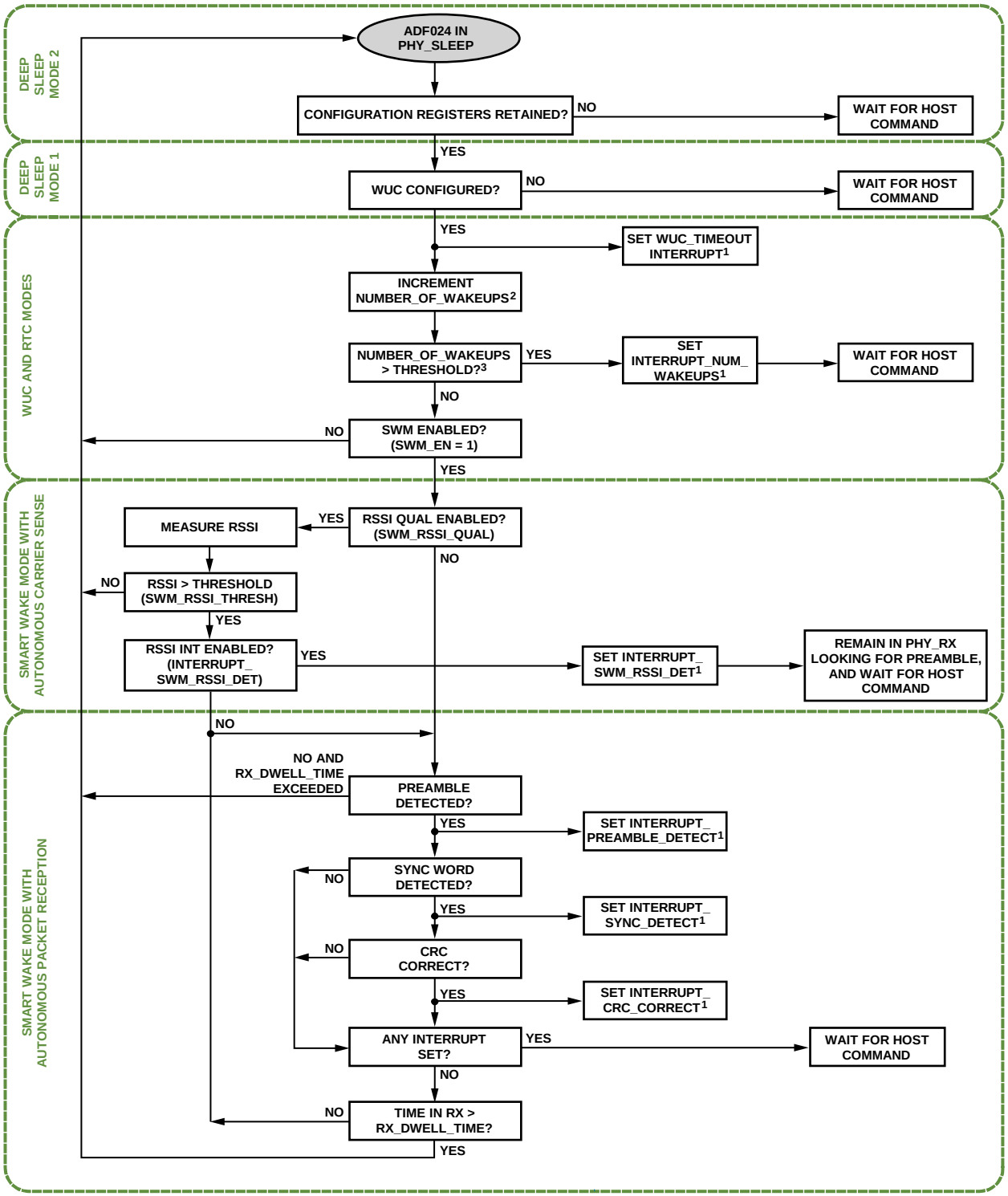
The operation of the smart wake mode with autonomous packet reception is illustrated in Figure 18 and the timing is illustrated in Figure 22.

Exiting Low Power Mode

As described in Figure 18, the ADF7024 waits for a host command on any of the termination conditions of the low power mode. It is also possible to perform an asynchronous exit from low power mode by completing the following steps:

1. Bring the $\overline{\text{CS}}$ pin of the SPI low and wait until the MISO output goes high.
2. Issue a CMD_HW_RESET command.

After a CMD_HW_RESET command, the host processor must follow the initialization procedure, as described in the Initialization section.



[1]AN INTERRUPT IS ONLY SET IF IT IS ENABLED IN THE INTERRUPT MASK REGISTER.
[2]NUMBER_OF_WAKEUPS[15:0] IS SPREAD ACROSS TWO REGISTERS: SWM_NUMBER_OF_WAKEUPS_0 AND SWM_NUMBER_OF_WAKEUPS_1.
[3]NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[15:0] IS SPREAD ACROSS TWO REGISTERS: SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_0 AND SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_1.

Figure 18. Low Power Mode Operation

LOW POWER MODE TIMING DIAGRAMS

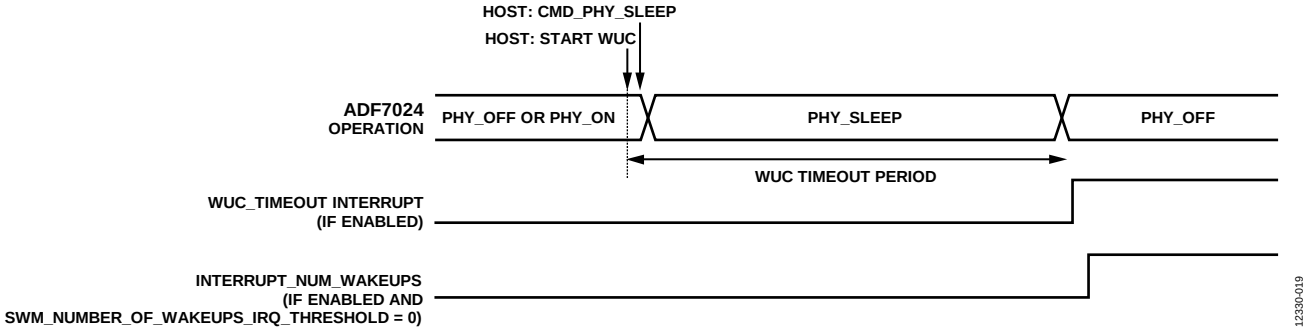


Figure 19. Low Power Mode Timing When Using the WUC

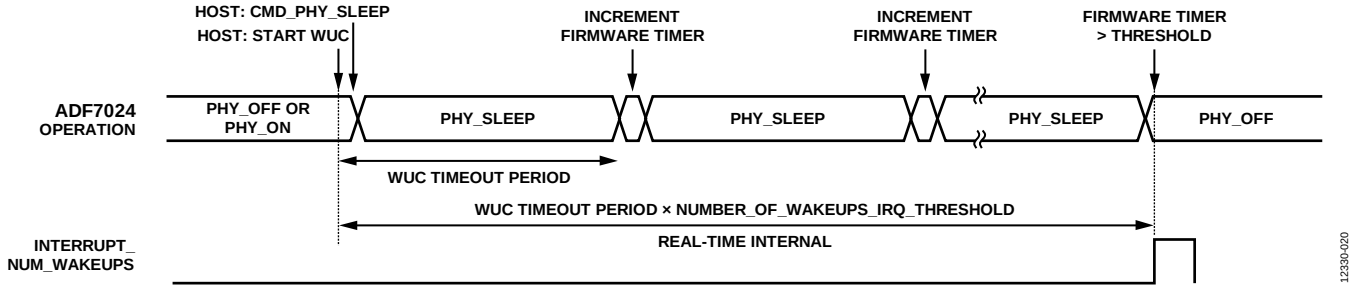


Figure 20. Low Power Mode Timing When Using the WUC and the Firmware Timer

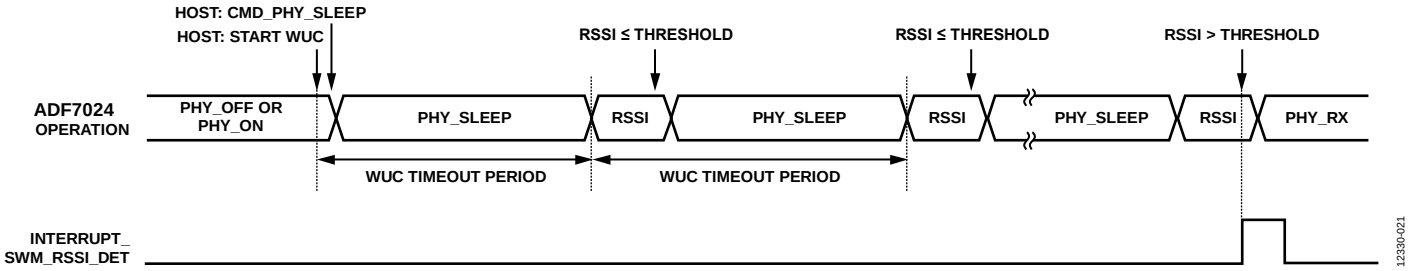


Figure 21. Low Power Mode Timing When Using the WUC, Firmware Timer, and SWM with Carrier Sense –

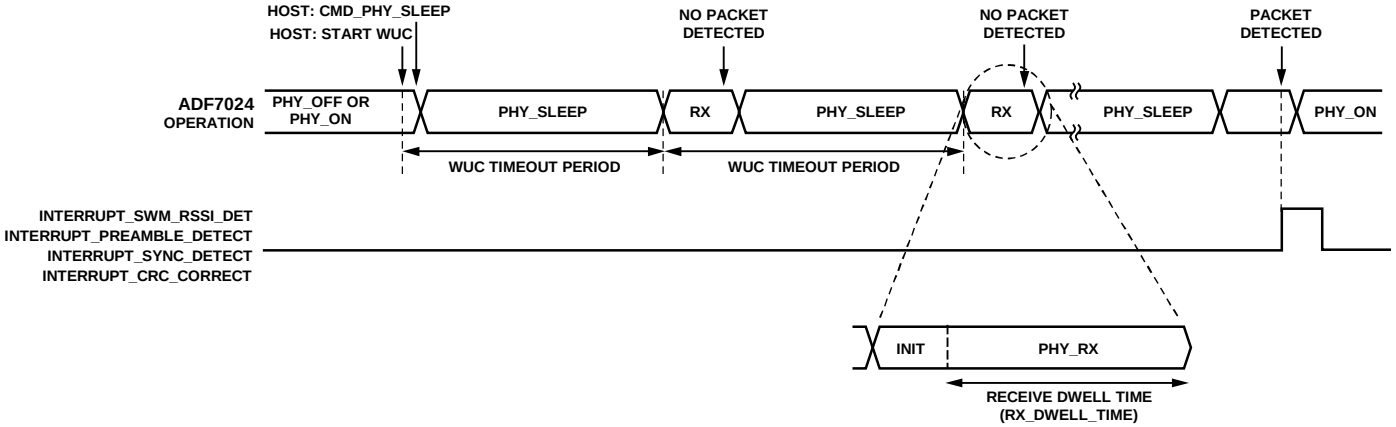


Figure 22. Low Power Mode Timing When Using the WUC, Firmware Timer, and SWM with Packet Reception

WUC SETUP

Circuit Description

The ADF7024 features a low power wake-up controller comprising a 16-bit wake-up timer with a 3-bit programmable prescaler, as shown in Figure 23. The prescaler clock source can be configured to use the 32.76 kHz internal RC oscillator (RC OSC). This combination of a programmable prescaler and a 16-bit down counter gives a total hardware timer range of 30.52 µs to 36.4 hours.

Configuration and Operation

The hardware WUC is configured via the following registers. The relevant fields of each register are detailed in the Auxiliary Registers Description section. All four of these registers are write only.

- WUC_CONFIG_HIGH (Address 0x30C)
- WUC_CONFIG_LOW (Address 0x30D)
- WUC_VALUE_HIGH (Address 0x30E)
- WUC_VALUE_LOW (Address 0x30F)

Configure the WUC as follows:

1. Clear all active interrupts by writing a Logic 1 to the bits that are high in the INTERRUPT_SOURCE_0 Register (Address 0x100) or the INTERRUPT_SOURCE_1 Register (Address 0x101).
2. Enable the required interrupts by writing a Logic 1 to the relevant bits of the INTERRUPT_MASK_0 Register (Address 0x100) or the INTERRUPT_MASK_1 Register (Address 0x101).
3. Write to WUC_CONFIG_HIGH and WUC_CONFIG_ LOW. Ensure that the WUC_ARM bit (Address 0x30D, Bit 0) = 1. Ensure that the WUC_RETAIN_CONFIGREG_EN bit (Address 0x30D, Bit 3) = 1 (retain the configuration registers during PHY_SLEEP). It is necessary to write to both registers in the following order: WUC_CONFIG_HIGH directly followed by WUC_CONFIG_LOW.
4. Write to WUC_VALUE_HIGH and then to WUC_VALUE_LOW. This write order configures the WUC_TIMER_VALUE[15:0] and, therefore, the WUC timeout period. The timer begins counting from the configured value after both of these registers are written to.

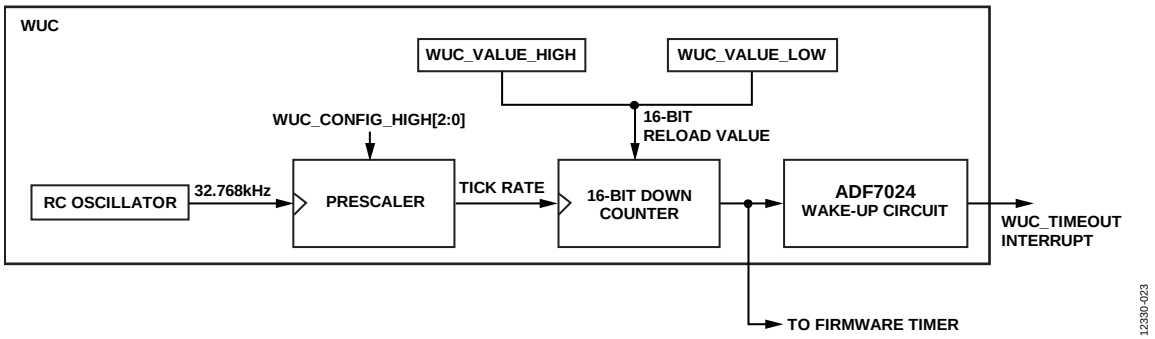


Figure 23. Hardware Wake-Up Controller (WUC)

FIRMWARE TIMER SETUP

The ADF7024 wakes up from the PHY_SLEEP state at the rate set by the WUC. A firmware timer is used to count the number of hardware wakeups and to generate an interrupt to the host processor. Therefore, the ADF7024 can be used to handle the wake-up timing of the host processor, reducing the overall system power consumption.

To set up the firmware timer, the host processor must set a value in the SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD registers (Address 0x104 and Address 0x105). This 16-bit value represents the number of times the device wakes up before it interrupts the host processor. At each wakeup, the ADF7024 increments the NUMBER_OF_WAKEUPS[15:0] registers (Address 0x102 and Address 103). If this value exceeds the value set by NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[15:0], the NUMBER_OF_WAKEUPS[15:0] value is cleared to 0. At this time, if the INTERRUPT_NUM_WAKEUPS bit (Bit 7) in the INTERRUPT_MASK_0 register (Address 0x100) is set, the device asserts the IRQ_GP3 pin and enters the PHY_OFF state.

CALIBRATING THE RC OSCILLATOR

Calibration of the 32.768 kHz RC oscillator requires two calibration routines; coarse calibration and fine calibration.

The coarse calibration is required for initial frequency centering of the oscillator. This coarse calibration can be executed as a one time factory calibration, with the result stored in the nonvolatile memory of the host processor for subsequent writing to the RCOSC_COARSE_CAL_VALUE (Bits[6:3]) in register WUC_CONFIG_HIGH (Address 0x30C), before initiating a fine calibration. Alternatively, the host processor can perform the coarse calibration routine after events such as initial system power-up and battery replacement. When the result is written to RCOSC_COARSE_CAL_VALUE, it is retained in low power modes and remains valid while the device is powered up, unless the host processor overwrites the register or a CMD_HW_RESET is issued. However, updates to the WUC_CONFIG_HIGH register become effective only after the WUC_CONFIG_LOW register is written to.

To meet the RC oscillator frequency accuracy specified in the ADF7024 data sheet, it is necessary to perform a coarse calibration of the RC oscillator.

A fine calibration is automatically performed after wakeup from PHY_SLEEP and after a cold start, but the calibration can also be initiated manually by the host processor. After a cold start, if a coarse calibration was previously performed, the RCOSC_COARSE_CAL_VALUE must be restored to WUC_CONFIG_HIGH (Address 0x30C), and a fine calibration must be initiated. Otherwise, a full coarse calibration, followed by a fine calibration must be performed. Prior to initiating either a coarse or fine calibration, it is necessary to check that the WUC_RCOSC_CAL_READY bit (Bit 5) in the WUC_STATUS register (Address 0x311) is equal to 1.

Performing a Fine Calibration of the RC Oscillator

To perform the fine calibration of the RC oscillator, take the following steps:

1. Write to the WUC_CONFIG_HIGH and WUC_CONFIG_LOW registers, setting the WUC_RCOSC_EN bit (Bit 6) high.
2. Write a 0 to WUC_RCOSC_CAL_EN (Bit 6) in the WUC_FLAG_RESET register.
3. Write a 1 to WUC_RCOSC_CAL_EN (Bit 6) in the WUC_FLAG_RESET register.

During calibration, the host microprocessor can write to and read from memory locations and issue commands to the ADF7024. The RC oscillator calibration status can be viewed in the WUC_STATUS register (Address 0x311).

A fine calibration typically takes 1.5 ms. The result of a fine calibration can be read back from the following two registers: RCOSC_CAL_READBACK_HIGH (Address 0x34F) and RCOSC_CAL_READBACK_LOW (Address 0x350).

Performing a Coarse Calibration of the RC Oscillator

Coarse calibration involves performing fine calibrations of the RC oscillator for different values of the RCOSC_COARSE_CAL_VALUE bits (Address 0x30C, Bits[6:3]) to determine the optimum value to be written to the WUC_CONFIG_HIGH register (Address 0x30C, Bits[6:3]).

The coarse calibration procedure is outlined in Figure 24. Typically, the optimum coarse tune state is State 5; therefore, the algorithm starts in State 5 to minimize the number of iterations.

The optimum RCOSC_COARSE_CAL_VALUE (Address 0x30C, Bits[6:3]) is usually determined once at 25°C, and the result is stored in the host processor. This result can be incorporated in the value written to the WUC_CONFIG_HIGH (Address 0x30C), prior to the fine calibrations of the RC oscillator.

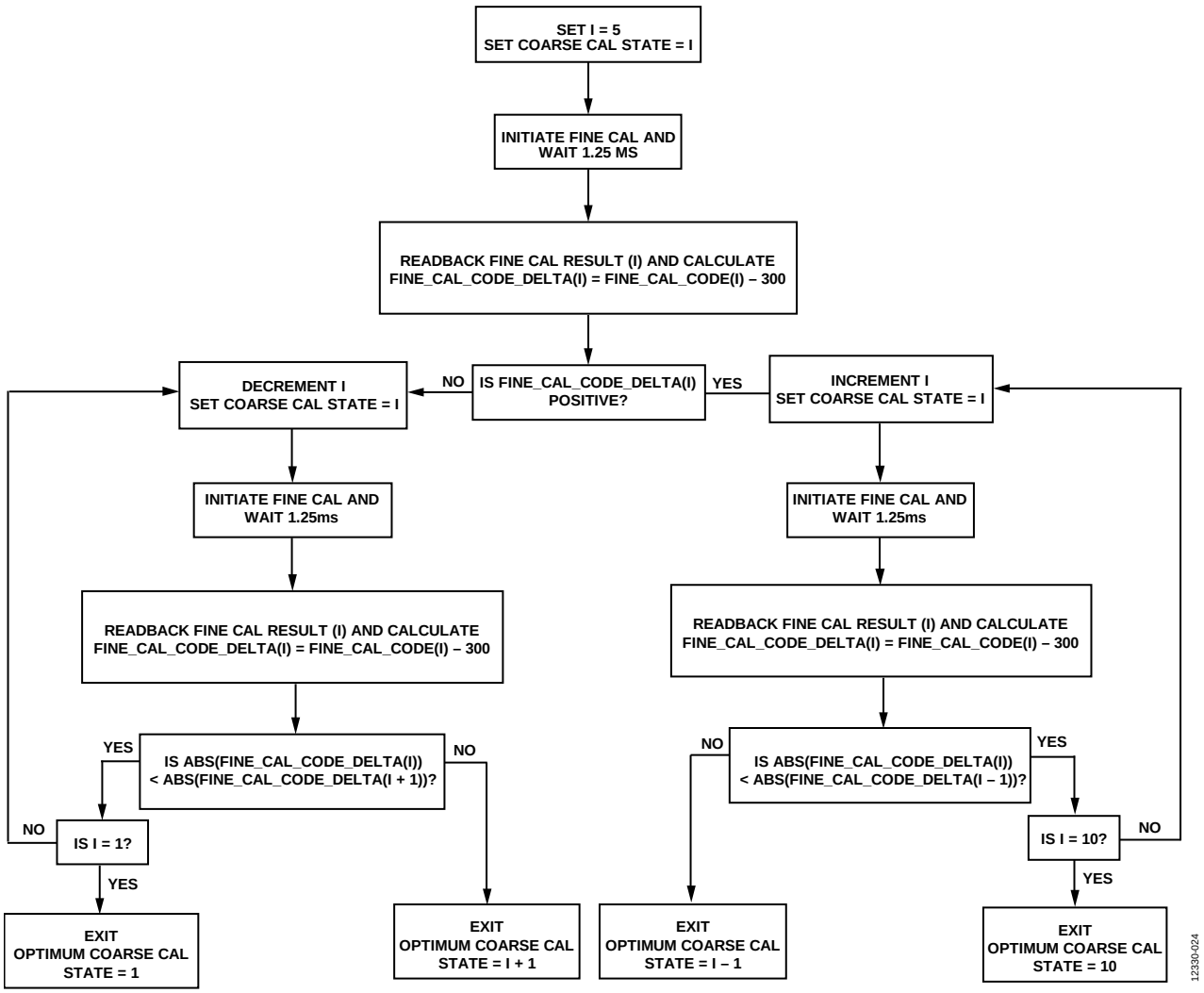


Figure 24. RC Oscillator Coarse Calibration Algorithm

DOWNLOADABLE FIRMWARE MODULES

The program RAM memory of the ADF7024 is used to store firmware modules that provide the ADF7024 with extra functionality. The binary code for firmware modules and details on their functionality are available from Analog Devices. The image rejection calibration firmware module is briefly described in this section. The firmware module is available online at ftp://ftp.analog.com/pub/RFL/FirmwareModules/ADF7024.

WRITING A MODULE TO PROGRAM RAM

The sequence to write a firmware module to program RAM is as follows:

1. Ensure that the ADF7024 is in PHY_OFF.
2. Issue the CMD_RAM_LOAD_INIT command.
3. Write the module to the program RAM using an SPI memory block write (see the Memory Access section).
4. Issue the CMD_RAM_LOAD_DONE command.
5. Poll the ADF7024 status word by issuing SPI_NOP commands and wait for CMD_READY = 1 in the status word.

The firmware module is now stored on the program RAM.

IMAGE REJECTION CALIBRATION MODULE

The calibration system initially disables the ADF7024 receiver, and an internal RF source is applied to the RF input at the image frequency. The algorithm then maximizes the receiver image rejection performance by repeatedly minimizing the quadrature gain and phase errors in the IF filter.

The calibration algorithm takes its initial estimates for quadrature phase correction and quadrature gain correction from the configuration registers, RADIO_IMAGE_REJECT_CAL_PHASE (Address 0x118) and RADIO_IMAGE_REJECT_CAL_AMPLITUDE (Address 0x119). After calibration, new optimum values of phase and gain are loaded back into these locations. These calibration values are maintained in the configuration registers during sleep mode and are automatically reapplied after a wake-up event, which keeps the number of calibrations required to a minimum. Configuring nonzero values for the gain and phase correction in the configuration registers has the disadvantage of causing a small degradation in the receiver sensitivity. The degradation is typically <1 dB.

Depending on the initial values of quadrature gain and phase correction, the calibration algorithm can take approximately 20 ms to find the optimum image rejection performance. However, the calibration time can be significantly less than 20 ms when the seed values used for gain and phase correction are close to optimum.

The image rejection performance is also dependent on temperature. To maintain optimum image rejection performance, a calibration must be activated whenever a temperature change of more than 10°C occurs. The ADF7024 on-chip temperature sensor can be used to determine when the temperature exceeds this limit.

To run the IR calibration, issue a CMD_IR_CAL. For the IR calibration to work successfully, ensure that the baseband filter calibration is enabled in the RADIO_CONTROL register (Address 0x11A).

PERIPHERAL FEATURES

ANALOG-TO-DIGITAL CONVERTER

The ADF7024 features an integrated SAR ADC for the digitization of analog signals that include the analog temperature sensor, the analog RSSI level, and an external analog input signal (Pin 30). The conversion time is typically 1 µs. The result of the conversion can be read from the ADC_READBACK_HIGH register (Address 0x327), and the ADC_READBACK_LOW register (Address 0x328). The ADC readback is an 8-bit value.

The signal source for the ADC input is selected via the ADC_CONFIG_LOW register (Address 0x359). In the PHY_RX state, the source is automatically set to the analog RSSI. The ADC is automatically enabled in PHY_RX. In other radio states, the host processor must enable the ADC by setting POWERDOWN_RX (Address 0x324) = 0x10.

To perform an ADC readback, complete the following steps:

1. Read ADC_READBACK_HIGH to initialize an ADC readback.
2. Read ADC_READBACK_LOW to return the ADC_READBACK[1:0] of the ADC sample.
3. Read ADC_READBACK_HIGH to return the ADC_READBACK[7:2] of the ADC sample.

TEMPERATURE SENSOR

The integrated temperature sensor has an operating range between −40°C and +85°C. To enable readback of the temperature sensor in PHY_OFF, PHY_ON, or PHY_TX, the following registers must be set:

1. Set POWERDOWN_RX (Address 0x324) = 0x10 to enable the ADC.
2. Set POWERDOWN_AUX (Address 0x325) = 0x02 to enable the temperature sensor.
3. Set ADC_CONFIG_LOW (Address 0x359) = 0x08 to set the ADC input to the temperature sensor.

The temperature is determined from the ADC readback value using the following formula:

$$Temperature\ (°C) = 0.9474 \times (ADC\_READBACK[7:0] - CalibrationValue[7:0]) + T_{CALIBRATION}$$

The calibration value[7:0] is determined via an ADC readback at a single known temperature, $T_{CALIBRATION}$.

TEST MODES TO SUPPORT EVALUATION

The ADF7024 has several test modes that can simplify the evaluation and debugging of applications utilizing the ADF7024.

TRANSMIT TEST MODES

There are several transmit test modes that are enabled by setting the VAR_TX_MODE parameter (Address 0x00D in the auxiliary RAM memory), as described in Table 26. To enable this test mode, complete the following steps:

1. Ensure that the configuration registers are configured in PHY_OFF and that the CMD_CONFIG_DEV command is issued.
2. Go to PHY_ON by issuing the CMD_PHY_ON command.
3. Set VAR_TX_MODE as described in Table 26. VAR_TX_MODE is contained in the packet RAM memory. The SPI_MEM_WR command for writing to this memory is 0x18.
4. Go to PHY_TX by issuing the CMD_PHY_TX command. The ADF7024 now remains in PHY_TX in the configured test mode.
5. To exit the test mode, return to PHY_ON by issuing the CMD_PHY_ON command and set VAR_TX_MODE = 0.

Table 26. Transmit Test Modes

VAR_TX_MODE (Address 0x00D in Auxiliary RAM Memory)	Mode
0	Default; no transmit test mode
1	Transmit random data (PN9) continuously
2	Transmit the preamble continuously
3	Transmit the carrier continuously
4 to 255	Reserved

RECEIVE TEST MODES

For the purpose of receiver bit error rate measurement, the ADF7024 provides a test mode to map the receive data and the receive clock to external pins. The receive data is available on the GP0 pin, and the receive clock is available on the GP2 pin. To enable this test mode, complete the following steps:

1. Ensure that the configuration registers are configured in PHY_OFF and that the CMD_CONFIG_DEV command is issued.
2. Go to PHY_ON by issuing the CMD_PHY_ON command.
3. Set GPIO_CONFIGURE = 0xA0 (Address 0x3FA) and DATA_MODE = 1 (in register PKT_LENGTH_CONTROL, Address 0x126)
4. Go to PHY_RX by issuing the CMD_PHY_RX command. The receive data and the receive data clock are now available on the GP0 and GP2 pins, respectively. The receive data is valid on the negative edge of the receive data clock.

To return to normal operation, return to PHY_ON and set GPIO_CONFIGURE = 0x00 and DATA_MODE = 0.

EMBEDDED PER TEST MODE

The ADF7024 features an embedded packet error rate (PER) function that, when configured, runs autonomously. Up to 65,535 packets can be transmitted, with a programmable delay between packets. The packet stored in the packet RAM is transmitted each time. If the cyclic redundancy check (CRC) is correct, the receiver determines that it has correctly received a packet.

The PER test is controlled from the PKT_TESTMODES register (Address 0x139), as defined in Table 27.

When the PER test mode is enabled, some of the packet RAM locations take on a new function, as shown in Table 28. Therefore, these locations are no longer available for packet data. When PER test mode is disabled, these locations are again available for packet data. Packet RAM locations 0x20 to 0xFF are available for packet data in the PER test. Bytes 0x00 to 0x1F are allocated for use by the ADF7024 and must not be used for packet data.

Registers Used with Embedded PER Test

Table 27. Address 0x139: PKT_TESTMODES Register Used with Embedded PER Tests

Bit	Name	R/W	Description
3	PER_IRQ_SELF_CLEAR	R/W	1: automatic clear of INTERRUPT_TX_EOF in transmit and INTERRUPT_CRC_CORRECT in receive 0: normal operation
2	PER_ENABLE	R/W	1: packet error rate test enabled 0: packet error rate test disabled
1	CONTINUOUS_TX	R/W	1: restart Tx after transmitting a packet 0: normal end of Tx
0	CONTINUOUS_RX	R/W	1: restart Rx after receiving a packet 0: normal end of Rx

Table 28. PER Test Settings in Packet RAM Memory

Address (Hex)	Normal Operation	PER Test Mode Operation	Description
0x011	Available for packet data	PER_COUNT_LOW	Bits[7:0] of PER_COUNT[15:0] (PER_COUNT increments in Rx and decrements in Tx).
0x012	Available for packet data	PER_COUNT_HIGH	Bits[15:8] of PER_COUNT[15:0] (PER_COUNT increments in Rx and decrements in Tx).
0x013	Available for packet data	PER_TX_WAIT_TIME	In Tx, delay between packets transmitted, in units of 10 µs.

Receiver PER Setup

To configure the ADF7024 as the receiver in a PER test, complete the following steps:

1. Ensure that the configuration registers are configured in PHY_OFF and that the CMD_CONFIG_DEV command is issued.
2. Go to PHY_ON by issuing the CMD_PHY_ON command.
3. Set PER_COUNT[15:0] = 0x0000 (Address 0x011, PER_COUNT_LOW[7:0] and Address 0x012, PER_COUNT_HIGH[7:0]) This setting initializes the PER counter to zero.
4. Set PER_IRQ_SELF_CLEAR = 1, PER_ENABLE = 1, and CONTINUOUS_RX = 1 (all in Register PKT_TESTMDOES, Address 0x139).
5. Go to PHY_RX by issuing the CMD_PHY_RX command.

The ADF7024 is now configured in PHY_RX for a PER test. Each time a valid packet (CRC correct) is received, the PER_COUNT registers are incremented, the CRC interrupt is cleared, and Rx restarts.

When testing is finished, PER_COUNT[15:0] (Address 0x011, PER_COUNT_LOW[7:0] and (Address 0x012, PER_COUNT_HIGH[7:0]) holds the number of received packets (correct CRCs).

Transmitter PER Setup

To configure the ADF7024 as the transmitter in a PER test, complete the following steps:

1. Ensure that the configuration registers are configured in PHY_OFF and that the CMD_CONFIG_DEV command is issued.
2. Go to PHY_ON by issuing the CMD_PHY_ON command.
3. Set PER_COUNT[15:0] equal to the desired number of transmit packets − 1.
4. Set PER_IRQ_SELF_CLEAR = 1, PER_ENABLE = 1 and CONTINUOUS_TX = 1 (all in register PKT_TESTMODES, Address 0x139).
5. Set PER_TX_WAIT_TIME (Address 0x013) to define the delay between packets in units of 10 µs. This delay is in addition to the PHY_TX to PHY_TX state transition time (see Table 14). The interpacket duration for a nonzero value in PER_TX_WAIT_TIME is, therefore, as follows:

   Interpacket Duration = (*PHY_TX to PHY_TX State Transition Ti*me) + *PER_TX_WAIT_TIME* × 10 µs

6. Go to PHY_TX by issuing the CMD_PHY_RX command.

The ADF7024 is now configured to be the transmitter in a PER test. After every TX_EOF interrupt, the PER_COUNT is decremented, the TX_EOF interrupt is cleared, and the Tx restarts after the interpacket duration. When PER_COUNT reaches zero, CONTINUOUS_TX (Bit 1 of PKT_TESTMODES) is cleared and packet transmission terminates.

Test Outcome

By comparing the number of packets received (PER_COUNT in the receiving device) with the number of packets transmitted (initial PER_COUNT + 1 in the transmitting device), the user can easily deduce the PER and the link quality.

APPLICATIONS INFORMATION

APPLICATION CIRCUIT

A typical application circuit for the ADF7024 is shown in Figure 25. All external components required for operation of the device, excluding supply decoupling capacitors, are shown. This example circuit uses a combined transmit and receive match. The bottom of the LFCSP package has an exposed pad that must be soldered to ground on the PCB. The component values for the matching and harmonic filtering are dependent on the RF frequency and the matching topology.

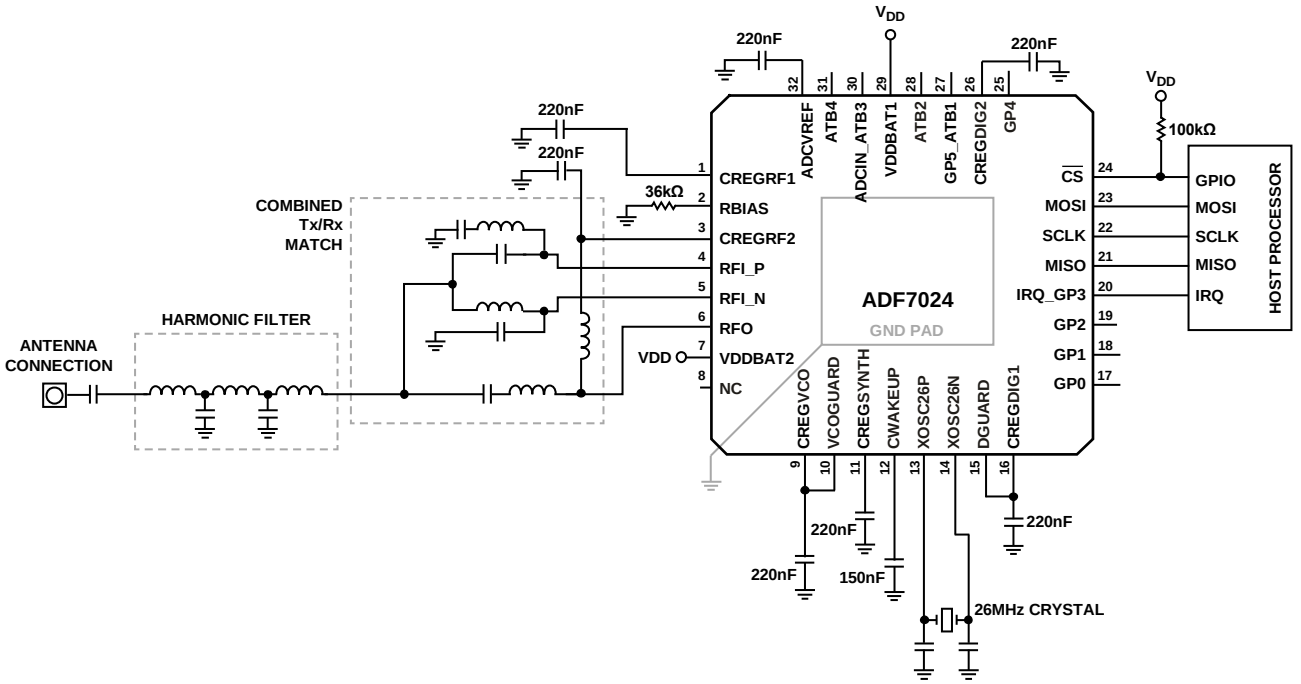


Figure 25. Typical ADF7024 Application Circuit Diagram

RF MATCHING

The ADF7024 exhibits optimum performance in terms of sensitivity, transmit power, and current consumption, only if its RF input and output ports are properly matched to the antenna impedance.

For cost-sensitive applications, the ADF7024 is equipped with an internal Tx/Rx switch that facilitates the use of a simple, combined, passive Tx/Rx matching network.

Alternatively, a separate Tx/Rx match can be used, in which case, an external RF switch can be used to switch the transmit and receive paths to the antenna. This separate Tx/Rx match yields slightly better receiver sensitivity and lower transmit power consumption in comparison with the combined match.

Combined Tx and Rx Match

The combined Tx and Rx match allows the transmit and receive paths to be combined without the use of an external transmit and receive switch. The matching network design is shown in Figure 26. The differential LNA match is a six element discrete balun with a single-ended input. The single-ended PA output is a three element match, consisting of the choke inductor to the CREGRF2 regulated supply and an inductor and capacitor series.

The LNA and PA paths are combined, and a fifth-order harmonic filter provides attenuation of the transmit harmonics. In a combined match, the off impedances of the PA and LNA must be considered. The off impedances can lead to a small loss in transmit power and degradation in receiver sensitivity in comparison with a separate single-ended PA and LNA match. However, with optimum matching, the typical loss in transmit power is <1 dB, and the degradation in sensitivity is <1 dB, when compared with the separate PA and LNA matching topology.

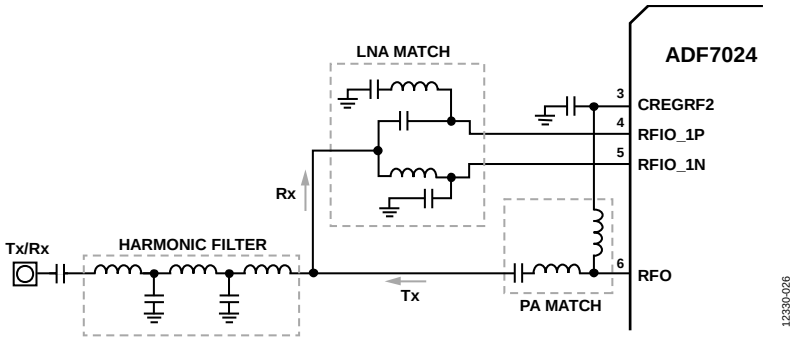


Figure 26. Combined Tx and Rx Match

Separate Tx and Rx Match

The separate PA and LNA matching configuration is shown in Figure 27. In designing this matching network, it is not necessary to consider the off impedances of the PA and LNA; therefore, achieving an optimum match is less complex than with the combined PA and LNA match. An external transmit and receive antenna switch (not shown in Figure 27) can be used to combine the transmit and receive paths to allow connection to an antenna.

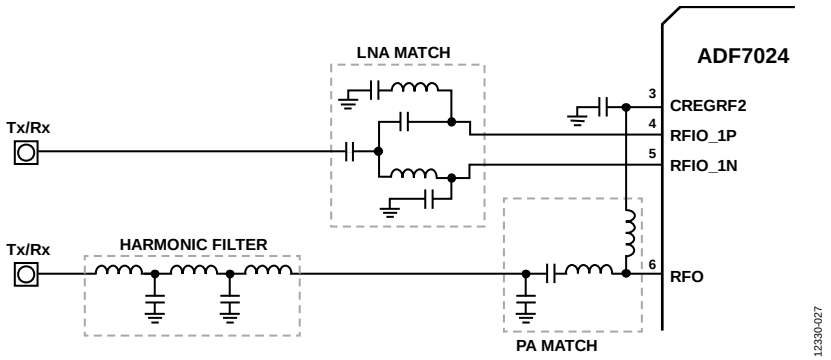


Figure 27. Separate Single-Ended PA and LNA Match

COMMAND REFERENCE

Table 29. Radio Control Commands

Command	Code	Description
CMD_PHY_OFF	0xB0	Performs a transition of the device into the PHY_OFF state
CMD_PHY_ON	0xB1	Performs a transition of the device into the PHY_ON state
CMD_PHY_RX	0xB2	Performs a transition of the device into the PHY_RX state
CMD_PHY_TX	0xB5	Performs a transition of the device into the PHY_TX state
CMD_PHY_SLEEP	0xBA	Performs a transition of the device into the PHY_SLEEP state
CMD_CONFIG_DEV	0xBB	Configures the radio, based on the configuration registers
CMD_GET_RSSI	0xBC	Performs an RSSI measurement
CMD_BB_CAL	0xBE	Performs a calibration of the IF filter
CMD_HW_RESET	0xC8	Performs a full hardware reset; device enters PHY_SLEEP state
CMD_RAM_LOAD_INIT	0xBF	Prepares the ADF7024 for a firmware module download
CMD_RAM_LOAD_DONE	0xC7	Performs a reset of the ADF7024 after download of a firmware module
CMD_IR_CAL[1]	0xBD	Initiates an image rejection calibration routine

[1] The image rejection calibration firmware module must be loaded to program RAM for this command to be functional.

Table 30. Memory Access Commands

Command	Code	Description
SPI_MEM_WR	00011xxxb = 0x18 (packet RAM, auxiliary RAM), 0x19 (configuration registers), 0x1B (auxiliary registers), and 0x1E (program RAM)	Writes data to any of the ADF7024 memory spaces sequentially. An 11-bit address is used to identify the memory locations. The most significant three bits of the address are incorporated into the command (xxxb). This command is followed by the remaining eight bits of the address, which are subsequently followed by the data bytes to be written.
SPI_MEM_RD	00111xxxb = 0x38 (packet RAM, auxiliary RAM), 0x39 (configuration registers), and 0x3B (auxiliary registers)	Reads data from the ADF7024 memory spaces sequentially. An 11-bit address is used to identify the memory locations. The most significant three bits of the address are incorporated into the command (xxxb). This command is followed by the remaining eight bits of the address, which are subsequently followed by the appropriate number of SPI_NOP commands.
SPI_MEMR_WR	00001xxxb = 0x08 (packet RAM, auxiliary RAM), 0x09 (configuration registers), and 0x0B (auxiliary registers)	Writes data to the ADF7024 memory spaces nonsequentially.
SPI_MEMR_RD	00101xxxb = 0x28 (packet RAM, auxiliary RAM), 0x29 (configuration registers), and 0x2B (auxiliary registers)	Reads data from the ADF7024 memory spaces nonsequentially.
SPI_NOP	0xFF	No operation. Use for dummy writes when polling the status word; used also as dummy data when performing a memory read.

REGISTER MAPS

Table 31. ADF7024 Configuration Registers

Address (Hex)	Register	Retained in PHY_SLEEP[1]	R/W
0x100	INTERRUPT_MASK_0	Yes	R/W
0x101	INTERRUPT_MASK_1	Yes	R/W
0x102	SWM_NUMBER_OF_WAKEUPS_0	Yes	R/W
0x103	SWM_NUMBER_OF_WAKEUPS_1	Yes	R/W
0x104	SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_0	Yes	R/W
0x105	SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_1	Yes	R/W
0x106	SWM_RX_DWELL_TIME	Yes	R/W
0x107	SWM_RX_DWELL_TICK	Yes	R/W
0x108	SWM_RSSI_THRESH	Yes	R/W
0x109	RADIO_CHANNEL_FREQ_0	Yes	R/W
0x10A	RADIO_CHANNEL_FREQ_1	Yes	R/W
0x10B	RADIO_CHANNEL_FREQ_2	Yes	R/W
0x10C	RADIO_PROFILE_0	Yes	R/W
0x10D	RADIO_PROFILE_1	Yes	R/W
0x10E	RADIO_PROFILE_2	Yes	R/W
0x10F	RADIO_PROFILE_3	Yes	R/W
0x110	RADIO_PROFILE_4	Yes	R/W
0x111	RADIO_PROFILE_5	Yes	R/W
0x112	RADIO_PROFILE_6	Yes	R/W
0x113	RADIO_AGC_MODE	Yes	R/W
0x114	RADIO_PA_RAMP	Yes	R/W
0x115	RADIO_PROFILE_7	Yes	R/W
0x116	RADIO_AFC_MODE	Yes	R/W
0x117	RADIO_PROFILE_8	Yes	R/W
0x118	RADIO_IMAGE_REJECT_CAL_PHASE	Yes	R/W
0x119	RADIO_IMAGE_REJECT_CAL_AMPLITUDE	Yes	R/W
0x11A	RADIO_CONTROL	Yes	R/W
0x11B	PKT_PREAMBLE_MATCH	Yes	R/W
0x11C	PKT_SYMBOL_MODE	Yes	R/W
0x11D	PKT_PREAMBLE_LEN	Yes	R/W
0x11E	PKT_CRC_POLY_0	Yes	R/W
0x11F	PKT_CRC_POLY_1	Yes	R/W
0x120	PKT_SYNC_CONTROL	Yes	R/W
0x121	PKT_SYNC_BYTE_0	Yes	R/W
0x122	PKT_SYNC_BYTE_1	Yes	R/W
0x123	PKT_SYNC_BYTE_2	Yes	R/W
0x124	PKT_TX_BASE_ADR	Yes	R/W
0x125	PKT_RX_BASE_ADR	Yes	R/W
0x126	PKT_LENGTH_CONTROL	Yes	R/W
0x127	PKT_LENGTH_MAX	Yes	R/W
0x128	RADIO_PROFILE_9	Yes	R/W
0x129	Reserved; set to 0x00	Yes	R/W
0x12A	Reserved; set to 0x00	Yes	R/W
0x12B	RADIO_PROFILE_10	Yes	R/W
0x12C	RADIO_PROFILE_11	Yes	R/W
0x12D	RADIO_PROFILE_12	Yes	R/W
0x12E	RADIO_PA_LEVEL	Yes	R/W
0x12F	RADIO_PROFILE_13	Yes	R/W
0x130	RADIO_PROFILE_14	Yes	R/W
0x131	RADIO_PROFILE_15	Yes	R/W

Address (Hex)	Register	Retained in PHY_SLEEP[1]	R/W
0x132	RADIO_PROFILE_16	Yes	R/W
0x133	RADIO_PROFILE_17	Yes	R/W
0x134	RADIO_PROFILE_18	Yes	R/W
0x135	RADIO_PROFILE_19	Yes	R/W
0x136	RADIO_PROFILE_20	Yes	R/W
0x137	RADIO_PROFILE_21	Yes	R/W
0x138	RADIO_PROFILE_22	Yes	R/W
0x139	PKT_TESTMODES	Yes	R/W
0x13A	Reserved; set to 0x04	Yes	R/W
0x13B	Reserved; set to 0x00	Yes	R/W
0x13C	Reserved; set to 0x00	Yes	R/W
0x13D	Reserved; set to 0x00	Yes	R/W
0x13E	Reserved; set to 0x00	Yes	R/W
0x13F	Reserved; set to 0x00	Yes	R/W

[1] Refer to the Low Power Modes section for details on how to ensure that this memory is retained in PHY_SLEEP.

Table 32. Auxiliary Registers

Address (Hex)	Register	Retained in PHY_SLEEP	R/W
0x30C	WUC_CONFIG_HIGH	No	W
0x30D	WUC_CONFIG_LOW	No	W
0x30E	WUC_VALUE_HIGH	No	W
0x30F	WUC_VALUE_LOW	No	W
0x310	WUC_FLAG_RESET	No	R/W
0x311	WUC_STATUS	No	R
0x312	RSSI_READBACK	No	R
0x319	IMAGE_REJECT_CAL_CONFIG	No	R/W
0x324	POWERDOWN_RX	No	R/W
0x325	POWERDOWN_AUX	No	R/W
0x327	ADC_READBACK_HIGH	No	R
0x328	ADC_READBACK_LOW	No	R
0x32D	BATTERY_MONITOR_THRESHOLD_VOLTAGE	No	R/W
0x32E	EXT_UC_CLK_DIVIDE	No	R/W
0x336	INTERRUPT_SOURCE_0	No	R/W
0x337	INTERRUPT_SOURCE_1	No	R/W
0x339	CALIBRATION_STATUS	No	R
0x345	RXBB_CAL_CALWRD_READBACK	No	R
0x34F	RCOSC_CAL_READBACK_HIGH	No	R
0x350	RCOSC_CAL_READBACK_LOW	No	R
0x359	ADC_CONFIG_LOW	No	R/W
0x35D	AGC_MODE	No	R/W
0x360	AGC_GAIN_STATUS	No	R
0x372	FREQUENCY_ERROR_READBACK	No	R
0x3D2	OSC_CONFIG	No	R/W
0x3F8	ANALOG_TEST_BUS	No	R/W
0x3F9	RSSI_TSTMUX_SEL	No	R/W
0x3FA	GPIO_CONFIGURE	No	R/W

Table 33. Auxiliary RAM Memory

Address	Register	Retained in PHY_SLEEP	R/W
0x000 to 0x00C	Reserved	No	R
0x00D	VAR_TX_MODE	No	R/W
0x00E to 0x00F	Reserved	No	R

Table 34. Packet RAM Memory under Normal Operation

Address	Memory Description	Retained in PHY_SLEEP	PER Test Mode Enabled[1]	R/W
0x010 to 0x0FF	Transmit and receive packet buffer	No	No	R/W

Table 35. Packet RAM Memory in PER Test Mode

Address	Memory Description	Retained in PHY_SLEEP	PER Test Mode Enabled[1]	R/W
0x010	Reserved	No	Yes	R/W
0x011	PER_COUNT_LOW	No	Yes	R/W
0x012	PER_COUNT_HIGH	No	Yes	R/W
0x013	PER_TX_WAIT_TIME	No	Yes	R/W
0x014 to 0x01F	Reserved	No	Yes	R/W
0x020 to 0x0FF	Transmit and receive packet buffer	No	Yes	R/W

[1] See the Embedded PER Test Mode section.

CONFIGURATION REGISTERS DESCRIPTION

The configuration registers can be written to in the PHY_OFF state only. After writing to the configuration registers, the command CMD_CONFIG_DEV must be issued to the ADF7024. When configuring the ADF7024 after a cold start, all 64 of the ADF7024 configuration registers must be written to.

Table 36. Address 0x100, Register INTERRUPT_MASK_0

Bit	Name	R/W	Description
[7]	INTERRUPT_NUM_WAKEUPS	R/W	Interrupt when the number of WUC wakeups (NUMBER_OF_WAKEUPS[15:0]) reaches the threshold (NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[15:0]). 1: interrupt enabled; 0: interrupt disabled.
[6]	INTERRUPT_SWM_RSSI_DET	R/W	Interrupt when the measured RSSI during smart wake mode exceeds the RSSI threshold value (SWM_RSSI_THRESH, Address 0x108). 1: interrupt enabled; 0: interrupt disabled.
[5]	Reserved	R/W	Set to 0.
[4]	INTERRUPT_TX_EOF	R/W	Interrupt when a packet finishes transmitting. 1: interrupt enabled; 0: interrupt disabled.
[3]	Reserved	R/W	Set to 0.
[2]	INTERRUPT_CRC_CORRECT	R/W	Interrupt when a received packet has the correct CRC. 1: interrupt enabled; 0: interrupt disabled.
[1]	INTERRUPT_SYNC_DETECT	R/W	Interrupt when a qualified sync word is detected in the received packet. 1: interrupt enabled; 0: interrupt disabled.
[0]	INTERRUPT_PREMABLE_DETECT	R/W	Interrupt when a qualified preamble is detected in the received packet. 1: interrupt enabled; 0: interrupt disabled.

Table 37. Address 0x101, Register INTERRUPT_MASK_1

Bit	Name	R/W	Description
[7]	BATTERY_ALARM	R/W	Interrupt when the battery voltage drops below the threshold value (BATTERY_MONITOR_THRESHOLD_VOLTAGE, Address 0x32D). 1: interrupt enabled; 0: interrupt disabled.
[6]	CMD_READY	R/W	Interrupt when the ADF7024 is ready to load a new command; mirrors the CMD_READY bit of the status word. 1: interrupt enabled; 0: interrupt disabled.
[5]	Reserved	R/W	Set to 0.
[4]	WUC_TIMEOUT	R/W	Interrupt when the WUC times out. 1: interrupt enabled; 0: interrupt disabled.
[3]	Reserved	R/W	Set to 0.
[2]	Reserved	R/W	Set to 0.
[1]	SPI_READY	R/W	Interrupt when the SPI is ready for access. 1: interrupt enabled; 0: interrupt disabled.
[0]	CMD_FINISHED	R/W	Interrupt when the ADF7024 finishes performing a command. 1: interrupt enabled; 0: interrupt disabled.

Table 38. Address 0x102, Register SWM_NUMBER_OF_WAKEUPS_0

Bit	Name	R/W	Description
[7:0]	NUMBER_OF_WAKEUPS[7:0]	R/W	Bits[7:0] of [15:0] of an internal 16-bit count of the number of wakeups (WUC timeouts) the device has gone through. NUMBER_OF_WAKEUPS[15:0] can be initialized to 0x0000.

Table 39. Address 0x103, Register SWM_NUMBER_OF_WAKEUPS_1

Bit	Name	R/W	Description
[7:0]	NUMBER_OF_WAKEUPS[15:8]	R/W	Bits[15:8] of [15:0] of an internal 16-bit count of the number of WUC wakeups the device has gone through. NUMBER_OF_WAKEUPS[15:0] can be initialized to 0x0000.

Table 40. Address 0x104, Register SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_0

Bit	Name	R/W	Description
[7:0]	NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[7:0]	R/W	Bits[7:0] of [15:0] (see Table 41). The threshold for the number of wakeups (WUC timeouts). The register value is a 16-bit count threshold that is compared against the NUMBER_OF_WAKEUPS parameter. When this threshold is exceeded, the device wakes up in the PHY_OFF state and optionally generates INTERRUPT_NUM_WAKEUPS.

Table 41. Address 0x105, Register SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_1

Bit	Name	R/W	Description
[7:0]	NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[15:8]	R/W	Bits[15:8] of [15:0] (see Table 40).

Table 42. Address 0x106, Register SWM_RX_DWELL_TIME

Bit	Name	R/W	Description
[7:0]	RX_DWELL_TIME	R/W	When the WUC is used and SWM is enabled, the radio powers up and enables the receiver on the channel defined in the configuration registers and listens for this time. If no preamble pattern is detected during this period, the device goes back to sleep. Receive Dwell Time (s) = *RX_DWELL_TIME/Rx Dwell Timer Tick Rate(Hz)* where the *Rx Dwell Timer Tick Rate* is defined by the RX_DWELL_TICK value in Register SWM_RX_DWELL_TICK (see Table 43).

Table 43. Address 0x107, Register SWM_RX_DWELL_TICK

Bit	Name	R/W	Description
[7:0]	RX_DWELL_TICK	R/W	Tick rate of the timer that controls the SWM receiver dwell time. $Rx\ Dwell\ Timer\ Tick\ Rate\ (\text{Hz}) = \frac{6.5\,\text{MHz}}{128 \times RX\_DWELL\_TICK}$ A value of 0x33 gives a tick rate of 995.7 Hz (timer period = 1.004 ms).

Table 44. Address 0x108, Register SWM_RSSI_THRESH

Bit	Name	R/W	Description
[7:0]	RSSI_THRESH	R/W	This register sets the RSSI threshold when in smart wake mode with RSSI detection enabled. $Threshold\ (\text{dBm}) = SWM\_RSSI\_THRESH - 107$

Table 45. Address 0x109, Register RADIO_CHANNEL_FREQ_0

Bit	Name	R/W	Description
[7:0]	CHANNEL_FREQ[7:0]	R/W	The RF channel frequency in hertz is set according to $Frequency\ (Hz) = f_{PFD} \times \frac{(RADIO\_CHANNEL\_FREQ[23:0])}{2^{16}}$ where f_{PFD} is the PFD frequency and is equal to 26 MHz.

Table 46. Address 0x10A, Register RADIO_CHANNEL_FREQ_1

Bit	Name	R/W	Description
[7:0]	CHANNEL_FREQ[15:8]	R/W	See the RADIO_CHANNEL_FREQ_0 description in Table 45.

Table 47. Address 0x10B, Register RADIO_CHANNEL_FREQ_2

Bit	Name	R/W	Description
[7:0]	CHANNEL_FREQ[23:16]	R/W	See the RADIO_CHANNEL_FREQ_0 description in Table 45.

Table 48. Address 0x10C, Register RADIO_PROFILE_0

Bit	Name	R/W	Description
[7:0]	RADIO_ PROFILE _0	R/W	This register is part of the radio profile. Refer to Table 11.

Table 49. Address 0x10D, Register RADIO_PROFILE_1

Bit	Name	R/W	Description
[7:0]	RADIO_ PROFILE _1	R/W	This register is part of the radio profile. Refer to Table 11.

Table 50. Address 0x10E, Register RADIO_PROFILE_2

Bit	Name	R/W	Description
[7:0]	RADIO_ PROFILE _2	R/W	This register is part of the radio profile. Refer to Table 11.

Table 51. Address 0x10F, Register RADIO_PROFILE_3

Bit	Name	R/W	Description
[7:0]	RADIO_ PROFILE _3	R/W	This register is part of the radio profile. Refer to Table 11.

Table 52. Address 0x110, Register RADIO_PROFILE_4

Bit	Name	R/W	Description
[7:0]	RADIO_ PROFILE _4	R/W	This register is part of the radio profile. Refer to Table 11.

Table 53. Address 0x111, Register RADIO_PROFILE_5

Bit	Name	R/W	Description
[7:0]	RADIO_ PROFILE _5	R/W	This register is part of the radio profile. Refer to Table 11.

Table 54. Address 0x112, Register RADIO_PROFILE_6

Bit	Name	R/W	Description
[7:0]	RADIO_ PROFILE _6	R/W	This register is part of the radio profile. Refer to Table 11.

Table 55. Address 0x113, Register RADIO_AGC_MODE

Bit	Name	R/W	Description
[7:6]	AGC_LOCK_MODE	R/W	This register configures the operation of the AGC. 0: AGC is free running while in PHY_RX. 1: Reserved. 2: Reserved. 3: The AGC locks after detection of the preamble (if preamble detection is enabled) or after detection of the sync word (if preamble detection is disabled). This setting is the recommended setting for most applications.
[5:0]	Reserved	R/W	Set to 0.

Table 56. Address 0x114, Register RADIO_PA_RAMP

Bit	Name	R/W	Description	
[7:3]	Reserved	R/W	Set to 0.	
[2:0]	PA_RAMP	R/W	This register sets the PA ramp rate. The PA ramps at the programmed rate until it reaches the level indicated by the PA_LEVEL (Address 0x12E, Bits[7:0]) setting. The ramp rate is configured as a certain number of PA level codes per data bit period.	
			PA_RAMP	**Ramp Rate (PA Level Codes per Transmit Data Bit)**
			0	Reserved
			1	256 codes per data bit
			2	128 codes per data bit
			3	64 codes per data bit
			4	32 codes per data bit
			5	16 codes per data bit
			6	8 codes per data bit
			7	4 codes per data bit
			An adequately long PA ramp rate is required, based on the data rate and the PA output power setting. Therefore, the PA_RAMP setting must be set so that $\text{Ramp Rate (Codes/Bit)} < 10^6 \times \frac{PA\_LEVEL}{Datarate \quad (bps)}$	

Table 57. Address 0x115, Register RADIO_PROFILE_7

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_7	R/W	This register is part of the radio profile. Refer to Table 11.

Table 58. Address 0x116, Register RADIO_AFC_MODE

Bit	Name	R/W	Description	
[7:5]	Reserved	R/W	Set to 0.	
[4]	Reserved	R/W	Set to 0.	
[3:2]	Reserved	R/W	Set to 2.	
[1:0]	AFC_LOCK_MODE	R/W	Sets the AFC mode.	
			AFC_LOCK_MODE	**Mode**
			0	Free running: AFC is free running.
			1	Disabled: AFC is disabled.
			2	Hold AFC: AFC is paused.
			3	Lock: AFC locks after the preamble or sync word (only locks on a sync word if PKT_PREAMBLE_MATCH = 0).

Table 59. Address 0x117, Register RADIO_PROFILE_8

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_8	R/W	This register is part of the radio profile. Refer to Table 11.

Table 60. Address 0x118, Register RADIO_IMAGE_REJECT_CAL_PHASE

Bit	Name	R/W	Description
[7]	Reserved	R/W	Set to 0.
[6:0]	IMAGE_REJECT_CAL_PHASE	R/W	This register sets the I/Q phase adjustment.

Table 61. Address 0x119, Register RADIO_IMAGE_REJECT_CAL_AMPLITUDE

Bit	Name	R/W	Description
[7]	Reserved	R/W	Set to 0.
[6:0]	IMAGE_REJECT_CAL_AMPLITUDE	R/W	This register sets the I/Q amplitude adjustment.

Table 62. Address 0x11A, Register RADIO_CONTROL

Bit	Name	R/W	Description
[7]	SWM_EN	R/W	1: Smart wake mode enabled. 0: Smart wake mode disabled.
[6]	BB_CAL	R/W	1: IF filter calibration enabled. 0: IF filter calibration disabled. If Bit 6 is set, IF filter calibration is automatically performed on the transition from the PHY_OFF state to the PHY_ON state.
[5]	SWM_RSSI_QUAL	R/W	1: RSSI qualify in smart wake mode enabled. 0: RSSI qualify in smart wake mode disabled.
[4]	TX_TO_RX_AUTO_TURNAROUND	R/W	If TX_TO_RX_AUTO_TURNAROUND = 1, the device automatically transitions to the PHY_RX state on the same RF channel frequency at the end of a packet transmission. If TX_TO_RX_AUTO_TURNAROUND = 0, this operation is disabled.
[3]	RX_TO_TX_AUTO_TURNAROUND	R/W	If RX_TO_TX_AUTO_TURNAROUND = 1, the device automatically transitions to the PHY_TX state on the same RF channel frequency at the end of a valid packet reception. If RX_TO_TX_AUTO_TURNAROUND = 0, this operation is disabled.
[2]	Reserved	R/W	Set to 0.
[1]	EXT_LNA_EN	R/W	1: external LNA control signal is enabled. The signal is logic high while the ADF7024 is in the PHY_RX state and is logic low while in any other nonsleep state. 0: external LNA control signal is disabled. The signal can be mapped to either the ATB2 (VDD logic output) or the ATB4 (1.8 V logic output) pin using the EXT_PA_LNA_ATB_CONFIG setting in Register PKT_TESTMODES (Address 0x139).
[0]	EXT_PA_EN	R/W	1: external PA control signal is enabled. The signal is logic high while the ADF7024 is in the PHY_TX state and is logic low while in any other nonsleep state. 0: external PA control signal is disabled. The signal can be mapped to either the GP5_ATB1 (VDD logic output) or the ADCIN_ATB3 (1.8 V logic output) pin using the EXT_PA_LNA_ATB_CONFIG setting in Register PKT_TESTMODES (Address 0x139).

Table 63. Address 0x11B, Register PKT_ PREAMBLE_MATCH

Bit	Name	R/W	Description	
[7:4]	Reserved	R/W	Set to 0.	
[3:0]	PREAMBLE_MATCH	R/W	**PREAMBLE_MATCH**	**Description**
			13 to 15	Reserved
			12	0 errors allowed
			11	One erroneous bit pair allowed in 12-bit pairs
			10	Two erroneous bit pairs allowed in 12-bit pairs
			9	Three erroneous bit pairs allowed in 12-bit pairs
			8	Four erroneous bit pairs allowed in 12-bit pairs
			1 to 7	Not recommended
			0	Preamble detection disabled

Table 64. Address 0x11C, Register PKT_SYMBOL_MODE

Bit	Name	R/W	Description
[7]	Reserved	R/W	Set to 0
[6]	MANCHESTER_ENC	R/W	1: Manchester encoding and decoding enabled 0: Manchester encoding and decoding disabled
[5]	Reserved	R/W	Set to 1
[4]	EIGHT_TEN_ENC	R/W	1: 8b/10b encoding and decoding enabled 0: 8b/10b encoding and decoding disabled
[3]	DATA_WHITENING	R/W	1: data whitening and dewhitening enabled 0: data whitening and dewhitening disabled
[2:0]	SYMBOL_LENGTH	R/W	1: If EIGHT_TEN_ENC = 1 0: If EIGHT_TEN_ENC = 0

Table 65. Address 0x11D, Register PKT_PREAMBLE_LEN

Bit	Name	R/W	Description
[7:0]	PREAMBLE_LEN	R/W	Length of preamble in bytes. Example: a Decimal 3 value results in a preamble of 24 bits.

Table 66. Address 0x11E, Register PKT_CRC_POLY_0

Bit	Name	R/W	Description
[7:0]	CRC_POLY[7:0]	R/W	Lower byte of CRC_POLY[15:0], which sets the CRC polynomial.

Table 67. Address 0x11F, Register PKT_CRC_POLY_1

Bit	Name	R/W	Description
[7:0]	CRC_POLY[15:8]	R/W	Upper byte of CRC_POLY[15:0], which sets the CRC polynomial. See the Packet Management section for more details on how to configure a CRC polynomial.

Table 68. Address 0x120, Register PKT_SYNC_CONTROL

Bit	Name	R/W	Description	
[7:6]	SYNC_ERROR_TOL	R/W	This register sets the sync word error tolerance in bits.	
			SYNC_ERROR_TOL	**Bit Error Tolerance**
			0	0 bit errors allowed.
			1	One bit error allowed.
			2	Two bit errors allowed.
			3	Three bit errors allowed.
[5]	Reserved	R/W	Set to 0.	
[4:0]	SYNC_WORD_LENGTH	R/W	This register sets the sync word length in bits; 24 bits is the maximum. Note that the sync word matching length can be any value up to 24 bits, but the transmitted sync word pattern is a multiple of eight bits. Therefore, for nonbyte length sync words, the transmitted sync pattern must be filled with the preamble pattern.	
			SYNC_WORD_LENGTH	**Length in Bits**
			0	0
			1	1
			…	…
			24	24

Table 69. Address 0x121, Register PKT_SYNC_BYTE_0

Bit	Name	R/W	Description
[7:0]	SYNC_BYTE[23:16]	R/W	Upper byte of the sync word pattern. The sync word pattern is transmitted with the most significant bit first, starting with SYNC_BYTE_0. For nonbyte length sync words, the reminder of the least significant byte must be filled with the preamble. If SYNC_WORD_LENGTH length is >16 bits, PKT_SYNC_BYTE_0, PKT_SYNC_BYTE_1, and PKT_SYNC_BYTE_2 are all transmitted for a total of 24 bits. If SYNC_WORD_LENGTH is between 8 bits and 15 bits, PKT_SYNC_BYTE_1 and PKT_SYNC_ BYTE_2 are transmitted. If SYNC_WORD_LENGTH is between 1 bit and 7 bits, PKT_SYNC_BYTE_2 is transmitted for a total of eight bits. If the SYNC WORD LENGTH is 0, no sync bytes are transmitted.

Table 70. Address 0x122, Register PKT_SYNC_BYTE_1

Bit	Name	R/W	Description
[7:0]	SYNC_BYTE[15:8]	R/W	Middle byte of the sync word pattern.

Table 71. Address 0x123, Register PKT_SYNC_BYTE_2

Bit	Name	R/W	Description
[7:0]	SYNC_BYTE[7:0]	R/W	Lower byte of the sync word pattern.

Table 72. Address 0x124, Register PKT_TX_BASE_ADR

Bit	Name	R/W	Description
[7:0]	TX_BASE_ADR	R/W	Address in the packet RAM of the transmit packet. This address indicates the location of the first byte of the transmit packet to the ADF7024.

Table 73. Address 0x125, Register PKT_RX_BASE_ADR

Bit	Name	R/W	Description
[7:0]	RX_BASE_ADR	R/W	Address in the packet RAM of the receive packet. The ADF7024 writes any qualified received packet to packet RAM, starting at this memory location.

Table 74. Address 0x126, Register PKT_LENGTH_CONTROL

Bit	Name	R/W	Description
[7]	DATA_BYTE	R/W	Over the air arrangement of each transmitted packet RAM byte. A byte is transmitted with either MSB or LSB first. The same setting must be used on both the Tx and the Rx sides of the link. 1: data byte MSB first. 0: data byte LSB first.
[6]	PKT_LENGTH_MODE	R/W	1: fixed packet length mode. Fixed packet length in Tx and Rx modes, defined by PACKET_LENGTH_MAX. 0: variable packet length mode. In Tx and Rx, packet length is defined by the first byte in the packet RAM.
[5]	CRC_EN	R/W	1: append CRC in transmit mode. Check CRC in receive mode. 0: no CRC addition in transmit mode. No CRC check in receive mode.
[4:3]	DATA_MODE	R/W	0: normal operation. 1: disables the packet handling capabilities of the ADF7024. Set this mode only when carrying out receive bit error rate testing as described in the Receive Test Modes section.
[2:0]	LENGTH_OFFSET	R/W	Offset value in bytes that is added to the packet length value so that the communications processor knows the correct number of bytes to read. The communications processor calculates the actual payload length as $Payload\ Length = Length + LENGTH\_OFFSET - 4$ where Length is the length field (the first byte in the payload) in variable packet length mode, or is PACKET_LENGTH_MAX in fixed packet length mode.

Table 75. Address 0x127, Register PKT_LENGTH_MAX

Bit	Name	R/W	Description
[7:0]	PKT_LENGTH_MAX	R/W	If the variable packet length mode is used (PKT_LENGTH_MODE = 0), PKT_LENGTH_MAX sets the maximum receive packet length in bytes. If the fixed packet length mode is used (PKT_LENGTH_MODE = 1), PKT_LENGTH_MAX sets the length of the fixed transmit and receive packet in bytes. Note that the packet length is defined as the number of bytes from the end of the sync word to the start of the CRC.

Table 76. Address 0x128, Register RADIO_PROFILE_9

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_9	R/W	This register is part of the radio profile. Refer to Table 11.

Table 77. Address 0x129, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x00.

Table 78. Address 0x12A, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x00.

Table 79. Address 0x12B, Register RADIO_PROFILE_10

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_10	R/W	This register is part of the radio profile. Refer to Table 11.

Table 80. Address 0x12C, Register RADIO_PROFILE_11

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_11	R/W	This register is part of the radio profile. Refer to Table 11.

Table 81. Address 0x12D, Register RADIO_PROFILE_12

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_12	R/W	This register is part of the radio profile. Refer to Table 11.

Table 82. Address 0x12E, Register RADIO_PA_LEVEL

Bit	Name	R/W	Description
[7:0]	PA_LEVEL	R/W	Power amplifier level. The PA_LEVEL can be set in the 3 to 63 range, which corresponds to a power range of −20 dBm to +13.5 dBm. Settings <3 are reserved and must not be used.

Table 83. Address 0x12F, Register RADIO_PROFILE_13

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_13	R/W	This register is part of the radio profile. Refer to Table 11.

Table 84. Address 0x130, Register RADIO_PROFILE_14

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_14	R/W	This register is part of the radio profile. Refer to Table 11.

Table 85. Address 0x131, Register RADIO_PROFILE_15

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_15	R/W	This register is part of the radio profile. Refer to Table 11.

Table 86. Address 0x132, Register RADIO_PROFILE_16

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_16	R/W	This register is part of the radio profile. Refer to Table 11.

Table 87. Address 0x133, Register RADIO_PROFILE_17

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_17	R/W	This register is part of the radio profile. Refer to Table 11.

Table 88. Address 0x134, Register RADIO_PROFILE_18

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_18	R/W	This register is part of the radio profile. Refer to Table 11.

Table 89. Address 0x135, Register RADIO_PROFILE_19

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_19	R/W	This register is part of the radio profile. Refer to Table 11.

Table 90. Address 0x136, Register RADIO_PROFILE_20

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_20	R/W	This register is part of the radio profile. Refer to Table 11.

Table 91. Address 0x137, Register RADIO_PROFILE_21

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_21	R/W	This register is part of the radio profile. Refer to Table 11.

Table 92. Address 0x138, Register RADIO_PROFILE_22

Bit	Name	R/W	Description
[7:0]	RADIO_PROFILE_22	R/W	This register is part of the radio profile. Refer to Table 11.

Table 93. Address 0x139, Register PKT_TESTMODES

Bit	Name	R/W	Description
[7]	EXT_PA_LNA_ATB_CONFIG	R/W	1: ATB3 and ATB4 used for control of external PA and external LNA or of external transmit and receive switch, respectively (1.8 V logic outputs) 0: ATB1 and ATB2 used for control of external PA and external LNA or of external transmit and receive switch, respectively (VDD logic outputs) Must also enable external PA and LNA control in Register 0x11A
[6:4]	Reserved	R/W	Set to 0
[3]	PER_IRQ_SELF_CLEAR	R/W	1: automatic clear of INTERRUPT_TX_EOF and INTERRUPT_CRC_CORRECT 0: normal operation
[2]	PER_ENABLE	R/W	1: packet error rate enabled 0: packet error rate disabled
[1]	CONTINUOUS_TX	R/W	1: restart Tx after transmitting a packet 0: normal end of Tx
[0]	CONTINUOUS_RX	R/W	1: restart Rx after transmitting a packet 0: normal end of Rx

Table 94. Address 0x13A, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x04

Table 95. Address 0x13B, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x00

Table 96. Address 0x13C, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x00

Table 97. Address 0x13D, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x00

Table 98. Address 0x13E, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x00

Table 99. Address 0x13F, Register Reserved

Bit	Name	R/W	Description
[7:0]	Reserved	R/W	Set to 0x00

AUXILIARY REGISTERS DESCRIPTION

The auxiliary register settings are not retained when the device enters the PHY_SLEEP state.

Table 100. Address 0x30C, Register WUC_CONFIG_HIGH

Bit	Name	R/W	Reset	Description		
[7]	Reserved	W	0	Set to 0.		
[6:3]	RCOSC_COARSE_CAL_VALUE	W	0	**RCOSC_COARSE_CAL_VALUE**	**Change in RC Oscillator Frequency**	**Coarse Tune State**
				0000	+83%	State 10
				0001	+66%	State 9
				1000	+50%	State 8
				1001	+33%	State 7
				1100	+16%	State 6
				1101	0%	State 5
				1110	−16%	State 4
				1111	−33%	State 3
				0110	−50%	State 2
				0111	−66%	State 1
[2:0]	WUC_PRESCALER	W	0	**WUC_PRESCALER**	**32.768 kHz Divider Value**	**WUC Tick Period**
				0	1	30.52 µs
				1	4	122.1 µs
				2	8	244.1 µs
				3	16	488.3 µs
				4	128	3.91 ms
				5	1024	31.25 ms
				6	8192	250 ms
				7	65,536	2000 ms

Do not write to Register WUC_CONFIG_LOW without updating Register WUC_CONFIG_HIGH first.

Table 101. Address 0x30D, Register WUC_CONFIG_LOW

Bit	Name	R/W	Reset	Description
[7]	Reserved	W	0	Set to 0
[6]	WUC_RCOSC_EN	W	0	1: enable 32 kHz RC oscillator 0: disable 32 kHz RC oscillator
[5]	Reserved	W	0	Set to 0
[4]	Reserved	W	0	Set to 1
[3]	WUC_RETAIN_CONFIGREG_EN	W	0	1: enable retention of the configuration registers during the PHY_SLEEP state 0: disable retention of the configuration registers during the PHY_SLEEP state
[2:1]	Reserved	W	0	Set to 0
[0]	WUC_ARM	W	0	1: enable wakeup on a WUC timeout event 0: disable wakeup on a WUC timeout event

Updates to Register WUC_VALUE_HIGH are only effective if Register WUC_VALUE_LOW has been written to first.

Table 102. Address 0x30E, Register WUC_VALUE_HIGH

Bit	Name	R/W	Reset	Description
[7:0]	WUC_TIMER_VALUE[15:8]	W	0	WUC timer reload value, Bits[15:8] of [15:0]. A wake-up event is triggered when the WUC unit is enabled and the timer counts down to 0. The timer is clocked with the prescaler output rate, which is set by WUC_PRESCALER in Register WUC_CONFIG_HIGH. An update to this register is only effective if WUC_VALUE_LOW is written to first.

Do not write to Register WUC_VALUE_LOW without updating register WUC_VALUE_HIGH first.

Table 103. Address 0x30F, Register WUC_VALUE_LOW

Bit	Name	R/W	Reset	Description
[7:0]	WUC_TIMER_VALUE[7:0]	W	0	WUC timer reload value, Bits[7:0] of [15:0]. See Register WUC_VALUE_HIGH (Address 0x30E).

Table 104. Address 0x310, Register WUC_FLAG_RESET

Bit	Name	R/W	Reset	Description
[1]	WUC_RCOSC_CAL_EN	R/W	0	1: enable 32 kHz RC oscillator calibration 0: disable 32 kHz RC oscillator calibration
[0]	WUC_FLAG_RESET	R/W		1: reset WUC_TMR_PRIM_TOFLAG and WUC_PORFLAG bits (Address 0x311, Table 105) 0: normal operation

Table 105. Address 0x311, Register WUC_STATUS

Bit	Name	R/W	Reset	Description
[7]	Reserved	R	0	Reserved.
[6]	WUC_RCOSC_CAL_ERROR	R	0	1: 32 kHz RC oscillator calibration exited with error. 0: without error (only valid if WUC_RCOSC_CAL_EN = 1).
[5]	WUC_RCOSC_CAL_READY	R	0	1: 32 kHz RC oscillator calibration finished. 0: in progress (only valid if WUC_RCOSC_CAL_EN = 1).
[4]	Reserved	R	0	Reserved.
[3]	Reserved	R	0	Reserved.
[2]	WUC_PORFLAG	R	0	1: A chip cold start event is registered. 0: not registered.
[1]	WUC_TMR_PRIM_TOFLAG	R	0	1: WUC timeout event is registered. 0: not registered (the output of a latch triggered by a timeout event).
[0]	WUC_TMR_PRIM_TOEVENT	R	0	1: WUC timeout event is present. 0: not present (this bit is set when the counter reaches 0; it is not latched).

Table 106. Address 0x312, Register RSSI_READBACK

Bit	Name	R/W	Reset	Description
[7:0]	RSSI_READBACK	R	0	Receive input power. After reception of a packet, the RSSI_READBACK value is valid. $RSSI\ (\text{dBm}) = RSSI\_READBACK - 107$

Table 107. Address 0x319, Register IMAGE_REJECT_CAL_CONFIG

Bit	Name	R/W	Reset	Description
[7:6]	Reserved	R/W	0	Reserved.
[5]	IMAGE_REJECT_CAL_OVWRT_EN	R/W	0	Overwrite control for image reject calibration results.
[4:3]	IMAGE_REJECT_FREQUENCY	R/W	0	Set the fundamental frequency of the IR calibration signal source. A harmonic of this frequency can be used as an internal RF signal source for the image rejection calibration. 0: IR calibration source disabled in the XTAL divider. 1: IR calibration source fundamental frequency = XTAL/4. 2: IR calibration source fundamental frequency = XTAL/8. 3: IR calibration source fundamental frequency = XTAL/16.
[2:0]	IMAGE_REJECT_POWER	R/W	0	Set power level of IR calibration source. 0: IR calibration source disabled at the mixer input. 1: Power level = minimum. 2: Power level = minimum. 3: Power level = minimum. 4: Power level = minimum × 2. 5: Power level = minimum × 3. 6: Power level = minimum × 3. 7: Power level = minimum × 4.

Table 108. Address 0x324, Register POWERDOWN_RX

Bit	Name	R/W	Reset	Description
[7:5]	Reserved	R/W	0	Reserved
[4]	ADC_PD_N	R/W	0	1: ADC enabled 0: ADC disabled
[3]	RSSI_PD_N	R/W	0	1: RSSI enabled 0: RSSI disabled
[2]	RXBBFILT_PD_N	R/W	0	1: IF filter enabled 0: IF filter disabled
[1]	RXMIXER_PD_N	R/W	0	1: mixer enabled 0: mixer disabled
[0]	LNA_PD_N	R/W	0	1: LNA enabled 0: LNA disabled

Table 109. Address 0x325, Register POWERDOWN_AUX

Bit	Name	R/W	Reset	Description
[7:2]	Reserved	R/W	0	Reserved
[1]	TEMPMON_PD_EN	R/W	0	1: enable 0: disable temperature monitor
[0]	BATTMON_PD_EN	R/W	0	1: enable 0: disable battery monitor

Table 110. Address 0x327, Register ADC_READBACK_HIGH

Bit	Name	R/W	Reset	Description
[7:6]	Reserved	R	0	Reserved
[5:0]	ADC_READBACK[7:2]	R	0	ADC readback of MSBs

Table 111. Address 0x328, Register ADC_READBACK_LOW

Bit	Name	R/W	Reset	Description
[7:6]	ADC_READBACK[1:0]	R	0	ADC readback of LSBs
[5:0]	Reserved	R	0	Reserved

Table 112. Address 0x32D, Register BATTERY_MONITOR_THRESHOLD_VOLTAGE

Bit	Name	R/W	Reset	Description
[7:5]	Reserved	R/W	0	Reserved.
[4:0]	BATTMON_VOLTAGE	R/W	0	The battery monitor threshold voltage sets the alarm level for the battery monitor. The alarm is raised by the interrupt. Battery monitor trip voltage is V_{TRIP} = 1.7 V + 62 mV × (BATTMON_VOLTAGE + 1).

Table 113. Address 0x32E, Register EXT_UC_CLK_DIVIDE

Bit	Name	R/W	Reset	Description
[7:4]	Reserved	R/W	0	Reserved.
[3:0]	EXT_UC_CLK_DIVIDE	R/W	4	Optional output clock frequency on GP5_ATB1. Output frequency = XTAL/EXT_UC_CLK_DIVIDE. To disable, set EXT_UC_CLK_DIVIDE = 0.

Table 114. Address 0x336, Register INTERRUPT_SOURCE_0

Bit	Name	R/W	Reset	Description
[7]	INTERRUPT_NUM_WAKEUPS	R/W	0	Asserted when the number of WUC wakeups (NUMBER_OF_WAKEUPS[15:0][1]) reaches the threshold (NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[15:0][2]).
[6]	INTERRUPT_SWM_RSSI_DET	R/W	0	Asserted when the measured RSSI during smart wake mode exceeds the RSSI threshold value (SWM_RSSI_THRESH, Address 0x108).
[5]	Reserved	R/W	0	Set to 0.
[4]	INTERRUPT_TX_EOF	R/W	0	Asserted when a packet has finished transmitting.
[3]	Reserved	R/W	0	Set to 0.
[2]	INTERRUPT_CRC_CORRECT	R/W	0	Asserted when a received packet has the correct CRC. If CRC detection is disabled, this interrupt is asserted when the received payload is written to the packet RAM.
[1]	INTERRUPT_SYNC_DETECT	R/W	0	Asserted when a qualified sync word is detected in the received packet.
[0]	INTERRUPT_PREAMBLE_DETECT	R/W	0	Asserted when a qualified preamble is detected in the received packet.

[1] NUMBER_OF_WAKEUPS[15:0] is spread across two registers: SWM_NUMBER_OF_WAKEUPS_0 and SWM_NUMBER_OF_WAKEUPS_1.
[2] NUMBER_OF_WAKEUPS_IRQ_THRESHOLD[15:0] is spread across two registers: SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_0 and SWM_NUMBER_OF_WAKEUPS_IRQ_THRESHOLD_1.

Table 115. Address 0x337, Register INTERRUPT_SOURCE_1

Bit	Name	R/W	Reset	Description
[7]	BATTERY_ALARM	R/W	0	Battery voltage drops below the user set threshold value.
[6]	CMD_READY	R/W	0	ADF7024 is ready to accept a new command.
[5]	Unused	R/W	0	Unused.
[4]	WUC_TIMEOUT	R/W	0	Wake-up timer times out.
[3]	Unused	R/W	0	Unused.
[2]	Unused	R/W	0	Unused.
[1]	SPI_READY	R/W	0	SPI ready for access.
[0]	CMD_FINISHED	R/W	0	Command finishes.

Table 116. Address 0x339, Register CALIBRATION_STATUS

Bit	Name	R/W	Reset	Description
[7:3]	Reserved	R	0	Reserved.
[2]	PA_RAMP_FINISHED	R	0	The PA has finished ramping.
[1]	SYNTH_CAL_READY	R	0	1: Synthesizer calibration finished successfully. 0: Synthesizer calibration in progress.
[0]	RXBB_CAL_READY	R	0	Receive IF filter calibration. 1: IF filter calibration complete 0: in progress (valid while RXBB_CAL_EN = 1).

Table 117. Address 0x345, Register RXBB_CAL_CALWRD_READBACK

Bit	Name	R/W	Reset	Description
[5:0]	RXBB_CAL_CALWRD	R	0	RXBB reference oscillator calibration word; valid after the RXBB calibration cycle completes.

Table 118. Address 0x34F, Register RCOSC_CAL_READBACK_HIGH

Bit	Name	R/W	Reset	Description
[7:0]	RCOSC_CAL_READBACK[15:8]	R	0x0	Fine RC oscillator calibration result, Bits[15:8]

Table 119. Address 0x350, Register RCOSC_CAL_READBACK_LOW

Bit	Name	R/W	Reset	Description
[7:0]	RCOSC_CAL_READBACK[7:0]	R	0x0	Fine RC oscillator calibration result, Bits[7:0]

Table 120. Address 0x359, Register ADC_CONFIG_LOW

Bit	Name	R/W	Reset	Description
[7:4]	Reserved	R/W	0	Set to 0
[3:2]	ADC_REF_CHSEL	R/W	0	0: RSSI (default) 1: external AIN 2: temperature sensor 3: unused
[1:0]	ADC_REFERENCE_CONTROL	R/W	0	The following reference values are valid for a 3 V supply: 0: 1.85 V (default) 1: 1.95 V 2: 1.75 V 3: 1.65 V

Table 121. Address 0x35D, Register AGC_MODE

Bit	Name	R/W	Reset	Description
[7]	Reserved	R/W	0	Set to 0.
[6:5]	AGC_LOCK	R/W	0	Use this setting to manually control the AGC while in PHY_RX. 0: AGC is free running. This setting unlocks the AGC if previously locked. 1: Reserved. 2: AGC is locked at the current gain level. 3: AGC is free running and configured to lock on preamble detection.
[4:3]	Reserved	R/W	0	Set to 0.
[2]	Reserved	R/W	0	Set to 0.
[1:0]	Reserved	R/W	0	Set to 0.

Table 122. Address 0x360, Register AGC_GAIN_STATUS

Bit	Name	R/W	Reset	Description
[7:5]	Reserved	R	0	Reserved
[4:3]	LNA_GAIN_READBACK	R	0	0: low 1: medium 2: high 3: reserved
[2]	MIXER_GAIN_READBACK	R	0	0: low 1: high
[1:0]	FILTER_GAIN_READBACK	R	0	0: low 1: medium 2: high 3: reserved

Table 123. Address 0x372, Register FREQUENCY_ERROR_READBACK

Bit	Name	R/W	Reset	Description
[7:0]	FREQUENCY_ERROR_READBACK	R	0	Frequency error between the received signal frequency and the receive channel frequency = FREQUENCY_ERROR_READBACK × 1 kHz. The FREQUENCY_ERROR_READBACK value is in twos complement format.

Table 124. Address 0x3D2, Register OSC_CONFIG

Bit	Name	R/W	Reset	Description
[7:6]	Reserved	R/W	0	Write 0
[5:3]	XOSC_CAP_DAC	R/W	0	26 MHz crystal oscillator (XOSC26N) tuning capacitor control word
[2:0]	Reserved	R/W	0	Write 0

Table 125. Address 0x3F8, Register ANALOG_TEST_BUS

Bit	Name	R/W	Reset	Description
[7:0]	ANALOG_TEST_BUS	R/W	0	To enable analog RSSI on ADCIN_ATB3, set ANALOG_TEST_BUS = 0x64 in conjunction with RSSI_TSTMUX_SEL = 0x3.

Table 126. Address 0x3F9, Register RSSI_TSTMUX_SEL

Bit	Name	R/W	Reset	Description
[7]	Reserved	R/W	0	Reserved.
[6:2]	Reserved	R/W	0	Reserved.
[1:0]	RSSI_TSTMUX_SEL	R/W	0	To enable analog RSSI on ADCIN_ATB3, set RSSI_TSTMUX_SEL = 0x3 in conjunction with ANALOG_TEST_BUS = 0x64.

Table 127. Address 0x3FA, Register GPIO_CONFIGURE

Bit	Name	R/W	Reset	Description
[7:0]	GPIO_CONFIGURE	R/W	0	0x00: default 0x21: slicer output on GP5_ATB1 (bypass CDR) 0x40: limiter outputs on GP0(Q) and GP1(I) 0x41: filtered limiter outputs on GP0(Q) and GP1(I) and unfiltered limiter outputs on GP2(Q) and IRQ_GP3 (I) 0x50: packet transmit data from ADF7024 on GP0 0x53: PA ramp finished on GP0 0xA0: Rx data on GP0 pin and Rx clock on GP2 pin. See the Receive Test Modes section