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The Power MOSFET

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4.1 Introduction

In this chapter, an overview of power MOSFET (metal oxide semiconductor field effect transistor) semiconductor switching devices will be given. The detailed discussion of the physical structure, fabrication, and physical behavior of the device and packaging is beyond the scope of this chapter. The emphasis here will be given on the terminal *i–v* switching characteristics of the available device, turn-on, and turn-off switching characteristics, PSPICE modeling and its current, voltage, and switching limits. Even though, most of today's available semiconductor power devices are made of silicon or germanium materials, other materials such as gallium arsenide, diamond, and silicon carbide are currently being tested.

One of the main contributions that led to the growth of the power electronics field has been the unprecedented advancement in the semiconductor technology, especially with respect to switching speed and power handling capabilities. The area of power electronics started by the introduction of the silicon controlled rectifier (SCR) in 1958. Since then, the field has grown in parallel with the growth of the power semiconductor device technology. In fact, the history of power electronics is very much connected to the development of switching devices and it emerged as a separate discipline when high power bipolar junction transistors (BJTs) and MOSFETs devices where introduced in the 1960s and 1970s. Since then, the introduction of new devices has been accompanied with dramatic improvement in power rating and switching performance. Because of their functional importance, drive complexity, fragility, cost, power electronic design engineer must be equipped with the thorough understanding of the device operation, limitation, drawbacks, and related reliability and efficiency issues.

In the 1980s, the development of power semiconductor devices took an important turn when new process technology was developed that allowed the integration of MOS and BJT technologies on the same chip. Thus far, two devices using this new technology have been introduced: integrated gate bipolar transistor (IGBT) and MOS controlled thyristor (MCT). Many of the IC processing methods and equipment have been adopted for the development of power devices. However, unlike microelectronic IC's which process information, power devices IC's process power, hence, their packaging and processing techniques are quite different. Power semiconductor devices represent the "heart" of modern power electronics, with two major desirable characteristics of power semiconductor devices that guided their development are: the *switching speed* and *power handling capabilities.*

The improvement of semiconductor processing technology along with manufacturing and packaging techniques has allowed power semiconductor development for high voltage and high current ratings and fast turn-*on* and turn-*off* characteristics. Today, switching devices are manufactured with amazing power handling capabilities and switching speeds as will be shown later. The availability of different devices with different switching speed, power handling capabilities, size, cost, ... etc. make it possible to cover many power

electronics applications. As a result, trade-offs are made when it comes to selecting power devices.

4.2 Switching in Power Electronic Circuits

As stated earlier, the heart of any power electronic circuit is the semiconductor-switching network. The question arises here is do we have to use switches to perform electrical power conversion from the source to the load? The answer of course is no, there are many circuits which can perform energy conversion without switches such as linear regulators and power amplifiers. However, the need for using semiconductor devices to perform conversion functions is very much related to the converter efficiency. In power electronic circuits, the semiconductor devices are generally operated as switches, i.e. either in the *on*-state or the *off*-state. This is unlike the case in power amplifiers and linear regulators where semiconductor devices operate in the linear mode. As a result, very large amount of energy is lost within the power circuit before the processed energy reaches the output. The need to use semiconductor switching devices in power electronic circuits is their ability to control and manipulate very large amounts of power from the input to the output with a relatively very low power dissipation in the switching device. Hence, resulting in a very high efficient power electronic system.

Efficiency is considered as an important figure of merit and has significant implications on the overall performance of the system. Low efficient power systems means large amounts of power being dissipated in a form of heat, resulting in one or more of the following implications:

1. Cost of energy increases due to increased consumption.
2. Additional design complications might be imposed, especially regarding the design of device heat sinks.
3. Additional components such as heat sinks increase cost, size, and weight of the system, resulting in low power density.
4. High power dissipation forces the switch to operate at low switching frequency, resulting in limited bandwidth, slow response, and most importantly, the size and weight of magnetic components (inductors and transformers), and capacitors remain large. Therefore, it is always desired to operate switches at very high frequencies. But, we will show later that as the switching frequency increases, the average switching power dissipation increases. Hence, a trade-off must be made between reduced size, weight, and cost of components vs reduced switching power dissipation, which means inexpensive low switching frequency devices.
5. Reduced component and device reliability.

For more than forty years, it has been shown that in order to achieve high efficiency, switching (mechanical or electrical) is the best possible way to accomplish this. However, unlike mechanical switches, electronic switches are far more superior because of their speed and power handling capabilities as well as reliability.

We should note that the advantages of using switches don't come at no cost. Because of the nature of switch currents and voltages (square waveforms), normally high order harmonics are generated in the system. To reduce these harmonics, additional input and output filters are normally added to the system. Moreover, depending on the device type and power electronic circuit topology used, driver circuit control and circuit protection can significantly increase the complexity of the system and its cost.

EXAMPLE 4.1 The purpose of this example is to investigate the efficiency of four different power circuits whose functions are to take in power from 24 volts dc source and deliver a 12 volts dc output to a 6 Ω resistive load. In other words, the tasks of these circuits are to serve as *dc transformer* with a ratio of 2:1. The four circuits are shown in Fig. 4.1a–d representing voltage divider circuit, zener-regulator, transistor linear regulator, and switching circuit, respectively. The objective is to calculate the efficiency of those four power electronic circuits.

SOLUTION.

Voltage Divider DC Regulator The first circuit is the simplest forming a voltage divider with $R = R_L = 6\,\Omega$ and $V_o = 12$ volts. The efficiency defined as the ratio of the average load power, P_L, to the average input power, P_{in}

$$\eta = \frac{P_L}{P_{in}}\%$$

$$= \frac{R_L}{R_L + R}\% = 50\%$$

In fact efficiency is simply $V_o/V_{in}\%$. As the output voltage becomes smaller, the efficiency decreases proportionally.

Zener DC Regulator Since the desired output is 12 V, we select a zener diode with zener breakdown $V_Z = 12$ V. Assume the zener diode has the *i–v* characteristic shown in Fig. 4.1e since $R_L = 6\,\Omega$, the load current, I_L, is 2 A. Then we calculate R for $I_Z = 0.2$ A (10% of the load current). This results in $R = 5.27\,\Omega$. Since the input power is $P_{in} = 2.2\,\text{A} \times 24\,\text{V} = 52.8\,\text{W}$ and the output power is $P_{out} = 24$ W. The efficiency of
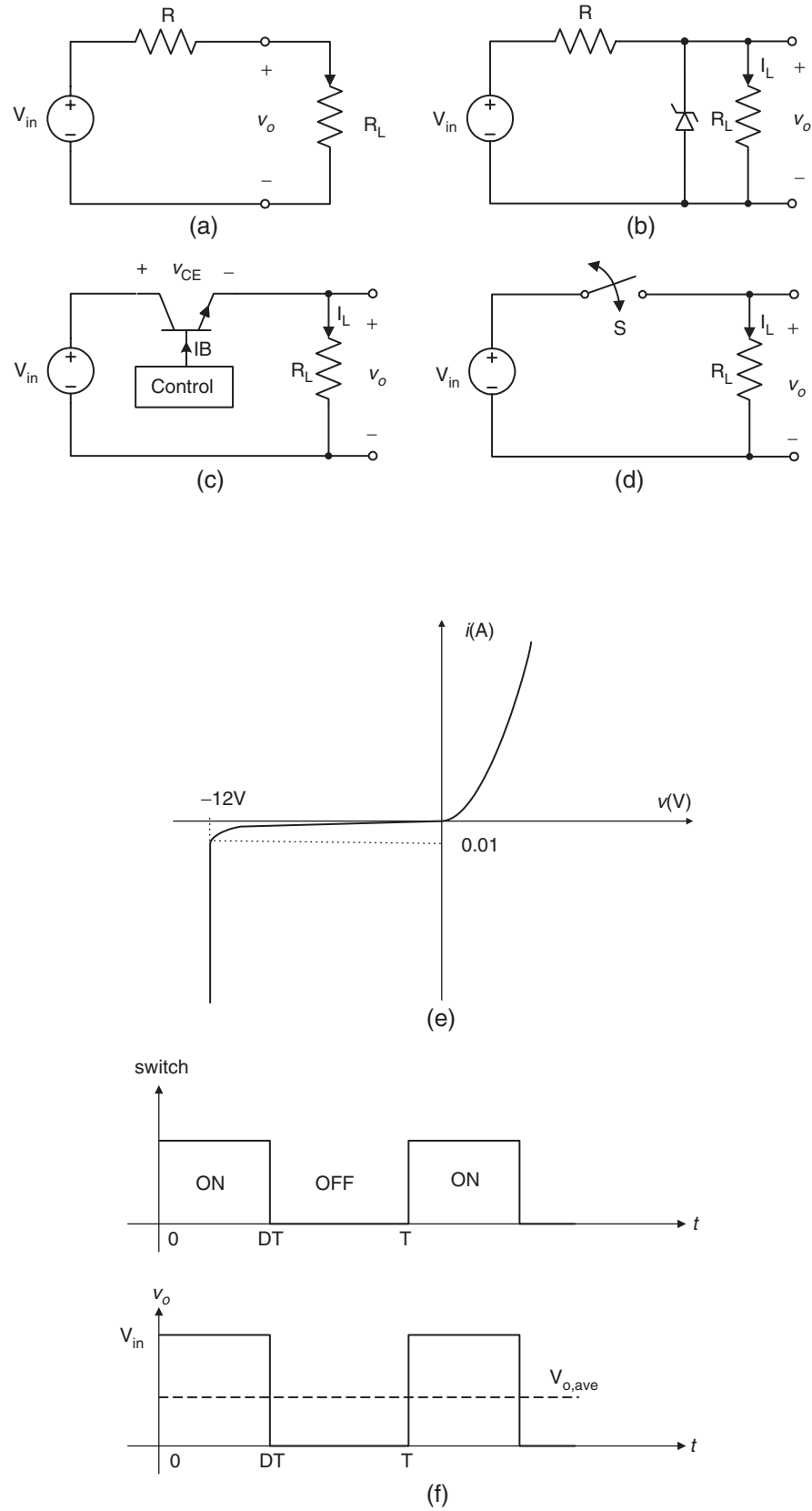
FIGURE 4.1   (a) Voltage divider; (b) zener regulator; (c) transistor regulator; (d) switching circuit; (e) *i–v* zener diode characteristics; and (f) switching waveform for S and corresponding output waveform.

the circuit is given by,

$$\eta = \frac{24\,\text{W}}{52.8\,\text{W}}\%$$

$$= 45.5\%$$

Transistor DC Regulator   It is clear from Fig. 4.1c that for $V_o = 12\,\text{V}$, the collector emitter voltage must be around 12 V. Hence, the control circuit must provide base current, I_B to put the transistor in the active mode with $V_{CE} \approx 12\,\text{V}$. Since the load current is 2 A, then collector current is approximately 2 A (assume small I_B). The total power dissipated in the transistor can be approximated by the following equation:

$$P_{diss} = V_{CE}I_C + V_{BE}I_B$$

$$\approx V_{CE}I_C \approx 12 \times 2 = 24\,\text{watts}$$

Therefore, the efficiency of the circuit is 50%.

Switching DC Regulator   Let us consider the switching circuit of Fig. 4.1d by assuming the switch is ideal and periodically turned *on* and *off* is shown in Fig. 4.1f. The output voltage waveform is shown in Fig. 4.1f. Even though the output voltage is not constant or pure dc, its average value is given by,

$$V_{o,ave} = \frac{1}{T}\int\limits_{0}^{T_0} V_{in}dt = V_{in}D$$

where D is the duty ratio equals the ratio of the on-time to the switching period. For $V_{o,ave} = 12\,\text{V}$, we set $D = 0.5$, i.e. the switch has a duty cycle of 0.5 or 50%. In case, the average output power is 48 W and the average input power is also 48 W, resulting in 100% efficiency! This is of course because we assumed the switch is ideal. However, let us assume a BJT switch is used in the above circuit with $V_{CE,sat} = 1\,\text{V}$ and I_B is small, then the average power loss across the switch is approximately 2 W, resulting in overall efficiency of 96%. Of course the switching circuit given in this example is over simplified, since the switch requires additional driving circuitry that was not shown, which also dissipates some power. But still, the example illustrates that high efficiency can be acquired by switching power electronic circuits when compared to the efficiency of linear power electronic circuits. Also, the difference between the linear circuit in Figs. 4.1b and c and the switched circuit of Fig. 4.1d is that the power delivered to the load in the later case in pulsating between zero and 96 watts. If the application calls for constant power delivery with little output voltage ripple, then an LC filter must be added to smooth out the output voltage.

The final observation is regarding what is known as load regulation and line regulation. The line regulation is defined as the ratio between the change in output voltage, ΔV_o, with respect to the change in the input voltage ΔV_{in}. This is a very important parameter in power electronics since the dc input voltage is obtained from a rectified line voltage that normally changes by $\pm 20\%$. Therefore, any off-line power electronics circuit must have a limited or specified range of line regulation. If we assume the input voltage in Figs. 4.1a,b is changed by 2 V, i.e. $\Delta V_{in} = 2\,\text{V}$, with R_L unchanged, the corresponding change in the output voltage ΔV_o is 1 V and 0.55 V, respectively. This is considered very poor line regulation. Figures 4.1c,d have much better line and load regulations since the closed-loop control compensate for the line and load variations.

4.3 General Switching Characteristics

4.3.1 The Ideal Switch

It is always desired to have the power switches perform as close as possible to the ideal case. Device characteristically speaking, for a semiconductor device to operate as an ideal switch, it must possess the following features:

1. No limit on the amount of current (known as forward or reverse current) the device can carry when in the conduction state (*on*-state);
2. No limit on the amount of the device-voltage ((known as forward or reverse blocking voltage) when the device is in the non-conduction state (*off*-state);
3. Zero *on*-state voltage drop when in the conduction state;
4. Infinite *off*-state resistance, i.e. zero leakage current when in the non-conduction state; and
5. No limit on the operating speed of the device when changes states, i.e. zero rise and fall times.

The switching waveforms for an ideal switch is shown in Fig. 4.2, where i_{sw} and v_{sw} are the current through and the voltage across the switch, respectively.

Both during the switching and conduction periods, the power loss is zero, resulting in a 100% efficiency, and with no switching delays, an infinite operating frequency can be achieved. In short, an ideal switch has infinite speed, unlimited power handling capabilities, and 100% efficiency. It must be noted that it is not surprising to find semiconductor-switching devices that can almost, for all practical purposes, perform as ideal switches for number of applications.
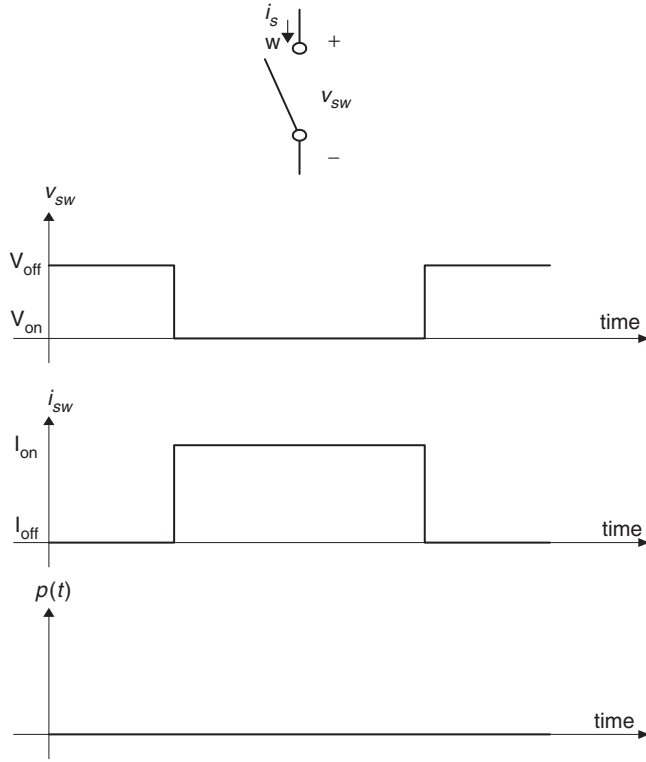
FIGURE 4.2 Ideal switching current, voltage, and power waveforms.

4.3.2 The Practical Switch

The practical switch has the following switching and conduction characteristics:

1. Limited power handling capabilities, i.e. limited conduction current when the switch is in the *on*-state, and limited blocking voltage when the switch is in the *off*-state.
2. Limited switching speed that is caused by the finite turn-*on* and turn-*off* times. This limits the maximum operating frequency of the device.
3. Finite *on*-state and *off*-state resistance's i.e. there exists forward voltage drop when in the *on*-state, and reverse current flow (leakage) when in the off-state.
4. Because of characteristics 2 and 3 above, the practical switch experiences power losses in the on and the off states (known as conduction loss), and during switching transitions (known as switching loss). Typical switching waveforms of a practical switch are shown in Fig. 4.3a.

The average switching power and conduction power losses can be evaluated from these waveforms. We should point out the exact practical switching waveforms vary from one device to another device, but Fig. 4.3a is a reasonably good representation. Moreover, other issues such as temperature dependence,

power gain, surge capacity, and over voltage capacity must be considered when addressing specific devices for specific applications. A useful plot that illustrates how switching takes place from *on* to *off* and vice versa is what is called *switching trajectory*, which is simply a plot of i_{sw} vs v_{sw}. Figure 4.3b shows several switching trajectories for the ideal and practical cases under resistive loads.

EXAMPLE 4.2 Consider a linear approximation of Fig. 4.3a as shown in Fig. 4.4a: (a) Give a possible circuit implementation using a power switch whose switching waveforms are shown in Fig. 4.4a, (b) Derive the expressions for the instantaneous switching and conduction power losses and sketch them, (c) Determine the total average power dissipated in the circuit during one switching frequency, and (d) The maximum power.

SOLUTION. (a) First let us assume that the turn-on time, t_{on}, and turn-off time, t_{off}, the conduction voltage V_{ON}, and the leakage current, I_{OFF}, are part of the switching characteristics of the switching device and have nothing to do with circuit topology.

When the switch is *off*, the blocking voltage across the switch is V_{OFF} that can be represented as a dc voltage source of value V_{OFF} reflected somehow across the switch during the *off*-state. When the switch is *on*, the current through the switch equals I_{ON}, hence, a dc current is needed in series with the switch when it is in the *on*-state. This suggests that when the switch turns *off* again, the current in series with the switch must be diverted somewhere else (this process is known as *commutation*). As a result, a second switch is needed to carry the main current from the switch being investigated when it's switched *off*. However, since i_{sw} and v_{sw} are linearly related as shown in Fig. 4.4b, a resistor will do the trick and a second switch is not needed. Figure 4.4 shows a one-switch implementation with S, the switch and R represents the switched-load.

(b) The instantaneous current and voltage waveforms during the transition and conduction times are given as follows

$$i_{sw}(t) = \begin{cases} \dfrac{t}{t_{ON}}(I_{ON} - I_{OFF}) + I_{OFF} & 0 \le t \le t_{ON} \\[2mm] I_{ON} & t_{ON} \le t \le T_s - t_{OFF} \\[2mm] -\dfrac{t - T_s}{t_{OFF}}(I_{ON} - I_{OFF}) + I_{OFF} & T_s - t_{OFF} \le t \le T_s \end{cases}$$

$$v_{sw}(t) = \begin{cases} -\dfrac{V_{OFF} - V_{ON}}{t_{ON}} \\ \quad \times (t - t_{ON}) + V_{ON} & 0 \le t \le t_{ON} \\[2mm] V_{ON} & t_{ON} \le t \le T_s - t_{OFF} \\[2mm] \dfrac{V_{OFF} - V_{ON}}{t_{OFF}} \\ \quad \times (t - (T_s - t_{OFF})) + V_{ON} & T_s - t_{OFF} \le t \le T_s \end{cases}$$
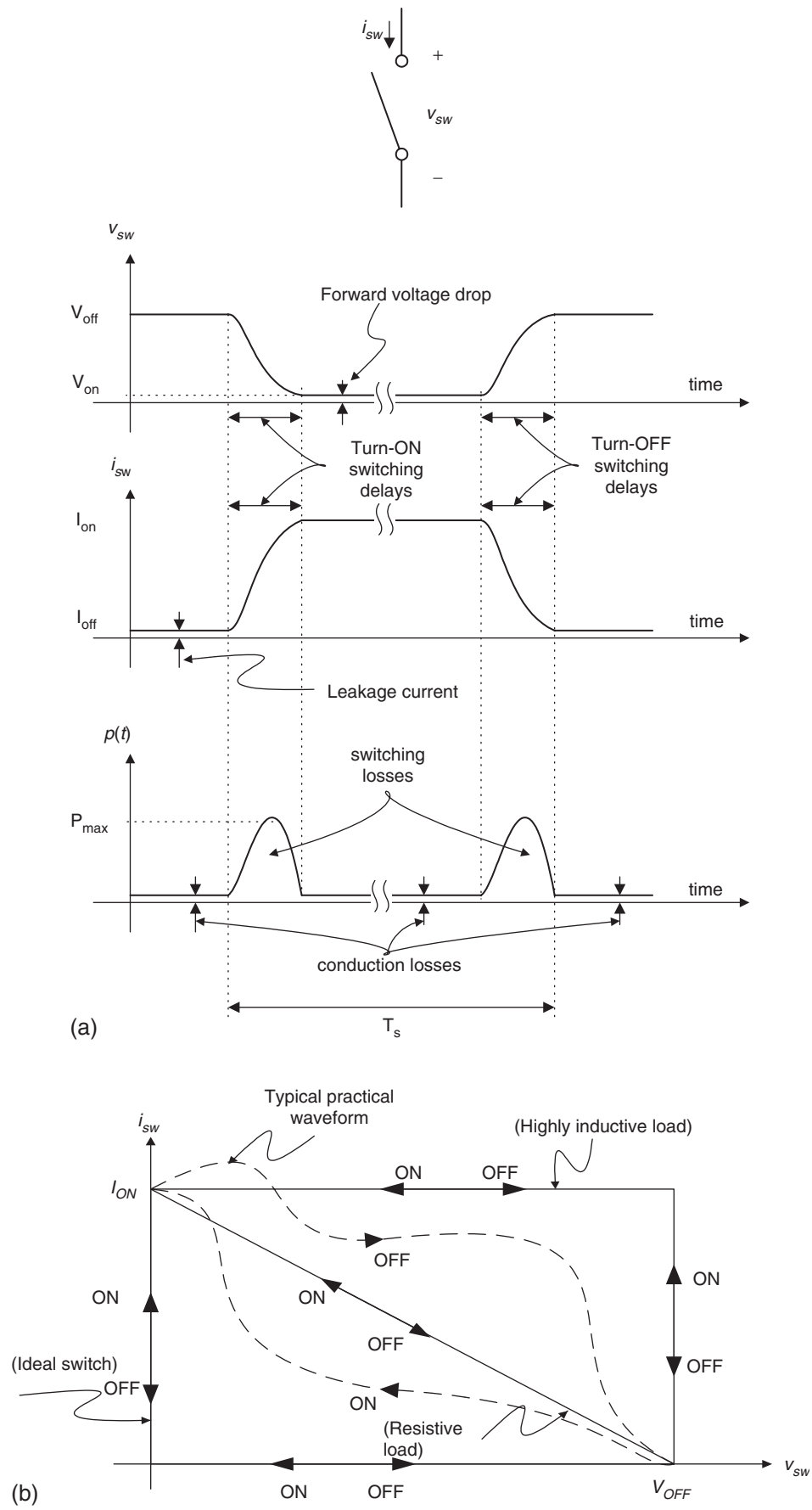
FIGURE 4.3 (a) Practical switching current, voltage, and power waveforms and (b) switching trajectory.
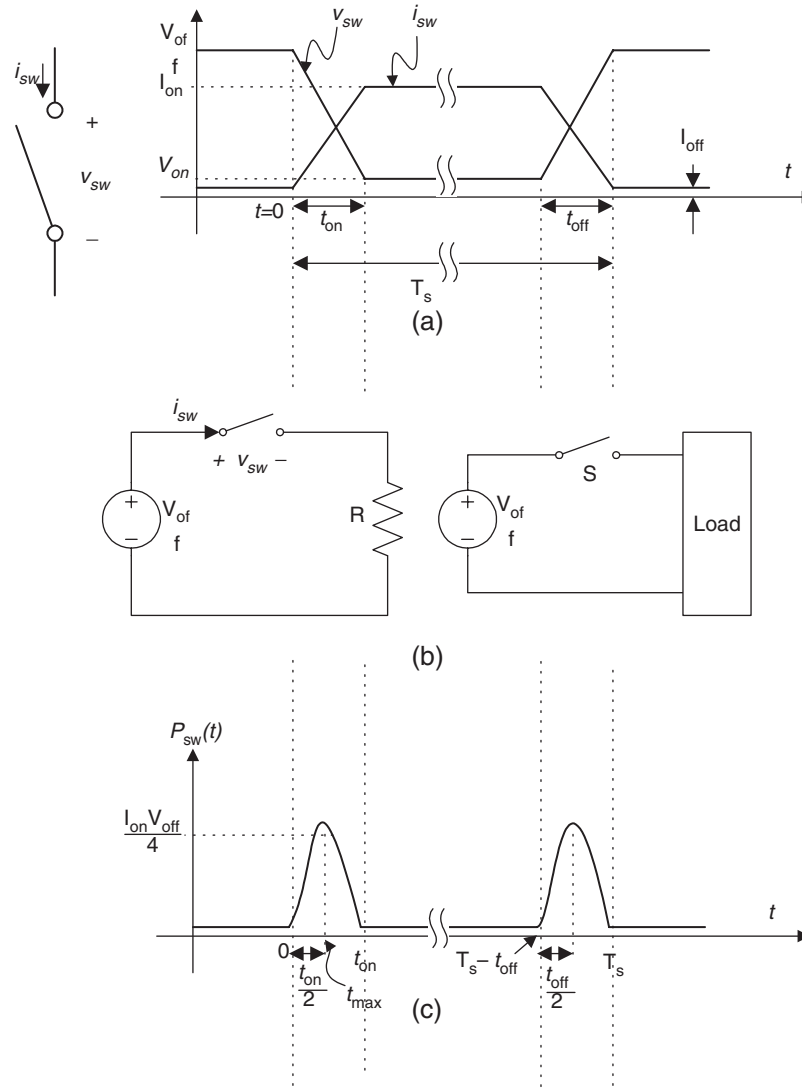
FIGURE 4.4 Linear approximation of typical current and voltage switching waveforms.

It can be shown that if we assume $I_{ON} \gg I_{OFF}$ and $V_{OFF} \gg V_{ON}$, then the instantaneous power, $p(t) = i_{sw}v_{sw}$ can be given as follows,

$$p(t) = \begin{cases} -\dfrac{V_{OFF}\,I_{ON}}{t_{ON}^2}\,(t - t_{ON})\,t & 0 \le t \le t_{ON} \\[2mm] V_{ON}\,I_{ON} & t_{ON} \le t \le T_s - t_{OFF} \\[2mm] -\dfrac{V_{OFF}\,I_{ON}}{t_{OFF}^2}(t - (T_s - t_{OFF}))\,(t - T_s) & T_s - t_{OFF} \le t \le T_s \end{cases}$$

Figure 4.4c shows a plot of the instantaneous power where the maximum power during turn-on and off is $V_{OFF}I_{ON}/4$.

(c) The total average dissipated power is given by

$$P_{ave} = \frac{1}{T_s}\int_0^{T_s} p(t)\,dt = \frac{1}{T_s}\left[\int_0^{t_{ON}} -\frac{V_{OFF}\,I_{ON}}{t_{ON}^2}(t - t_{ON})t\,dt \right.$$

$$+ \int_{t_{ON}}^{T_s - t_{OFF}} V_{ON}\,I_{ON}\,dt$$

$$\left. + \int_{T_s - t_{OFF}}^{T_s} -\frac{V_{OFF}\,I_{ON}}{t_{OFF}^2}(t - (T_s - t_{OFF}))(t - T_s)\,dt \right]$$

The evaluation of the above integral gives

$$P_{ave} = \frac{V_{OFF}I_{ON}}{T_s}\left(\frac{t_{ON}+t_{OFF}}{6}\right)$$

$$+ \frac{V_{ON}I_{ON}}{T_s}(T_s - t_{OFF} - t_{ON})$$

The first expression represents the total switching loss, whereas the second expression represents the total conduction loss over one switching cycle. We notice that as the frequency increases, the average power increases linearly. Also the power dissipation increases with the increase in the forward conduction current and the reverse blocking voltage.

(d) The maximum power occurs at the time when the first derivative of $p(t)$ during switching is set to zero, i.e.

$$\left.\frac{dp(t)}{dt}\right|_{t=t_{max}} = 0$$

solve the above equation for t_{max}, we obtain values at turn on and off, respectively,
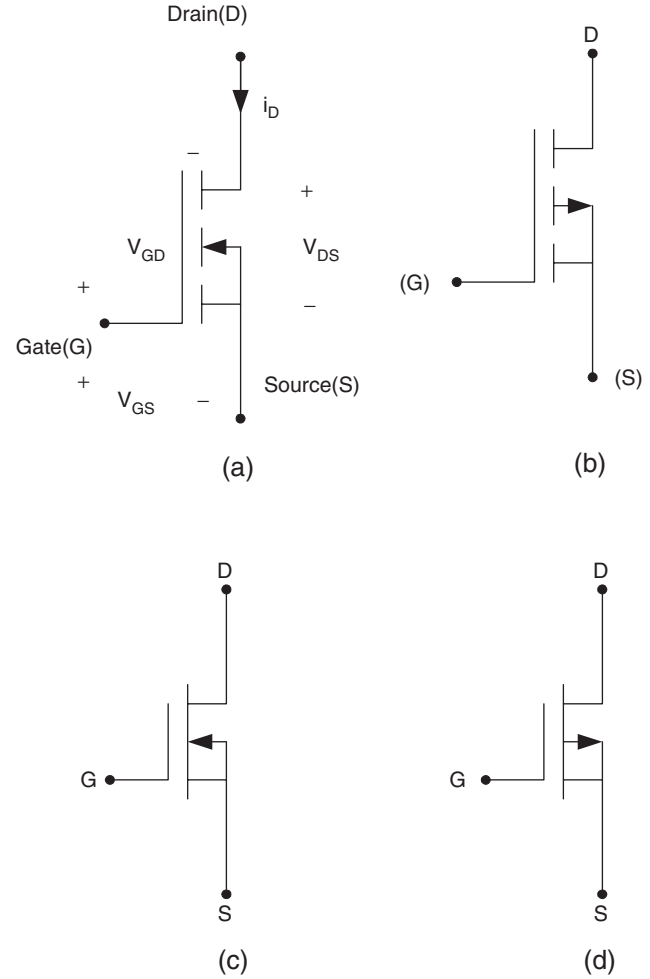
$$t_{max} = \frac{t_{rise}}{2}$$

$$t_{max} = T - \frac{t_{fall}}{2}$$

Solving for the maximum power, we obtain

$$P_{max} = \frac{V_{off}I_{on}}{4}$$

FIGURE 4.5 Device symbols: (a) n-channel enhancement-mode; (b) p-channel enhancement-mode; (c) n-channel depletion-mode; and (d) p-channel depletion-mode.

4.4 The Power MOSFET

Unlike the bipolar junction transistor (BJT), the MOSFET device belongs to the *Unipolar Device family, since it uses only the majority carriers in conduction.* The development of the metal oxide semiconductor technology for micro-electronic circuits opened the way for developing the power metal oxide semiconductor field effect transistor (MOSFET) device in 1975. Selecting the most appropriate device for a given application is not an easy task, requiring knowledge about the device characteristics, its unique features, innovation, and engineering design experience. Unlike low power (signal devices), power devices are more complicated in structure, driver design, and understanding of their operational *i–v* characteristics. This knowledge is very important for power electronics engineer to design circuits that will make these devices close to ideal. The device symbol for a p- and n-channel enhancement and depletion types are shown in Fig. 4.5. Figure 4.6 shows the *i–v* characteristics for the

n-channel enhancement-type MOSFET. It is the fastest power switching device with switching frequency more than 1 MHz, with voltage power ratings up to 1000 V and current rating as high as 300 A.

MOSFET regions of operations will be studied shortly.

4.4.1 MOSFET Structure

Unlike the lateral channel MOSFET devices used in many IC technology in which the gate, source, and drain terminals are located in the same surface of the silicon wafer, power MOSFET use vertical channel structure in order to increase the device power rating [1]. In the vertical channel structure, the source and drain are in opposite side of the silicon waver. Figure 4.7a shows vertical cross-sectional view for a power MOSFET. Figure 4.7b shows a more simplified representation. There are several discrete types of the vertical structure power MOSFET available commercially today such as V-MOSFET,
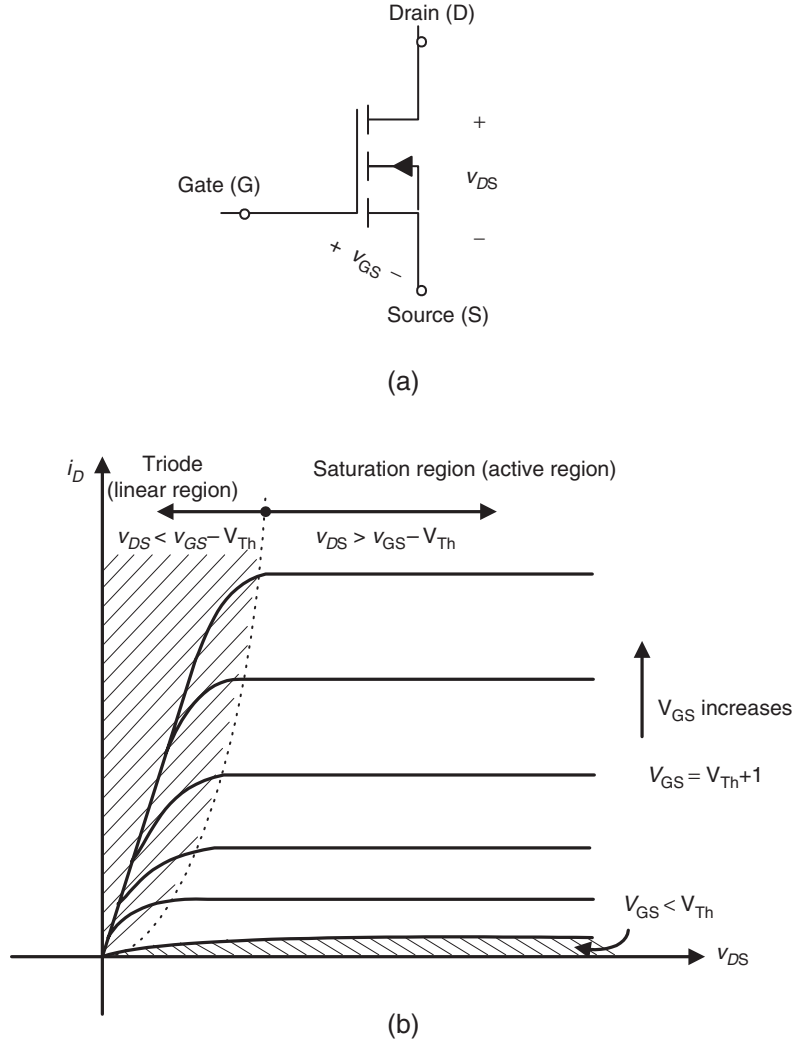
FIGURE 4.6   (a) n-Channel enhancement-mode MOSFET and (b) its i_D vs v_{DS} characteristics.

U-MOSFET, D-MOSFET, and S-MOSFET [1, 2]. The P–N junction between p-base (also referred to as body or bulk region) and the n-drift region provide the forward voltage blocking capabilities. The source metal contact is connected directly to the p-base region through a break in the n^+ source region in order to allow for a fixed potential to p-base region during the normal device operation. When the gate and source terminal are set the same potential ($V_{GS} = 0$), no channel is established in the p-base region, i.e. the channel region remain unmodulated. The lower doping in the n-drift region is needed in order to achieve higher drain voltage blocking capabilities. For the drain–source current, I_D, to flow, a conductive path must be established between the n^+ and n^- regions through the p-base diffusion region.

***A. On-state Resistance***   When the MOSFET is in the on-state (triode region), the channel of the device behaves like a constant resistance, $R_{DS(on)}$, that is linearly proportional to the change between v_{DS} and i_D as given by the following relation:

$$R_{DS(ON)} = \frac{\partial v_{DS}}{\partial i_D}\Big|_{V_{GS=Constant}} \qquad (4.1)$$

The total conduction (on-state) power loss for a given MOSFET with forward current I_D and on-resistance $R_{DS(on)}$ is given by,
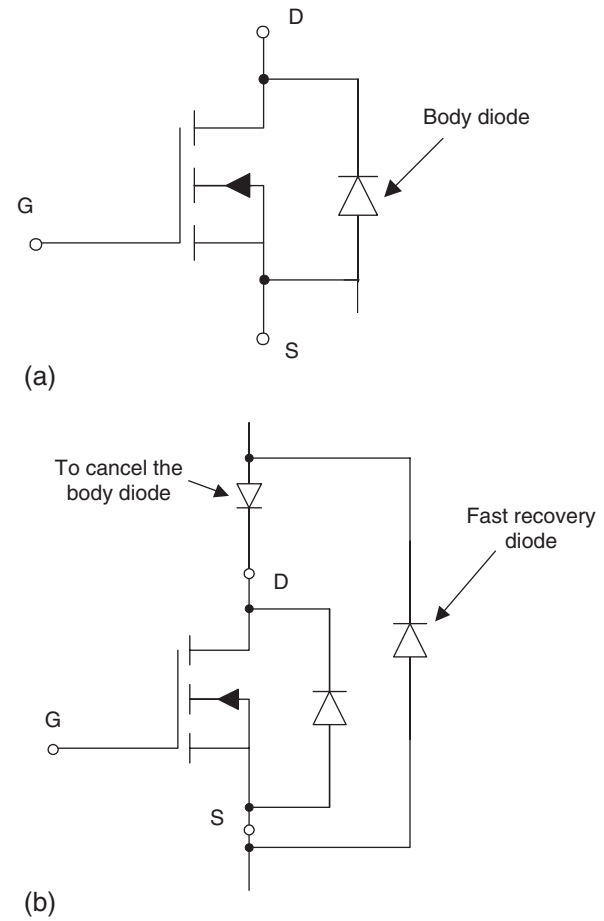
$$P_{on,diss} = I_D^2 R_{DS(on)} \qquad (4.2)$$

The value of $R_{DS(on)}$ can be significant and it varies between tens of milliohms and a few ohms for low-voltage and high-voltage MOSFETS, respectively. The *on*-state resistance is an important data sheet parameter, since it determines the forward voltage drop across the device and its total power losses.

(a)

(b)
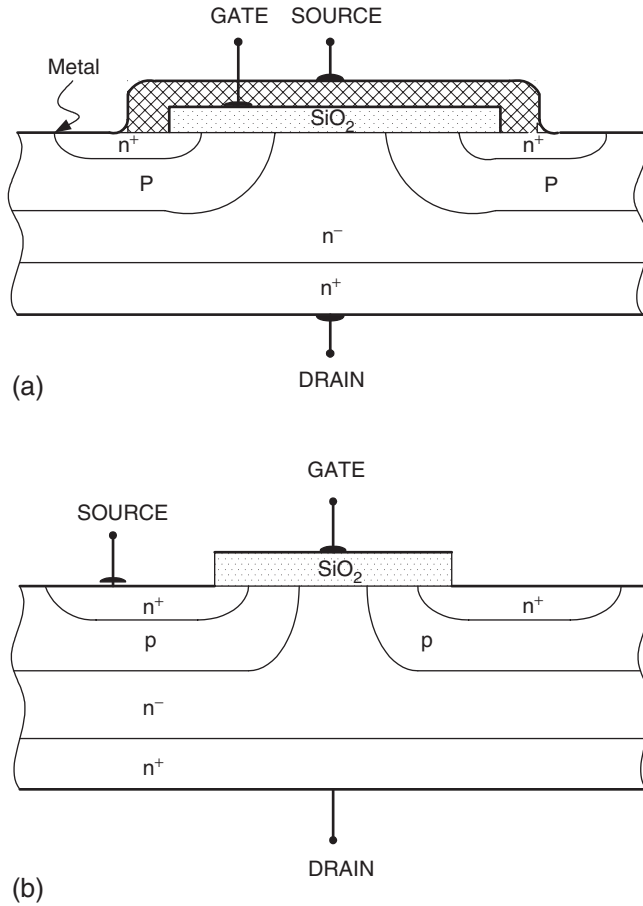
FIGURE 4.7 (a) Vertical cross-sectional view for a power MOSFET and (b) simplified representation.

(a)

(b)

**FIGURE 4.8** (a) MOSFET Internal body diode and (b) implementation of a fast body diode.

Unlike the current-controlled bipolar device, which requires base current to allow the current to flow in the collector, the power MOSFET device is a voltage-controlled unipolar device and requires only a small amount of input (gate) current. As a result, it requires less drive power than the BJT. However, it is a non-latching current like the BJT i.e. a gate source voltage must be maintained. Moreover, since only majority carriers contribute to the current flow, MOSFETs surpass all other devices in switching speed with switching speeds exceeding a few megahertz. Comparing the BJT and the MOSFET, the BJT has higher power handling capabilities and smaller switching speed, while the MOSFET device has less power handling capabilities and relatively fast switching speed. The MOSFET device has higher *on*-state resistor than the bipolar transistor. Another difference is that the BJT parameters are more sensitive to junction temperature when compared to the MOSFET, and unlike the BJT, MOSFET devices do not suffer from second breakdown voltages, and sharing current in parallel devices is possible.

B. Internal Body Diode   The modern power MOSFET has an internal diode called a body diode connected between the source and the drain as shown in Fig. 4.8a. This diode provides a reverse direction for the drain current, allowing a bi-directional switch implementation. Even though the MOSFET body diode has adequate current and switching speed ratings, in some power electronic applications that require the use of ultra-fast diodes, an external fast recovery diode is added in anti-parallel fashion after blocking the body diode by a slow recovery diode as shown in Fig. 4.8b.

C. Internal Capacitors   Another important parameter that effect the MOSFET's switching behavior is the parasitic capacitance between the device's three terminals, namely, gate-to-source, C_{gs}, gate-to-drain, C_{gd}, and drain-to-source (C_{ds}) capacitance as shown in Fig. 4.9a. Figure 4.9b shows the physical representation of these capacitors. The values of these capacitances are non-linear and a function of device structure, geometry, and bias voltages. During turn on, capacitor C_{gd} and C_{gs} must be charged through the gate, hence, the design
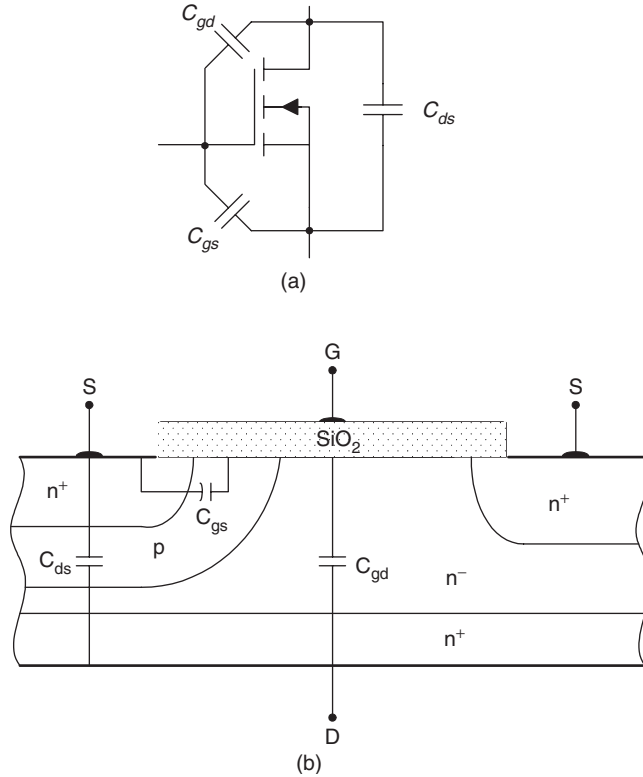
FIGURE 4.9 (a) Equivalent MOSFET representation including junction capacitances and (b) representation of this physical location.

of the gate control circuit must take into consideration the variation in this capacitance (Fig. 4.9b). The largest variation occurs in the gate-to-drain capacitance as the drain-to-gate voltage varies. The MOSFET parasitic capacitance are given in terms of the device data sheet parameters C_{iss}, C_{oss}, and C_{rss} as follows,

$$C_{gd} = C_{rss}$$

$$C_{gs} = C_{iss} - C_{rss}$$

$$C_{ds} = C_{oss} - C_{rss}$$

where C_{rss} = small-signal reverse transfer capacitance.
      C_{iss} = small-signal input capacitance with the drain and source terminals are shorted.
      C_{oss} = small-signal output capacitance with the gate and source terminals are shorted.

The MOSFET capacitances C_{gs}, C_{gd}, and C_{ds} are non-linear and function of the dc bias voltage. The variations in C_{oss} and C_{iss} are significant as the drain-to-source and gate-to-source voltages cross zero, respectively. The objective of the drive circuit is to charge and discharge the gate-to-source and gate-to-drain parasitic capacitance to turn *on* and *off* the device, respectively.

In power electronics, the aim is to use power-switching devices to operate at higher and higher frequencies. Hence, size and weight associated with the output transformer, inductors, and filter capacitors will decrease. As a result, MOSFETs are used extensively in power supply design that requires high switching frequencies including switching and resonant mode power supplies and brushless dc motor drives. Because of its large conduction losses, its power rating is limited to a few kilowatts. Because of its many advantages over the BJT devices, modern MOSFET devices have received high market acceptance.

4.4.2 MOSFET Regions of Operation

Most of the MOSFET devices used in power electronics applications are of the n-channel, enhancement-type like that which is shown in Fig. 4.6a. For the MOSFET to carry drain current, a channel between the drain and the source must be created. This occurs when the gate-to-source voltage exceeds the device threshold voltage, V_{Th}. For $v_{GS} > V_{Th}$, the device can be either in the triode region, which is also called "constant resistance" region, or in the saturation region, depending on the value of v_{DS}. For given v_{GS}, with small $v_{DS}(v_{DS} < v_{GS} - V_{Th})$, the device operates in the triode region(saturation region in the BJT), and for larger $v_{DS}(v_{DS} > v_{GS} - V_{Th})$, the device enters the saturation region (active region in the BJT). For $v_{GS} < V_{Th}$, the device turns off, with drain current almost equals zero. Under both regions of operation, the gate current is almost zero. This is why the MOSFET is known as a voltage-driven device, and therefore, requires simple gate control circuit.

The characteristic curves in Fig. 4.6b show that there are three distinct regions of operation labeled as triode region, saturation region, and cut-off-region. When used as a switching device, only triode and cut-off regions are used, whereas, when it is used as an amplifier, the MOSFET must operate in the saturation region, which corresponds to the active region in the BJT.

The device operates in the cut-off region (off-state) when $v_{GS} < V_{Th}$, resulting in no induced channel. In order to operate the MOSFET in either the triode or saturation region, a channel must first be induced. This can be accomplished by applying gate-to-source voltage that exceeds V_{Th}, i.e.

$$v_{GS} > V_{Th}$$

Once the channel is induced, the MOSFET can either operate in the triode region (when the channel is continuous with no pinch-off, resulting in the drain current proportioned to the channel resistance) or in the saturation region (the channel pinches off, resulting in constant I_D). The gate-to-drain bias voltage (v_{GD}) determines whether the induced channel enter pinch-off or not. This is subject to the following restriction.

For triode mode of operation, we have

$$v_{GD} > V_{Th}$$

$$v_{GD} < V_{Th}$$

And for the saturation region of operation,

Pinch-off occurs when $v_{GD} = V_{Th}$.

In terms of v_{DS}, the above inequalities may be expressed as follows:

1. For triode region of operation

$$v_{DS} < v_{GS} - V_{Th} \quad \text{and} \quad v_{GS} > V_{Th} \qquad (4.3)$$

2. For saturation region of operation

$$v_{DS} > v_{GS} - V_{Th} \quad \text{and} \quad v_{GS} > V_{Th} \qquad (4.4)$$

3. For cut-off region of operation

$$v_{GS} < V_{Th} \qquad (4.5)$$

It can be shown that drain current, i_D, can be mathematically approximated as follows:

$$i_D = K[2(v_{GS} - V_{Th})v_{DS} - v_{DS}^2] \quad \text{Triode Region} \qquad (4.6)$$

$$i_D = K(v_{GS} - V_{Th})^2 \qquad \text{Saturation Region} \quad (4.7)$$

where, $\quad K = \dfrac{1}{2}\mu_n C_{OX}\left(\dfrac{W}{L}\right)$

μ_n = electron mobility
C_{OX} = oxide capacitance per unit area
L = length of the channel
W = width of the channel.

Typical values for the above parameters are given in the PSPICE model discussed later. At the boundary between the saturation (active) and triode regions, we have,

$$v_{DS} = v_{GS} - V_{Th} \qquad (4.8)$$

Resulting in the following equation for i_D,

$$i_D = kv_{DS}^2 \qquad (4.9)$$

The input transfer characteristics curve for i_D and v_S. v_{GS} is when the device is operating in the saturation region shown in Fig. 4.10.

The large signal equivalent circuit model for a n-channel enhancement-type MOSFET operating in the saturation mode
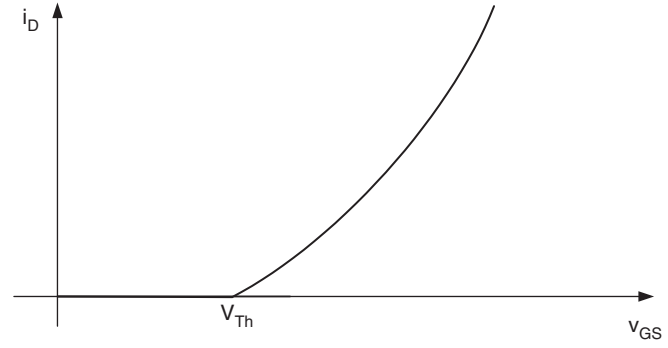

FIGURE 4.10　Input transfer characteristics for a MOSFET device when operating in the saturation region.
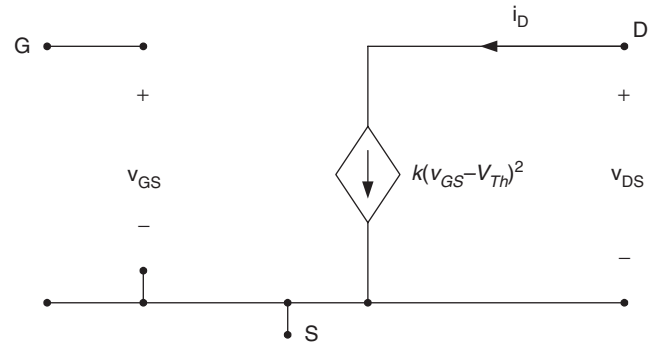

FIGURE 4.11　Large signal equivalent circuit model.

is shown in Fig. 4.11. The drain current is represented by a current source as the function of V_{Th} and v_{GS}.

If we assume that once the channel is pinched-off, the drain–source current will no longer be constant but rather depends on the value of v_{DS} as shown in Fig. 4.12. The increased value of v_{DS} results in reduced channel length, resulting in a phenomenon known as channel-length modulation [3, 4]. If the v_{DS}–i_D lines are extended as shown in Fig. 4.12, they all intercept the v_{DS}-axis at a single point labeled $-1/\lambda$, where λ is a positive constant MOSFET parameter. The term $(1 + \lambda v_{DS})$ is added to the i_D equation in order to account for the increase in i_D due to the channel-length modulation, i.e. i_D is given by,

$$i_D = k(v_{GS} - V_{Th})^2(1 + \lambda v_{DS}) \quad \text{Saturation Region} \quad (4.10)$$

From the definition of the r_o given in Eq. (4.1), it is easy to show the MOSFET output resistance which can be expressed as follows:

$$r_o = \frac{1}{\lambda k(v_{GS} - V_{Th})} \qquad (4.11)$$

If we assume the MOSFET is operating under small signal condition, i.e. the variation in v_{GS} on i_D vs v_{GS} is in the
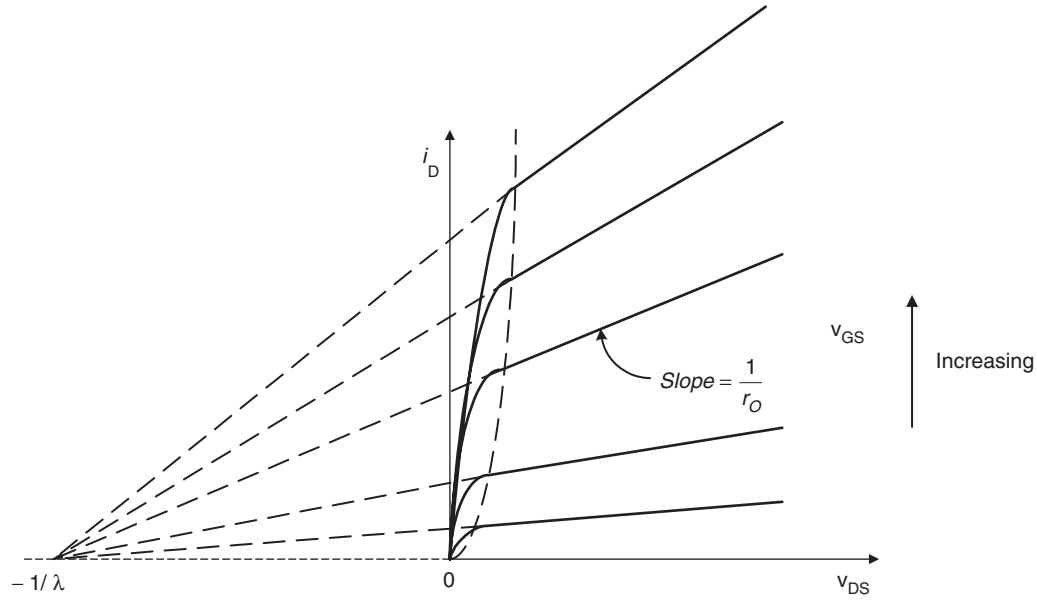
FIGURE 4.12 MOSFET characteristics curve including output resistance.

neighborhood of the dc operating point Q at i_D and v_{GS} as shown in Fig. 4.13. As a result, the i_D current source can be represented by the product of the slope g_m and v_{GS} as shown in Fig. 4.14.

4.4.3 MOSFET Switching Characteristics

Since the MOSFET is a majority carrier transport device, it is inherently capable of a high frequency operation [5–8]. But still the MOSFET has two limitations:

1. High input gate capacitances.
2. Transient/delay due to carrier transport through the drift region.

As stated earlier the input capacitance consists of two components: the gate-to-source and gate-to-drain capacitances. The input capacitances can be expressed in terms of the device
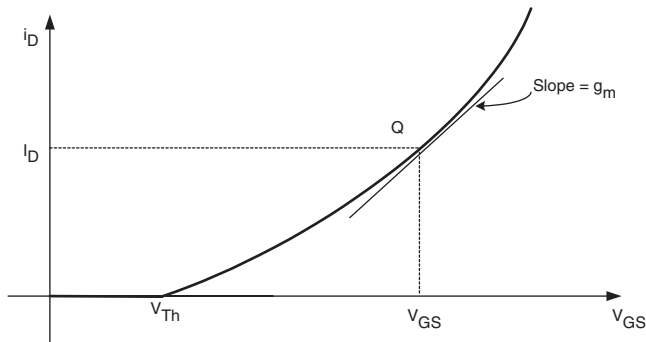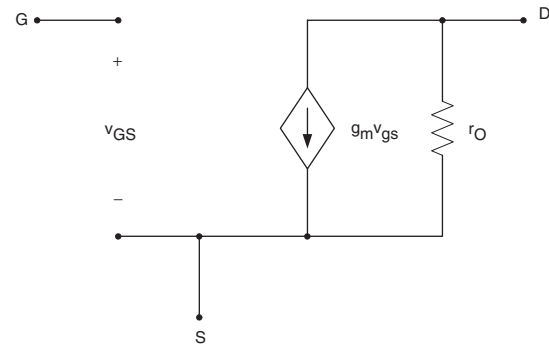

FIGURE 4.14 Small-signal equivalent circuit including MOSFET output resistance.

junction capacitances by applying Miller theorem to Fig. 4.15a. Using Miller theorem, the total input capacitance, C_{in}, seen between the gate-to-source is given by,

$$C_{in} = C_{gs} + (1 + g_m R_L)C_{gd} \qquad (4.12)$$

The frequency response of the MOSFET circuit is limited by the charging and discharging times of C_{in}. Miller effect is inherent in any feedback transistor circuit with resistive load that exhibits a feedback capacitance from the input and output. The objective is to reduce the feedback gate-to-drain resistance. The output capacitance between the drain-to-source, C_{ds}, does not affect the turn-on and turn-off MOSFET switching characteristics. Figure 4.16 shows how C_{gd} and C_{gs} vary under increased drain-source, v_{Ds}, voltage.
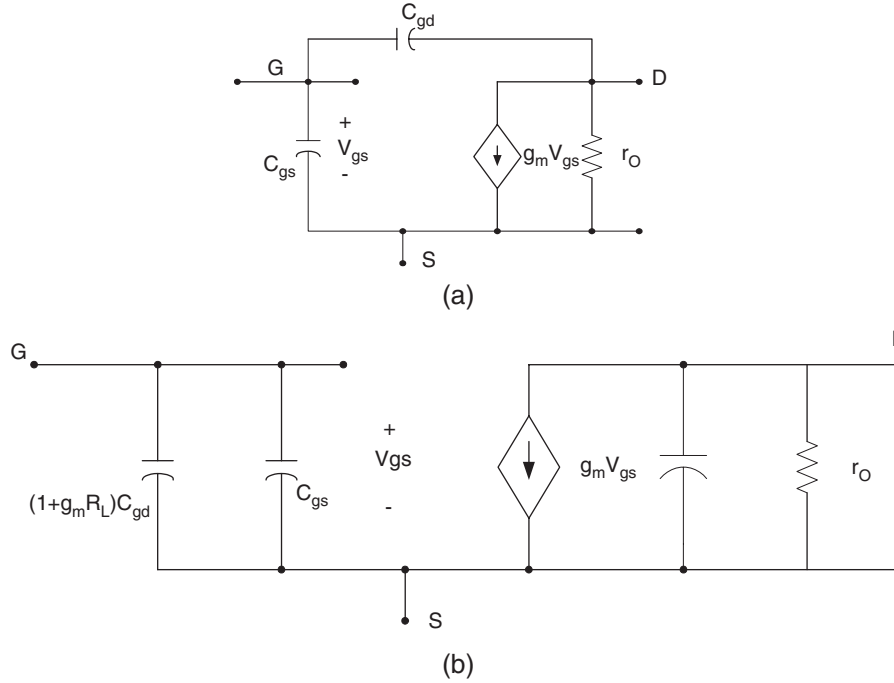

FIGURE 4.13 Linearized i_D vs v_{GS} curve with operating dc point (Q).

FIGURE 4.15   (a) Small-signal model including parasitic capacitances and (b) equivalent circuit using Miller theorem.
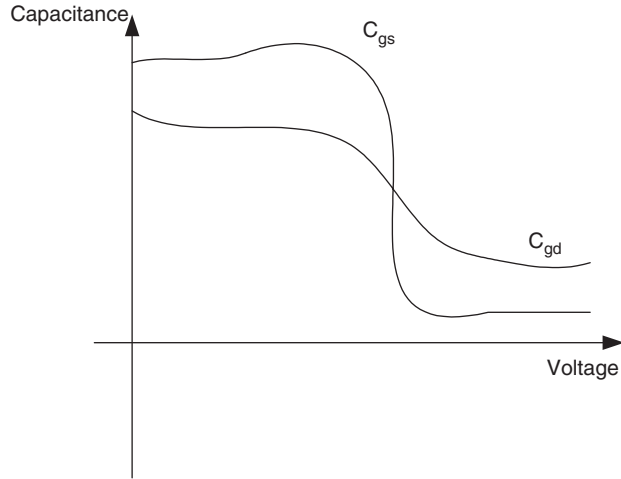

FIGURE 4.16   Variation of C_{gd} and C_{gs} as a function of v_{DS}.

In power electronics applications, the power MOSFETs are operated at high frequencies in order to reduce the size of the magnetic components. In order to reduce the switching losses, the power MOSFETs are maintained in either the on-state (conduction state) or the off-state (forward blocking) state.

It is important we understand the internal device behavior; therefore, the parameters that govern the device transition from the on-state and off-states. To investigate the on and off switching characteristics, we consider the simple power electronic circuit shown in Fig. 4.17a under inductive load.

The fly back diode D is used to pick up the load current when the switch is off. To simplify the analysis we will assume the load inductance is L_0 large enough so that the current through it is constant as shown in Fig. 4.17b.

A. Turn-on Analysis   Let us assume initially the device is off, the load current, I_0, flows through D as shown in the Fig. 4.18a $v_{GG} = 0$. The voltage $v_{DS} = V_{DD}$ and $i_G = i_D$. At $t = t_0$, the voltage v_{GG} is applied as shown in Fig. 4.19a. The voltage across C_{GS} starts charging through R_G. The gate–source voltage, v_{GS}, controls the flow of the drain-to-source current i_D. Let us assume that for $t_0 \le t < t_1$, $v_{GS} < V_{Th}$, i.e. the MOSFET remains in the cut-off region with $i_D = 0$, regardless of v_{DS}. The time interval (t_1, t_0) represents the delay turn-on time needed to change C_{GS} from zero to V_{Th}. The expression for the time interval $\Delta t_{10} = t_1 - t_0$ can be obtained as follows:

The gate current is given by,
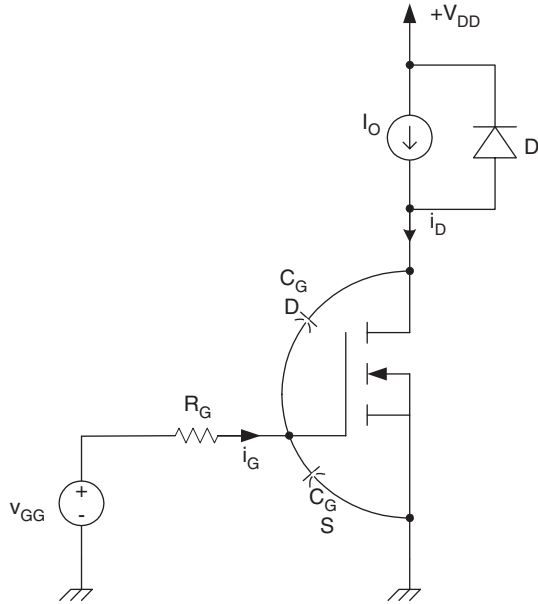
$$i_G = \frac{v_{GG} - v_{GS}}{R_G}$$

$$= i_{C_{GS}} + i_{C_{GD}}$$

$$= C_{GS}\frac{dv_{GS}}{dt} - C_{GD}\frac{d(v_G - v_D)}{dt} \qquad (4.13)$$

where v_G and v_D are gate-to-ground and drain-to-ground voltages, respectively.
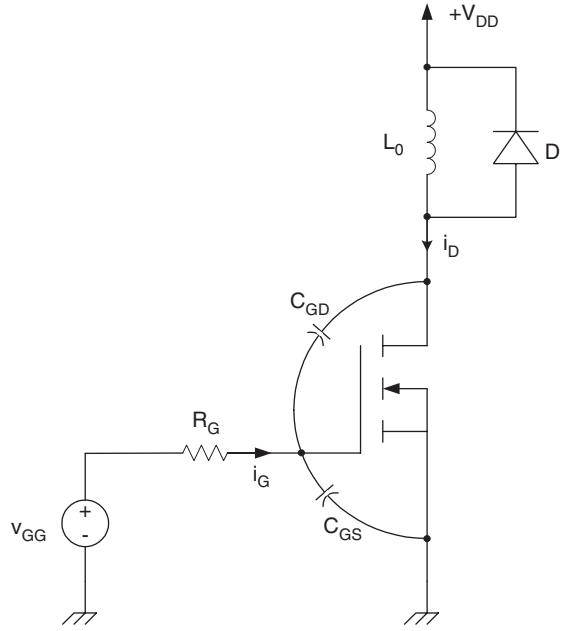
(a)

(b)

FIGURE 4.17 (a) Simplified equivalent circuit used to study turn-on and turn-off characteristics of the MOSFET and (b) simplified equivalent circuit.

Since we have $v_G = v_{GS}$, $v_D = +V_{DD}$, then i_G is given by

$$i_G = C_{GS}\frac{dv_{GS}}{dt} + C_{GD}\frac{dv_{GS}}{dt} = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} \quad (4.14)$$

From Eqs. (4.13) and (4.14), we obtain,

$$\frac{V_{GG} - v_{GS}}{R_G} = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} \quad (4.15)$$

Solving Eq. (4.15) for $v_{GS}(t)$ for $t > t_0$ with $v_{GS}(t_0) = 0$, we obtain,

$$v_{GS}(t) = V_{GG}(1 - e^{(t-t_0)/\tau}) \quad (4.16)$$
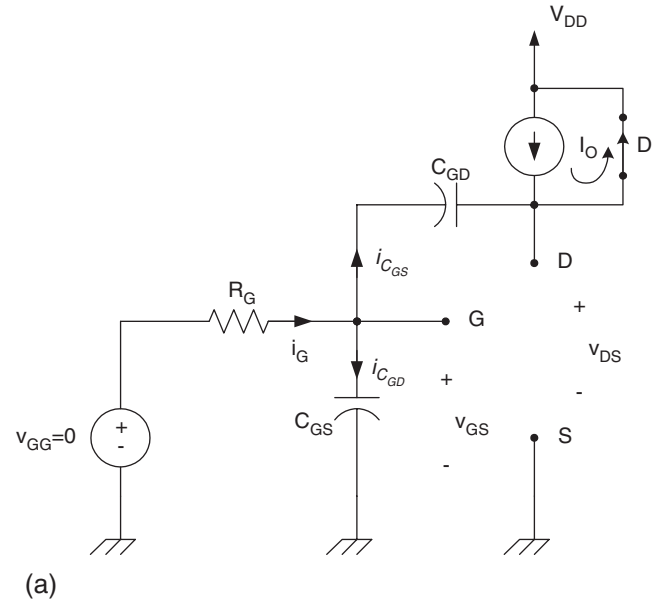
(a)
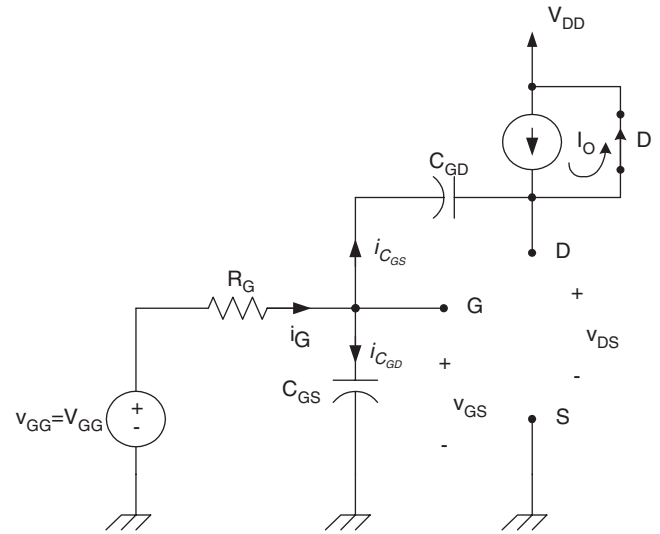
(b)

FIGURE 4.18 Equivalent modes: (a) MOSFET is in the off-state for $t < t_0$, $v_{GG} = 0$, $v_{DS} = V_{DD}$, $i_G = 0$, $i_D = 0$; (b) MOSFET in the off-state with $v_{GS} < V_{Th}$ for $t_1 > t > t_0$; (c) $v_{GS} > V_{Th}$, $i_D < I_0$ for $t_1 < t < t_2$; (d) $v_{GS} > V_{Th}$, $i_D = I_0$ for $t_2 \leq t < t_3$; and (e) $V_{GS} > V_{Th}$, $i_D = I_o$ for $t_3 \leq t < t_4$.

where,

$$\tau = R_G(C_{GS} + C_{GD})$$

The gate current, i_G, is given by,

$$i_G = \frac{v_{GG} - v_{GS}}{R_G}$$

$$i_G = \frac{V_{GG}}{R_G}e^{-(t-t_0)/\tau} \tag{4.17}$$

As long as $v_{GS} < V_{Th}$, i_D remains zero. At $t = t_1$, v_{GS} reaches V_{Th} causing the MOSFET to start conducting. Waveforms for i_G and v_{GS} are shown in Fig. 4.19. The time interval $(t_1 - t_0)$ is given by,
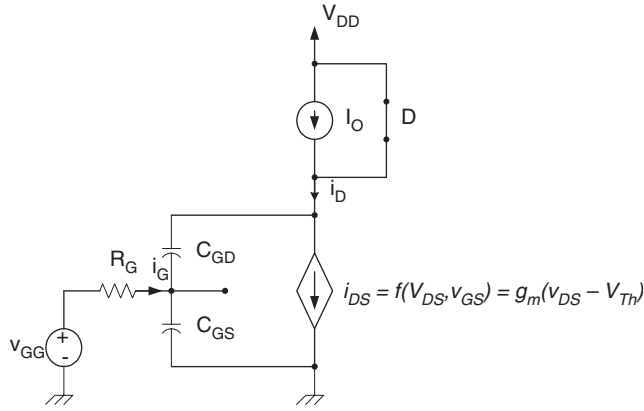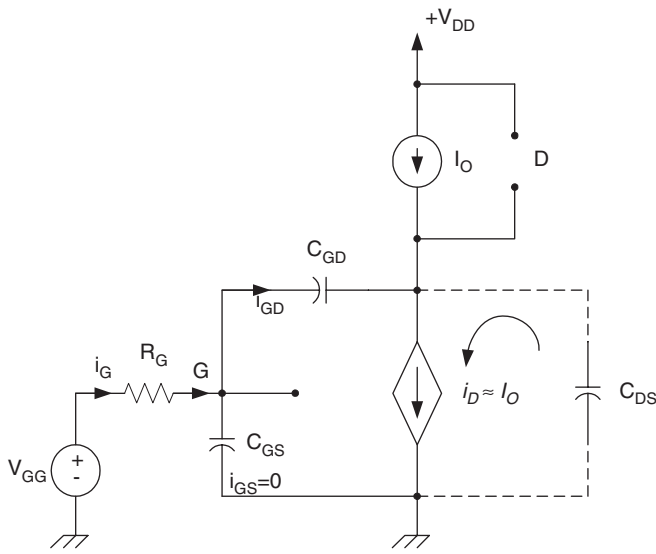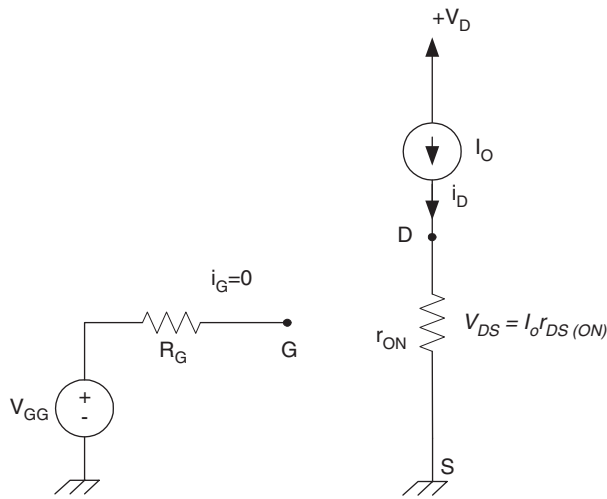
$$\Delta t_{10} = t_1 - t_0 = -\tau \ln\left(1 - \frac{V_{Th}}{V_{GG}}\right)$$

Δt_{10} represents the first delay interval in the turn-on process.

For $t > t_1$ with $v_{GS} > V_{Th}$, the device starts conducting and its drain current is given as a function of v_{GS} and V_{Th}. In fact i_D starts flowing exponentially from zero as shown in Fig. 4.19d. Assume the input transfer characteristics for the MOSFET is limited as shown in Fig. 4.20 with slope of g_m that is given by

$$g_m = \frac{(\partial i_D/\partial v_{GS})}{I_D} = \frac{2\sqrt{I_{DSS}I_D}}{V_{Th}} \tag{4.18}$$

The drain current can be approximately given as follows:

$$i_D(t) = g_m(v_{GS} - V_{Th}) \tag{4.19}$$

As long as $i_D(t) < I_0$, D remains on and $v_{DS} = V_{DD}$ as shown in Fig. 4.18c.

The equation for $v_{GS}(t)$ remains the same as in Eq. (4.16), hence, Eq. (4.19) results in $i_D(t)$ given by,

$$i_D(t) = g_m(V_{GG} - V_{Th}) - g_m V_{GG}e^{-(t-t_1)/\tau} \tag{4.20}$$

The gate current continues to decrease exponentially as shown in Fig. 4.19c. At $t = t_2$, i_D reaches its maximum value of I_0, turning D off. The time interval $\Delta t_{21} = (t_2 - t_1)$ is obtained from Eq. (4.20) by setting $i_D(t_2) = I_0$.

$$\Delta t_{21} = \tau \ln \frac{g_m V_{GG}}{g_m(V_{GG} - V_{Th}) - I_0} \tag{4.21}$$

For $t > t_2$, the diode turns off and $i_D \approx I_0$ as shown in Fig. 4.18d. Since the drain current is nearly a constant, then
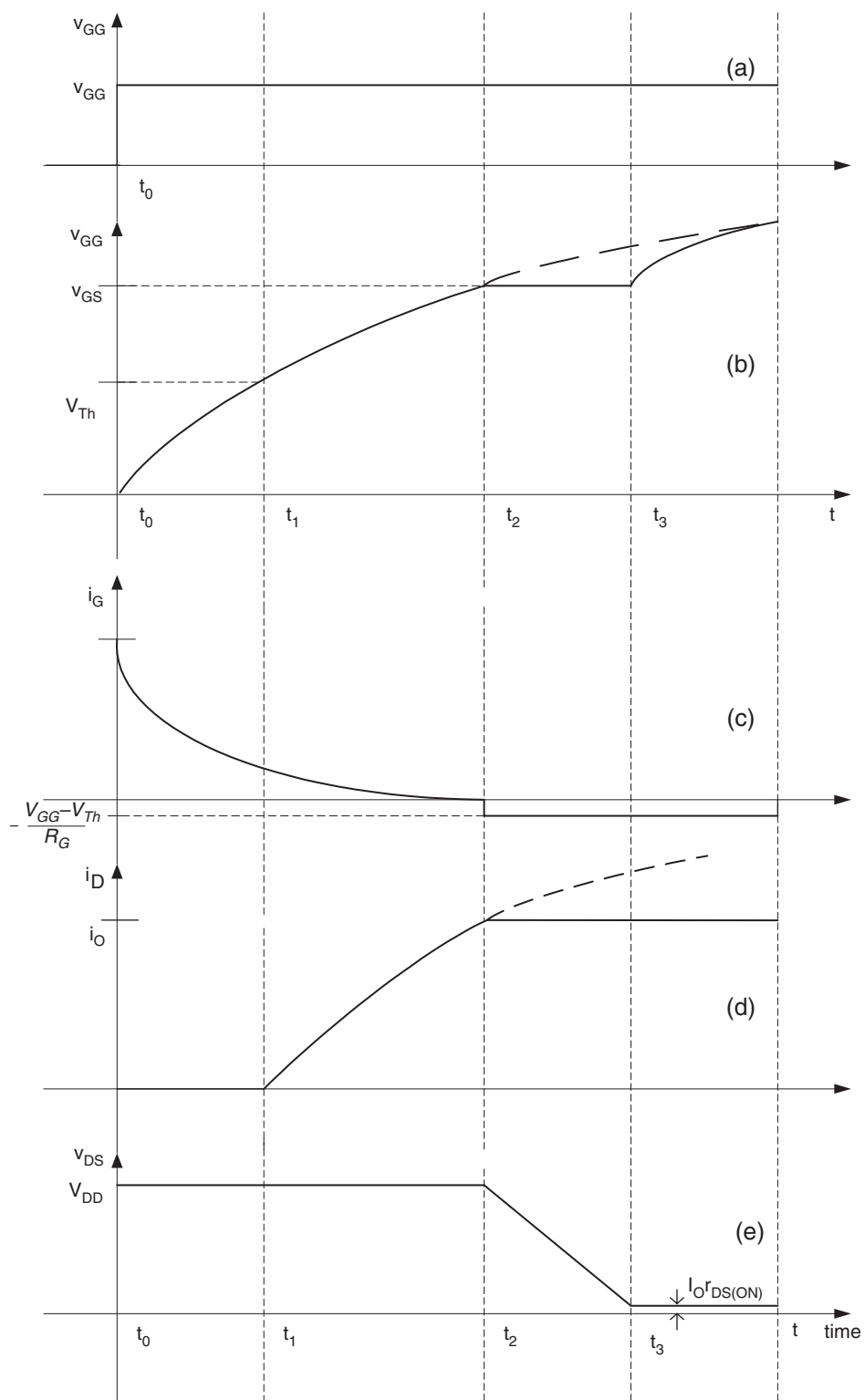
(c)

(d)

(e)

FIGURE 4.18 *continued*

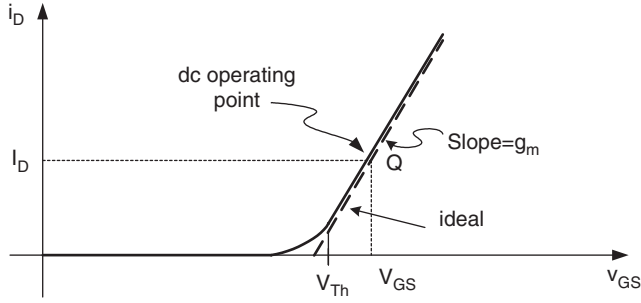**FIGURE 4.19**   Turn-on waveform switiching.

FIGURE 4.20 Input transfer characteristics.

the gate–source voltage is also constant according to the input transfer characteristic of the MOSFET, i.e.

$$i_D = g_m(v_{GS} - V_{Th}) \approx I_0 \qquad (4.22)$$

Hence,

$$v_{GS}(t) = \frac{I_0}{g_m} + V_{Th} \qquad (4.23)$$

At $t = t_2$, $i_G(t)$ is given by,

$$i_G(t_2) = \frac{V_{GG} - v_{GS}(t_2)}{V_{Th}} = \frac{V_{GG} - (I_0/g_m) - V_{Th}}{V_{Th}} \qquad (4.24)$$

Since the time constant τ is very small, it is safe to assume $v_{GS}(t_2)$ reaches its maximum, i.e.

$$v_{GS}(t_2) \approx V_{GG}$$

and

$$i_G(t_2) \approx 0$$

For $t_2 \leq t < t_3$, the diode turns off the load current I_0 (drain current i_D), which starts discharging the drain-to-source capacitance.

Since v_{GS} is constant, the entire gate current flows through C_{GD}, resulting in the following relation,

$$i_G(t) = i_{C_{GD}}$$

$$= C_{GD}\frac{d(v_G - v_D)}{dt}$$

Since v_G is constant and $v_s = 0$, we have

$$i_G(t) = -C_{GD}\frac{dv_{DS}}{dt}$$

$$= -\frac{V_{GG} - V_{Th}}{R_G}$$

Solving for $v_{DS}(t)$ for $t > t_2$, with $v_{DS}(t_2) = V_{DD}$, we obtain

$$v_{DS}(t) = -\frac{V_{GG} - V_{Th}}{R_G C_{GD}}(t - t_2) + V_{DD} \quad \text{For } t > t_2 \quad (4.25)$$

This is a linear discharge of C_{GD} as shown in Fig. 4.19e

The time interval $\Delta t_{32} = (t_3 - t_2)$ is determined by assuming that at $t = t_3$, the drain-to-source voltage reaches its minimum value determined by its on resistance, $v_{DS(ON)}$ i.e. $v_{DS(ON)}$ is given by,

$$v_{DS(ON)} \approx I_0 r_{DS(ON)}$$

$$= \text{constant}$$

For $t > t_3$, the gate current continues to charge C_{GD} and since v_{DS} is constant, v_{GS} starts charging at the same rate as in interval $t_0 \leq t < t_1$, i.e.

$$v_{GS}(t) = V_{GG}(1 - e^{-(t-t_3)/\tau})$$

The gate voltage keeps increasing exponentially until $t = t_3$ when it reaches V_{GG}, at which $i_G = 0$ and the device fully turns on as shown in Fig. 4.18e.

The equivalent circuit model when the MOSFET is completely turned on is for $t > t_1$. At this time, the capacitors C_{GS} and C_{GD} are charged with V_{GG} and $(I_0 r_{ds(ON)-V_{GG}})$, respectively.

The time interval $\Delta t_{32} = (t_3 - t_2)$ is obtained by evaluating v_{DS} at $t = t_3$ as follows

$$v_{DS}(t_3) = -\frac{V_{GG} - V_{Th}}{R_G C_{GD}}(t_3 - t_2) + V_{DD} \qquad (4.26)$$

$$= I_0 r_{DS(ON)}$$

Hence, $\Delta t_{32} = (t_3 - t_2)$ is given by,

$$\Delta t_{32} = t_3 - t_2 = R_G C_{GD}\frac{\left(V_{DD} - I_D r_{DS(ON)}\right)}{V_{GG} - V_{Th}} \qquad (4.27)$$

The total delay in turning on the MOSFET is given by

$$t_{ON} = \Delta t_{10} + \Delta t_{21} + \Delta t_{32} \qquad (4.28)$$

Notice the MOSFET sustains high voltage and current simultaneously during intervals Δt_{21} and Δt_{32}. This results in large power dissipation during turn on, that contributes to the overall switching losses. The smaller the R_G, the smaller Δt_{21} and Δt_{32} become.

B. Turn-off Characteristics To study the turn-off characteristic of the MOSFET, we will consider Fig. 4.17b again by assuming the MOSFET is ON and in steady state at $t > t_0$ with the equivalent circuit of Fig. 4.18e. Therefore, at $t = t_0$ we have the following initial conditions.

$$v_{DS}(t_0) = I_D r_{DS(ON)}$$

$$v_{GS}(t_0) = V_{GG}$$

$$i_{DS}(t_0) = I_0$$

$$i_G(t_0) = 0 \tag{4.29}$$

$$v_{C_{GS}}(t_0) = V_{GG}$$

$$v_{C_{GD}}(t_0) = V_{GG} - I_0 r_{DS(ON)}$$

At $t = t_0$, the gate voltage, $v_{GG}(t)$ is reduced to zero as shown in Fig. 4.21a. The equivalent circuit at $t > t_0$ is shown in Fig. 4.22a.

If we assume the drain-to-source voltage remains constant, C_{GS} and C_{GD} are discharging through R_G as governed by the following relations

$$i_G = \frac{-v_G}{R_G} = i_{C_{GS}} + i_{C_{GD}}$$

$$= C_{GS}\frac{dv_{GS}}{dt} + C_{GD}\frac{dv_{GD}}{dt}$$

Since v_{DS} is assumed constant, then i_G becomes,

$$i_G = \frac{-v_{GS}}{R_G}$$

$$= (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} \tag{4.30}$$

Hence, evaluating for v_{GS} for $t \geq t_0$, we obtain

$$v_{GS}(t) = v_{GS}(t_0)e^{-(t-t_0)/\tau} \tag{4.31}$$

where,

$$v_{GS}(t_0) = v_{GG}$$
$$\tau = (C_{GS} + C_{GD})R_G$$

As v_{GS} continues to decrease exponentially, drawing current from C_{GD} will reach a constant value at which drain current is fixed, i.e. $I_D = I_0$. From the input transfer characteristics, the value of v_{GS} when $I_D = I_0$ is given by,

$$v_{GS} = \frac{I_0}{g_m} + V_{Th} \tag{4.32}$$

The time interval $\Delta t_{10} = t_1 - t_0$ can be obtained easily by setting Eq. (4.31) to (4.32) at $t = t_1$.

The gate current during the $t_2 \leq t < t_1$ is given by

$$i_G = -\frac{V_{GG}}{R_G} - e^{-(t-t_0)/\tau} \tag{4.33}$$

Since, for $t_2 - t_1$, the gate-to-source voltage is constant and equals $v_{GS}(t_1) = (I_0/g_m) + V_{Th}$ as shown in Fig. 4.21b, then the entire gate current is being drawn from C_{GD}, hence,

$$i_G = C_{GD}\frac{dv_{GD}}{dt} = C_{GD}\frac{d(v_{GS} - v_{DS})}{dt} = -C_{GD}\frac{dv_{DS}}{dt}$$

$$= \frac{v_{GS}(t_1)}{R_G} = \frac{1}{R_G}\left(\frac{I_0}{g_m} + V_{Th}\right)$$

Assuming i_G constant at its initial value at $t = t_1$, i.e.

$$i_G = \frac{v_{GS}(t_1)}{R_G} = \frac{1}{R_G}\left(\frac{I_0}{g_m} + V_{Th}\right)$$

Integrating both sides of the above equation from t_1 to t with $v_{DS}(t_1) = -v_{DS(ON)}$, we obtain,

$$v_{DS}(t) = v_{DS(ON)} + \frac{1}{R_G C_{GD}}\left(\frac{I_0}{g_m} + V_{Th}\right)(t - t_1) \tag{4.34}$$

hence, v_{DS} charges linearly until it reaches V_{DD}.

At $t = t_2$, the drain-to-source voltage becomes equal to V_{DD}, forcing D to turn on as shown in Fig. 4.22c.

The drain-to-source current is obtained from the transfer characteristics and given by

$$i_{DS}(t) = g_m(v_{GS} - V_{Th})$$

where $v_{GS}(t)$ is obtained from the following equation

$$i_G = -\frac{v_{GS}}{R_G} = (C_{GS} + C_{GD})\frac{dv_{GS}}{dt} \tag{4.35}$$

Integrate both sides from t_2 to t with $v_{GS}(t_2) = (I_0/g_m) + V_{Th}$, we obtain the following expression for $v_{GS}(t)$,

$$v_{GS}(t) = \left(\frac{I_0}{g_m} + V_{Th}\right)e^{-(t-t_2)/\tau} \tag{4.36}$$

Hence the gate current and drain-to-source current are given by,

$$i_G(t) = \frac{-1}{R_G}\left(\frac{I_0}{g_m} + V_{Th}\right)e^{-(t-t_2)/\tau} \tag{4.37}$$

$$i_{DS}(t) = g_m V_{Th}(e^{-(t-t_2)/\tau} - 1) + I_0 e^{-(t-t_2)/\tau} \tag{4.38}$$

The time interval between $t_2 \leq t < t_3$ is obtained by evaluating $v_{GS}(t_3) = V_{Th}$, at which the drain current becomes
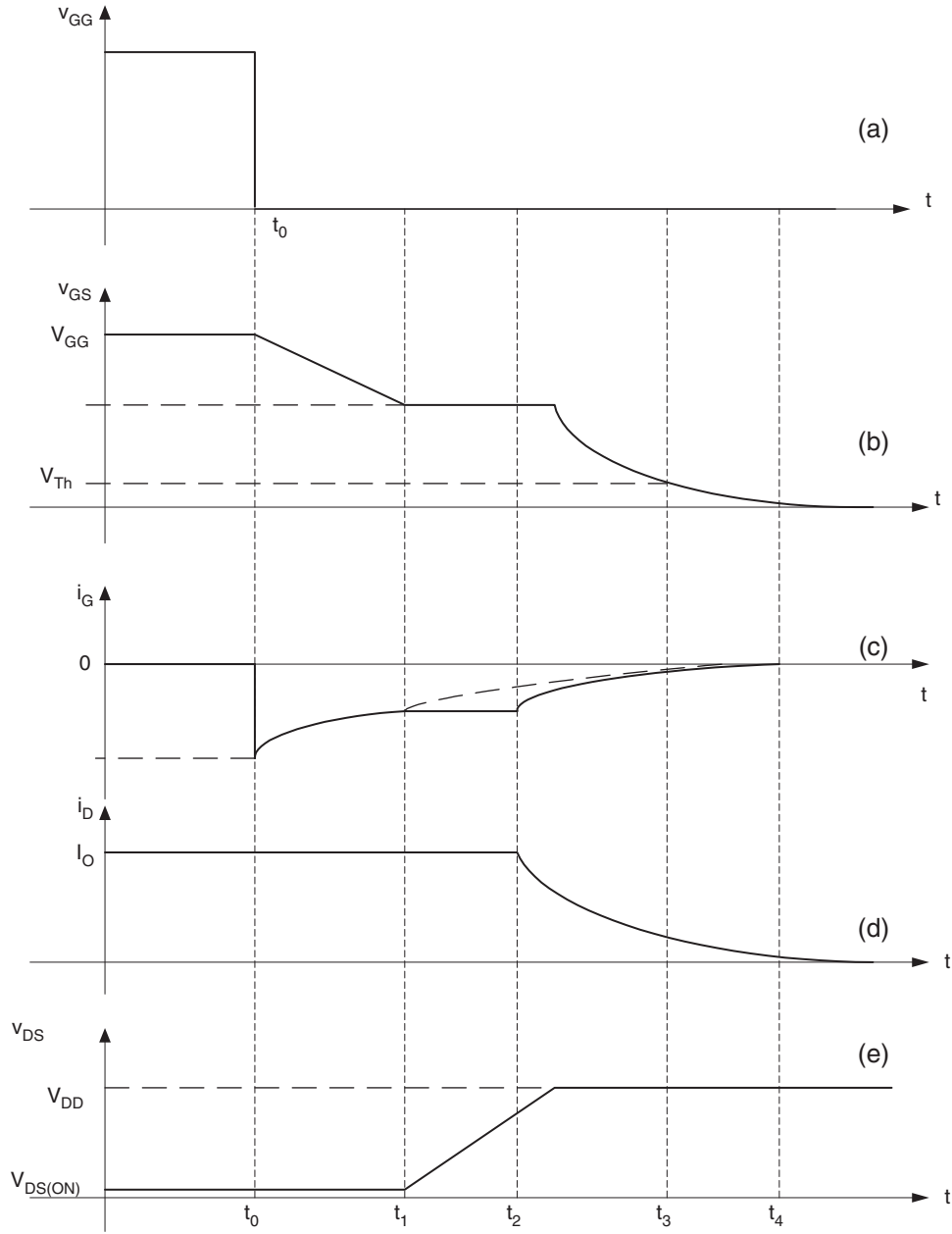
FIGURE 4.21   Turn-off switching waveforms.

approximately zero and the MOSFET turn off hence,

$$v_{GS}(t_3) = V_{Th}$$

$$= \left(\frac{I_0}{g_m} + V_{Th}\right) e^{-(t_3-t_2)/\tau}$$

Solving for $\Delta t_{32} = t_3 - t_2$ we obtain,

$$\Delta t_{32} = t_3 - t_2 = \tau \ln\left(1 + \frac{I_0}{V_{Th}g_m}\right) \quad (4.39)$$

For $t > t_3$, the gate voltage continues to decrease exponentially to zero, at which the gate current becomes zero and C_{GD} charges to $-V_{DD}$. Between t_3 and t_4, I_D discharges to zero as shown in the equivalent circuit Fig. 4.22d.

The total turn-off time for the MOSFET is given by,

$$t_{off} = \Delta t_{10} + \Delta t_{21} + \Delta t_{32} + \Delta t_{43}$$

$$\approx \Delta t_{21} + \Delta t_{32} \quad (4.40)$$

The time intervals that most effect the power dissipation are Δt_{21} and Δt_{32}. It is clear that in order to reduce
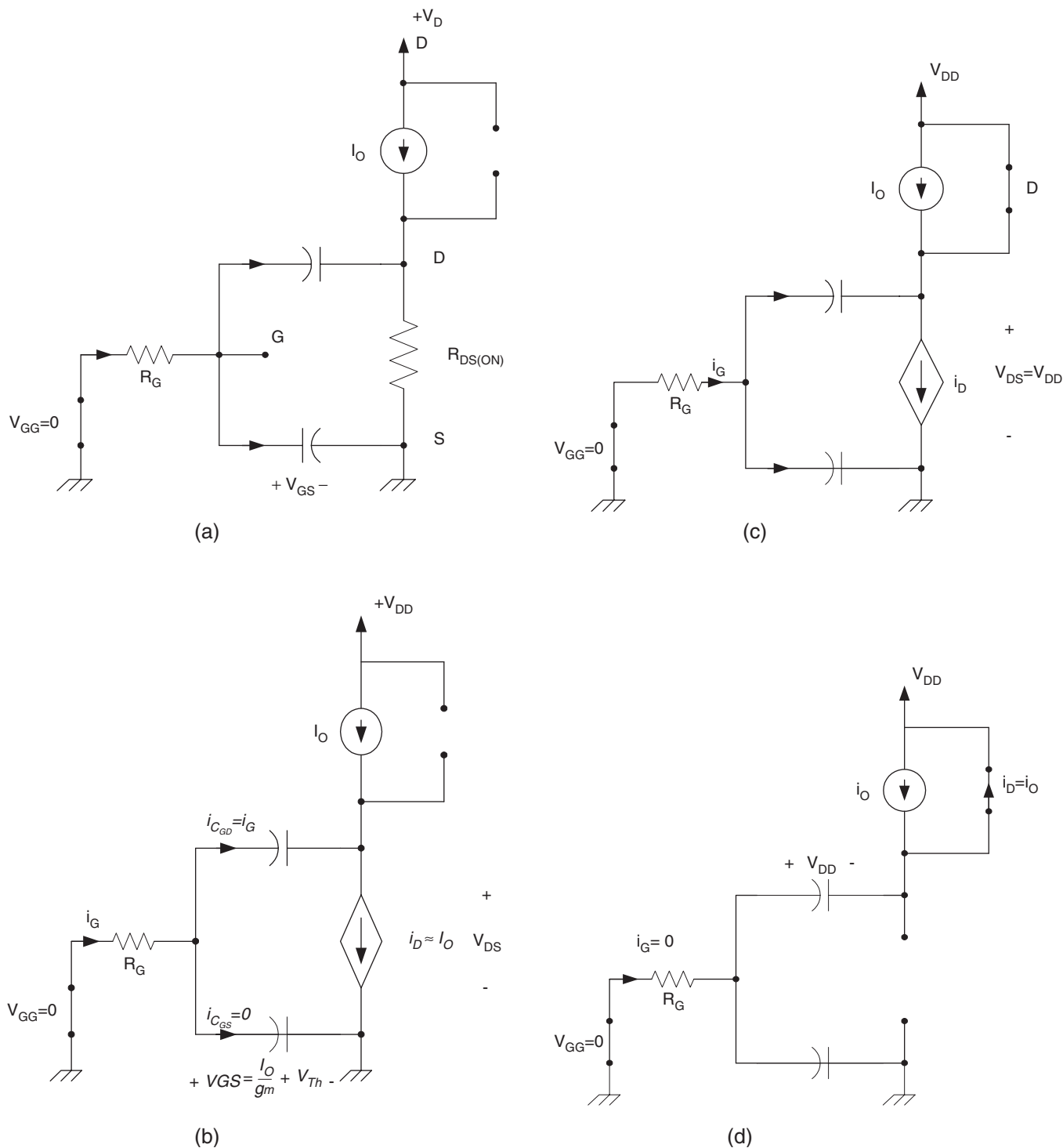
FIGURE 4.22   Equivalent circuits: (a) $t_0 \leq t < t_1$; (b) $t_1 \leq t < t_2$; (c) $t_2 \leq t < t_3$; and (d) $t_3 \leq t < t_4$.

the MOSFET t_{on} and t_{off} times, the gate–drain capacitance must be reduced. Readers are encouraged to see the reference by Baliga for detailed discussion on the turn-on and turn-off characteristics of the MOSFET and to explore various fabrication methods.

C. Safe Operation Area   The safe operation area (SOA) of a device provides the current and voltage limits. The device must handle to avoid destructive failure. Typical SOA for a MOSFET device is shown in Fig. 4.23. The maximum current limit while the device is on is determined by the maximum
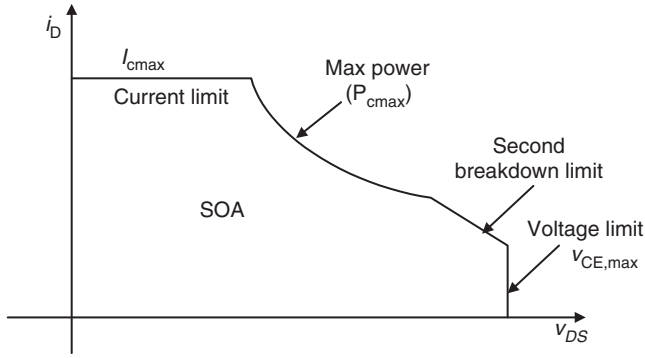
FIGURE 4.23   Safe operation area for MOSFET.
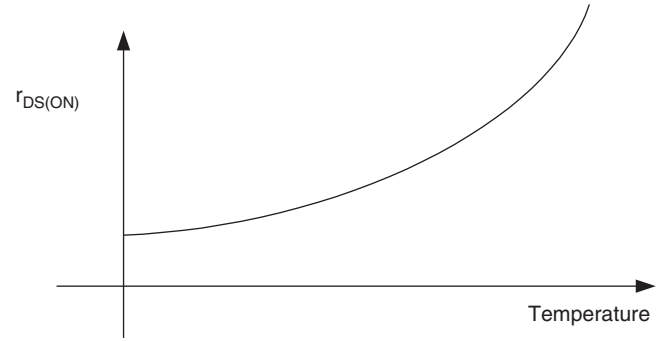
FIGURE 4.25   The on-state resistance as a fraction of temperature.

power dissipation

$$P_{diss,ON} = I_{DS(ON)}R_{DS(ON)}$$

As the drain–source voltage starts increasing, the device starts leaving the on-state and enters the saturation (linear) region. During the transition time, the device exhibits large voltage and current simultaneously. At higher drain–source voltage values that approach the avalanche breakdown it is observed that power MOSFET suffers from second breakdown phenomenon. The second breakdown occurs when the MOSFET is in the blocking state (off) and a further increase in v_{DS} will cause a sudden drop in the blocking voltage. The source of this phenomenon in MOSFET is caused by the presence of a parasitic n-type bipolar transistor as shown in Fig. 4.24.

The inherent presence of the body diode in the MOSFET structure makes the device attractive to application in which bi-directional current flow is needed in the power switches.
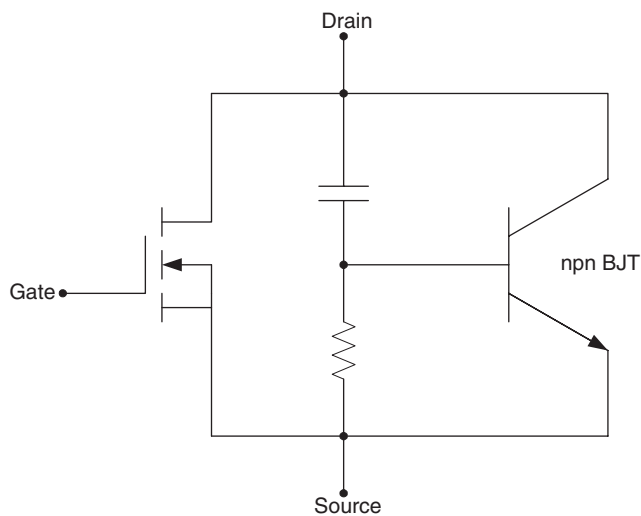
FIGURE 4.24   MOSFET equivalent circuit including the parasitic BJT.

Today's commercial MOSFET devices have excellent high operating temperatures. The effect of temperature is more prominent on the on-state resistance as shown in Fig. 4.25.

As the on-state resistance increases, the conduction losses also increase. This large $v_{DS(ON)}$ limits the use of the MOSFET in high voltage applications. The use of silicon carbide instead of silicon has reduced $v_{DS(ON)}$ by many folds.

As the device technology keeps improving in terms of improving switch speeds, increased power handling capabilities, it is expected that the MOSFET will continue to replace BJTs in all types of power electronics systems.

4.4.4 MOSFET PSPICE Model

The PSPICE simulation package has been used widely by electrical engineers as an essential software tool for circuit design. With the increasing number of devices available in the market place, PSPICE allows for the accurate extraction and understanding of various device parameters and their variation effect on the overall design prior to their fabrication. Today's PSPICE library is rich with numerous commercial MOSFET models. This section will give a brief overview of how the MOSFET model is implemented in PSPICE. A brief overview of the PSPICE modeling of the MOSFET device will be given here.

A. PSPICE Static Model   There are four different types of MOSFET models that are also known as *levels*. The simplest MOSFET model is called LEVEL1 model and is shown in Fig. 4.26 [9, 10].

LEVEL2 model uses the same parameters as LEVEL1, but it provides a better model for Ids by computing the model coefficients KP, VTO, LAMBDA, PHI, and GAMMA directly from the geometrical, physical, and technological parameters [10]. LEVEL3 is used to model the short-channel devices and LEVEL4 represents the Berkeley Short-channel IGFET model (BSIM-model).

FIGURE 4.26   PSPICE LEVEL1 MOSFET static model.

The triode region, $v_{GS} > V_{Th}$ and $v_{DS} < v_{GS}$ and $v_{DS} < v_{GS} - V_{Th}$ the drain current is given by,

$$i_D = \frac{K_P}{2} \frac{W}{L - 2X_{jl}} \left(v_{GS} - V_{Th} - \frac{v_{DS}}{2} \right) v_{DS}(1 + \lambda v_{DS})$$

$$(4.41)$$

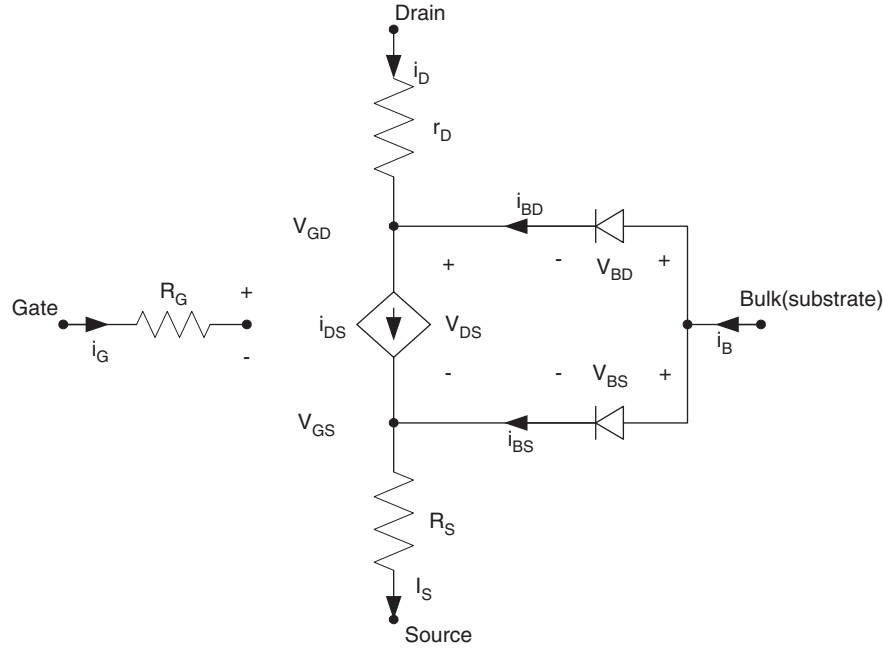In the saturation (linear) region, where $v_{GS} > V_{Th}$ and $v_{DS} > v_{GS} - V_{Th}$, the drain current is given by

$$I_D = \frac{K_P}{2} \frac{W}{L - 2X_{jl}} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS}) \qquad (4.42)$$

where K_P is the transconductance and X_{jl} is the lateral diffusion.

The threshold voltage, V_{Th}, is given by,

$$V_{Th} = V_{T0} + \partial \left(\sqrt{2\phi_P - V_{BS}} - \sqrt{2\phi_P} \right) \qquad (4.43)$$

where,

$V_{T0} =$ Zero-bias threshold voltage.
$\delta \quad =$ Body-effect parameter.
$\phi_P \quad =$ Surface inversion potential.

Typically, $X_{ij} \ll L$ and $\lambda \approx 0$.

The term $(1 + \lambda V_{DS})$ is included in the model as empirical connection to model the effect of the output conductance when the MOSFET is operating in triode region. λ is known as the channel-length modulation parameter.

When the bulk and source terminals are connected together, i.e. $V_{BS} = 0$, the device threshold voltage equals the zero-bias threshold voltage, i.e.

$$V_{Th} = V_{T0}$$

V_{T0} is positive for the n-channel enhancement-mode devices and negative for the n-channel depletion-mode devices.

The parameters K_P, V_{T0}, δ, ϕ are electrical parameters that can be either specified directly in the MODEL statement under the Pspice keywords KP, VTO, GAMMA, and PHI, respectively, as shown in Table 4.1. They also can be calculated when the geometrical and physical parameters are known. The two-substrate currents that flow from the bulk to the source, I_{BS} and from the bulk to the drain, I_{BD} are simply diode currents, which are given by,

$$I_{BS} = I_{SS} \left(e^{-(V_{BS}/V_T)} - 1 \right) \qquad (4.44)$$

$$I_{BD} = I_{DS} \left(e^{-(V_{BD}/V_T)} - 1 \right) \qquad (4.45)$$

where I_{SS} and I_{DS} are the substrate source and substrate drain saturation currents. These currents are considered equal and given as I_S in the MODEL statement with a default value of 10^{-14} A. Where the equation symbols and their corresponding PSPICE parameter names are shown in Table 4.1.

In PSPICE, a MOSFET device is described by two statements: the first statement start with the letter M and the

TABLE 4.1 PSPICE MOSFET parameters

Symbol	Name	Description	Default	Units
(a) Device dc and parasitic parameters				
Level	LEVEL	Model type (1, 2, 3, or 4)	1	–
V_{TO}	VTO	Zero-bias threshold voltage	0	V
λ	LAMDA	Channel-length modulation [1,2*]	0	v^{-1}
γ	GAMMA	Body-effect (bulk) threshold parameter	0	$v^{-1/2}$
Φ_ρ	PHI	Surface inversion potential	0.6	V
η	ETA	Static feedback[3]	0	–
κ	KAPPA	Saturation field factor[3]	0.2	–
μ_0	UO	Surface mobility	600	$cm^2/V \cdot s$
I_s	IS	Bulk saturation current	10^{-14}	A
J_s	JS	Bulk saturation current/area	0	A/m^2
J_{SSW}	JSSW	Bulk saturation current/length	0	A/m
N	N	Bulk emission coefficient n	1	–
P_B	PB	Bulk junction voltage	0.8	V
P_{BSW}	PBSW	Bulk sidewall diffusion voltage	PB	V
R_D	RD	Drain resistance	0	Ω
R_S	RS	Source resistance	0	Ω
R_G	RG	Gate resistance	0	Ω
R_B	RB	Bulk resistance	0	Ω
R_{ds}	RDS	Drain–source shunt resistance	α	Ω
R_{sh}	RSH	Drain and source diffusion sheet resistance	0	$Ω/m^2$
(b) Device process and dimensional parameters				
N_{sub}	NSUB	Substrate doping density	None	cm^{-3}
W	W	Channel width	DEFW	m
L	L	Channel length	DEFL	m
W_D	WD	Lateral Diffusion width	0	m
X_{jl}	LD	Lateral Diffusion length	0	m
K_p	KP	Transconductance coefficient	20 μ	A/v^2
t_{OX}	TOX	Oxide thickness	10^{-7}	m
N_{SS}	NSS	Surface-state density	None	cm^{-2}
N_{FS}	NFS	Fast surface-state density	0	cm^{-2}
N_A	NSUB	Substrate doping	0	cm^{-3}
T_{PG}	TPG	Gate material	1	–
		+1 Opposite of substrate	–	–
		−1 Same as substrate	–	–
		0 Aluminum	–	–
X_j	XJ	Metallurgical junction depth[2,3]	0	m
μ_0	UO	Surface mobility	600	$cm^2/V \cdot s$
U_c	UCRIT	Mobility degradation critical field[2]	10^4	V/cm
U_e	UEXP	Mobility degradation exponent[2]	0	–
U_t	VMAX	Maximum drift velocity of carriers[2]	0	m/s
N_{eff}	NEFF	Channel charge coefficient[2]	1	–
δ	DELTA	Width effect on threshold[2,3]	0	–
θ	THETA	Mobility modulation[3]	0	–
(c) Device capacitance parameters				
C_{BD}	CBD	Bulk-drain zero-bias capacitance	0	F
C_{BS}	CBS	Bulk-source zero-bias capacitance	0	F
C_j	CJ	Bulk zero-bias bottom capacitance	0	F/m^2
C_{jsw}	CJSW	Bulk zero-bias perimeter capacitance/length	0	F/m
M_j	MJ	Bulk bottom grading coefficient	0.5	–
M_{jsw}	MJSW	Bulk sidewall grading coefficient	0.33	–
F_C	FC	Bulk forward-bias capacitance coefficient	0.5	–
C_{GSO}	CGSO	Gate–source overlap capacitance/channel width	0	F/m
C_{GDO}	CGDO	Gate–drain overlap capacitance/channel width	0	F/m
C_{GBO}	CGBO	Gate-bulk overlap capacitance/channel length	0	F/m
X_{QC}	XQC	Fraction of channel charge that associates with drain[1,2]	0	–
K_F	KF	Flicker noise coefficient	0	–
α_F	AF	Flicker noise exponent	0	–

*These numbers indicate that this parameter is available in this level number, otherwise it is available in all levels.

second statement starts with .Model that defines the model used in the first statement. The following syntax is used:

```
M<device_name><Drain_node_number>
<Gate_node_number>
<Source_node_number><Substrate_node number>
<Model_name>
* [<param_1>=<value_1><param_2>=<value_2>....]
.MODEL <Model_name><type_name>
[(<param_1>=<value_1>
<param_2>=<value_2>....]
```

where the starting letter "M" in M<device_name> statement indicates that the device is a MOSFET and <device_name>is a user specified label for the given device, the <Model_name> is one of the hundreds of device models specified in the PSPICE library, <Model_name> the same name specified in the device name statement, <type_name> is either NMOS of PMOS, depending on whether the device is n-channel or p-channel MOS, respectively, that follows by optional list of parameter types and their values. The length *L* and the width *W* and other parameters can be specified in the M<device_name>, in the .MODEL or .OPTION statements. User may select not to include any value, and PSPICE will use the specified default values in the model. For normal operation (physical construction of the MOS devices), the source and bulk substrate nodes must be connected together. In all the PSPICE library files, a default parameter values for L, W, AS, AD, PS, PD, NRD, and NDS are included, hence, user should not specify such values in the device "M" statement or in the OPTION statement.

The power MOSFET device PSPICE models include relatively complete static and dynamic device characteristics given in the manufacturing data sheet. In general, the following effects are specified in a given PSPICE model: dc transfer curves, on-resistance, switching delays, and gate drive characteristics and reverse-mode "body-diode" operation. The device characteristics that are not included in the model are noise, latch-ups, maximum voltage, and power ratings. Please see OrCAD Library Files.

> **EXAMPLE 4.3** Let us consider an example of using IRF MOSFET that was connected as shown in Fig. 4.27.
>
> It was decided that the device should have a blocking voltage (V_{DSS}) of 600 V and drain current, i_d, of 3.6 A. The device selected is IRF CC30 with case TO220. This device is listed in PSPICE library under model number IRFBC30 as follows:

```
*Library of Power MOSFET Models
*Copyright OrCAD, Inc. 1998 All Rights Reserved.
*
*$Revision: 1.24 $
*$Author: Rperez $
*$Date: 19 October 1998 10:22:26 $
*
. Model IRFBC30 NMOS NMOS
```
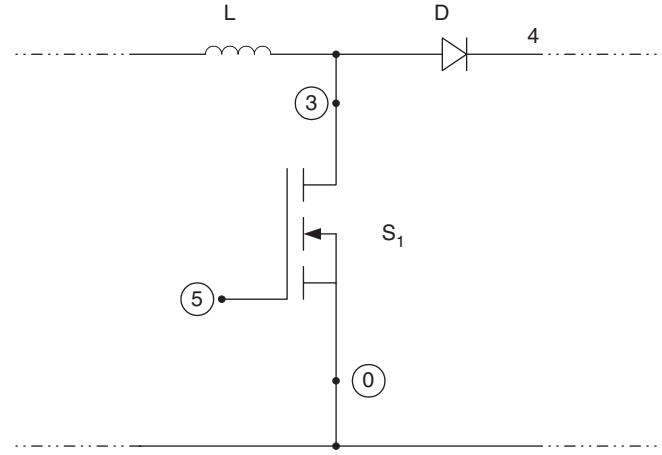

FIGURE 4.27 Example of a power electronic circuit that uses a power MOSFET.

The PSPICE code for the MOS device labeled S1 used in Fig. 4.27 is given by,

```
MS1 3 5 0 0 IRFBC30
.MODEL IRFBC30
.Model IRFBC30 NMOS(Level=3 Gamma=0 Delta=0
 Eta=0 Theta=0 Kappa=0.2 Vmax=0 Xj=0
+ Tox=100n Uo=600 Phi=.6 Rs=5.002m Kp=20.43u
 W=.35 L=2u Vto=3.625
+ Rd=1.851 Rds=2.667MEG Cbd=790.1p Pb=.8 Mj=.5
 Fc=.5 Cgso=1.64n
+ Cgdo=123.9p Rg=1.052 Is=720.2p N=1 Tt=685)
* Int'l Rectifier pid=IRFCC30 case=TO220
```

4.4.5 MOSFET Large-signal Model

The equivalent circuit of Fig. 4.28 includes five device parasitic capacitances. The capacitors C_{GB}, C_{GS}, C_{GD}, represent the charge-storage effect between the gate terminal and the bulk, source, and drain terminals, respectively. These are non-linear two-terminal capacitors expressed as function of W, L, C_{ox}, V_{GS}, V_{T0}, V_{DS}, and C_{GBO}, C_{GSO}, C_{GDO}, where the capacitors C_{GBO}, C_{GSO}, C_{GDO} are outside the channel region, known as overlap capacitances, that exist between the gate electrode and the other three terminals, respectively. Table 4.1 shows the list of PSPICE MOSFET capacitance parameters and their default values. Notice that the PSPICE overlap capacitors keywords (C_{GBO}, C_{GSO}, C_{GDO}) are proportional either to the MOSFET width or length of the channel as follows:

$$C_{GBO} = \frac{C_{GBO}}{L}$$

$$C_{GSO} = \frac{C_{GSO}}{W} \qquad (4.46)$$
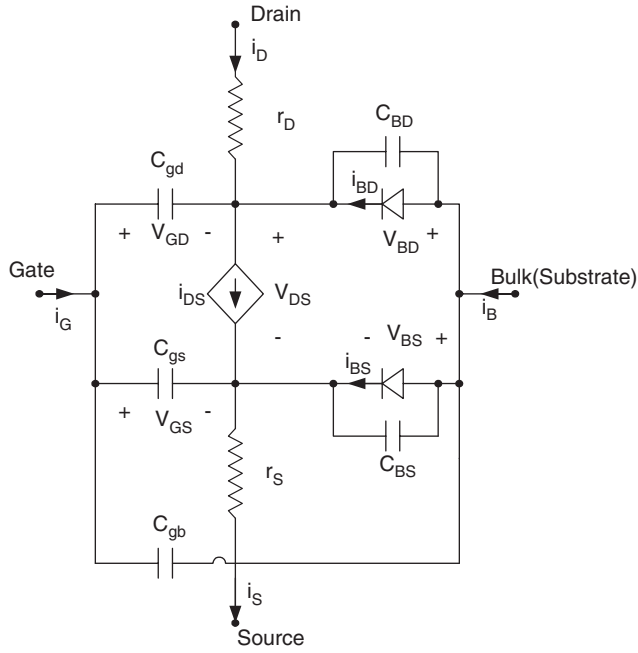
$$C_{GDO} = \frac{C_{GDO}}{W}$$

FIGURE 4.28 Large-signal model for the n-channel MOSFET.

FIGURE 4.29 Small-signal equivalent circuit model for MOSFET.

In the triode region, $v_{GS} > v_{DS} - V_{Th}$, the terminal capacitors are given by,

$$C_{GS} = L_W C_{OX} \left[1 - \left(\frac{v_{GS} - v_{DS} - V_{Th}}{2(v_{GS} - V_{Th}) - V_{DS}} \right)^2 \right] + C_{GSO}$$

$$C_{GD} = L_W C_{OX} \left[1 - \left(\frac{v_{GS} - V_{Th}}{2(v_{GS} - V_{Th}) - v_{DS}} \right)^2 \right] + C_{GDO}$$

$$C_{GB} = C_{GBO} L \tag{4.47}$$

In the saturation (linear) region, we have

$$C_{GS} = \frac{2}{3} L_W C_{OX} + C_{GSO}$$

$$C_{GB} = C_{GB0} L \tag{4.48}$$

$$C_{GD} = C_{GD0}$$

where C_{OX} is the per-unit-area oxide capacitance given by,

$$C_{OX} = \frac{K_{OX} E_0}{T_{OX}}$$

K_{OX} = Oxide's relative dielectric constant.
E_0 = Free space dielectric constant equals
       8.854×10^{-12} F/m.
T_{OX} = Oxide's thickness layer given as T_{OX} in Table 4.1.

Finally, the diffusion and junction region capacitances between the bulk-to-channel (drain and source) are modeled by C_{BD} and C_{BS} across the two diodes. Because for almost all power MOSFETs, the bulk and source terminals are connected together and at zero potential, diodes D_{BD} and D_{BS} don't have forward bias, resulting in very small conductance values, i.e. small diffusion capacitances. The small-signal model for MOSFET devices is given in Fig. 4.29.

EXAMPLE 4.4   Figure 4.30a shows an example of a soft-switching power factor connection circuit that has two MOSFETs. Its PSPICE simulation waveforms are shown in Fig. 4.30b.

Table 4.2 shows the PSPICE code for Fig. 4.30a.

4.4.6 Current MOSFET Performance

The current focus of MOSFET technology development is much more broad than power handling capacity and switching speed; the size, packaging, and cooling of modern MOSFET technology is a major focus. Of course, the development of higher power and efficiency is still paramount, but as modern electronics have become increasingly smaller, the packaging and cooling of power circuits has become more important. It has been indicated by manufacturers that many of their modern MOSFETs are not limited by their semiconductor, but by the packaging. If the MOSFET cannot properly disperse heat, the device will become overheated, which will lead to failure.

An example of modern MOSFET technology is the DirectFET surface mounted MOSFET manufactured by International Rectifier. Part number IRF6662, for example, can handle 47 A at 100 V, while consuming a board space of

(a)

(b)
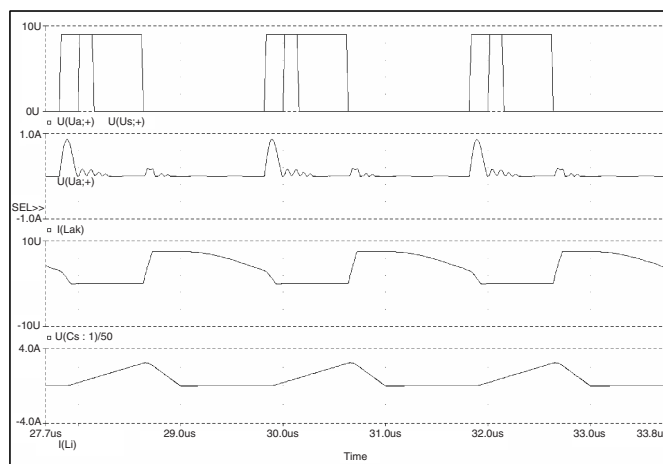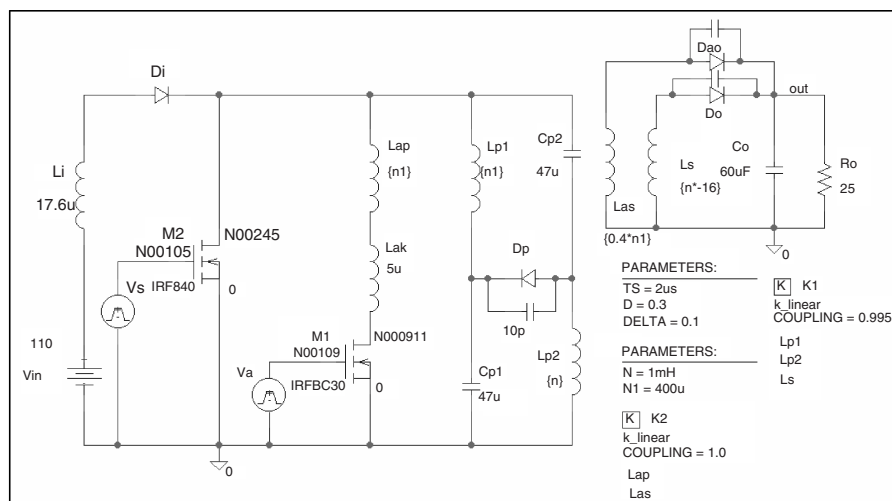
FIGURE 4.30 (a) Example of power electronic circuit and (b) PSPICE simulation waveforms.

DirectFET™ ISOMETRIC

board through a large contact patch, and by using materials with high heat conductivity, the switch has a very high surface area vs volume ratio, which allows for the heat to be dissipated through the top heat sink as well as through the circuit board.

Another example of manufacturers that are focusing on packaging and cooling to increase the performance of their products is Vishay's PolarPAK and PowerPAK. These devices have a 65% smaller board surface area than traditional SO-8 packages. Also, the thermal conductivity of the package is 88%

5×6 mm, and being only 0.6 mm thick. This switch is efficient at frequencies greater than 1 MHz, and the packaging can dissipate over 50% more heat than traditional surface mounted MOSFETs of similar power ratings. The power density of this switch is many times the power density of similarly rated devices made by International Rectifier in the past. One major factor in the performance gain of this product line is dual-sided cooling. By designing the package to mount to the

TABLE 4.2 PSPICE MOSFET capacitance parameters and their default values for Fig. 4.30a

```
* source ZVT-ZCS
D_Do                              N00111  OUT  Dbreak
V_Vs                              N00105  0  DC  0  AC  0  PULSE  0  9  0  0  0  {D*Ts}  {Ts}
L_Ls                              0  N00111  {n*.16}
Kn_K1                             L_Lp1  L_Lp2  L_Ls    0.995
C_Co                              OUT  0  60uF  IC=50
V_Vin                             N00103  0  110
L_Li                              N00103  N00099    17.6u  IC=0
V_Va                              N00109  0  DC  0  AC  0  PULSE  0  9  {-Delta*Ts/1.1}  0  0  {2.0*Delta*Ts}
{Ts}
D_Dp                              N00121  N00169  Dbreak
C_C7                              N00111  OUT    30p
R_Ro                              OUT  0  25
C_C8                              N00143  OUT    10p
D_Dao                             N00143  OUT  Dbreak
D_Di                              N00099  N00245  Dbreak
L_Lp2                             N00121  0    {n}  IC=0
C_C9                              N00169  N00121    10p
L_Las                             N00143  0  {0.4*n1}
Kn_K2                             L_Lap  L_Las    1.0
L_Lp1                             N00245  N00169    {n}  IC=0
L_Lap                             N00245  N000791    {n1}
C_Cp2                             N00245  N00121  47u  IC=170
C_Cp1                             N00169  0    47u  IC=170
L_Lak                             N000791  N000911    5u  IC=0
M_M1                              N000911  N00109  0  0  IRFBC30
M_M2                              N00245  N00105  0  0  IRF840
.PARAM  D=0.3  DELTA=0.1  N1=400u  N=1mH    TS=2us
```

```
         **** MOSFET MODEL PARAMETERS
**************************************************
              IRFBC30        IRF840
              NMOS           NMOS
LEVEL         3              3
L             2.000000E-06   2.000000E-06
W             .35            .68
VTO           3.625          3.879
KP            20.430000E-06  20.850000E-06
GAMMA         0              0
PHI           .6             .6
LAMBDA        0              0
RD            1.851          .6703
RS            5.002000E-03   6.382000E-03
RG            1.052          .6038
RDS           2.667000E+06   2.222000E+06
IS            720.200000E-12 56.030000E-12
JS            0              0
PB            .8             .8
PBSW          .8             .8
CBD           790.100000E-12 1.415000E-09
CJ            0              0
CJSW          0              0
TT            685.000000E-09 710.000000E-09
CGSO          1.640000E-09   1.625000E-09
CGDO          123.900000E-12 133.400000E-12
CGBO          0              0
TOX           100.000000E-09 100.000000E-09
XJ            0              0
UCRIT         10.000000E+03  10.000000E+03
DELTA         0              0
ETA           0              0
DIOMOD        1              1
VFB           0              0
LETA          0              0
WETA          0              0
U0            0              0
TEMP          0              0
VDD           0              0
XPART         0              0
```

greater than traditional devices. The PolarPAK device increases the performance by cooling the part from the top and the bottom of the package. These advances in packaging and cooling have allowed the devices to have power densities greater than 250 W/mm^3 as well, while maintaining high efficiencies into the megahertz.

Another important characteristic of any solid-state device is the expected service life. For MOSFETs, manufacturers have indicated that the mean time before failure (MTBF) approximately decreases by 50% for every 10°C that the operational temperature increases. For this reason, the current

Examples of modern MOSFETs

Device type	Rated voltage	Rated current	Frequency limit	Rated power	Footprint mm^2
High voltage	1000 V	6.1 A	1 MHz	6 kW	310
High voltage	600 V	40 A	1 MHz	24 kW	320
High power	100 V	180 A	500 kHz	18 kW	310
High current	40 V	280 A	1 MHz	11 kW	310
High efficiency	30 V	40 A	2 MHz	1.2 kW	31.5
High efficiency	30 V	60 A	2 MHz	1.8 kW	36
High efficiency	100 V	47 A	2 MHz	4.7 kW	30.9
High freq. – low power	10 V	0.7 A	200 MHz	7 W	21

advancement in cooling and packaging has a direct effect on the longevity of the components. While there are definite increases in device longevity every year, the easiest way to have a large impact on the life of the device is to keep the temperature down.

As development continues, MOSFETs will become smaller, more efficient, higher power density, and higher frequency of operation. As such, MOSFETs will continue to expand into applications that typically use other forms of power switches.

4.5 Future Trends in Power Devices

As stated earlier, depending on the applications, the power range processed in power electronic range is very wide, from hundreds of milliwatts to hundreds of megawatts, therefore, it is very difficult to find a single switching device type to cover all power electronic applications. Today's available power devices have tremendous power and frequency rating range as well as diversity. Their forward current ratings range from a few amperes to a few kiloamperes, blocking voltage rating ranges from a few volts to a few of kilovolts, and switching frequency ranges from a few hundred of hertz to a few megahertz as illustrated in Table 4.3. This table illustrates the relative comparison between available power semiconductor devices. We only give relative comparison because there is no straightforward technique that gives ranking of these devices. As we accumulate this table, devices are still being developed very rapidly with higher current, voltage ratings, and switching frequency.

It is expected that improvement in power handling capabilities and increasing frequency of operation of power devices will continue to drive the research and development in semiconductor technology. From power MOSFET to power MOS-IGBT and to power MOS-controlled thyristors, power rating has consistently increased by a factor of 5 from one type to another. Major research activities will focus on obtaining new device structure based on MOS-BJT technology integration to rapidly increase power ratings. It is expected that the power MOS-BJT technology will capture more than 90% of the total power transistor market.

The continuing development of power semiconductor technology has resulted in power systems with driver circuit, logic and control, device protection, and switching devices being designed and fabricated on a single-chip. Such power IC modules are called "smart power" devices. For example, some of today's power supplies are available as IC's for use in low-power applications. No doubt the development of smart power devices will continue in the near future, addressing more power electronic applications.

TABLE 4.3 Comparison of power semiconductor devices

Device type	Year made available	Rated voltage	Rated current	Rated frequency	Rated power	Forward voltage
Thyristor (SCR)	1957	6 kV	3.5 kA	500 Hz	100's MW	1.5–2.5 V
Triac	1958	1 kV	100 A	500 Hz	100's kW	1.5–2 V
GTO	1962	4.5 kV	3 kA	2 kHz	10's MW	3–4 V
BJT (Darlington)	1960s	1.2 kV	800 A	10 kHz	1 MW	1.5–3 V
MOSFET	1976	500 V	50 A	1 MHz	100 kW	3–4 V
IGBT	1983	1.2 kV	400 A	20 kHz	100's kW	3–4 V
SIT		1.2 kV	300 A	100 kHz	10's kW	10–20 V
SITH		1.5 kV	300 A	10 kHz	10's kW	2–4 V
MCT	1988	3 kV	2 kV	20–100 kHz	10's MW	1–2 V

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