6

Thyristors

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6.1 Introduction

Thyristors are usually three-terminal devices that have four layers of alternating *p*-type and *n*-type material (i.e. three *p*–*n* junctions) comprising its main power handling section. In contrast to the linear relation which exists between load and control currents in a transistor, the thyristor is bistable. The control terminal of the thyristor, called the gate (*G*) electrode, may be connected to an integrated and complex structure as a part of the device. The other two terminals, called the anode (*A*) and cathode (*K*), handle the large applied potentials (often of both polarities) and conduct the major current through the thyristor. The anode and cathode terminals are connected in series with the load to which power is to be controlled.

Thyristors are used to approximate ideal closed (no voltage drop between anode and cathode) or open (no anode current flow) switches for control of power flow in a circuit. This differs from low-level digital switching circuits that are designed to deliver two distinct small voltage levels while conducting small currents (ideally zero). Thyristor circuits must have the capability of delivering large currents and be able to withstand large externally applied voltages. All thyristor types are controllable in switching from a forward-blocking state (positive potential applied to the anode with respect to the cathode, with correspondingly little anode current flow) into a forward-conduction state (large forward anode current flowing, with a small anode–cathode potential drop). Most thyristors have the characteristic that after switching from a forward-blocking state into the forward-conduction state, the gate signal can be removed and the thyristor will remain in its forward-conduction mode. This property is termed "latching" and is an important distinction between thyristors and other types of power electronic devices. Some thyristors are also controllable in switching from forward-conduction back to a forward-blocking state. The particular design of a thyristor will determine its controllability and often its application.

Thyristors are typically used at the highest energy levels in power conditioning circuits because they are designed to handle the largest currents and voltages of any device technology (systems approximately with voltages above 1 kV or currents above 100 A). Many medium-power circuits (systems operating at less than 1 kV or 100 A) and particularly

low-power circuits (systems operating below 100 V or several amperes) generally make use of power bipolar transistors, power metal oxide semiconductor field effect transistors (MOSFETs) or insulated gate bipolar transistors (IGBTs) as the main switching elements because of the relative ease in controlling them. IGBT technology, however, continues to improve and multiple silicon die are commonly packaged together in a module. These modules are replacing thyristors in applications operating up to 3 kV that require controllable turn-off because of easier gate-drive requirements. Power diodes are used throughout all levels of power conditioning circuits and systems for component protection and wave shaping.

A thyristor used in some ac power circuits (50 or 60 Hz in commercial utilities or 400 Hz in aircraft) to control ac power flow can be made to optimize internal power loss at the expense of switching speed. These thyristors are called phase-control devices, because they are generally turned from a forward-blocking into a forward-conducting state at some specified phase angle of the applied sinusoidal anode–cathode voltage waveform. A second class of thyristors is used in association with dc sources or in converting ac power at one amplitude and frequency into ac power at another amplitude and frequency, and must generally switch on and off relatively quickly. A typical application for the second class of thyristors is in converting a dc voltage or current into an ac voltage or current. A circuit that performs this operation is often called an inverter, and the associated thyristors used are referred to as inverter thyristors.

There are four major types of thyristors: (i) the silicon-controlled rectifier (SCR); (ii) the gate turn-off thyristor (GTO) and its close relative the integrated gate commutated thyristor (IGCT); (iii) the MOS-controlled thyristor (MCT) and its various forms; and (iv) the static induction thyristor (SITh). MCTs are so-named because many parallel enhancement mode, MOSFET structures of one charge type are integrated into the thyristor for turn-on and many more MOSFETs of the other charge type are integrated into the thyristor for turn-off. A SITh or field-controlled thyristor (FCTh), has essentially the same construction as a power diode with a gate structure that can pinch-off anode current flow. Although MCTs, derivative forms of the MCT and SIThs have the advantage of being essentially voltage-controlled devices (i.e. little control current is required for turn-on or turn-off, and therefore require simplified control circuits attached to the gate electrode), they are currently only found in niche applications such as pulse power. Detailed discussion of variations of MCTs and SIThs, as well as additional references on these devices are discussed by Hudgins in [1]. Other types of thyristors include the Triac (a pair of anti-parallel SCRs integrated together to form a bi-directional current switch) and the programmable unijunction transistor (PUT).

The SCRs and GTOs are designed to operate at all power levels. These devices are primarily controlled using electrical signals (current), though some types are made to be controlled using optical energy (photons) for turn-on. Subclasses of SCRs and GTOs are reverse conducting types and symmetric structures that block applied potentials in the reverse and forward polarities. Other variations of GTOs are the gate-commutated turn-off thyristor (GCT), commonly available as the IGCT, and the bi-directional controlled thyristor (BCT). Most power converter circuits incorporating thyristors make use of SCRs, GTOs, or IGCTs, and hence the chapter will focus on these devices, though the basics of operation are applicable to all thyristor types.

All power electronic devices must be derated (e.g. power dissipation levels, current conduction, voltage blocking, and switching frequency must be reduced), when operating above room temperature (defined as approximately 25°C). Bipolar-type devices have thermal runaway problems, in that if allowed to conduct unlimited current, these devices will heat up internally causing more current to flow, thus generating more heat, and so forth until destruction. Devices that exhibit this behavior are *pin* diodes, bipolar transistors, and thyristors.

Almost all power semiconductor devices are made from silicon (Si). Research and development continues in developing other types of devices in silicon carbide (SiC), gallium nitride (GaN), and related material systems. However, the physical description and general behavior of thyristors is unimportant to the semiconductor material system used, though the discussion and any numbers cited in the chapter will be associated with Si devices.

6.2 Basic Structure and Operation

Figure 6.1 shows a conceptual view of a typical thyristor with the three *p–n* junctions and the external electrodes labeled. Also shown in the figure is the thyristor circuit symbol used in electrical schematics.

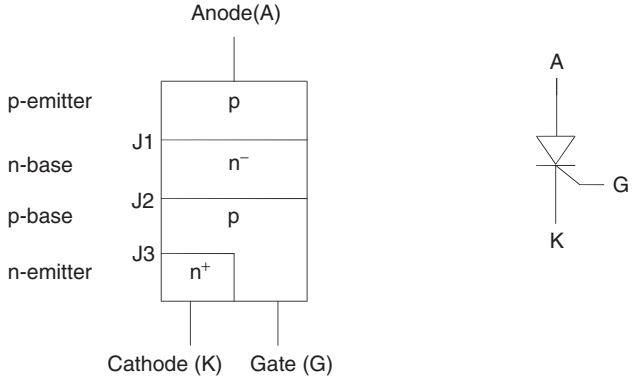

FIGURE 6.1 Simple cross section of a typical thyristor and the associated electrical schematic symbols.

A high-resistivity region, *n*-base, is present in all thyristors. It is this region, the *n*-base and associated junction, J_2 of Fig. 6.1, which must support the large applied forward voltages that occur when the switch is in its off- or forward-blocking state (non-conducting). The *n*-base is typically doped with impurity phosphorous atoms at a concentration of 10^{13} to $10^{14}\,cm^{-3}$. The *n*-base can be tens to hundreds of micrometer thick to support large voltages. High-voltage thyristors are generally made by diffusing aluminum or gallium into both surfaces to create *p*-doped regions forming deep junctions with the *n*-base. The doping profile of the *p*-regions ranges from about 10^{15} to $10^{17}\,cm^{-3}$. These *p*-regions can be up to tens of micrometer thick. The cathode region (typically only a few micrometer thick) is formed by using phosphorous atoms at a doping density of 10^{17} to $10^{18}\,cm^{-3}$.

The higher the forward-blocking voltage rating of the thyristor, the thicker the *n*-base region must be. However, increasing the thickness of this high-resistivity region results in slower turn-on and turn-off (i.e. longer switching times and/or lower frequency of switching cycles because of more stored charge during conduction). For example, a device rated for a forward-blocking voltage of 1 kV will, by its physical construction, switch much more slowly than one rated for 100 V. In addition, the thicker high-resistivity region of the 1 kV device will cause a larger forward voltage drop during conduction than the 100 V device carrying the same current. Impurity atoms, such as platinum or gold, or electron irradiation are used to create charge-carrier recombination sites in the thyristor. The large number of recombination sites reduces the mean carrier lifetime (average time that an electron or hole moves through the Si before recombining with its opposite charge-carrier type). A reduced carrier lifetime shortens the switching times (in particular the turn-off or recovery time) at the expense of increasing the forward-conduction drop. There are other effects associated with the relative thickness and layout of the various regions that make up modern thyristors, but the major tradeoff between forward-blocking voltage rating and switching times, and between forward-blocking voltage rating and forward-voltage drop during conduction should be kept in mind. (In signal-level electronics an analogous tradeoff appears as a lowering of amplification (gain) to achieve higher operating frequencies, and is often referred to as the gain-bandwidth product.)

Operation of thyristors is as follows. When a positive voltage is applied to the anode (with respect to cathode), the thyristor is in its forward-blocking state. The center junction, J_2 (see Fig. 6.1) is reverse biased. In this operating mode the gate current is held to zero (open circuit). In practice, the gate electrode is biased to a small negative voltage (with respect to the cathode) to reverse bias the GK-junction J_3 and prevent charge-carriers from being injected into the *p*-base. In this condition only thermally generated leakage current flows through the device and can often be approximated as zero in value (the actual value of the leakage current is typically many orders of magnitude lower than the conducted current in the on-state). As long as the forward applied voltage does not exceed the value necessary to cause excessive carrier multiplication in the depletion region around J_2 (avalanche breakdown), the thyristor remains in an off-state (forward-blocking). If the applied voltage exceeds the maximum forward-blocking voltage of the thyristor, it will switch to its on-state. However, this mode of turn-on causes non-uniformity in the current flow, is generally destructive, and should be avoided.

When a positive gate current is injected into the device, J_3 becomes forward biased and electrons are injected from the *n*-emitter into the *p*-base. Some of these electrons diffuse across the *p*-base and get collected in the *n*-base. This collected charge causes a change in the bias condition of J_1. The change in bias of J_1 causes holes to be injected from the *p*-emitter into the *n*-base. These holes diffuse across the *n*-base and are collected in the *p*-base. The addition of these collected holes in the *p*-base acts the same as gate current. The entire process is regenerative and will cause the increase in charge carriers until J_2 also becomes forward biased and the thyristor is latched in its on-state (forward-conduction). The regenerative action will take place as long as the gate current is applied in sufficient amount and for a sufficient length of time. This mode of turn-on is considered to be the desired one as it is controlled by the gate signal.

This switching behavior can also be explained in terms of the two-transistor analog shown in Fig. 6.2. The two transistors are regeneratively coupled so that if the sum of their forward current gains (α's) exceeds unity, each drives the other into saturation. Equation 6.1 describes the condition necessary for the thyristor to move from a forward-blocking state into the forward-conduction state. The forward current gain (expressed as the ratio of collector current to emitter current) of the *pnp* transistor is denoted by α_p, and that of the *npn* as α_n. The α's are current dependent and increase slightly as the current increases. The center junction J_2 is reverse biased under forward applied voltage (positive, v_{AK}). The associated electric field in the depletion region around the junction can result

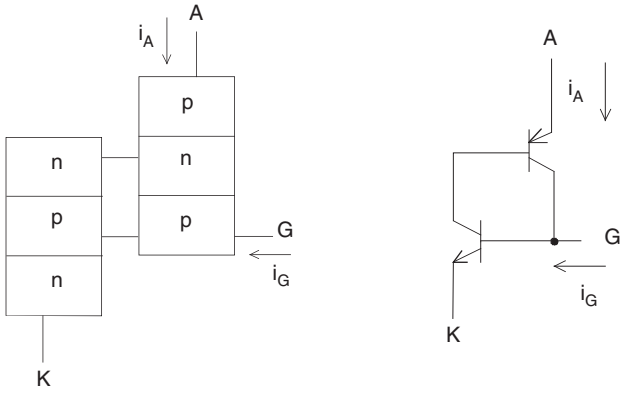

FIGURE 6.2 Two-transistor behavioral model of a thyristor.

in significant carrier multiplication, denoted as a multiplying factor M on the current components, I_{co} and i_G.

$$i_A = \frac{MI_{co} + M\alpha_n i_G}{1 - M(\alpha_n + \alpha_p)} \tag{6.1}$$

In the forward-blocking state, the leakage current I_{co} is small, both α's are small, and their sum is less than unity. Gate current increases the current in both transistors, increasing their α's. Collector current in the *npn* transistor acts as base current for the *pnp*, and analogously, the collector current of the *pnp* acts as base current driving the *npn* transistor. When the sum of the two α's equals unity, the thyristor switches to its on-state (latches). This condition can also be reached, without any gate current, by increasing the forward applied voltage so that carrier multiplication (M >> 1) at J_2 increases the internal leakage current, thus increasing the two α's. A third way to increase the α's exists by increasing the device (junction) temperature. Increasing the temperature causes a corresponding increase in the leakage current I_{co} to the point where latching can occur. The typical manifestation of this temperature dependence is to cause an effective lowering of the maximum blocking voltage that can be sustained by the thyristor.

Another way to cause a thyristor to switch from forward-blocking to forward-conduction exists. Under a forward applied voltage, J_2 is reverse biased while the other two junctions are forward-biased in the blocking mode. The reverse-biased junction of J_2 is the dominant capacitance of the three and determines the displacement current that flows. If the rate of increase in the applied v_{AK} (dv_{AK}/dt) is sufficient, it will cause a significant displacement current through the J_2 capacitance. This displacement current can initiate switching similar to an externally applied gate current. This dynamic phenomenon is inherent in all thyristors and causes there to be a limit (dv/dt) to the time rate of applied v_{AK} that can be placed on the device to avoid uncontrolled switching. Alterations to the basic thyristor structure can be produced that increase the dv/dt limit and will be discussed in Section 6.4.

Once the thyristor has moved into forward-conduction, any applied gate current is superfluous. The thyristor is latched and, for SCRs, cannot be returned to a blocking mode by using the gate terminal. Anode current must be commutated away from the SCR for a sufficient time to allow stored charge in the device to recombine. Only after this recovery time has occurred, can a forward voltage be reapplied (below the dv/dt limit of course) and the SCR again be operated in a forward-blocking mode. If the forward voltage is reapplied before sufficient recovery time has elapsed, the SCR will move back into forward-conduction. For GTOs and IGCTs, a large applied reverse gate current (typically in the range of 10–50% of the anode current for GTOs, and 100% of the anode current for IGCTs) applied for a sufficient time can remove enough charge near the GK junction to cause it to turn-off. This interrupts the base current to the *pnp* transistor, leaving the *pnp* open-base, causing thyristor turn-off. This is similar in principle to use negative base current to quickly turn-off a traditional bipolar transistor.

6.3 Static Characteristics

6.3.1 Current–Voltage Curves for Thyristors

A plot of the anode current (i_A) as a function of anode–cathode voltage (v_{AK}) is shown in Fig. 6.3. The forward-blocking mode is shown as the low-current portion of the graph (solid curve around operating point "1"). With zero gate current and positive v_{AK}, the forward characteristic in the off- or blocking-state is determined by the center junction J_2, which is reverse biased. At operating point "1" very little current flows (I_{co} only) through the device. However, if the applied voltage exceeds the forward-blocking voltage, the thyristor switches to its on- or conducting-state (shown as operating point "2") because of carrier multiplication (M in Eq. (6.1)). The effect of gate current is to lower the blocking voltage at which switching takes place. The thyristor moves rapidly along the negatively-sloped portion of the curve until it reaches a stable operating point determined by the external circuit (point "2"). The portion of the graph indicating forward-conduction shows the large values of i_A that may be conducted at relatively low values of v_{AK}, similar to a power diode.

As the thyristor moves from forward-blocking to forward-conduction, the external circuit must allow sufficient anode current to flow to keep the device latched. The minimum anode current that will cause the device to remain in forward-conduction as it switches from forward-blocking is called the

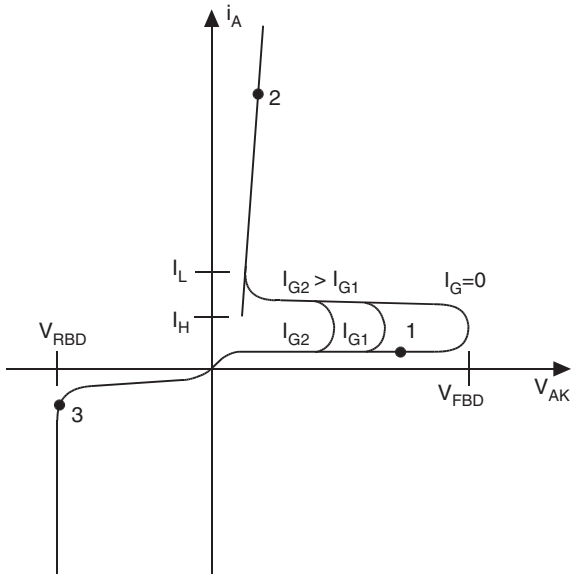

FIGURE 6.3 Static characteristic *i–v* curve typical of thyristors.

latching current I_L. If the thyristor is already in forward-conduction and the anode current is reduced, the device can move its operating mode from forward-conduction back to forward-blocking. The minimum value of anode current necessary to keep the device in forward-conduction after it has been operating at a high anode current value is called the holding current I_H. The holding current value is lower than the latching current value as indicated in Fig. 6.3.

The reverse thyristor characteristic, quadrant III of Fig. 6.3, is determined by the outer two junctions (J_1 and J_3), which are reverse biased in this operating mode (applied v_{AK} is negative). Symmetric thyristors are designed so that J_1 will reach reverse breakdown due to carrier multiplication at an applied reverse potential near the forward breakdown value (operating point "3" in Fig. 6.3). The forward- and reverse-blocking junctions are usually fabricated at the same time with a very long diffusion process (10–50 h) at high temperatures (>1200°C). This process produces symmetric blocking properties. Wafer edge termination processing causes the forward-blocking capability to be reduced to about 90% of the reverse-blocking capability. Edge termination is discussed below. Asymmetric devices are made to optimize forward-conduction and turn-off properties, and as such reach reverse breakdown at a lower voltage than that applied in the forward direction. This is accomplished by designing the asymmetric thyristor with a much thinner *n*-base than is used in symmetric structures. The thin *n*-base leads to improved properties such as lower forward drop and shorter switching times. Asymmetric devices are generally used in applications when only forward voltages (positive, v_{AK}) are to be applied (including many inverter designs).

The form of the gate-to-cathode *i–v* characteristic of SCRs, GTOs and IGCTs is similar to that of a diode. With positive gate bias, the gate–cathode junction is forward biased and permits the flow of a large current in the presence of a low voltage drop. When negative gate voltage is applied to an SCR, the gate–cathode junction is reverse biased and prevents the flow of current until the avalanche breakdown voltage is reached. In a GTO or IGCT, a negative gate voltage is applied to provide a low impedance path for anode current to flow out of the device instead of out the cathode. In this way the cathode region (base–emitter junction of the equivalent *npn* transistor) turns off, thus pulling the equivalent *npn* transistor out of conduction. This causes the entire thyristor to return to its blocking state. The problem with the GTO and IGCT is that the gate-drive circuitry is typically required to sink 10–50% (for the GTO) or 100% (for the IGCT) of the anode current to achieve turn-off.

6.3.2 Edge and Surface Terminations

Thyristors are often made with planar diffusion technology to create the cathode region. Formation of these regions creates cylindrical curvature of the metallurgical gate–cathode junction. Under reverse bias, the curvature of the associated depletion region results in electric field crowding along the curved section of the p^+ diffused region. The field crowding seriously reduces the breakdown potential below that expected for the bulk semiconductor. A floating field ring, an extra *p* diffused region with no electrical connection at the surface, is often added to modify the electric field profile and thus reduce it to a value below or at the field strength in the bulk. An illustration of a single floating field ring is shown in Fig. 6.4. The spacing, *W*, between the main anode region and the field ring is critical. Multiple rings can also be employed to further modify the electric field in high-voltage rated thyristors.

Another common method for altering the electric field at the surface is by using a field plate as shown in cross section in Fig. 6.5. By forcing the potential over the oxide to be the same as at the surface of the p^+ region, the depletion region can be extended so that the electric field intensity is reduced near the curved portion of the diffused p^+ region. A common practice is to use field plates with floating field rings to obtain optimum breakdown performance.

High-voltage thyristors are made from single wafers of Si and must have edge terminations other than floating field rings or field plates to promote bulk breakdown and limit leakage

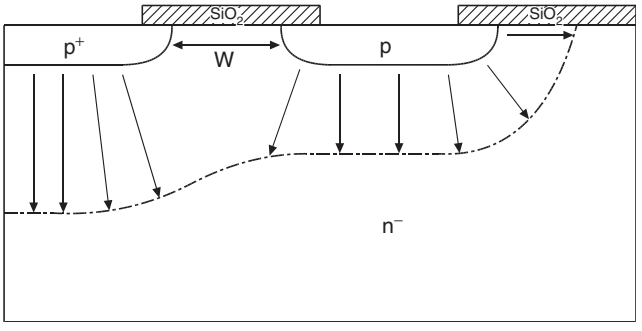

FIGURE 6.4 Cross section showing a floating field ring to decrease the electric field intensity near the curved portion of the main anode region (left-most p^+ region).

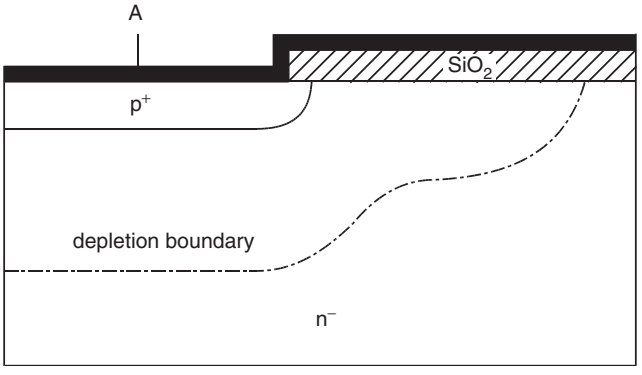

FIGURE 6.5 Cross section showing a field plate used to reduce the electric field intensity near the curved portion of the p^+-region (anode).

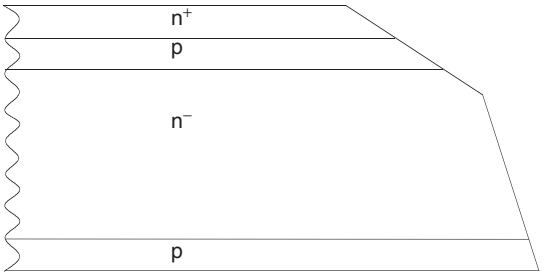

FIGURE 6.6 Cross section of a thyristor showing the negative bevel (upper p–n^- and p–n^+ junctions) and positive bevel (lower p–n^- junction) used for edge termination of large-area devices.

current at the surface. Controlled bevel angles can be created using lapping and polishing techniques during production of large-area thyristors. Two types of bevel junctions can be created: (i) a positive bevel defined as one in which the junction area decreases when moving from the highly-doped to the lightly-doped side of the depletion region and (ii) a negative bevel defined as one in which the junction area increases when moving from the highly-doped to the lightly-doped side of the depletion region. In practice, the negative bevel must be lapped at an extremely shallow angle to reduce the surface field below the field intensity in the bulk. All positive bevel angles between 0 and 90° result in a lower surface field than in the bulk. Figure 6.6 shows the use of a positive bevel for the J_1 junction and a shallow negative bevel for the J_2 and J_3 junctions on a thyristor cross section to make maximum use of the Si area for conduction and still reduce the surface electric field. Further details of the use of beveling, field plates, and field rings can be found in Ghandi [2] and Baliga [3].

6.3.3 Packaging

Thyristors are available in a wide variety of packages, from small plastic ones for low-power (i.e. TO-247), to stud-mount packages for medium-power, to press-pack (also called flat-pack) for the highest power devices. The press-packs must be mounted under pressure to obtain proper electrical and thermal contact between the device and the external metal electrodes. Special force-calibrated clamps are made for this purpose. Large-area thyristors cannot be directly attached to the large copper pole piece of the press-pack because of the difference in the coefficient of thermal expansion (CTE), hence the use of a pressure contact for both anode and cathode. Figure 6.7 shows typical thyristor stud-mount and press-pack packages.

Many medium power thyristors are appearing in modules where a half- or full-bridge (and associated anti-parallel diodes) is put together in one package. A power module package should have five characteristics:

i) electrical isolation of the baseplate from the semiconductor;
ii) good thermal performance;
iii) good electrical performance;
iv) long life/high reliability; and
v) low cost.

Electrical isolation of the baseplate from the semiconductor is necessary in order to contain both halves of a phase leg in one package as well as for convenience (modules switching different phases can be mounted on one heatsink) and safety (heatsinks can be held at ground potential).

Thermal performance is measured by the maximum temperature rise in the Si die at a given power dissipation level with a fixed heat sink temperature. The lower the die temperature, the better the package. A package with a low thermal resistance from junction-to-sink can operate at higher power densities for the same temperature rise or lower temperatures for the same power dissipation than a more thermally resistive package. While maintaining low device temperature is generally preferable, temperature variation affects majority carrier and bipolar devices differently. Roughly speaking, in a bipolar device such as a thyristor, switching losses increase and

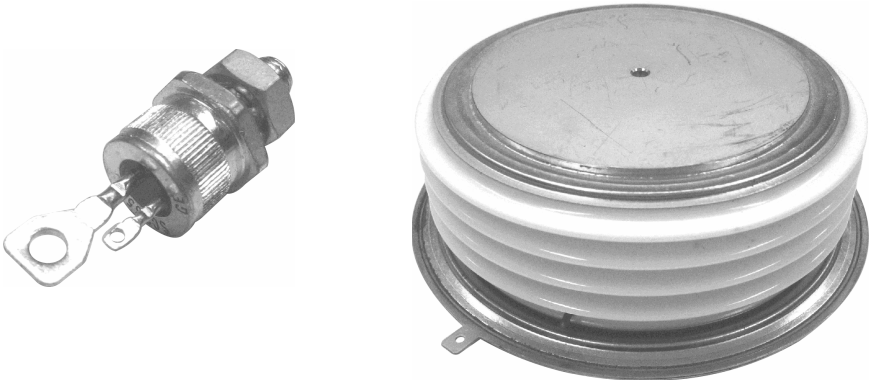

FIGURE 6.7 Examples of thyristor packaging: stud-mount (left) and press-pack/capsule (right).

TABLE 6.1 Thermal conductivity of thyristor package materials

Material	Thermal conductivity (W/m·K) at 300 K
Silicon	150
Copper (baseplate and pole pieces)	390–400
AlN substrate	170
Al_2O_3 (Alumina)	28
Aluminum (Al)	220
Tungsten (W)	167
Molybdenum (Mo)	138
Metal matrix composites (MMC)	170
Thermal grease (heatsink compound)	0.75
60/40 solder (Pb/Sn eutectic)	50
95/5 solder (Pb/Sn high temperature)	35

TABLE 6.2 CTE for thyristor package materials

Material	CTE (μm/m·K) at 300 K
Silicon	4.1
Copper (baseplate and pole pieces)	17
AlN substrate	4.5
Al_2O_3 (Alumina)	6.5
Tungsten (W)	4.6
Molybdenum (Mo)	4.9
Aluminum (Al)	23
Metal matrix composites (MMC)	5–20
60/40 solder (Pb/Sn eutectic)	25

conduction losses decrease with increasing temperature. In a majority carrier device, such as a MOSFET, conduction losses increase with increasing temperature. The thermal conductivity of typical materials used in thyristor packages is shown in Table 6.1.

Electrical performance refers primarily to the stray inductance in series with the die, as well as the capability of mounting a low-inductance bus to the terminals. Another problem is the minimization of capacitive cross-talk from one switch to another, which can cause an abnormal on-state condition by charging the gate of an off-state switch, or from a switch to any circuitry in the package (as would be found in a hybrid power module). Capacitive coupling is a major cause of electromagnetic interference (EMI). As the stray inductance of the module and the bus sets a minimum switching loss for the device – because the switch must absorb the stored inductive energy – it is very important to minimize inductance within the module. Reducing the parasitic inductance reduces the high-frequency ringing during transients that is another cause of radiated electromagnetic interference. Since stray inductance can cause large peak voltages during switching transients, minimizing it helps to maintain the device within its safe area of operation.

Long life and high reliability are primarily attained through minimization of thermal cycling, minimization of ambient temperature, and proper design of the transistor stack. Thermal cycling fatigues material interfaces because of coefficient of thermal expansion (CTE) mismatch between dissimilar materials. As the materials undergo temperature variation, they expand and contract at different rates which stresses the interface between the layers and can cause interface deterioration (e.g. cracking of solder layers or wire debonding). Chemical degradation processes such as dendrite growth and impurity migration are accelerated with increasing temperature, so keeping the absolute temperature of the device low, as well as minimizing the temperature changes to which it is subjected is important. Typical CTE values for common package materials are given in Table 6.2.

Low cost is achieved in a variety of ways. Both manufacturing and material costs must be taken into account when designing a power module. Materials that are difficult to machine or process, even if they are relatively cheap in raw form (molybdenum, for example), should be avoided. Manufacturing processes that lower yield also drive up costs. In addition, a part that is very reliable can reduce future costs by reducing the need for repair and replacement.

The basic half-bridge module has three power terminals: plus, minus and phase. Advanced modules differ from traditional high power commercial modules in several ways. The baseplate is metallized aluminum nitride (AlN) ceramic rather than the typical 0.125" thick nickel-plated copper baseplate with a soldered metallized ceramic substrate for electrical isolation. This AlN baseplate stack provides a low thermal resistance from die to heatsink. The copper terminal power busses are attached by solder to the devices in a wirebond-free, low-inductance, low-resistance, device interconnect configuration. The balance of the assembly is typical for module manufacturing with attachment of shells, use of dielectric gels, and hard epoxies and adhesive to seal the finished module. Details of the thermal performance of modules and advanced modules can be found in Beker *et al.* [4] and Godbold *et al.* [5].

6.4 Dynamic Switching Characteristics

The time rate of rise of anode current (di/dt) during turn-on and the time rate of rise of anode–cathode voltage (dv/dt) during turn-off are important parameters to control for ensuring proper and reliable operation. All thyristors have maximum limits for di/dt and dv/dt that must not be exceeded. Devices capable of conducting large currents in the on-state, are necessarily made with large surface areas through which the current flows. During turn-on, localized areas of a device (near the gate region) begin to conduct current. The initial turn-on of an SCR is shown in Fig. 6.8. The cross section illustrates how injected gate current flows to the nearest cathode region, causing this portion of the *npn* transistor to begin conducting. The *pnp* transistor then follows the *npn* into conduction such that anode current begins flowing only in a small portion of the

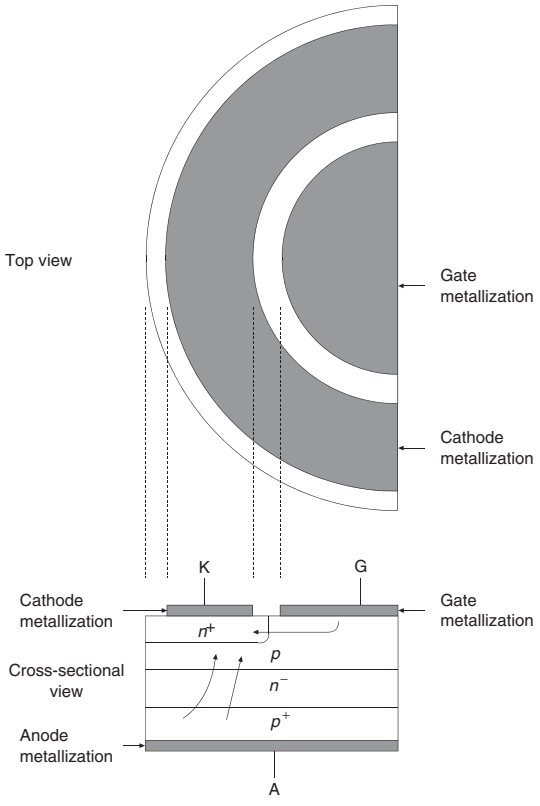

FIGURE 6.8 Top view and associated cross section of gate–cathode periphery showing initial turn-on region in a center-fired thyristor.

cathode region. If the local current density becomes too large (in excess of several thousand amperes per square centimeter), then self-heating will damage the device. Sufficient time (referred to as plasma spreading time) must be allowed for the entire cathode area to begin conducting before the localized currents become too high. This phenomenon results in a maximum allowable rate of rise of anode current in a thyristor and is referred to as a *di/dt* limit. In many high-frequency applications, the entire cathode region is never fully in conduction. Prevention of *di/dt* failure can be accomplished if the rate of increase of conduction area exceeds the *di/dt* rate such that the internal junction temperature does not exceed a specified critical temperature (typically approximately 350°C). This critical temperature decreases as the blocking voltage increases. Adding series inductance to the thyristor to limit *di/dt* below its maximum usually causes circuit design problems.

Another way to increase the *di/dt* rating of a device is to increase the amount of gate–cathode periphery. Inverter SCRs (so-named because of their use in high-frequency power converter circuits that convert dc to ac, i.e. invert) are designed so that there is a large amount of gate edge adjacent to a significant amount of cathode edge. A top surface view of two typical gate–cathode patterns, found in large thyristors, is shown in Fig. 6.9. An inverter SCR often has a stated maximum *di/dt* limit of approximately 2000 A/μs. This value has been shown to be conservative [6], and by using excessive gate current under certain operating conditions, an inverter SCR can be operated reliably at 10,000 A/μs–20,000 A/μs.

A GTO takes the interdigitation of the gate and cathode to the extreme (Fig. 6.9, left). In Fig. 6.10 a cross section of a GTO shows the amount of interdigitation. A GTO often has cathode islands that are formed by etching the Si. A metal plate can be placed on the top to connect the individual cathodes into a large arrangement of electrically parallel cathodes. The gate metallization is placed so that the gate surrounding each cathode is electrically in parallel as well. This construction not only allows high *di/dt* values to be reached, as in an inverter SCR, but also provides the capability to turn-off the anode current by shunting it away from the individual cathodes and out of the gate electrode upon reverse biasing of the gate. During turn-off, current is decreasing while voltage across the device is increasing. If the forward voltage becomes too high while sufficient current is still flowing, then the device will drop back into its conduction mode instead of completing its turn-off cycle. Also, during turn-off, the power dissipation can

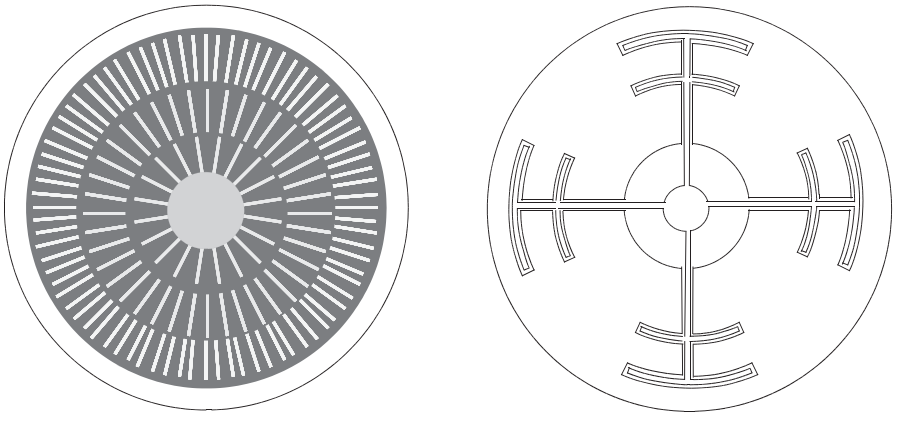

FIGURE 6.9 Top view of typical interdigitated gate–cathode patterns used for thyristors.

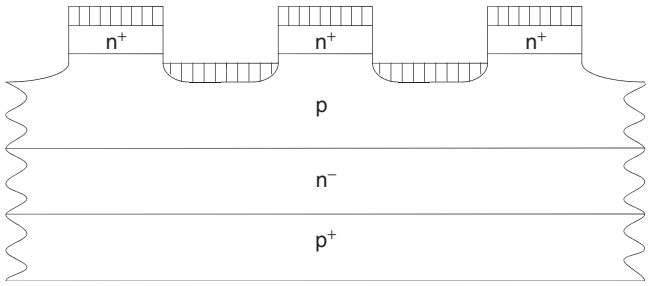

FIGURE 6.10 Cross section of a GTO showing the cathode islands and interdigitation with the gate (*p*-base).

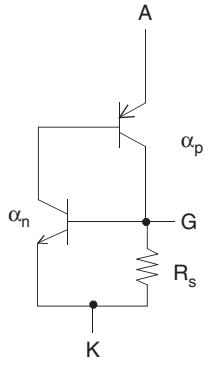

FIGURE 6.11 Two-transistor equivalent circuit showing the addition of a resistive shunt path for anode current.

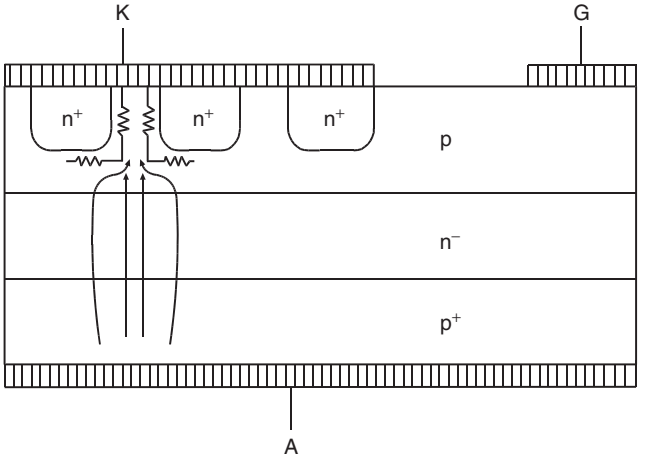

FIGURE 6.12 Cross section showing cathode shorts and the resulting resistive shunt path for anode current.

become excessive if the current and voltage are simultaneously too large. Both of these turn-off problems can damage the device as well as other portions of the circuit.

Another switching problem that occurs is associated primarily with thyristors, though other power electronic devices suffer some degradation of performance from the same problem. This problem is that thyristors can self-trigger into a forward-conduction mode from a forward-blocking mode if the rate of rise of forward anode–cathode voltage is too large. This triggering method is due to displacement current through the associated junction capacitances (the capacitance at J_2 dominates because it is reverse biased under forward applied voltage). The displacement current contributes to the leakage current I_{co}, shown in Eq. (6.1). The SCRs, GTOs and IGCTs, therefore, have a maximum *dv/dt* rating that should not be exceeded (typical values are 100–1000 V/μs). Switching into a reverse-conducting from a reverse-blocking state, due to an applied reverse *dv/dt*, is not possible because the values of the reverse α's of the equivalent transistors can never be made large enough to cause the necessary feedback (latching) effect. An external capacitor is often placed between the anode and cathode of the thyristor to help control the *dv/dt* experienced. Capacitors and other components that are used to form such protection circuits, known as snubbers, may be found in all power semiconductor devices.

6.4.1 Cathode Shorts

As the temperature in the thyristor increases above 25°C, the minority carrier lifetime and the corresponding diffusion lengths in the *n*- and *p*-bases increase. This leads to an increase in the α's of the equivalent transistors. Discussion of the details of the minority carrier diffusion length and its role in determining the current gain factor α can be found in Sze [7]. Referring to Eq. (6.1), it is seen that a lower applied bias will give a carrier multiplication factor M sufficient to switch the device from forward-blocking into conduction, because of this increase of the α's with increasing temperature. Placing a shunt resistor in parallel with the base–emitter junction of the equivalent *npn* transistor (shown in Fig. 6.11) will result in an effective current gain, α_{neff}, that is lower than α_n, as given by Eq. (6.2), where v_{GK} is the applied gate–cathode voltage, R_s is the equivalent lumped value for the distributed current shunting structure, and the remaining factors form the appropriate current factor based on the applied bias and characteristics of the gate–cathode junction. The shunt current path is implemented by providing intermittent shorts, called cathode shorts, between the *p*-base (gate) region and the n^+-emitter (cathode) region in the thyristor as illustrated in Fig. 6.12. The lumped shunt resistance value is in the range of 1–15 Ω as measured from gate to cathode.

$$\alpha_{neff} = \alpha_n \left(\frac{1}{1 + (v_{GK}\alpha_n)/(R_s i_0 \ exp(qv_{GK}/kT))} \right) \qquad (6.2)$$

Low values of anode current (e.g. those associated with an increase in temperature under forward-blocking conditions) will flow through the shunt path to the cathode contact, bypassing the n^+-emitter and keeping the device out of its forward-conduction mode. As the anode current becomes

large, the potential drop across the shunt resistance will be sufficient to forward bias the gate–cathode junction, J_3, and bring the thyristor into forward-conduction. The cathode shorts also provide a path for displacement current to flow without forward biasing J_3. The *dv/dt* rating of the thyristor is thus improved as well as the forward-blocking characteristics by using cathode shorts. However, the shorts do cause a lowering of cathode current handling capability because of the loss of some of the cathode area (n^+-region) to the shorting pattern, an increase in the necessary gate current to obtain switching from forward-blocking to forward-conduction, and an increase in complexity of manufacturing of the thyristor. The loss of cathode area due to the shorting-structure is from 5 to 20%, depending on the type of thyristor. By careful design of the cathode short windows to the *p*-base, the holding current can be made lower than the latching current. This is important so that the thyristor will remain in forward-conduction when used with varying load impedances.

6.4.2 Anode Shorts

A further increase in forward-blocking capability can be obtained by introducing anode shorts in addition to the cathode shorts. This reduces α_p in a similar manner that cathode shorts reduce α_n. An illustration of this is provided in Fig. 6.13. In this structure both J_1 and J_3 are shorted (anode and cathode shorts), so that the forward-blocking capability of the thyristor is completely determined by the avalanche breakdown characteristics of J_2. Anode shorts will result in the complete loss of reverse-blocking capability and is only suitable for thyristors used in asymmetric circuit applications.

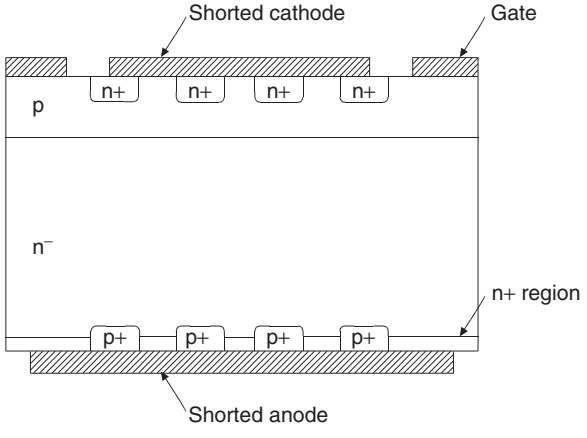

FIGURE 6.13 Cross section showing integrated cathode and anode shorts.

6.4.3 Amplifying Gate

The cathode-shorting structure will reduce the gate sensitivity dramatically. To increase this sensitivity and yet retain the benefits of the cathode-shorts, a structure called an amplifying gate (or regenerative gate) is used, as shown in Fig. 6.14 (and Fig. 6.9, right). When the gate current (1) is injected into the *p*-base through the pilot-gate contact, electrons are injected into the *p*-base by the n^+-emitter with a given emitter injection efficiency. These electrons traverse through the *p*-base (the time taken for this process is called the transit time) and accumulate near the depletion region. This negative charge accumulation leads to injection of holes from the anode. The device then turns on after a certain delay, dictated by the *p*-base transit time, and the pilot anode current (2) begins to flow through a small region near the pilot-gate contact as shown in Fig. 6.14.

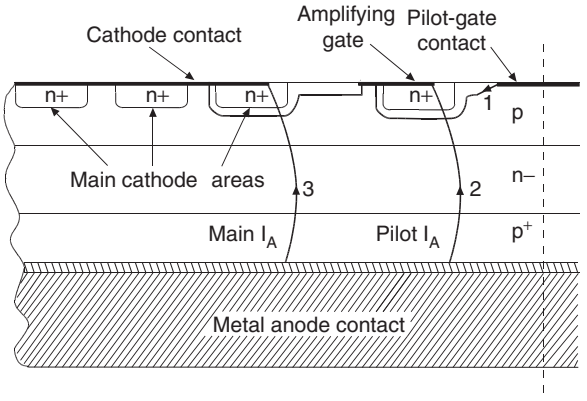

FIGURE 6.14 Cross section showing the amplifying gate structure in a thyristor.

This flow of pilot anode current corresponds to the initial sharp rise in the anode current waveform (phase I), as shown in Fig. 6.15. The device switching then goes into phase II, during which the anode current remains fairly constant, suggesting that the resistance of the region has reached its lower limit. This is due to the fact that the pilot anode current (2) takes a finite time to traverse through the *p*-base laterally and become the gate current for the main cathode area. The n^+-emitters start to inject electrons which traverse the *p*-base vertically and after a certain finite time (transit time of the *p*-base) reach the depletion region. The total time taken by the lateral traversal of pilot anode current and the electron transit time across the *p*-base is the reason for observing this characteristic phase II interval. The width of the phase II interval is comparable to the switching delay, suggesting that the *p*-base transit time is of primary importance. Once the main cathode region turns on, the resistance of the device decreases and the anode current begins to rise again (transition from phase II to III). From this time onward in the switching cycle, the plasma spreading velocity will dictate the rate at which the conduction area will increase. The current density during phase I and II can be quite large, leading to a considerable increase in the local temperature and device failure. The detailed effect of the amplifying gate on the anode current rise will only be noticed

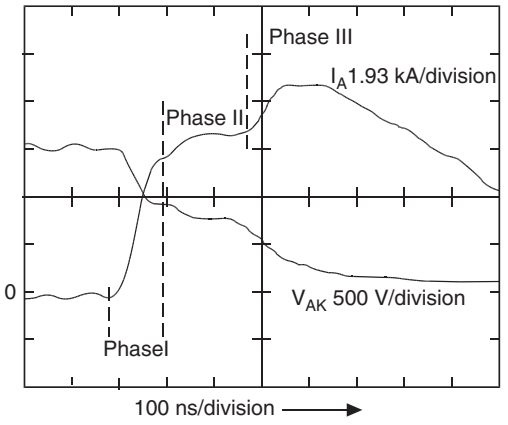

FIGURE 6.15 Turn-on waveforms showing the effect of the amplifying gate in the anode current rise.

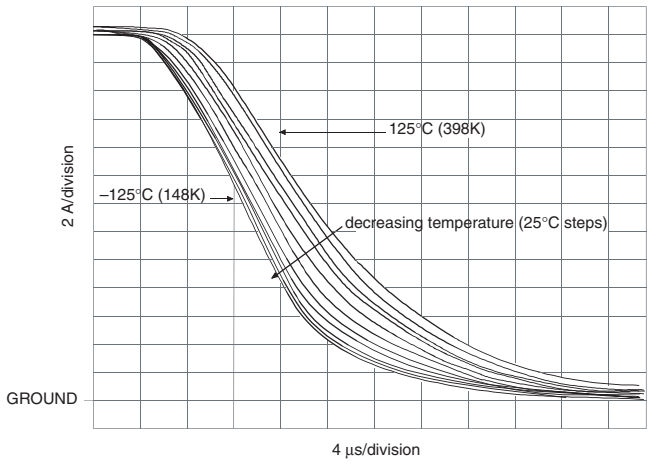

FIGURE 6.16 Temperature effect on the anode current tail during turn-off.

at high levels of *di/dt* (in the range of 1000 A/μs), shown in Fig. 6.15. It can be concluded that the amplifying gate will increase gate sensitivity at the expense of some *di/dt* capability, as demonstrated by Sankaran [8]. This lowering of *di/dt* capability can be somewhat off-set by an increase in gate–cathode interdigitation as previously discussed.

6.4.4 Temperature Dependencies

The forward-blocking voltage of an SCR has been shown to be reduced from 1350 V at 25°C to 950 V at −175°C in a near linear fashion [8]. Above 25°C, the forward-blocking capability is again reduced, due to changes in the minority carrier lifetime which cause the leakage current to increase and the associated breakover voltage to decrease. Several dominant physical parameters associated with semiconductor devices are sensitive to temperature variations, causing their dependent device characteristics to change dramatically. The most important of these parameters are: (i) the minority carrier lifetimes (which control the high-level injection lifetimes); (ii) the hole and electron mobilities; (iii) the impact ionization collision cross sections; and (iv) the free-carrier concentrations (primarily the ionized impurity-atom concentration). Almost all of the impurity atoms are ionized at temperatures above 0°C, and so further discussion of the temperature effects on ionization is not relevant for normal operation. As the temperature increases above 25°C, the following trends are observed: the carrier lifetimes increase, giving longer recovery times and greater switching losses; the carrier mobilities are reduced, increasing the on-state voltage drop; and at very high temperatures, the intrinsic carrier concentration becomes sufficiently high that the depletion layer will not form and the device cannot switch off. A more detailed discussion of these physical parameters is beyond the scope of this article, but references are listed for those persons interested in pursuing relevant information about temperature effects.

It is well known that charge carrier recombination events are more efficient at lower temperatures. This shows up as a larger potential drop during forward-conduction and a shorter recovery time during turn-off. A plot of the anode current during turn-off, at various temperatures, for a typical GTO is shown in Fig. 6.16.

An approximate relation between the temperature and the forward drop across the *n*-base of a thyristor is discussed in detail by Herlet [10] and Hudgins *et al.* [11]. Temperature dependent equations relating the anode current density, J_A and the applied anode–cathode voltage V_{AK} are also given in Reference [11]; these include the junction potential drops in the device, the temperature dependence of the bandgap energy, and the *n*-base potential drop. Data from measurements at forward current densities of approximately 100 A/cm^2 on a GTO rated for 1 kV symmetric blocking gives forward voltage drops of 1.7 V at –50°C and 1.8 V at 150°C.

6.5 Thyristor Parameters

Understanding of a thyristor's maximum ratings and electrical characteristics is required for proper application. Use of a manufacturer's data sheet is essential for good design practice. *Ratings* are maximum or minimum values that set limits on device capability. A measure of device performance under specified operating conditions is a *characteristic* of the device. A summary of some of the maximum ratings which must be considered when choosing a thyristor for a given application is provided in Table 6.3. Thyristor types shown in parentheses indicate a maximum rating unique to that device. Both forward and reverse repetitive and non-repetitive voltage ratings must be considered, and a properly rated device must be chosen so that the maximum voltage ratings are never exceeded. In most cases, either forward or reverse voltage

TABLE 6.3 Thyristor maximum ratings specified by manufacturers

Symbol	Description
V_{RRM}	Peak repetitive reverse voltage
V_{RSM}	Peak non-repetitive reverse voltage (transient)
$V_{R(DC)}$	DC reverse blocking voltage
V_{DRM}	Peak repetitive forward off-state voltage
V_{DSM}	Peak non-repetitive forward off-state voltage (transient)
$V_{D(DC)}$	DC forward-blocking voltage
$I_{T(RMS)}$, $I_{F(RMS)}$	RMS forward on-state current
$I_T(AV)$, $I_{F(AV)}$	Average forward on-state current at specified case or junction temperature
I_{TSM}, $I_{F(TSM)}$	Peak one-cycle surge on-state current (values specified at 60 and 50 Hz)
I_{TGQ} (GTO)	Peak controllable current
I^2t	Non-repetitive pulse overcurrent capability ($t = 8.3$ ms for a 60 Hz half cycle)
P_T	Maximum power dissipation
di/dt	Critical rate of rise of on-state current at specified junction temperature, gate current and forward-blocking voltage
P_{GM} (P_{FGM} for GTO)	Peak gate power dissipation (forward)
P_{RGM} (GTO)	Peak gate power dissipation (reverse)
$P_{G(AV)}$	Average gate power dissipation
V_{FGM}	Peak forward gate voltage
V_{RGM}	Peak reverse gate voltage
I_{FGM}	Peak forward gate current
I_{RGM} (GTO)	Peak reverse gate current
T_{STG}	Storage temperature
T_j	Junction operating temperature
V_{RMS}	Voltage isolation (modules)

transients in excess of the non-repetitive maximum ratings result in destruction of the device. The maximum root mean square (RMS) or average current ratings given are usually those which cause the junction to reach its maximum rated temperature. Because the maximum current will depend upon the current waveform and upon thermal conditions external to the device, the rating is usually shown as a function of case temperature and conduction angle. The peak single half-cycle surge-current rating must be considered, and in applications where the thyristor must be protected from damage by overloads, a fuse with an I^2t rating smaller than the maximum rated value for the device must be used. Maximum ratings for both forward and reverse gate voltage, current and power also must not be exceeded.

The maximum rated operating junction temperature T_J must not be exceeded, since device performance, in particular voltage-blocking capability, will be degraded. Junction temperature cannot be measured directly but must be calculated from a knowledge of steady-state thermal resistance $R_{\Theta(J-C)}$, and the average power dissipation. For transients or surges, the transient thermal impedance ($Z_{\Theta(J-C)}$) curve must be used (provided in manufacturer's data sheets). The maximum average power dissipation P_T is related to the maximum rated operating junction temperature and the case temperature by the steady-state thermal resistance. In general, both the maximum dissipation and its derating with increasing case temperature are provided.

The number and type of thyristor characteristics specified varies widely from one manufacturer to another. Some characteristics are given only as typical values of minima or maxima, while many characteristics are displayed graphically. Table 6.4 summarizes some of the typical characteristics provided as maximum values. The maximum value means that the manufacturer guarantees that the device will not exceed the value given under the specified operating or switching conditions. A minimum value means that the manufacturer guarantees that the device will perform at least, as well as the characteristic given under the specified operating or switching conditions. Thyristor types shown in parenthesis indicate a characteristic unique to that device. Gate conditions of both voltage and current to ensure either non-triggered or triggered device operation are included. The turn-on and turn-off transients of the thyristor are characterized by switching times like the

TABLE 6.4 Typical thyristor characteristic maximum and minimum values specified by manufacturers

Symbol	Description
V_{TM}, V_{FM}	Maximum on-state voltage drop(at specified junction temperature and forward current)
I_{DRM}	Maximum forward off-state current (at specified junction temperature and forward voltage)
I_{RRM}	Maximum reverse off-state current (at specified junction temperature and reverse voltage)
dv/dt	Minimum critical rate of rise of off-state voltage at specified junction temperature and forward-blocking voltage level
V_{GT}	Maximum gate trigger voltage (at specified temperature and forward applied voltage)
V_{GD}, V_{GDM}	Maximum gate non-trigger voltage (at specified temperature and forward applied voltage)
I_{GT}	Maximum gate trigger current (at specified temperature and forward applied voltage)
T_{gt} (GTO)	Maximum turn-on time (under specified switching conditions)
T_q	Maximum turn-off time (under specified switching conditions)
t_D	Maximum turn-on delay time (for specified test)
$R_{\Theta(J-C)}$	Maximum junction-to-case thermal resistance
$R_{\Theta(C-S)}$	Maximum case-to-sink thermal resistance (interface lubricated)

turn-off time listed in Table 6.4. The turn-on transient can be divided into three intervals: (i) gate-delay interval; (ii) turn-on of initial area; and (iii) spreading interval. The gate-delay interval is simply the time between application of a turn-on pulse at the gate and the time the initial cathode area turns on. This delay decreases with increasing gate drive current and is of the order of a few microseconds. The second interval, the time required for turn-on of the initial area, is quite short, typically less than 1 μs. In general, the initial area turned on is a small percentage of the total useful device area. After the initial area turns on, conduction spreads (spreading interval or plasma spreading time) throughout the device in tens of microseconds for high-speed or thyristors. The plasma spreading time may take up to hundreds of microseconds in large-area phase-control devices.

Table 6.5 lists many of the thyristor parameters that appear as listed values or as information on graphs. The definition of each parameter and the test conditions under which they are measured are given in the table as well.

6.6 Types of Thyristors

In recent years, most development effort has gone into continued integration of the gating and control electronics into thyristor modules, and the use of MOS-technology to create gate structures integrated into the thyristor itself. Many variations of this theme are being developed and some technologies should rise above the others in the years to come. Further details concerning most of the following discussion of thyristor types can be found in [1].

6.6.1 SCRs and GTOs

The highest power handling devices continue to be bipolar thyristors. High powered thyristors are large diameter devices, some well in excess of 100 mm, and as such have a limitation on the rate of rise of anode current, a *di*/*dt* rating. The depletion capacitances around the *p*–*n* junctions, in particular the center junction J_2, limit the rate of rise in forward voltage that can be applied even after all the stored charge, introduced during conduction, is removed. The associated displacement current under application of forward voltage during the thyristor blocking state sets a *dv*/*dt* limit. Some effort in improving the voltage hold-off capability and over-voltage protection of conventional SCRs is underway by incorporating a lateral high resistivity region to help dissipate the energy during breakover. Most effort, though, is being placed in the further development of high performance GTOs and IGCTs because of their controllability and to a lesser extent in optically triggered structures that feature gate circuit isolation.

High voltage GTOs with symmetric blocking capability require thick *n*-base regions to support the high electric field. The addition of an *n*+ buffer layer next to the *p*+-anode allows high voltage forward-blocking and a low forward voltage drop during conduction because of the thinner *n*-base required. Cylindrical anode shorts have been incorporated to facilitate excess carrier removal from the *n*-base during turn-off and still retain the high blocking capability. This device structure can control 200 A, operating at 900 Hz, with a 6 kV hold-off. Some of the design tradeoff between the *n*-base width and turn-off energy losses in these structures have been determined. A similar GTO incorporating an n^+-buffer layer and a *pin* structure has been fabricated that can control up to 1 kA (at a forward drop of 4 V) with a forward blocking capability of 8 kV. A reverse conducting GTO has been fabricated that can block 6 kV in the forward direction, interrupt a peak current of 3 kA and has a turn-off gain of about 5.

The IGCT is a modified GTO structure. It is designed and manufactured so that it commutates all of the cathode current away from the cathode region and diverts it out of the gate contact. The IGCT is similar to a GTO in structure except that it always has a low-loss *n*-buffer region between the *n*-base and *p*-emitter. The IGCT device package is designed to result in a very low parasitic inductance and is integrated with a specially designed gate-drive circuit. The gate drive contains all the necessary *di*/*dt* and *dv*/*dt* protection; the only connections required are a low-voltage power supply for the gate drive and an optical signal for controlling the gate. The specially designed gate drive and ring-gate package circuit allows the IGCT to be operated without a snubber circuit, and to switch with a higher anode *di*/*dt* than a similar GTO. At blocking voltages of 4.5 kV and higher the IGCT provides better performance than a conventional GTO. The speed at which the cathode current is diverted to the gate (di_{GQ}/dt) is directly related to the peak snubberless turn-off capability of the IGCT. The gate drive circuit can sink current for turn-off at di_{GQ}/dt values in excess of 7000 A/μs. This hard gate drive results in a low charge storage time of about 1 μs. The low storage time and the fail-short mode makes the IGCT attractive for high-power, high-voltage series applications; examples include high-power converters in excess of 100 MVA, static vol-ampere reactive (VAR) compensators and converters for distributed generation such as wind power.

6.6.2 MOS-controlled Thyristors

The cross section of the *p*-type MCT unit cell is given in Fig. 6.17. When the MCT is in its forward-blocking state and a negative gate–anode voltage is applied, an inversion layer is formed in the *n*-doped material that allows holes to flow laterally from the *p*-emitter (*p*-channel FET source) through the channel to the *p*-base (*p*-channel FET drain). This hole flow is the base current for the *npn* transistor. The *n*-emitter then injects electrons which are collected in the *n*-base, causing the *p*-emitter to inject holes into the *n*-base so that the *pnp* transistor is turned on and latches the MCT. The MCT is brought

TABLE 6.5 Symbols and definitions of major thyristor parameters

R_θ	Thermal resistance	Specifies the degree of temperature rise per unit of power, measuring junction temperature from a specified external point. Defined when junction power dissipation results in steady-state thermal flow.
$R_{\theta(J-A)}$	Junction-to-ambient thermal resistance	The steady-state thermal resistance between the junction and ambient.
$R_{\theta(J-C)}$	Junction-to-case thermal resistance	The steady-state thermal resistance between the junction and case surface.
$R_{\theta(J-S)}$	Junction-to-sink thermal resistance	The steady-state thermal resistance between the junction and the heatsink mounting surface.
$R_{\theta(C-S)}$	Contact thermal resistance	The steady-state thermal resistance between the surface of the case and the heatsink mounting surface.
Z_θ	Transient thermal impedance	The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same interval causing the change of temperature difference.
$Z_{\theta(J-A)}$	Junction-to-ambient transient thermal impedance	The transient thermal impedance between the junction and ambient.
$Z_{\theta(J-C)}$	Junction-to-case transient thermal impedance	The transient thermal impedance between the junction and the case surface.
$Z_{\theta(J-S)}$	Junction-to-sink transient thermal impedance	The transient thermal impedance between the junction and the heatsink mounting surface.
T_A	Ambient temperature	It is the temperature of the surrounding atmosphere of a device when natural or forced-air cooling is used, and is not influenced by heat dissipation of the device.
T_S	Sink temperature	The temperature at a specified point on the device heatsink.
T_C	Case temperature	The temperature at a specified point on the device case.
T_J	Junction temperature	The device junction temperature rating. Specifies the maximum and minimum allowable operation temperatures.
T_{STG}	Storage temperature	Specifies the maximum and minimum allowable storage temperatures (with no electrical connections).
V_{RRM}	Peak reverse blocking voltage	Within the rated junction temperature range, and with the gate terminal open circuited, specifies the repetitive peak reverse anode to cathode voltage applicable on each cycle.
V_{RSM}	Transient peak reverse-blocking voltage	Within the rated junction temperature range, and with the gate terminal open circuited, specifies the non-repetitive peak reverse anode to cathode voltage applicable for a time width equivalent to less than 5 ms.
$V_{R(DC)}$ SCR only	dc reverse-blocking voltage	Within the rated junction temperature range, and with the gate terminal open-circuited, specifies the maximum value for dc anode to cathode voltage applicable in the reverse direction.
V_{DRM}	Peak forward-blocking voltage	Within the rated junction temperature range, and with the gate terminal open circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), specifies the repetitive peak off-state anode to cathode voltage applicable on each cycle. This does not apply for transient off-state voltage application.
V_{DSM}	Transient peak forward-blocking voltage	Within the rated junction temperature range, and with the gate terminal open circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), specifies the non-repetitive off-state anode to cathode voltage applicable for a time width equivalent to less than 5 ms. This gives the maximum instantaneous value for non-repetitive transient off-state voltage.
$V_{D(DC)}$	dc forward-blocking voltage	Within the rated junction temperature range, and with the gate terminal open circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), specifies the maximum value for dc anode to cathode voltage applicable in the forward direction.
dv/dt	Critical rate of rise of off-state voltage $dv/dt = (0.632V_D)/\tau V_D$ is specified off-state voltage τ is time constant for exponential	At the maximum rated junction temperature range, and with the gate terminal open circuited (SCR), or with a specified reverse voltage between the gate and cathode (GTO), this specifies the maximum rate of rise of off-state voltage that will not drive the device from an off-state to an on-state when an exponential off-state voltage of specified amplitude is applied to the device.
V_{TM}	Peak on-state voltage	At specified junction temperature, and when on-state current (50 or 60 Hz, half sine wave of specified peak amplitude) is applied to the device, indicates peak value for the resulting voltage drop.

TABLE 6.5—*Contd.*

$I_{T(RMS)}$	RMS on-state current	At specified case temperature, indicates the RMS value for on-state current that can be continuously applied to the device.
$I_{T(AV)}$	Average on-state current	At specified case temperature, and with the device connected to a resistive or inductive load, indicates the average value for forward-current (sine half wave, commercial frequency) that can be continuously applied to the device.
I_{TSM}	Peak on-state current	Within the rated junction temperature range, indicates the peak-value for non-repetitive on-state current (sine half wave, 50 or 60 Hz). This value indicated for one cycle, or as a function of a number of cycles.
I^2t	Current-squared time	The maximum, on-state, non-repetitive short-time thermal capacity of the device and is helpful in selecting a fuse or providing a coordinated protection scheme of the device in the equipment. This rating is intended specifically for operation less than one half cycle of a 180° (degree) conduction angle sinusoidal wave form. The off-state blocking capability cannot be guaranteed at values near the maximum I^2t.
di/dt	Critical rate of Rise of on-state current	At specified case temperature, specified off-state voltage, specified gate conditions, and at a frequency of less than 60 Hz, indicates the maximum rate of rise of on-state current which the thyristor will withstand when switching from an off-state to an on-state, when using recommended gate drive.
I_{RRM}	Peak reverse leakage current	At maximum rated junction temperature, indicates the peak value for reverse current flow when a voltage (sine half wave, 50 or 60 Hz, and having a peak value as specified for repetitive peak reverse-voltage rating) is applied in a reverse direction to the device.
I_{DRM}	Peak forward-leakage current	At maximum rated junction temperature, indicates the peak value for off-state current flow when a voltage (sine half wave, 50 or 60 Hz, and having a peak value for repetitive off-state voltage rating) is applied in a forward direction to the device. For a GTO, a reverse voltage between the gate and cathode is specified.
P_{GM} (SCR) P_{GFM} (GTO)	Peak gate power dissipation peak gate forward power dissipation	Within the rated junction temperature range, indicates the peak value for maximum allowable power dissipation over a specified time period, when the device is in forward-conduction between the gate and cathode.
$P_{G(AV)}$	Average gate power dissipation	Within the rated junction temperature range, indicates the average value for maximum allowable power dissipation when the device is forward-conducting between the gate and cathode.
P_{GRM} GTO only	Peak gate reverse power dissipation	Within the rated junction temperature range, indicates the peak value for maximum allowable power dissipation in the reverse direction between the gate and cathode, over a specified time period.
$P_{GR(AV)}$ GTO only	Average gate reverse power dissipation	Within the rated junction temperature range, indicates the average value for maximum allowable power dissipation in the reverse direction between the gate and cathode.
I_{GFM}	Peak forward gate current	Within the rated junction temperature range, indicates the peak value for forward current flow between the gate and cathode.
I_{GRM} GTO only	Peak reverse gate current	Within the rated junction temperature range, indicates peak value for reverse current that can be conducted between the gate and cathode.
V_{GRM}	Peak reverse gate voltage	Within the rated junction temperature range, indicates the peak value for reverse voltage applied between the gate and cathode.
V_{GFM}	Peak forward gate voltage	Within the rated junction temperature range, indicates the peak value for forward voltage applied between the gate and cathode.
I_{GT}	Gate current to trigger	At a junction temperature of 25°C, and with a specified off-voltage, and a specified load resistance, indicates the minimum gate dc current required to switch the thyristor from an off-state to an on-state.
V_{GT}	Gate voltage to trigger	At a junction temperature of 25°C, and with a specified off-state voltage, and a specified load resistance, indicates the minimum dc gate voltage required to switch the thyristor from an off-state to an on-state.
V_{GDM} SCR Only	Non-triggering gate voltage	At maximum rated junction temperature, and with a specified off-state voltage applied to the device, indicates the maximum dc gate voltage which will not switch the device from an off-state to an on-state.
I_{TGQ} GTO only	Gate controlled turn-off current	Under specified conditions, indicates the instantaneous value for on-current usable in gate control, specified immediately prior to device turn-off.

continued

TABLE 6.5—*Contd.*

R_θ	Thermal resistance	Specifies the degree of temperature rise per unit of power, measuring junction temperature from a specified external point. Defined when junction power dissipation results in steady-state thermal flow.
t_{on} SCR only	Turn-on time	At specified junction temperature, and with a peak repetitive off-state voltage of half rated value, followed by device turn-on using specified gate current, and when specified on-state current of specified di/dt flows, indicated as the time required for the applied off-state voltage to drop to 10% of its initial value after gate current application. Delay time is the term used to define the time required for applied voltage to drop to 90% of its initial value following gate-current application. The time required for the voltage level to drop from 90 to 10% of its initial value is referred to as rise time. The sum of both these defines turn-on time.
T_q SCR Only	Turn-off time	Specified at maximum rated junction temperature. Device set up to conduct on-state current, followed by application of specified reverse anode-cathode voltage to quench on-state current, and then increasing the anode-cathode voltage at a specified rate of rise as determined by circuit conditions controlling the point where the specified off-state voltage is reached. Turn-off time defines the minimum time which the device will hold its off-state, starting from the time on-state current reached zero until the time forward voltage is again applied (i.e. applied anode–cathode voltage becomes positive again).
t_{gt} GTO only	Turn-on time	When applying forward current to the gate, indicates the time required to switch the device from an off-state to an on-state.
t_{qt} GTO only	Turn-off time	When applying reverse current to the gate, indicates the time required to switch the device from an on-state to an off-state.

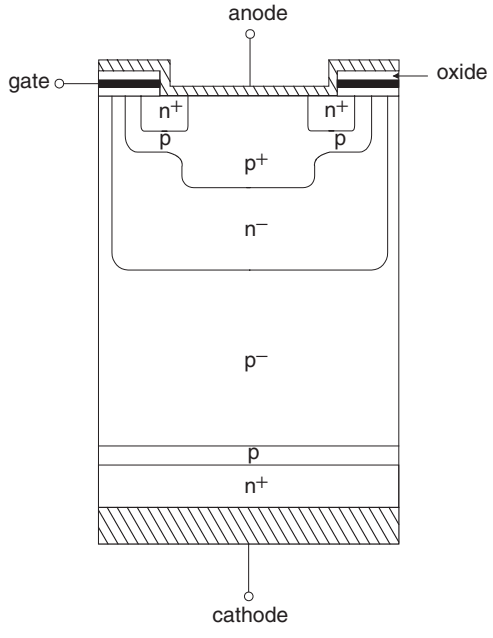

FIGURE 6.17 Cross section of unit cell of a *p*-type MCT.

out of conduction by applying a positive gate–anode voltage. This signal creates an inversion layer that diverts electrons in the *n*-base away from the *p*-emitter and into the heavily doped *n*-region at the anode. This *n*-channel FET current amounts to a diversion of the *pnp* transistor base current so that its base–emitter junction turns off. Holes are then no longer available for collection by the *p*-base. The elimination of this hole current (*npn* transistor base current) causes the *npn* transistor to turn-off. The remaining stored charge recombines and returns the MCT to its blocking state.

The seeming variability in fabrication of the turn-off FET structure continues to limit the performance of MCTs, particularly current interruption capability, though these devices can handle two to five times the conduction current density of IGBTs. Numerical modeling and its experimental verification show that ensembles of cells are sensitive to current filamentation during turn-off. All MCT device designs suffer from the problem of current interruption capability. Turn-on is relatively simple, by comparison; both the turn-on and conduction properties of the MCT approach the one-dimensional thyristor limit.

Other variations on the MCT structure have been demonstrated, namely the emitter switched thyristor (EST) and the dual-gate emitter switched thyristor (DG-EST) [12]. These comprise integrated lateral MOSFET structures which connect a floating thyristor *n*-emitter region to an *n*+ thyristor cathode region. The MOS channels are in series with the floating *n*-emitter region, allowing triggering of the thyristor with electrons from the *n*-base and interruption of the current to initiate turn-off. The DG-EST behaves as a dual-mode device, with the two gates allowing an IGBT mode to operate during switching and a thyristor mode to operate in the on-state.

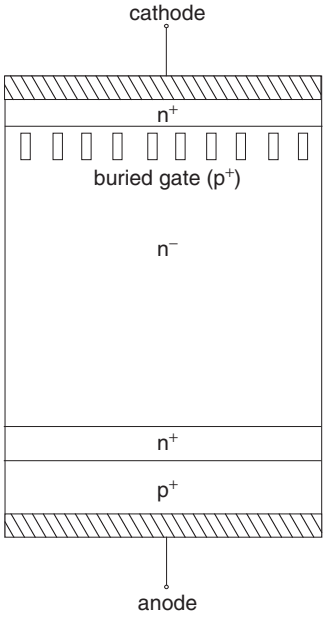

FIGURE 6.18 Cross section of a SITh or FCT.

6.6.3 Static Induction Thyristors

A SITh or FCTh has a cross section similar to that shown in Fig. 6.18. Other SITh configurations have surface gate structures. The device is essentially a *pin* diode with a gate structure that can pinch-off anode current flow. High power SIThs have a sub-surface gate (buried-gate) structure to allow larger cathode areas to be utilized, and hence larger current densities are possible.

Planar gate devices have been fabricated with blocking capabilities of up to 1.2 kV and conduction currents of 200 A, while step-gate (trench-gate) structures have been produced that are able to block up to 4 kV and conduct 400 A. Similar devices with a "Verigrid" structure have been demonstrated that can block 2 kV and conduct 200 A, with claims of up to 3.5 kV blocking and 200 A conduction. Buried-gate devices that block 2.5 kV and conduct 300 A have also been fabricated. Recently there has been a resurgence of interest in these devices for fabrication in SiC.

6.6.4 Optically Triggered Thyristors

Optically gated thyristors have traditionally been used in power utility applications where series stacks of devices are necessary to achieve the high voltages required. Isolation between gate drive circuits for circuits such as static VAR compensators and high voltage dc to ac inverters (for use in high voltage dc (HVDC) transmission) have driven the development of this class of devices, which are typically available in ratings from 5 to 8 kV. The cross section is similar to that shown in Fig. 6.19, showing the photosensitive region and the amplifying gate structures. Light-triggered thyristors (LTTs) may also integrate over-voltage protection.

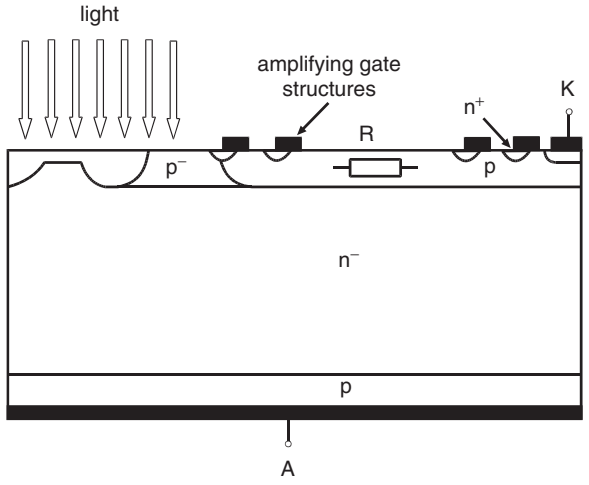

FIGURE 6.19 Cross section of a light-triggered thyristors (LTT).

One of the most recent devices can block 6 kV forward and reverse, conduct 2.5 kA average current, maintain a *di*/*dt* capability of 300 A/μs and a *dv*/*dt* capability of 3000 V/μs, with a required trigger power of 10 mW. An integrated light triggered and light quenched SITh has been produced that can block 1.2 kV and conduct up to 20 A (at a forward drop of 2.5 V). This device is an integration of a normally off buried-gate static induction photo-thyristor and a normally off *p*-channel darlington surface-gate static induction phototransistor. The optical trigger and quenching power required is less than 5 and 0.2 mW, respectively.

6.6.5 Bi-directional Thyristors

The BCT is an integrated assembly of two anti-parallel thyristors on one Si wafer. The intended applications for this switch are VAR compensators, static switches, soft starters and motor drives. These devices are rated up to 6.5 kV blocking. Cross-talk between the two halves has been minimized. A cross section of the BCT is shown in Fig. 6.20. Note that each surface has a cathode and an anode (opposite devices). The small gate–cathode periphery necessarily restricts the BCT to low-frequency applications because of its *di/dt* limit.

Low-power devices similar to the BCT, but in existence for many years, are the diac and triac. A simplified cross section of a diac is shown in Fig. 6.21. A positive voltage applied to the anode with respect to the cathode forward biases J_1, while reverse biasing J_2. J_4 and J_3 are shorted by the metal contacts. When J_2 is biased to breakdown, a lateral current flows in the p_2 region. This lateral flow forward biases the edge of J_3, causing carrier injection. The result is that the device switches into its thyristor mode and latches. Applying a reverse voltage causes the opposite behavior at each junction, but

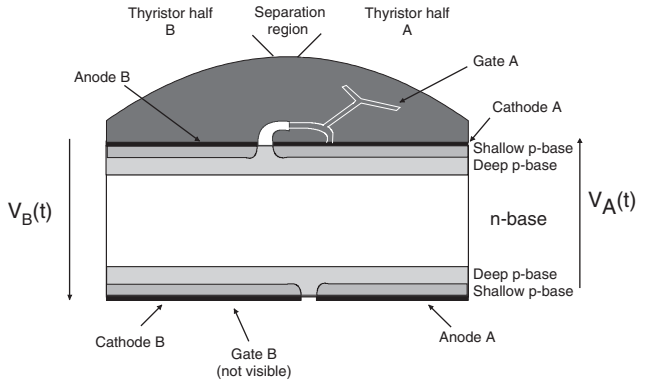

FIGURE 6.20 Cross section of a bi-directional control thyristor (BCT).

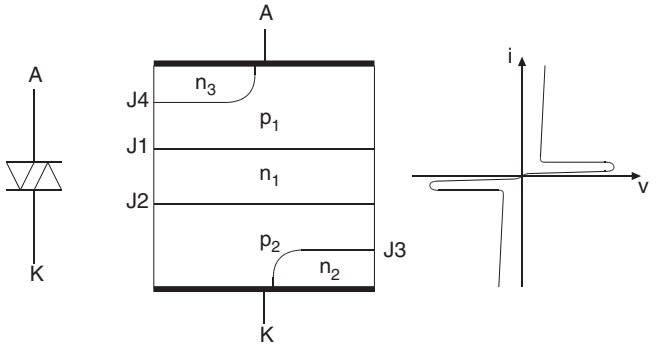

FIGURE 6.21 Cross section and *i–v* plot of a diac.

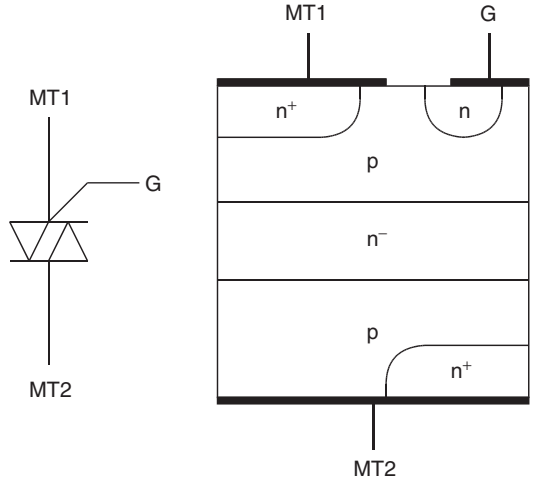

FIGURE 6.22 Cross section of a triac.

with the same result. Figure 6.21 also shows the *i–v* plot for a diac.

The addition of a gate connection, to form a triac, allows the breakover to be controlled at a lower forward voltage. Figure 6.22 shows the structure for the triac. Unlike the diac, this is not symmetrical, resulting in differing forward and reverse breakover voltages for a given gate voltage. The device is fired by applying a gate pulse of the same polarity relative to MT1 as that of MT2.

6.7 Gate Drive Requirements

6.7.1 Snubber Circuits

To protect a thyristor, from a large *di/dt* during turn-on and a large *dv/dt* during turn-off, a snubber circuit is needed. A general snubber topology is shown in Fig. 6.23. The turn-on snubber is made by inductance L_1 (often $L1$ is stray inductance only). This protects the thyristor from a large *di/dt* during the turn-on process. The auxiliary circuit made by R_1 and D_1 allows the discharging of L_1 when the thyristor is turned off. The turn-off snubber is made by resistor R_2 and capacitance C_2. This circuit protects a GTO from large *dv/dt* during the turn-off process. The auxiliary circuit made by D_2 and R_2 allows the discharging of C_2 when the thyristor is turned on. The circuit of capacitance C_2 and inductance L_1 also limits the value of *dv/dt* across the thyristor during forward-blocking. In addition, L_1 protects the thyristor from reverse over-currents. R_1 and diodes D_1, D_2 are usually omitted in ac circuits with converter-grade thyristors. A similar second set of *L*, *C* and *R* may be used around this circuit in HVDC applications.

6.7.2 Gate Circuits

It is possible to turn on a thyristor by injecting a current pulse into its gate. This process is known as gating, triggering or firing the thyristor. The most important restrictions are on the maximum peak and duration of the gate pulse current.

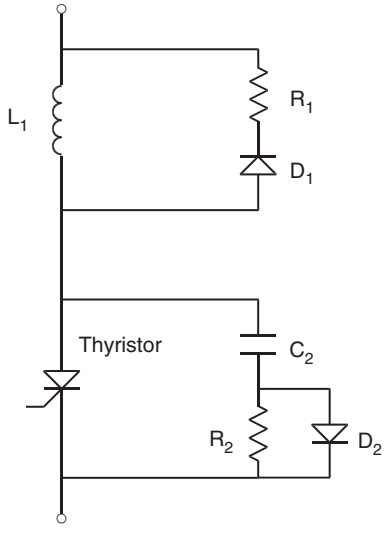

FIGURE 6.23 Turn-on (top elements) and turn-off (bottom elements) snubber circuits for thyristors.

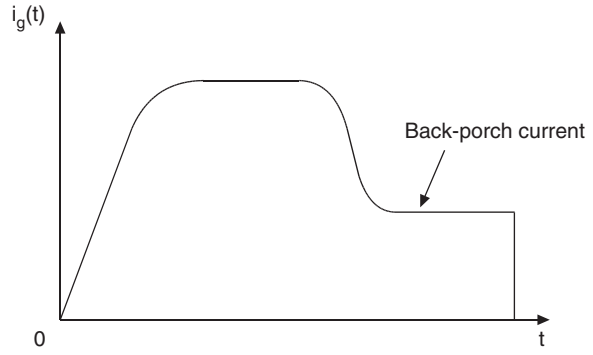

FIGURE 6.24 Gate current waveform showing large initial current followed by a suitable back-porch value.

In order to allow a fast turn-on, and a correspondingly large anode *di/dt* during the turn-on process, a large gate current pulse is supplied during the initial turn-on phase with a large di_G/dt. The gate current is kept on, at lower value, for some times after the thyristor turned on in order to avoid unwanted turn-off of the device; this is known as the "back-porch" current. A shaped gate current waveform of this type is shown in Fig. 6.24.

Figure 6.25 shows typical gate *i–v* characteristics for the maximum and minimum operating temperatures. The dashed line represents the minimum gate current and corresponding gate voltage needed to ensure that the thyristor will be triggered at various operating temperatures. It is also known as the locus of minimum firing points. On the data sheet it is possible find a line representing the maximum operating power of the thyristor gating internal circuit. The straight line, between V_{GG} and V_{GG}/R_G, represents the current voltage characteristic of the equivalent trigger circuit. If the equivalent trigger circuit line intercepts the two gate *i–v* characteristics for the maximum and minimum operating temperatures between where they intercept the dashed lines (minimum gate current to trigger and maximum gate power dissipation), then the trigger circuit is able to turn-on the thyristor at any operating temperature without destroying or damaging the device.

In order to keep the power circuit and the control circuit electrically unconnected, the gate signal generator and the gate of the thyristor are often connected through a transformer. There is a transformer winding for each thyristor, and in this way unwanted short circuits between devices are avoided. A general block diagram of a thyristor gate-trigger circuit is shown in Fig. 6.26. This application is for a standard bridge configuration often used in power converters.

Another problem can arise if the load impedance is high, particularly if the load is inductive and the supply voltage is low. In this situation, the latching current may not be reached during the trigger pulse. A possible solution to this problem could be the use of a longer current pulse. However, such a solution is not attractive because of the presence of the isolation transformer. An alternative solution is the generation of a series of short pulses that last for the same duration as a single long pulse. A single short pulse, a single long pulse and a series of short pulses are shown in Fig. 6.27. Reliable gating of the thyristor is essential in many applications.

There are many gate trigger circuits that use optical isolation between the logic-level electronics and a drive stage (typically MOSFETs) configured in a push–pull output. The dc power supply voltage for the drive stage is provided

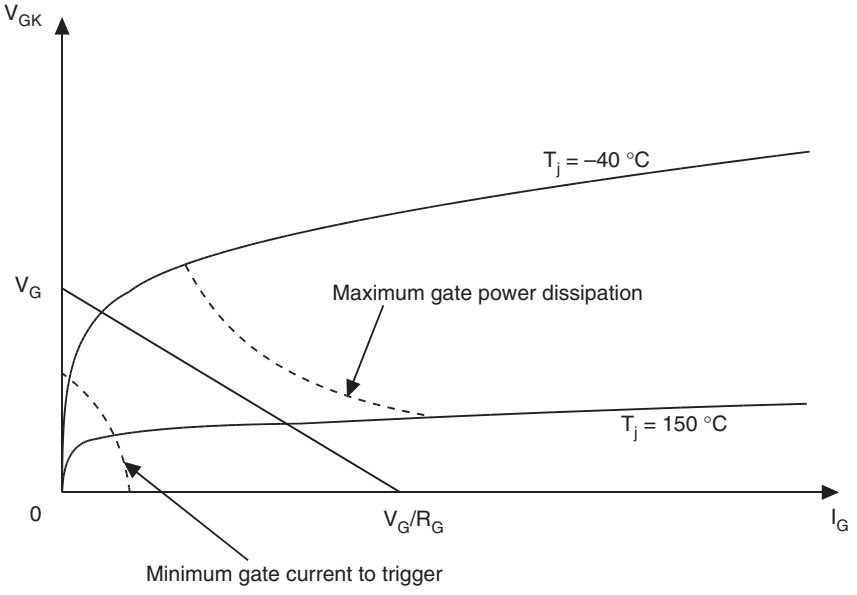

FIGURE 6.25 Gate *i–v* curve for a typical thyristor.

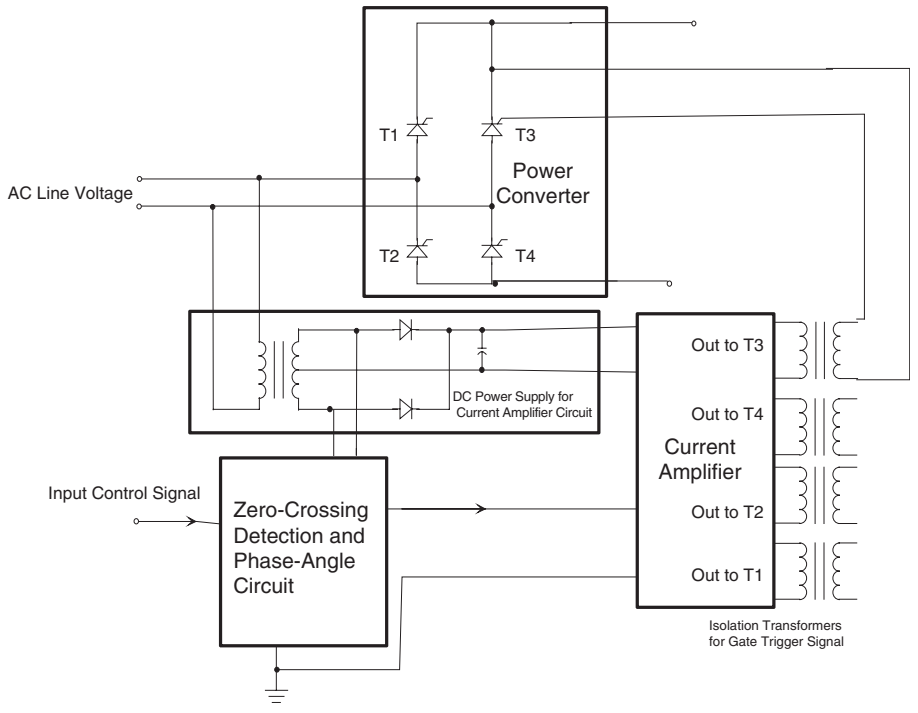

FIGURE 6.26 Block diagram of a transformer-isolated gate drive circuit.

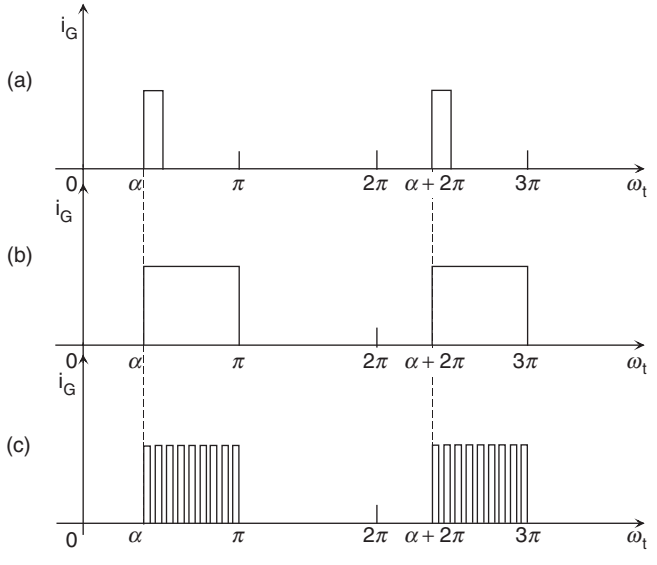

FIGURE 6.27 Multiple gate pulses used as an alternative to one long current pulse.

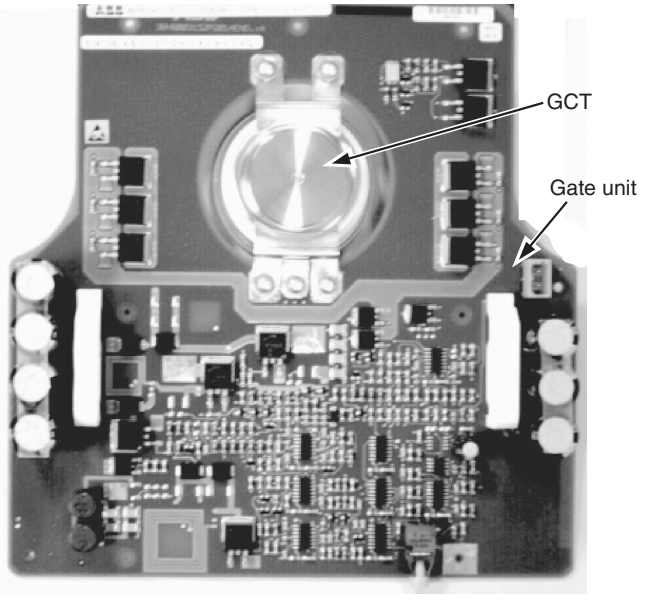

FIGURE 6.28 Typical layout of an IGCT gate drive.

through transformer isolation. Many device manufacturers supply drive circuits available on printed circuit (PC) boards or diagrams of suggested circuits.

IGCT gate drives consist of an integrated module to which the thyristor is connected via a low-inductance mounting; an example is given in Fig. 6.28. Multiple MOSFETs and capacitors connected in parallel may be used to source or sink the necessary currents to turn the device on or off. Logic in the module controls the gate drive from a fiber-optic trigger input, and provides diagnostic feedback from a fiber-optic output. A simple power supply connection is also required.

6.8 PSpice Model

Circuit simulators such as Spice and PSpice are widely used as tools in the design of power systems. For this purpose equivalent circuit models of thyristors have been developed. A variety of models have been proposed with varying degrees of complexity and accuracy. Frequently the simple two-transistor model described in Section 6.2 is used in PSpice. This simple structure, however, cannot model the appropriate negative-differential-resistance (NDR) behavior as the thyristor moves from forward-blocking to forward-conduction. Few other models for conventional thyristors have been reported. A PSpice model for a GTO has been developed by Tsay *et al.* [13], which captures much of thyristor behavior, such as the static *i–v* curve shown in Fig. 6.3, dynamic characteristics (turn-on and turn-off times), device failure modes (e.g. current crowding due to excessive *di/dt* at turn-on and spurious turn-on due to excessive *dv/dt* at turn-off), and thermal effects. Specifically, three resistors are added to the two-transistor model to create the appropriate behavior.

The proposed two-transistor, three-resistor model (2T-3R) is shown in Fig. 6.29. This circuit exhibits the desired NDR behavior. Given the static *i–v* characteristics for an SCR or GTO, it is possible to obtain similar curves from the model by choosing appropriate values for the three resistors and for the forward current gains α_p and α_n of the two transistors. The process of curve fitting can be simplified by keeping in mind that resistor R_1 tends to affect the negative slope of the *i–v* characteristic, resistor R_2 tends to affect the value of the holding current I_H and resistor R_3 tends to affect the value of the forward breakdown voltage V_{FBD}. When modeling thyristors with cathode or anode shorts, as described in Section 6.4, the presence of these shorts determines the values of R_1 and R_2, respectively. In the case of a GTO or IGCT, an important device characteristic is the so-called turn-off gain $K_{off}=I_A/|I_G|$, i.e. the ratio of the anode current to the negative gate current required to turn-off the device. An approximate formula relating the turn-off gain to the α's of the two transistors is given by,

$$K_{off} = \frac{\alpha_n}{\alpha_n + \alpha_p - 1} \tag{6.3}$$

The ability of this model to predict dynamic effects depends on the dynamics included in the transistor models. If transistor junction capacitances are included, it is possible to model the *dv/dt* limit of the thyristor. Too high a value of dv_{AK}/dt will cause significant current to flow through the J_2 junction capacitance. This current acts like gate current and can turn on the device.

This model does not accurately represent spatial effects such as current crowding at turn-on (the *di/dt* limit), when only part of the device is conducting, and, in the case of a GTO, current crowding at turn-off, when current is extracted from the gate to turn-off the device. Current crowding is caused by the location of the gate connection with respect to the conducting area of the thyristor and by the magnetic field generated by the changing conduction current. To model these effects, Tsay *et al.* [13] propose a multi-cell circuit model, in which the device is discretized in a number of conducting cells, each having the structure of Fig. 6.29. This model, shown in Fig. 6.30, takes into account the mutual inductive coupling, the delay in the gate turn-off signal due to positions of the cells relative to the gate connection, and non-uniform gate- and cathode-contact resistance. In particular, the *RC* delay circuits (series *R* with a shunt C tied to the cathode node) model the time delays between the gate triggering signals due to the position of the cell with respect to the gate connection; coupled inductors, *M*, model magnetic coupling between cells; resistors, R_{KC}, model non-uniform contact resistance; and resistors, R_{GC}, model gate contact resistances. The various circuit elements in the model can be estimated from device geometry and measured electrical characteristics. The choice of the number of cells is a tradeoff between accuracy and complexity. Example values of the *RC* delay network, R_{GC}, R_{KC}, and *M* are given in Table 6.6.

Other GTO thyristor models have been developed which offer improved accuracy at the expense of increased complexity. The model by Tseng *et al.* [14] includes charge storage

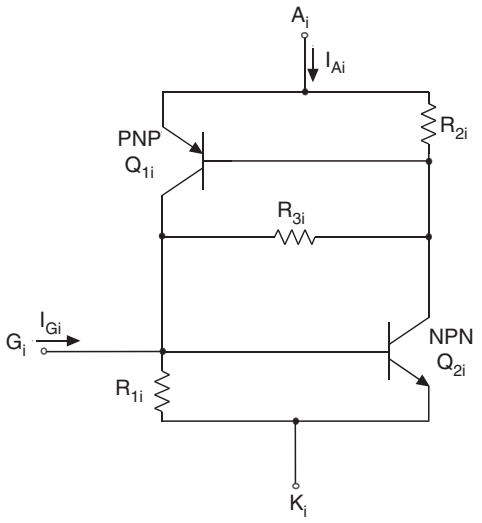

FIGURE 6.29 A two-transistor, three-resistor model for SCRs and GTOs.

TABLE 6.6 Element values for each cell of a multi-cell GTO model

Model component	Symbol	Value
Delay resistor	*R*	1 μΩ
Delay capacitor	*C*	1 nF
Mutual coupling inductance	*M*	10 nH
Gate contact resistance	R_{GC}	1 mΩ
Cathode contact resistance	R_{KC}	1 mΩ

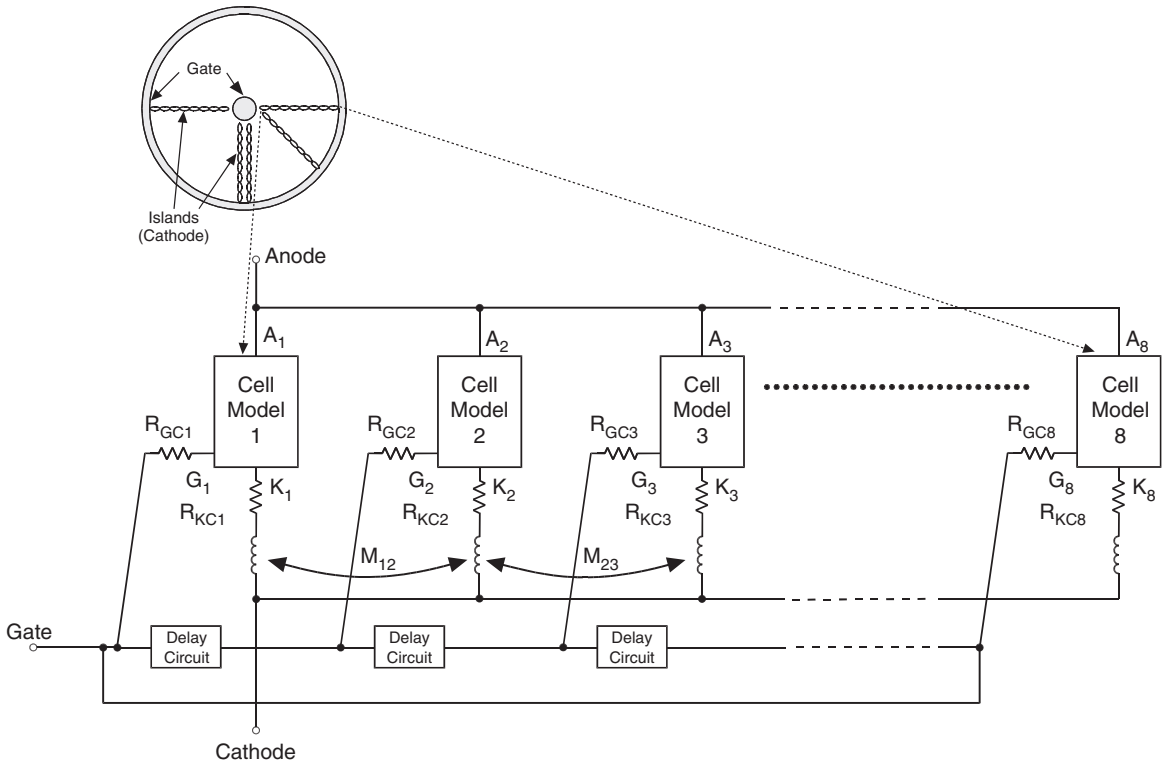

FIGURE 6.30 Thyristor multi-cell circuit model containing eight cells.

effects in the *n*-base, and its application to a multi-cell model, as in Fig. 6.30, has been demonstrated successfully. Models for the IGCT, based on the lumped-charge approach [15] and the Fourier-based solution of the ambipolar diffusion equation (ADE) [16], have also been developed.

6.9 Applications

The most important application of thyristors is for line-frequency phase-controlled rectifiers. This family includes several topologies, of which one of the most important is used to construct HVDC transmission systems. A single-phase controlled rectifier is shown in Fig. 6.31.

The use of thyristors instead of diodes allows the average output voltage to be controlled by appropriate gating of the thyristors. If the gate signals to the thyristors were continuously applied, the thyristors in Fig. 6.31 would behave as diodes. If no gate currents are supplied they behave as open circuits. Gate current can be applied any time (phase delay) after the forward voltage becomes positive. Using this phase-control feature, it is possible to produce an average dc output voltage less than the average output voltage obtained from an uncontrolled diode rectifier.

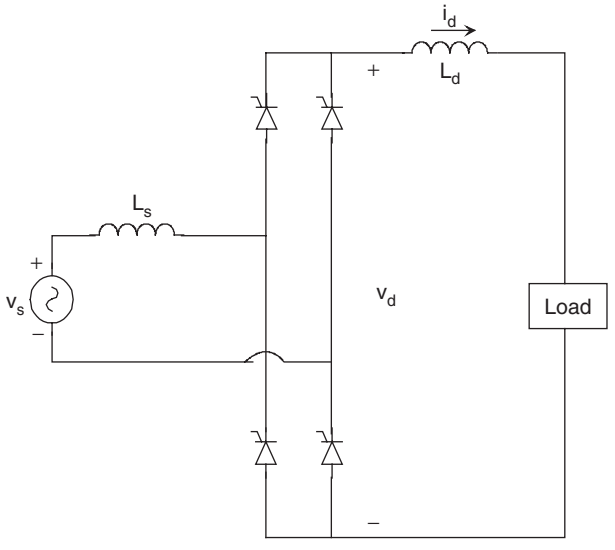

FIGURE 6.31 Single-phase controlled rectifier circuit.

6.9.1 DC–AC Utility Inverters

Three-phase converters can be made in different ways, according to the system in which they are employed. The basic circuit used to construct these topologies – the three-phase controlled rectifier – is shown in Fig. 6.32.

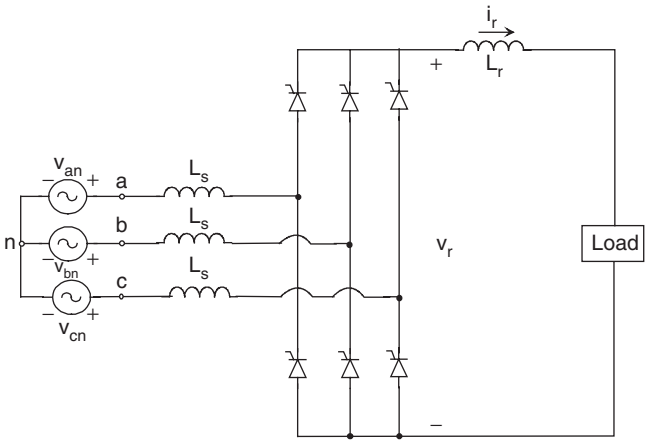

FIGURE 6.32 A three-phase controlled bridge circuit used as a basic topology for many converter systems.

Starting from this basic configuration, it is possible to construct more complex circuits in order to obtain high-voltage or high-current outputs, or just to reduce the output ripple by constructing a multi-phase converter. One of the most important systems using the topology shown in Fig. 6.32 as a basic circuit is the HVDC system represented in Fig. 6.33. This system is made by two converters, a transmission line, and two ac systems. Each converter terminal is made of two poles. Each pole is made by two six-pulse line-frequency converters connected through Δ-Y and Y-Y transformers in order to obtain a twelve-pulse converter and a reduced output ripple. The filters are required to reduce the current harmonics generated by the converter.

When a large amount of current and relatively low voltage is required, it is possible to connect in parallel, using a specially designed inductor, two six-pulse line-frequency converters connected through Δ-Y and Y-Y transformers. The special inductor is designed to absorb the voltage between the two converters, and to provide a pole to the load. This topology is shown in Fig. 6.34. This configuration is often known as a twelve-pulse converter. Higher pulse numbers may also be found.

6.9.2 Motor Control

Another important application of thyristors is in motor control circuits. Historically thyristors have been used heavily in traction, although most new designs are now based on IGBTs. Such motor control circuits broadly fall into four types: i) chopper control of a dc motor from a dc supply; ii) single- or three-phase converter control of a dc motor from an ac supply; iii) inverter control of an ac synchronous or induction machine from a dc supply and iv) cycloconverter control of an ac machine from an ac supply. An example of a GTO chopper is given in Fig. 6.35. L_1, R_1, D_1, and C_1 are the turn-on snubber; R_2, D_2, and C_2 are the turn-off snubber; finally R_3 and D_3 form the snubber for the freewheel diode D_3. A thyristor cycloconverter is shown in Fig. 6.36; the waveforms show the fundamental component of the output voltage for one phase. Three double converters are used to produce a three-phase

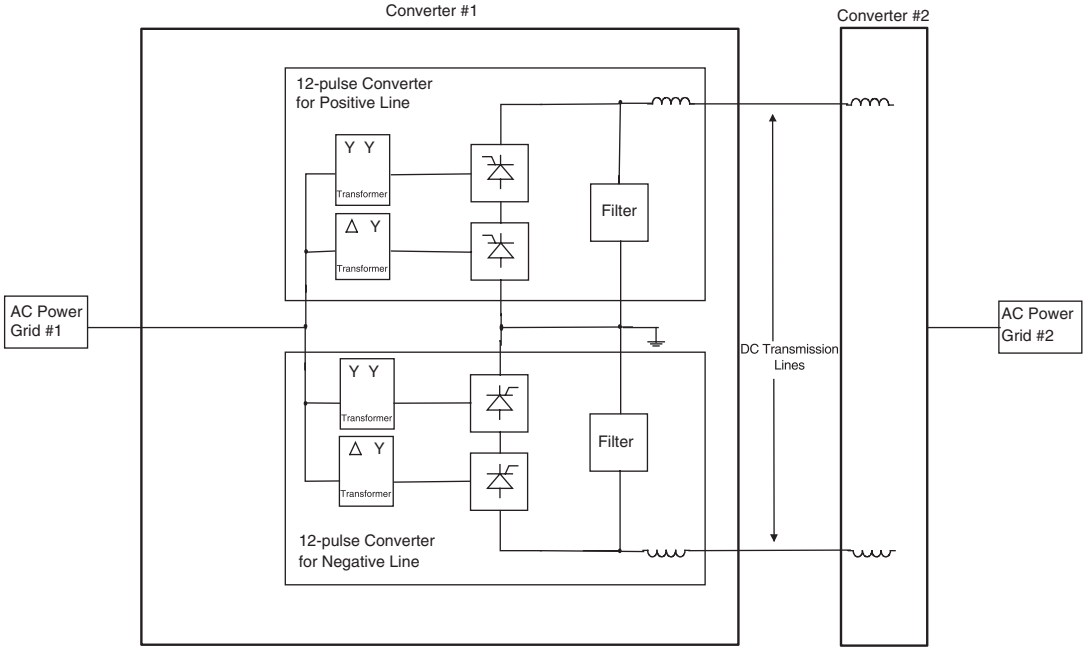

FIGURE 6.33 A HVDC transmission system.

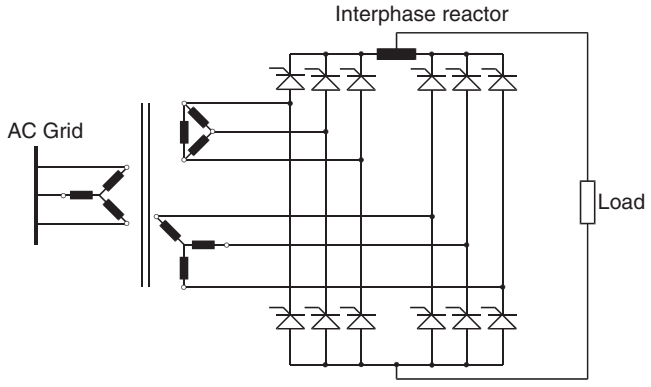

FIGURE 6.34 Parallel connection of two six-pulse converters for high current applications.

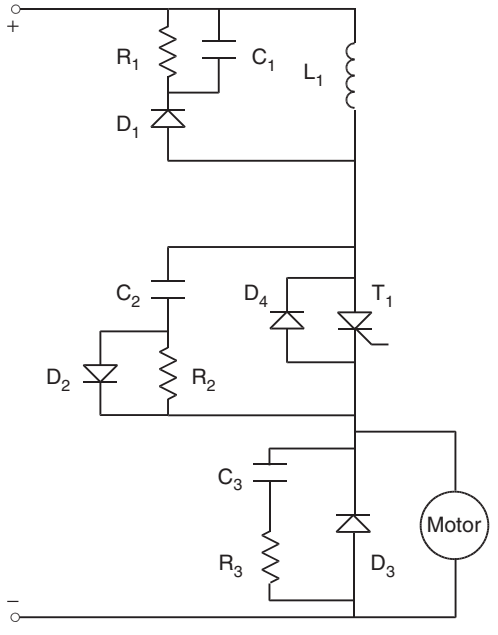

FIGURE 6.35 GTO chopper for dc motor control.

variable-frequency, variable voltage sinusoidal output for driving ac motors. However, the limited frequency range (less than a third of the line frequency) restricts the application to large, low-speed machines at high powers.

A single- or three-phase thyristor converter (controlled rectifier) may be used to provide a variable dc supply for controlling a dc motor. Such a converter may also be used as the front end of a three-phase induction motor drive. The variable voltage, variable frequency motor drive requires a dc supply, which is supplied by the thyristor converter. The drive may use a square-wave or PWM voltage source inverter (VSI), or a current source inverter (CSI). Figure 6.37 shows a square-wave or PWM VSI with a controlled rectifier on the input side. The switch block inverter may be made of thyristors (usually GTOs or IGCTs) for high power, although most new designs

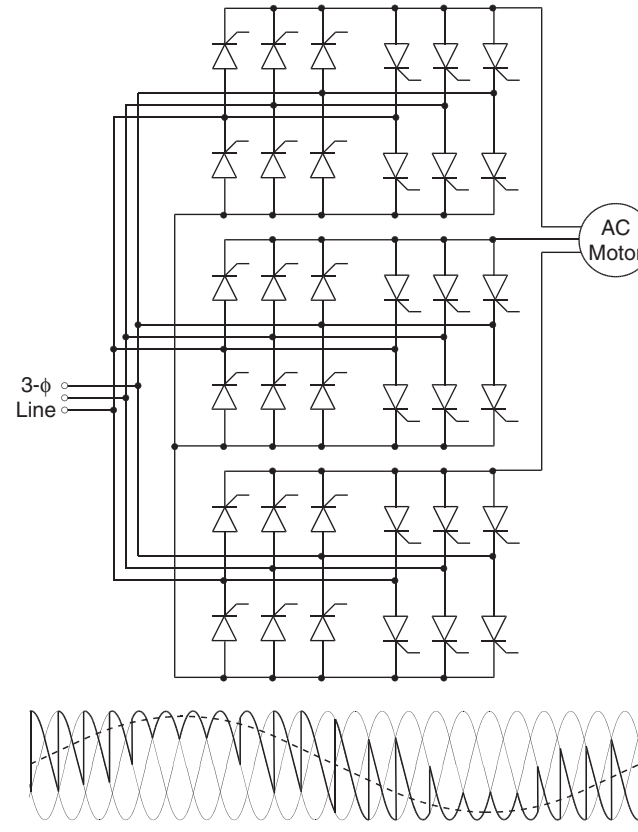

FIGURE 6.36 Cycloconverter for control of large ac machines.

now use IGBTs. Low-power motor controllers generally use IGBT inverters.

In motor control, thyristors are also used in CSI topologies. When the motor is controlled by a CSI, a controlled rectifier is also needed on the input side. Figure 6.38 shows a typical CSI inverter. The capacitors are needed to force the current in the thyristors to zero at each switching event. This is not needed when using GTOs. This inverter topology does not need any additional circuitry to provide the regenerative braking (energy recovery when slowing the motor). Historically, two back-to-back connected line-frequency thyristor converters have been employed to allow bi-directional power flow, and thus regenerative braking. Use of anti-parallel GTOs with symmetric blocking capability, or the use of diodes in series with each asymmetric GTO, reduces the number of power devices needed, but greatly increases the control complexity.

6.9.3 VAR Compensators and Static Switching Systems

Thyristors are also used to switch capacitors or inductors in order to control the reactive power in the system. Such arrangements may also be used in phase-balancing circuits for

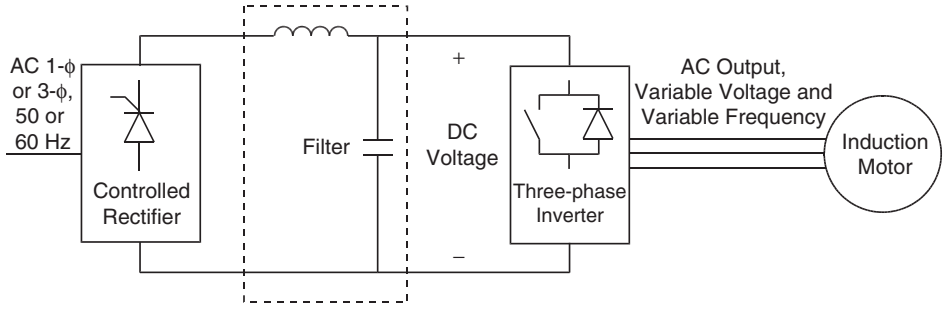

FIGURE 6.37 PWM or square-wave inverter with a controlled rectifier input.

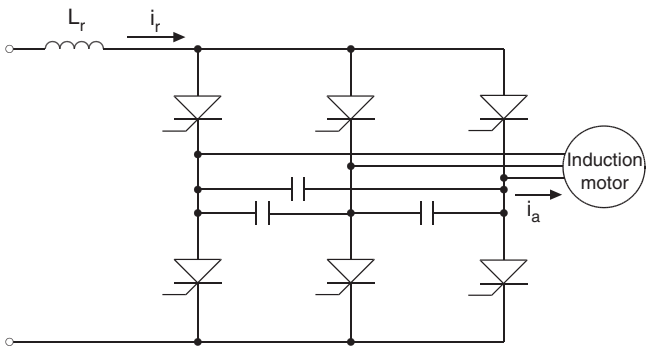

FIGURE 6.38 CSI on the output section of a motor drive system using capacitors for power factor correction.

balancing the load fed from a three-phase supply. Examples of these circuits are shown in Fig. 6.39. These circuits act as static VAR controllers. The topology represented on the left of Fig. 6.39 is called a thyristor-controlled inductor (TCI) and it acts as a variable inductor where the inductive VAR supplied can be varied quickly. Because the system may require either inductive or capacitive VAR compensation, it is possible to connect a bank of capacitors in parallel with a TCI. The topology shown on the right of Fig. 6.39 is called a thyristor-switched capacitor (TSC). Capacitors can be switched out by blocking the gate pulse of all thyristors in the circuit. The problem of this topology is the voltage across the capacitors at the thyristor turn-off. At turn-on the thyristor must be gated at the instant of the maximum ac voltage to avoid large over-currents. Many recent SVCs have used GTOs.

A similar application of thyristors is in solid-state fault current limiters and circuit breakers. In normal operation, the thyristors are continuously gated. However, under fault conditions they are switched rapidly to increase the series impedance in the load and to limit the fault current. Key advantages are the flexibility of the current limiting, which is independent of the location of the fault and the change in load impedance, the reduction in fault level of the supply, and a smaller voltage sag during a short-circuit fault.

A less important application of thyristors is as a static transfer switch, used to improve the reliability of uninterruptible power supplies (UPS) as shown in Fig. 6.40. There are two modes of using the thyristors. The first leaves the load permanently connected to the UPS system and in case of emergency disconnects the load from the UPS and connects it directly to the power line. The second mode is opposite to the first one. Under normal conditions the load is permanently connected to the power line, and in event of a line outage, the load is disconnected from the power line and connected to the UPS system.

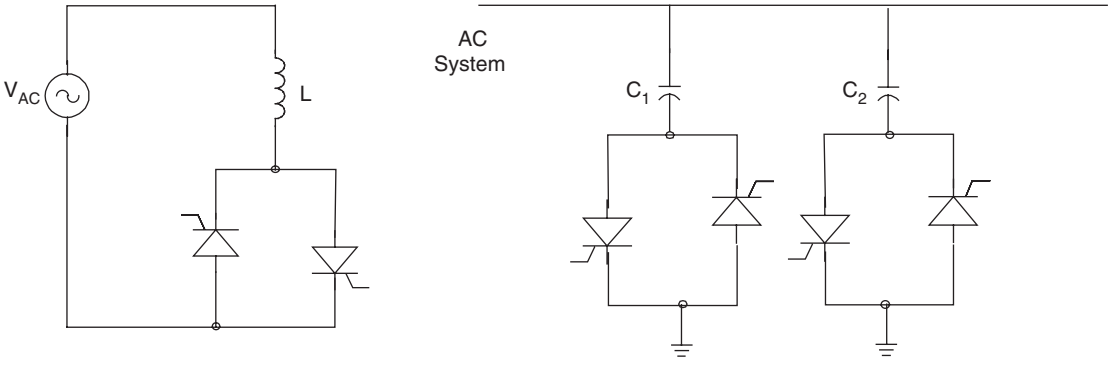

FIGURE 6.39 Per phase TCI and TSC system.

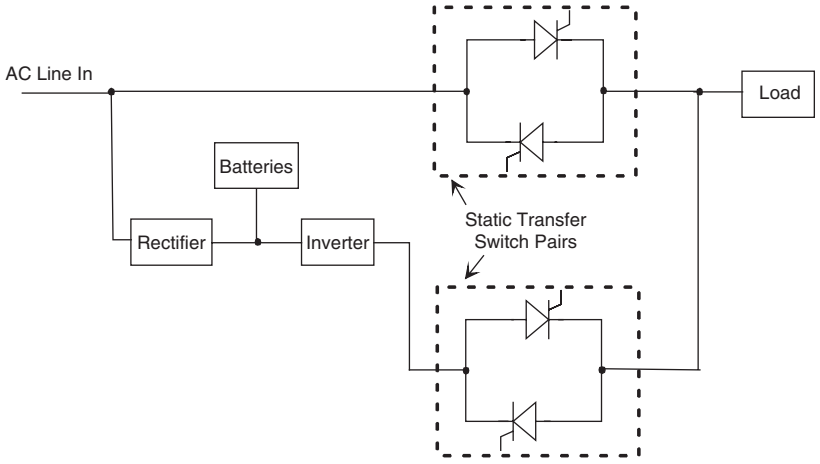

FIGURE 6.40 Static transfer switch used in an UPS system.

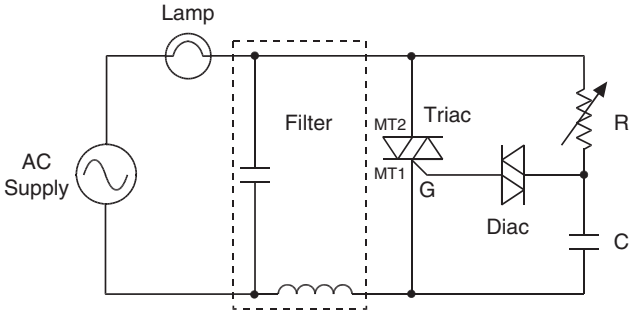

FIGURE 6.41 Basic dimmer circuit used in lighting control.

6.9.4 Lighting Control Circuits

An important circuit used in lighting control is the dimmer, based on a triac and shown in Fig. 6.41. The *R–C* network applies a phase shift to the gate voltage, delaying the triggering of the triac. Varying the resistance, controls the firing angle of the triac and therefore the voltage across the load. The diac is used to provide symmetrical triggering for the positive and negative half-cycles, due to the non-symmetrical nature of the triac. This ensures symmetrical waveforms and elimination of even harmonics. An *L–C* filter is often used to reduce any remaining harmonics.

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