23

Power Supplies

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23.1 Introduction

Power supplies are used in most electrical equipment. Their applications cut across a wide spectrum of product types, ranging from consumer appliances to industrial utilities, from milliwatts to megawatts, from hand-held tools to satellite communications.

By definition, a power supply is a device which converts the output from an ac power line to a steady dc output or multiple outputs. The ac voltage is first rectified to provide a pulsating dc, and then filtered to produce a smooth voltage. Finally, the voltage is regulated to produce a constant output level despite variations in the ac line voltage or circuit loading. Figure 23.1 illustrates the process of rectification, filtering, and regulation in a dc power supply. The transformer, rectifier, and filtering circuits are discussed in other chapters. In this chapter, we will concentrate on the operation and characteristics of the regulator stage of a dc power supply.

In general, the regulator stage of a dc power supply consists of a feedback circuit, a stable reference voltage, and a control circuit to drive a pass element (a solid-state device such as transistor, MOSFET, etc.). The regulation is done by sensing variations appearing at the output of the dc power supply. A control signal is produced to drive the pass element to cancel any variation. As a result, the output of the dc power supply is maintained essentially constant. In a transistor regulator, the pass element is a transistor, which can be operated in its active region or as a switch, to regulate the output voltage. When the transistor operates at any point in its active region, the regulator is referred to as a *linear voltage regulator*. When the transistor operates only at cutoff and at saturation, the circuit is referred to as a *switching regulator*.

Linear voltage regulators can be further classified as either series or shunt types. In a series regulator, the pass transistor is connected in series with the load as shown in Fig. 23.2. Regulation is achieved by sensing a portion of the output voltage through the voltage divider network R_1 and R_2, and comparing this voltage with the reference voltage V_{REF} to produce a resulting error signal that is used to control the conduction of the pass transistor. This way, the voltage drop across the pass transistor is varied and the output voltage delivered to the load circuit is essentially maintained constant.

In the shunt regulator shown in Fig. 23.3, the pass transistor is connected in parallel with the load, and a voltage-dropping

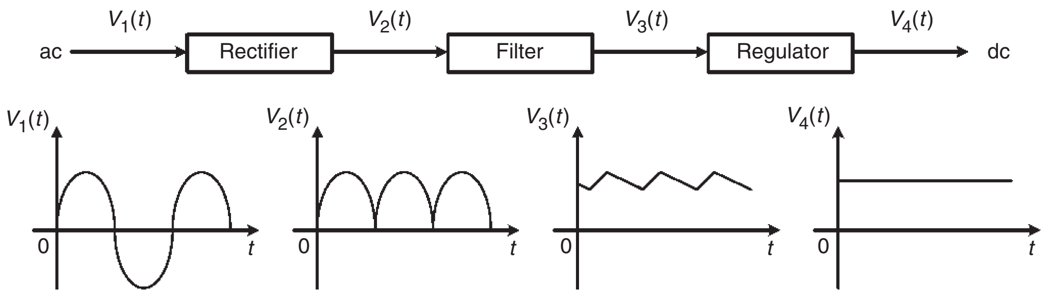


FIGURE 23.1 Block diagram of a dc power supply.

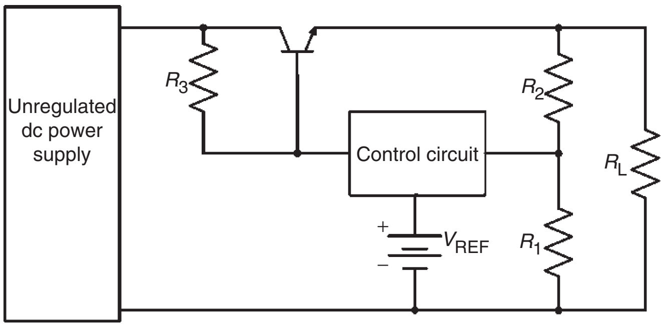


FIGURE 23.2 A linear series voltage regulator.

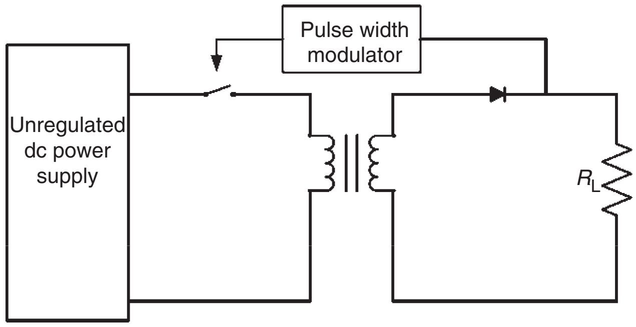


FIGURE 23.4 A simplified form of a switching regulator.

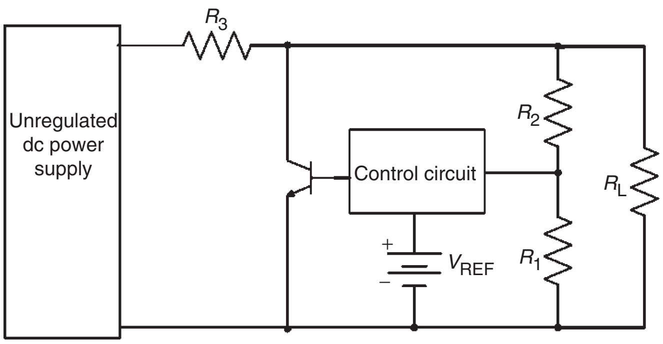


FIGURE 23.3 A linear shunt voltage regulator.

resistor R_3 is connected in series with the load. Regulation is achieved by controlling the current conduction of the pass transistor such that the current through R_3 remains essentially constant. This way, the current through the pass transistor is varied and the voltage across the load remains constant.

As opposed to linear voltage regulators, switching regulators employ solid-state devices, which operate as switches: either completely *on* or completely *off*, to perform power conversion. Because the switching devices are not required to operate in their active regions, switching regulators enjoy a much lower power loss than those of linear voltage regulators. Figure 23.4 shows a switching regulator in a simplified form. The high-frequency switch converts the unregulated dc voltage from one level to another dc level at an adjustable duty cycle. The output of the dc supply is regulated by means of a feedback control that employs a pulse-width-modulator (PWM) controller, where the control voltage is used to adjust the duty cycle of the switch.

Both linear and switching regulators are capable of performing the same function of converting an unregulated input into a regulated output. However, these two types of regulators have significant differences in properties and performances. In designing power supplies, the choice of using certain type of regulator in a particular design is significantly based on the cost and performance of the regulator itself. In order to use the more appropriate regulator type in the design, it is necessary to understand the requirements of the application and select the type of regulator that best satisfies those requirements. Advantages and disadvantages of linear regulators, as compared to switching regulators, are given below:

1. Linear regulators exhibit efficiency of 20–60%, whereas switching regulators have a much higher efficiency, typically 70–95%.
2. Linear regulators can only be used as a step-down regulator, whereas switching regulators can be used in both step-up and step-down operations.

3. Linear regulators require a mains-frequency transformer for off-the-line operation. Therefore, they are heavy and bulky. On the other hand, switching regulators use high-frequency transformers and can therefore be small in size.
4. Linear regulators generate little or no electrical noise at their outputs, whereas switching regulators may produce considerable noise if they are not properly designed.
5. Linear regulators are more suitable for applications of less than 20 W, whereas switching regulators are more suitable for large power applications.

In this chapter, we will examine the circuit operation, characteristics, and applications of linear and switching regulators. In Section 23.2, we will look at the basic circuits and properties of linear series voltage regulators. Some current-limiting techniques will be explained. In Section 23.3, linear shunt regulators will be covered. The important characteristics and uses of linear Integrated Circuit (IC) regulators will be discussed in Section 23.4. Finally, the operation and characteristics of switching regulators will be discussed in Section 23.5. Important design guidelines for switching regulators will also be given in this section.

23.2 Linear Series Voltage Regulator

A zener diode regulator can maintain a fairly constant voltage across a load resistor. It can be used to improve the voltage regulation and reduce the ripple in a power supply. However, the regulation is poor and the efficiency is low because of the non-zero resistance in the zener diode. To improve the regulation and efficiency of the regulator, we have to limit the zener current to a smaller value. This can be accomplished by using an amplifier in series with the load as shown in Fig. 23.5. The effect of this amplifier is to limit the variation of the current I_D through the zener diode D_z. This circuit is known as a linear series voltage regulator because the transistor is in series with the load.

Because of the current-amplifying property of the transistor, I_D is reduced by a factor of $(\beta + 1)$, where β is the dc current gain of the transistor. Hence there is a small voltage drop across the diode resistance and the zener diode approximates an ideal voltage source. The output voltage V_o of the regulator is

$$V_o = V_z + V_{BE} \tag{23.1}$$

where V_z is the zener voltage and V_{BE} is the base-to-emitter voltage of the transistor. The change in output voltage is

$$\begin{aligned} \Delta V_o &= \Delta V_z + \Delta V_{BE} \\ &= \Delta I_D r_d + \Delta I_L r_e \end{aligned} \tag{23.2}$$

where r_d is the dynamic resistance of the zener diode and r_e is the output resistance of the transistor. Assume that V_i and V_z are constant. With $\Delta I_D \approx \Delta I_L/(\beta + 1)$, the change in output voltage is then

$$\Delta V_o \approx \Delta I_L r_e \tag{23.3}$$

If V_i is not constant, then the current I will change with the input voltage. In calculating the change in output voltage, this current change must be absorbed by the zener diode.

In designing linear series voltage regulators, it is imperative that the series transistor must work within the rated Safe Operation Area (SOA) and be protected from excess heat dissipation because of current overload. The emitter-to-collector voltage V_{CE} of Q_1 is given by

$$V_{CE} = V_i - V_o \tag{23.4}$$

Thus, with specified output voltage, the maximum allowable V_{CE} for a given Q_1 is determined by the maximum input

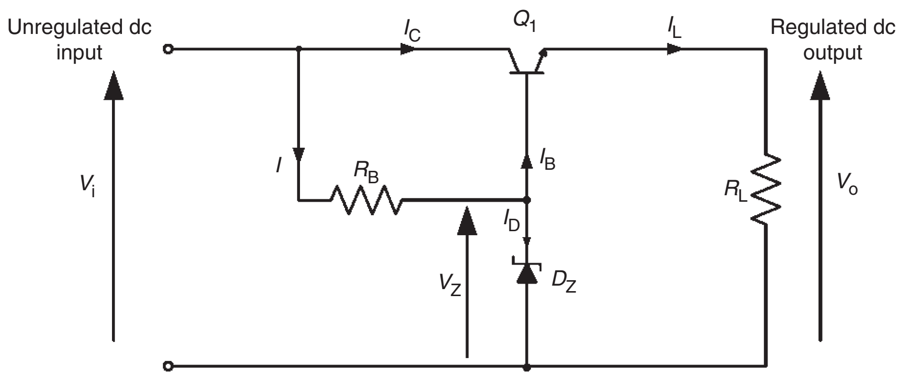


FIGURE 23.5 Basic circuit of a linear series regulator.

voltage to the regulator. The power dissipated by Q_1 can be approximated by

$$P_{Q1} \approx (V_i - V_o)I_L \tag{23.5}$$

Consequently, the maximum allowable power dissipated in Q_1 is determined by the combination of the input voltage V_i and the load current I_L of the regulator. For a low output voltage and a high loading current regulator, the power dissipated in the series transistor is about 50% of the power delivered to the output.

In many high-current high-voltage regulator circuits, it is necessary to use a Darlington-connected transistor pair so that the voltage, current, and power ratings of the series element are not exceeded. The method is shown in Fig. 23.6. An additional desirable feature of this circuit is that the reference diode dissipation can be reduced greatly. The maximum base current I_{B1} is then $I_L/(\beta_1 + 1)(\beta_2 + 1)$, where β_1 and β_2 are the dc current gain of Q_1 and Q_2 respectively. This current is usually of the order of less than 1 mA. Consequently, a low-power reference diode can be used.

23.2.1 Regulating Control

The series regulators shown in Figs. 23.5 and 23.6 do not have feedback loop. Although they provide satisfactory performance for many applications, their output resistances and ripples cannot be reduced. Figure 23.7 shows an improved form of the series regulator, in which negative feedback is employed to improve the performance. In this circuit, transistors Q_3 and Q_4 form a single-ended differential amplifier, and the gain of this amplifier is established by R_6. Here D_z is a stable zener diode reference, biased by R_4. For higher accuracy, D_z can be replaced by an IC reference such as REF series from Burr-Brown. Resistors R_1 and R_2 form a voltage divider for output voltage sensing. Finally, transistors Q_1 and Q_2 form a Darlington pair output stage. The operation of the regulator can be explained as follows. When Q_1 and Q_2 are on, the output voltage increases, and hence the voltage V_A at the base of Q_3 also increases. During this time, Q_3 is off and Q_4 is on. When V_A reaches a level that is equal to the reference voltage V_{REF} at the base of Q_4, the base-emitter junction of Q_3 becomes forward-biased. Some Q_1 base current will divert into the collector of Q_3. If the output voltage V_o starts to rise above V_{REF}, Q_3 conduction increases to further decrease the conduction of Q_1 and Q_2, which will in turn maintain output voltage regulation. Figure 23.8 shows another improved series regulator that uses an operational amplifier to control the conduction of the pass transistor.

One of the problems in the design of linear series voltage regulators is the high-power dissipation in the pass transistors. If an excess load current is drawn, the pass transistor can be quickly damaged or destroyed. In fact, under short-circuit conditions, the voltage across Q_2 in Fig. 23.7, will be the input voltage V_i, and the current through Q_2 will be greater than the rated full-load output current. This current will cause Q_1 to exceed its rated SOA unless the current is reduced. In the next section, some current-limiting techniques will be presented to overcome this problem.

23.2.2 Current Limiting and Overload Protection

In some series voltage regulators, overloading causes permanent damage to the pass transistors. The pass transistors must be kept from excessive power dissipation under current overloads or short circuit conditions. A current-limiting mechanism must be used to keep the current through the transistors at a safe value as determined by the power rating of the transistors. The mechanism must be able to respond quickly to protect the transistor and yet permit the regulator to

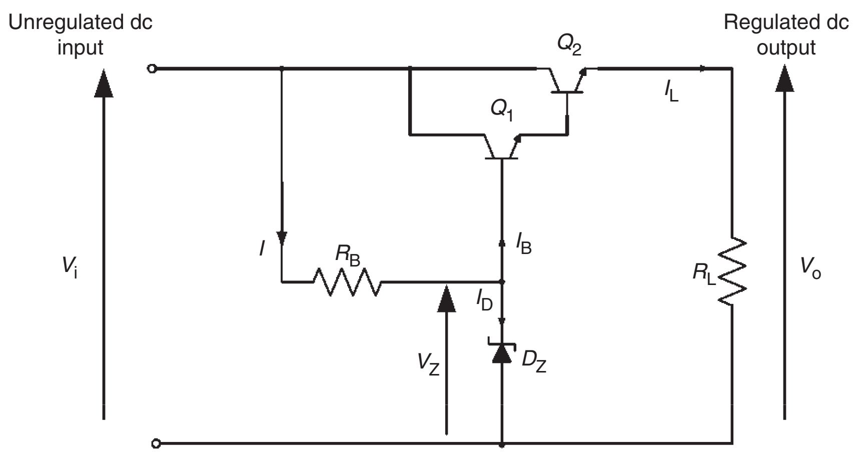


FIGURE 23.6 A linear series regulator with Darlington-connected amplifier.

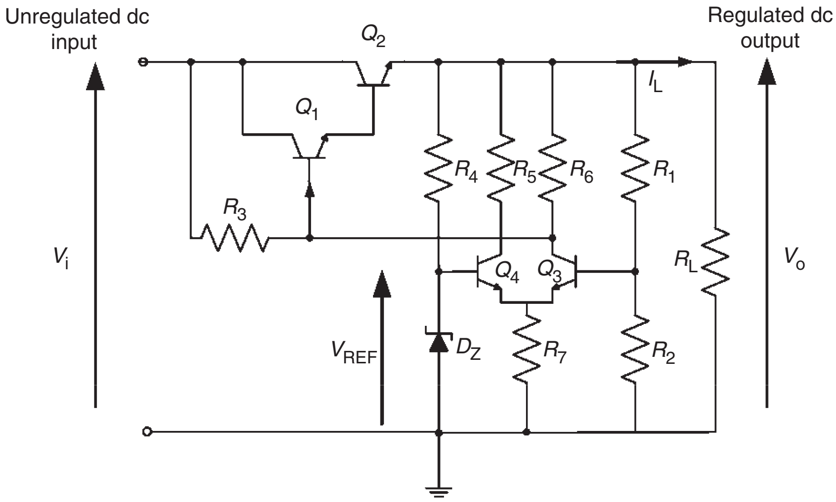


FIGURE 23.7 An improved form of discrete component series regulator.

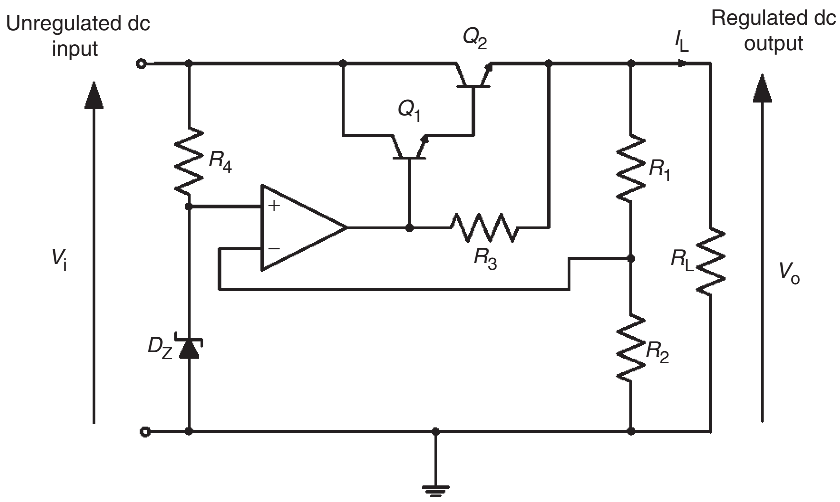


FIGURE 23.8 An improved form of op-amp series regulator.

return to normal operation as soon as the overload condition is removed. One of the current-limiting techniques to prevent current overload, called the constant current-limiting method, is shown in Fig. 23.9(a). Current limiting is achieved by the combined action of the components shown inside the dashed line. The voltage developed across the current-limit resistor R_3 and the base-to-emitter voltage of current-limit transistor Q_3 is proportional to the circuit output current I_L. During current overload, I_L reaches a predetermined maximum value that is set by the value of R_3 to cause Q_3 to conduct. As Q_3 starts to conduct, Q_3 shunts a portion of the Q_1 base current. This action, in turn, decreases and limits I_L to a maximum value $I_{L(max)}$. Since the base-to-emitter voltage V_{BE} of Q_3 cannot exceed above 0.7 V, the voltage across R_3 is held at this value and $I_{L(max)}$ is limited to

$$I_{L(max)} = \frac{0.7\,\text{V}}{R_3} \tag{23.6}$$

Consequently, the value of the short-circuit current is selected by adjusting the value of R_3. The voltage–current characteristic of this circuit is shown in Fig. 23.9(b).

In many high-current regulators, foldback current limiting is always used to protect against excessive current. This technique is similar to the constant current-limiting method, except that as the output voltage is reduced as a result of load impedance moving toward zero, the load current is also reduced. Therefore, a series voltage regulator that includes

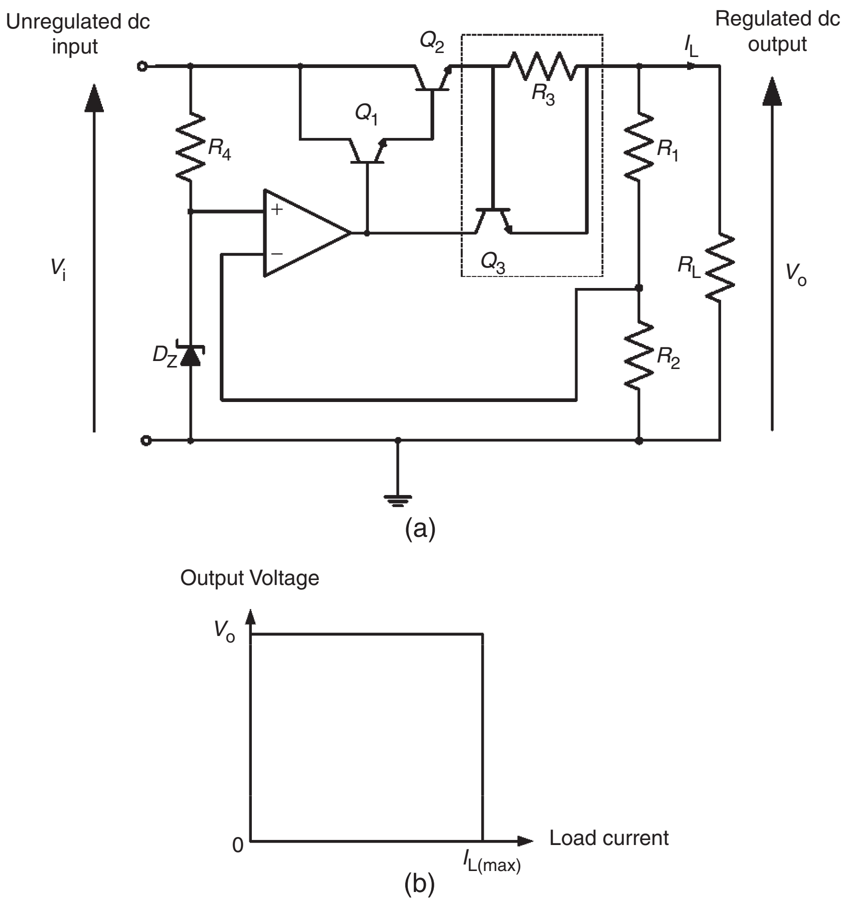


FIGURE 23.9 Series regulator with constant current limiting: (a) circuit and (b) voltage–current characteristic.

a foldback current-limiting circuit has the voltage–current characteristic shown in Fig. 23.10. The basic idea of foldback current limiting, with reference to Fig. 23.11, can be explained as follows. The foldback current-limiting circuit (in dashed outline) is similar to the constant current-limiting circuit, with the exception of resistors R_5 and R_6. At low output current, the current-limit transistor Q_3 is cutoff.

A voltage proportional to the output current I_L is developed across the current-limit resistor R_3. This voltage is applied to the base of Q_3 through the divider network R_5 and R_6. At the point of transition into current-limit, any further increase in I_L will increase the voltage across R_3 and hence across R_5, and Q_3 will progressively be turned on. As Q_1 conducts, it shunts a portion of the Q_1 base current. This action, in turn, causes the output voltage to fall. As the output voltage falls, the voltage across R_6 decreases and the current in R_6 also decreases, and more current is shunted into the base of Q_3. Hence, the current required in R_3 to maintain the conduction state of Q_3 is also decreased. Consequently, as the load resistance is reduced, the output voltage and current fall, and the current-limit point decreases toward a minimum when the output voltage is short-circuited. In summary, any regulator using foldback current limiting can have peak load current up to $I_{L(max)}$. But when the output becomes shorted, the current drops to a lower value to prevent overheating of the series transistors.

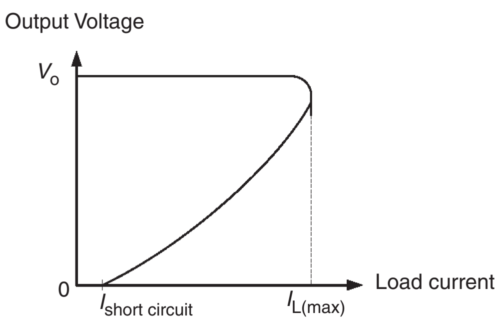


FIGURE 23.10 Voltage–current characteristic of foldback current-limit.

23.3 Linear Shunt Voltage Regulator

The second type of linear voltage regulator is the shunt regulator. In the basic circuit shown in Fig. 23.12, the pass transistor

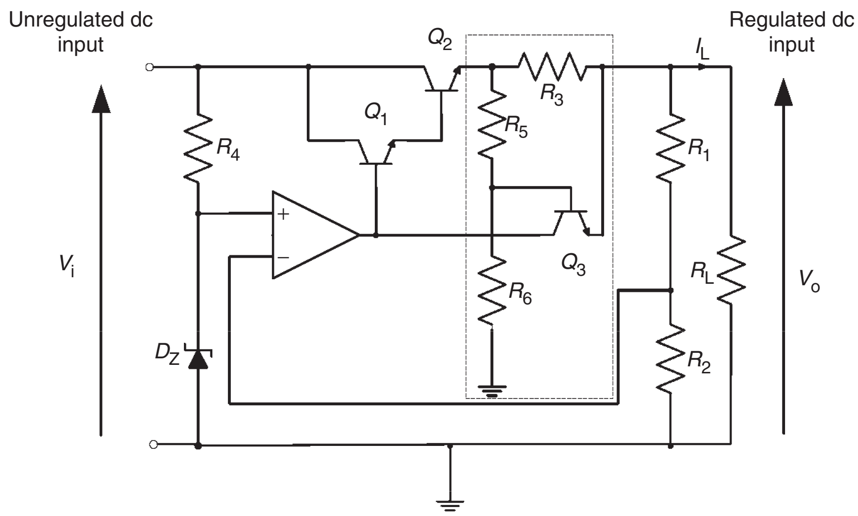


FIGURE 23.11 Series regulator with foldback current limiting.

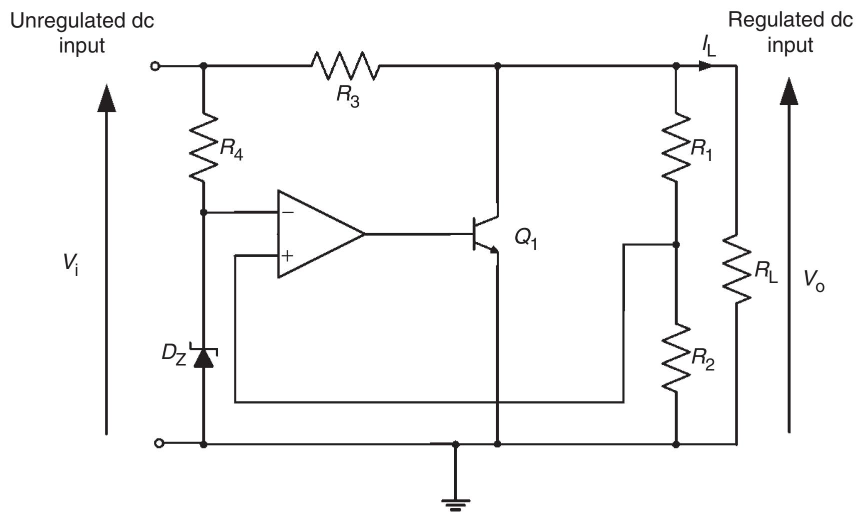


FIGURE 23.12 Basic circuit of a linear shunt regulator.

Q_1 is connected in parallel with the load. A voltage-dropping resistor R_3 is in series with this parallel network. The operation of the circuit is similar to that of the series regulator, except that regulation is achieved by controlling the current through Q_1. The operation of the circuit can be explained as follows. When the output voltage tries to increase because of a change in load resistance, the voltage at the non-inverting terminal of the operational amplifier also increases. This voltage is compared with a reference voltage and the resulting difference voltage causes Q_1 conduction to increase. With constant V_i and V_o, I_L will decrease and V_o will remain constant. The opposite action occurs when V_o tries to decrease. The voltage appearing at the base of Q_1 causes its conduction to decrease. This action offsets the attempted decrease in V_o and maintains it at an almost constant level.

Analytically, the current flowing in R_3 is

$$I_{R3} = I_{Q1} + I_L \tag{23.7}$$

and

$$I_{R3} = \frac{V_i - V_o}{R_3} \tag{23.8}$$

With I_L and V_o constant, a change in V_i will cause a change in I_{Q1}.

$$\Delta I_{Q1} = \frac{\Delta V_i}{R_3} \tag{23.9}$$

With V_i and V_o constant,

$$\Delta I_{Q1} = -\Delta I_L \tag{23.10}$$

Equation (23.10) shows that if I_{Q1} increases, I_L decreases, and vice versa. Although shunt regulators are not as efficient as series regulators for most applications, they have the advantage of greater simplicity. This topology offers inherently short-circuit protection. If the output is shorted, the load current is limited by the series resistor R_3 and is given by

$$I_{L(max)} = \frac{V_i}{R_3} \tag{23.11}$$

The power dissipated by Q_1 can be approximated by

$$\begin{aligned} P_{Q1} &\approx V_o I_C \\ &= V_o(I_{R3} - I_L) \end{aligned} \tag{23.12}$$

For a low value of I_L, the power dissipated in Q_1 is large and the efficiency of the regulator may drop to 10% under this condition.

To improve the power handling of the shunt transistor, one or more transistors connected in the common-emitter configuration in parallel with the load can be employed, as shown in Fig. 23.13.

23.4 Integrated Circuit Voltage Regulators

The linear series and shunt voltage regulators presented in the previous sections have been developed by various solid-state device manufacturers and are available in integrated circuit (IC) form. Like discrete voltage regulators, linear IC voltage regulators maintain an output voltage at a constant value despite variations in load and input voltage.

In general, linear IC voltage regulators are three-terminal devices that provide regulation of a fixed positive voltage, a fixed negative voltage, or an adjustable set voltage. The basic connection of a three-terminal IC voltage regulator to a load is shown in Fig. 23.14. The IC regulator has an unregulated input voltage V_i applied to the input terminals, a regulated voltage V_o at the output, and a ground connected to the third terminal. Depending on the selected IC regulator, the circuit can be operated with load currents ranging from milliamperes to tens of amperes and output power from milliwatts to tens

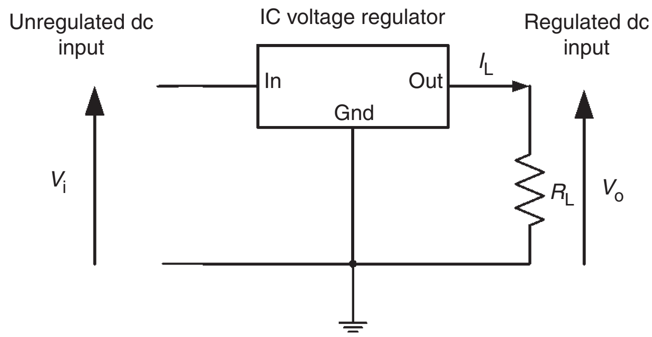


FIGURE 23.14 Basic connection of a three-terminal IC voltage regulator.

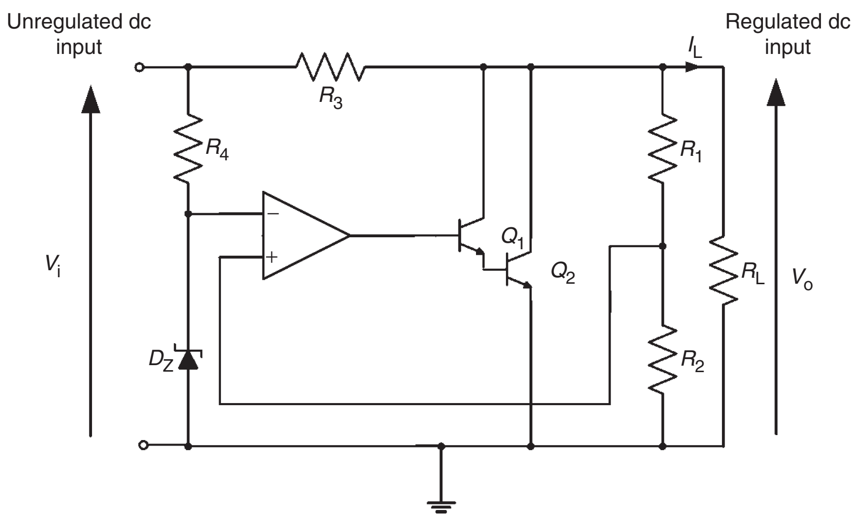


FIGURE 23.13 Linear shunt regulator with two transistors as shunt element.

of watts. Note that the internal construction of IC voltage regulators may be somewhat more complex and different from that previously described for discrete voltage regulator circuits. However, the external operation is much the same. In this section, some typical linear IC regulators are presented and their applications are also given.

23.4.1 Fixed Positive and Negative Linear Voltage Regulators

The 78XX series of regulators provide fixed regulated voltages from 5 to 24 V. The last two digits of the IC part number denote the output voltage of the device. For example, a 7824 IC regulator produces a +24 V regulated voltage at the output. The standard configuration of a 78XX fixed positive voltage regulator is shown in Fig. 23.15. The input capacitor C_1 acts as a line filter to prevent unwanted variations in the input line, and the output capacitor C_2 is used to filter the high-frequency noise that may appear at the output. In order to ensure proper operation, the input voltage of the regulator must be at least 2 V above the output voltage. Table 23.1 shows the minimum and maximum input voltages of the 78XX series fixed positive voltage regulator.

The 79XX series voltage regulator is identical to the 78XX series except that it provides negative regulated voltages instead of positive ones. Figure 23.16 shows the standard configuration of a 79XX series voltage regulator. A list of 79XX series regulators is provided in Table 23.2. The regulation of the circuit can be maintained as long as the output voltage is at least 2–3 V greater than the input voltage.

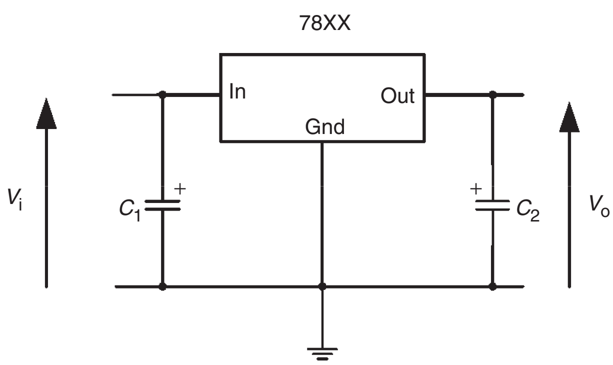


FIGURE 23.15 The 78XX series fixed positive voltage regulator.

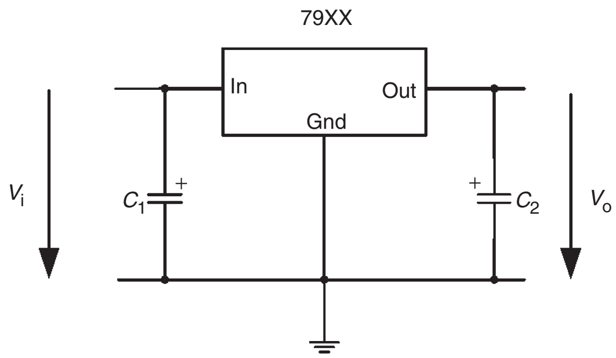


FIGURE 23.16 The 79XX series fixed negative voltage regulator.

TABLE 23.1 Minimum and maximum input voltages for 78XX series regulators

Type number	Output voltage V_o(V)	Minimum V_i(V)	Maximum V_i(V)
7805	+5	7	20
7806	+6	8	21
7808	+8	10.5	25
7809	+9	11.5	25
7812	+12	14.5	27
7815	+15	17.5	30
7818	+18	21	33
7824	+24	27	38

TABLE 23.2 Minimum and maximum input voltages for 79XX series regulators

Type number	Output voltage V_o(V)	Minimum V_i(V)	Maximum V_i(V)
7905	−5	−7	−20
7906	−6	−8	−21
7908	−8	−10.5	−25
7909	−9	−11.5	−25
7912	−12	−14.5	−27
7915	−15	−17.5	−30
7918	−18	−21	−33
7924	−24	−27	−38

23.4.2 Adjustable Positive and Negative Linear Voltage Regulators

The IC voltage regulators are also available in circuit configurations that allow the user to set the output voltage to a desired regulated value. The LM317 adjustable positive voltage regulator, for example, is capable of supplying an output current of more than 1.5 A over an output voltage range of 1.2–37 V. Figure 23.17 shows how the output voltage of an LM317 can be adjusted by using two external resistors R_1 and R_2. The capacitors C_1 and C_2 have the same function as those in the fixed linear voltage regulator.

As indicated in Fig. 23.17, the LM317 has a constant 1.25 V reference voltage, V_{REF}, across the output and the adjustment terminals. This constant reference voltage produces a constant current through R_1 regardless of the value of R_2. The output voltage V_o is given by

$$V_o = V_{REF}\left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 \qquad (23.13)$$

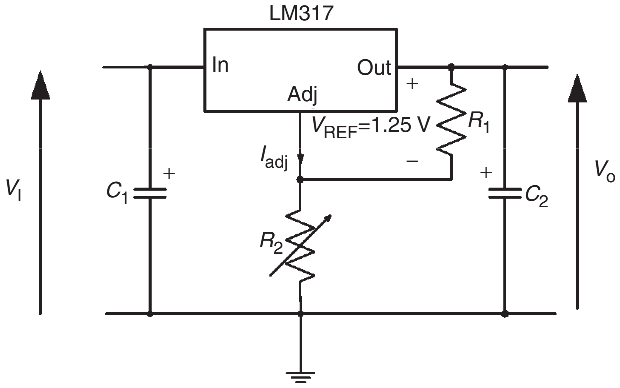


FIGURE 23.17 The LM317 adjustable positive voltage regulator.

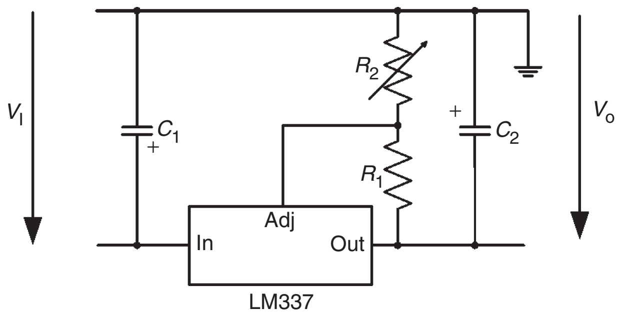


FIGURE 23.18 The LM337 adjustable negative voltage regulator.

where I_{adj} is a constant current into the adjustment terminal and has a value of approximately 50 μA for the LM317. As can be seen from Eq. (23.13), with fixed R_1, V_o can be adjusted by varying R_2.

The LM337 adjustable voltage regulator is similar to the LM317 except that it provides negative regulated voltages instead of positive ones. Figure 23.18 shows the standard configuration of a LM337 voltage regulator. The output voltage can be adjusted from –1.2 to –37 V, depending on the external resistors R_1 and R_2.

23.4.3 Applications of Linear IC Voltage Regulators

Most IC regulators are limited to an output current of 2.5 A. If the output current of an IC regulator exceeds its maximum allowable limit, its internal pass transistor will dissipate an amount of energy more than it can tolerate. As a result, the regulator will be shutdown.

For applications that require more than the maximum allowable current limit of a regulator, an external pass transistor can be used to increase the output current. Figure 23.19 illustrates such a configuration. This circuit has the capability of producing higher current to the load, but still preserving the thermal shutdown and short-circuit protection of the IC regulator.

A constant current-limiting scheme, as discussed in Section 23.2.2, is implemented by using the transistor Q_2 and the resistor R_2 to protect the external pass transistor Q_1 from excessive current under current-overload or short-circuit conditions. The value of the external current-sensing resistor R_1 determines the value of current at which Q_1 begins to conduct. As long as the current is less than the value set by R_1, the transistor Q_1 is off, and the regulator operates normally as shown in Fig. 23.15. But when the load current I_L starts to increase, the voltage across R_1 also increases. This turns on the external transistor Q_1 and conducts the excess current. The value of R_1 is determined by

$$R_1 = \frac{0.7\,\text{V}}{I_{max}} \tag{23.14}$$

where I_{max} is the maximum current that the voltage regulator can handle internally.

23.5 Switching Regulators

The linear series and shunt regulators have control transistors that are operating in their linear active regions. Regulation is achieved by varying the conduction of the transistors to

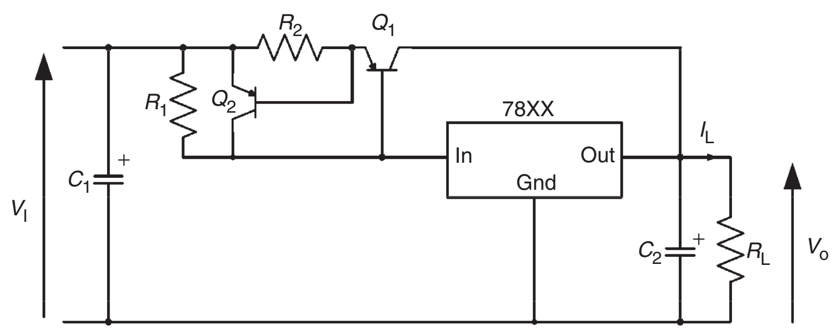


FIGURE 23.19 A 78XX series regulator with an external pass transistor.

maintain the output voltage at a desirable level. The switching regulator is different in that the control transistor operates as a switch, either in cutoff or saturation region. Regulation is achieved by adjusting the on-time of the control transistor. In this mode of operation, the control transistor does not dissipate as much power as that in the linear types. Therefore, switching voltage regulators have a much higher efficiency and can provide greater load currents at low voltage than linear regulators.

Unlike their linear counterparts, switching regulators can be implemented by many different topologies such as forward and flyback. In order to select an appropriate topology for an application, it is necessary to understand the merits and drawbacks of each topology and the requirements of the application. Basically, most topologies can work for various applications. Therefore, we have to determine from the factors such as cost, performances, and application that make one topology more desirable than the others. However, no matter which topology we decide to use, the basic building blocks of an off-the-line switching power supply are the same, as depicted in Fig. 23.1.

In this section, some popular switching regulator topologies, namely flyback, forward, half-bridge, and full-bridge topologies, are presented. Their basic operation is described, and the critical waveforms are shown and explained. The merits, drawbacks, and application areas of each topology are discussed. Finally, the control circuitry and PWM of the regulators will also be discussed.

23.5.1 Single-ended Isolated Flyback Regulators

An isolated flyback regulator consists of four main circuit elements: a power switch, a rectifier diode, a transformer, and a filter capacitor. The power switch, which can be either a power transistor or a MOSFET, is used to control the flow of energy in the circuit. A transformer is placed between the input source and the power switch to provide DC isolation between the input and the output circuits. In addition to being an energy storage element, the transformer also performs a stepping up or down function for the regulator. The rectifier diode and filter capacitor form an energy transfer mechanism to supply energy to maintain the output voltage of the supply. Note that there are two distinct operating modes for flyback regulators: *continuous* and *discontinuous*. However, both modes have an identical circuit. It is only the transformer magnetizing current that determines the operating mode of the regulator. Figure 23.20(a) shows a simplified isolated flyback regulator. The associated steady-state waveforms, resulting from a discontinuous-mode operation, is shown in Fig. 23.20(b). As shown in the figure, the voltage regulation of the regulator is achieved by a control circuit, which controls the conduction period or duty cycle of the switch, to keep the output voltage at a constant level. For clarity, the schematics and operation of the control circuit will be discussed in a separate section.

23.5.1.1 Discontinuous-mode Flyback Regulators

Under steady-state conditions, the operation of the regulator can be explained as follows. When the power switch Q_1 is on, the primary current I_p starts to build up and stores energy in the primary winding. Because of the opposite-polarity arrangement between the input and output windings of the transformer, the rectifier diode D_R is reverse-biased. In this period of time, there is no energy transferred from the input to the load R_L. The output voltage is supported by the load current I_L, which is supplied from the output filter capacitor C_F. When Q_1 is turned off, the polarity of the windings reverses as a result of the fact that I_p cannot change instantaneously. This causes D_R to turn on. Now D_R is conducting, charging the output capacitor C_F and delivering current to R_L. This charging action ends at the point where all the magnetic energy stored in the secondary winding during the first half-cycle is emptied. At this point, D_R will cease to conduct and R_L absorbs energy just from C_F until Q_1 is switched on again.

During the Q_1 on-time, the voltage across the primary winding of the transformer is V_i. The current in the primary winding I_p increases linearly and is given by

$$I_p = \frac{V_i t_{on}}{L_p} \tag{23.15}$$

where L_p is the primary magnetizing inductance. At the end of the on-time, the primary current reaches a value equal to $I_{p(pk)}$ and is given by

$$I_{p(pk)} = \frac{V_i DT}{L_p} \tag{23.16}$$

where D is the duty cycle and T is the switching period. Now when Q_1 turns off, the magnetizing current in the transformer forces the reversal of polarities on the windings. At the instant of turn off, the amplitude of the secondary current $I_{s(pk)}$ is

$$I_{s(pk)} = \left(\frac{N_p}{N_s}\right) I_{p(pk)} \tag{23.17}$$

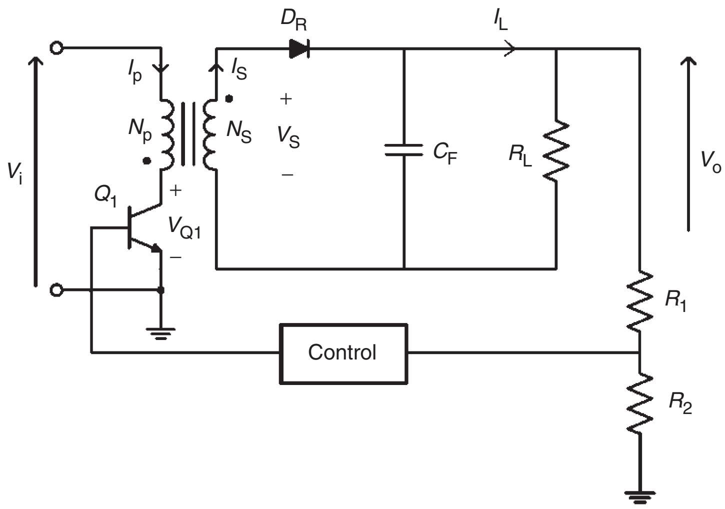
This current decreases linearly at the rate of

$$\frac{dI_s}{dt} = \frac{V_o}{L_s} \tag{23.18}$$

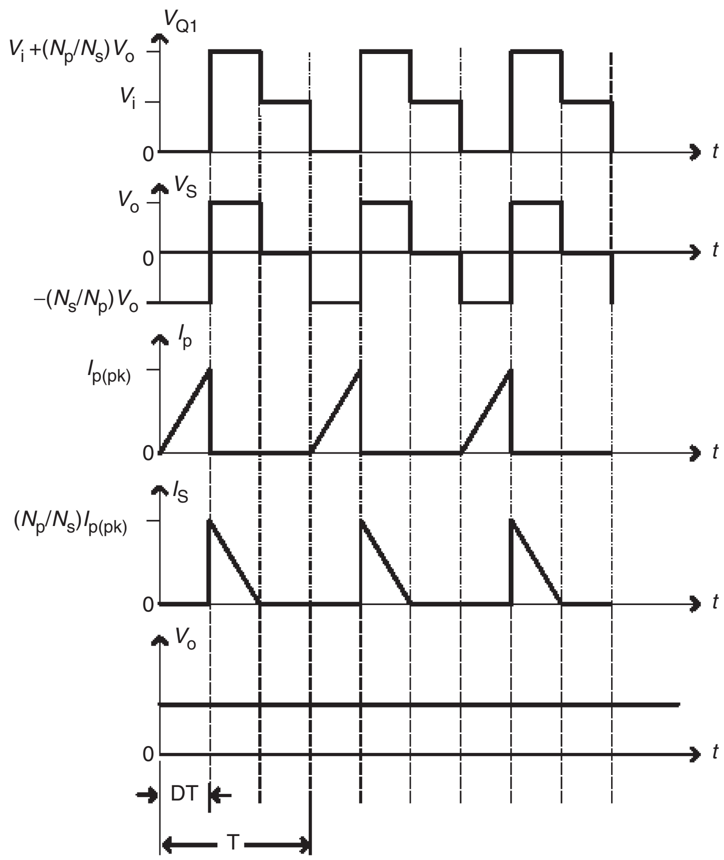
where L_s is the secondary magnetizing inductance.

In the discontinuous-mode operation, $I_{s(pk)}$ will decrease linearly to zero before the start of the next cycle. Since the energy transfer from the source to the output takes place only in the first half cycle, the power drawn from V_i is then

$$P_{in} = \frac{L_p I_p^2}{2T} \tag{23.19}$$



(a)



(b)

FIGURE 23.20 A simplified isolated flyback regulator: (a) circuit and (b) the associated waveforms.

Substituting Eq. (23.15) into Eq. (23.19), we have

$$P_{in} = \frac{(V_i t_{on})^2}{2TL_p} \tag{23.20}$$

The output power P_o may be written as

$$\begin{aligned} P_o &= \eta P_{in} \\ &= \frac{\eta (V_i t_{on})^2}{2TL_p} = \frac{V_o^2}{R_L} \end{aligned} \tag{23.21}$$

where η is the efficiency of the regulator. Then, from Eq. (23.21), the output voltage V_o is related to the input voltage V_i by

$$V_o = V_i D \sqrt{\frac{\eta R_L T}{2L_p}} \tag{23.22}$$

Since the collector voltage V_{Q1} of Q_1 is maximum when V_i is maximum, the maximum collector voltage $V_{Q1(max)}$, as shown in the Fig. 23.20(b), is given by

$$V_{Q1(max)} = V_{i(max)} + \left(\frac{N_p}{N_s}\right) V_o \tag{23.23}$$

The primary peak current $I_{p(pk)}$ can be found in terms of P_o by combining Eq. (23.16) and Eq. (23.21) and then eliminating L_p as

$$\begin{aligned} I_{p(pk)} &= \frac{2V_o^2}{\eta V_i D R_L} \\ &= \frac{2P_o}{\eta V_i D} \end{aligned} \tag{23.24}$$

The maximum collector current $I_{C(\max)}$ of the power switch Q_1 at turn on is

$$\begin{aligned} I_{C(max)} &= I_{p(pk)} \\ &= \frac{2P_o}{\eta V_i D} \end{aligned} \tag{23.25}$$

As can be seen from Eq. (23.21), V_o will be maintained constant by keeping the product $V_i t_{on}$ constant. Since maximum on-time $t_{on(max)}$ occurs at minimum supply voltage $V_{i(min)}$, the maximum allowable duty cycle for the discontinuous-mode can be found from Eq. (23.22) as

$$D_{max} = \frac{V_o}{V_{i(min)}} \sqrt{\frac{2L_p}{\eta R_L T}} \tag{23.26}$$

and V_o at D_{max} is then

$$V_o = V_{i(min)} D_{max} \sqrt{\frac{\eta R_L T}{2L_p}} \tag{23.27}$$

23.5.1.2 Continuous-mode Flyback Regulators

In the continuous-mode operation, the power switch is turned on before all the magnetic energy stored in the secondary winding empties itself. The primary and secondary current waveforms have a characteristic appearance as shown in Fig. 23.21. This mode produces a higher power capability without increasing the peak currents. During the on-time, the primary current I_p rises linearly from its initial value $I_p(0)$ and is given by

$$I_p = I_p(0) + \frac{V_i t_{on}}{L_p} \tag{23.28}$$

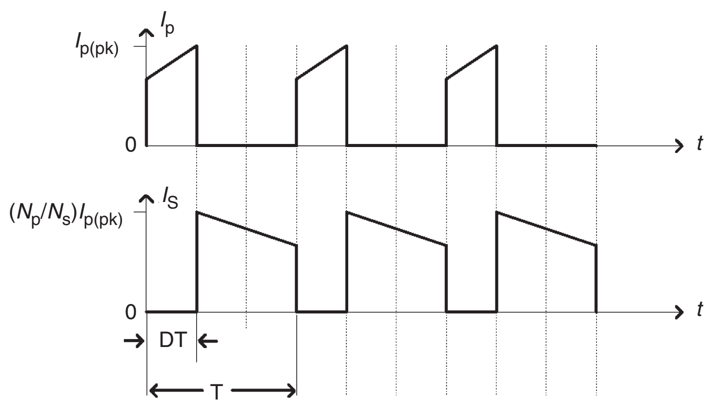


FIGURE 23.21 The primary and secondary winding currents of a flyback regulator operated in the continuous-mode.

At the end of the on-time, the primary current reaches a value equal to $I_{p(pk)}$ and is given by

$$I_{p(pk)} = I_p(0) + \frac{V_i DT}{L_p} \tag{23.29}$$

In general, $I_p(0) \gg V_i DT/L_p$; thus, Eq. (23.29) can be written as

$$I_{p(pk)} \approx I_p(0) \tag{23.30}$$

The secondary current I_s at the instant of turn off is given by

$$\begin{aligned} I_{s(pk)} &= \left(\frac{N_p}{N_s}\right) I_{p(pk)} \\ &= \left(\frac{N_p}{N_s}\right)\left(I_p(0) + \frac{V_i DT}{L_p}\right) \\ &\approx \left(\frac{N_p}{N_s}\right) I_p(0) \end{aligned} \tag{23.31}$$

This current decreases linearly at the rate of

$$\frac{dI_s}{dt} = \frac{V_o}{L_s} \tag{23.32}$$

The output power P_o is equal to V_o times the time-average of the secondary current pulses and is given by

$$\begin{aligned} P_o &= V_o I_s \frac{T - t_{on}}{T} \\ &\approx V_o I_{s(pk)} \frac{T - t_{on}}{T} \end{aligned} \tag{23.33}$$

or

$$I_{s(pk)} = \frac{P_o}{V_o(1 - t_{on}/T)} \tag{23.34}$$

For an efficiency of η, the input power P_{in} is

$$\begin{aligned} P_{in} &= \frac{P_o}{\eta} \\ &= V_i I_p \frac{t_{on}}{T} \\ &\approx V_i I_{p(pk)} \frac{t_{on}}{T} \end{aligned} \tag{23.35}$$

or

$$I_{p(pk)} = \frac{P_o}{\eta V_i\,(t_{on}/T)} \tag{23.36}$$

Combining Eqs. (23.31), (23.34), and (23.36) and solving for V_o, we have

$$V_o = \left(\frac{N_s}{N_p}\right) \frac{\eta V_i D}{1 - D} \tag{23.37}$$

The output voltage at D_{max} is then

$$V_o = \left(\frac{N_s}{N_p}\right) \frac{\eta V_{i(min)} D_{max}}{1 - D_{max}} \tag{23.38}$$

The maximum collector current $I_{C(max)}$ for the continuous-mode is then given by

$$\begin{aligned} I_{C(\max)} &= I_{p(pk)} \\ &= \frac{P_o}{\eta V_i D_{max}} \end{aligned} \tag{23.39}$$

The maximum collector voltage of Q_1 is the same as that in the discontinuous-mode and is given by

$$V_{Q1(max)} = V_{i(max)} + \left(\frac{N_p}{N_s}\right) V_o \tag{23.40}$$

The maximum allowable duty cycle for the continuous-mode can be found from Eqs. (23.38) and is given by

$$D_{max} = \frac{1}{1 + \left(\frac{N_s}{N_p}\right)\frac{\eta V_{i(min)}}{V_o}} \tag{23.41}$$

At the transition from the discontinuous-mode to continuous-mode (or from continuous-mode to discontinuous-mode), the relationships in Eqs. (23.27) and (23.38) must hold. Thus, equating these two equations, we have

$$V_{i(min)} D_{max} \sqrt{\frac{\eta R_L T}{2 L_p}} = \frac{N_s}{N_p} \frac{D_{max}}{1 - D_{max}} \eta V_{i(min)} \tag{23.42}$$

Solving this equation for L_p to give the critical inductance $L_{p(limit)}$, at which the transition occurs, we have

$$\begin{aligned} L_{p(limit)} &= \frac{1}{2\eta} T R_L \left[(1 - D_{max}) \frac{N_p}{N_s}\right]^2 \\ &= \frac{1}{2\eta} T \frac{V_o^2}{P_o} \left[(1 - D_{max}) \frac{N_p}{N_s}\right]^2 \end{aligned} \tag{23.43}$$

Replacing V_o with Eq. (23.38) and solving for $L_{p(limit)}$, we have

$$L_{p(limit)} = \frac{1}{2} \eta T \frac{D_{max}^2 V_{i(min)}^2}{P_o} \tag{23.44}$$

Then, for a given D_{max}, input, and output quantities, the inductance value $L_{p(limit)}$ in Eq. (23.44) determines the mode of operation for the regulator. If $L_p < L_{p(limit)}$, then the circuit is operated in the discontinuous-mode. Otherwise, if $L_P > L_{p(limit)}$, the circuit is operated in the continuous-mode.

In designing flyback regulators, regardless of their operating modes, the power switch must be able to handle the peak collector voltage at turn off and the peak collector currents at turn on as shown in Eqs. (23.23), (23.25), (23.39), and (23.40). The flyback transformer, because of its unidirectional use of the *B–H* curve, has to be designed so that it will not be driven into saturation. To avoid saturation, the transformer needs a relatively large core with an air gap in it.

Although the continuous and discontinuous modes have an identical circuit, their operating properties differ significantly. As opposed to the discontinuous-mode, the continuous-mode can provide higher power capability without increasing the peak current $I_{p(pk)}$. It means that, for the same output power, the peak currents in the discontinuous-mode are much higher than those operated in the continuous-mode. As a result, a higher current rating and, therefore, a more expensive power transistor is needed. Moreover, the higher secondary peak currents in the discontinuous-mode will have a larger transient spike at the instant of turn off. However, despite all these problems, the discontinuous-mode is still much more widely used than its continuous-mode counterpart. There are two main reasons. First, the inherently smaller magnetizing inductance gives the discontinuous-mode a quicker response and a lower transient output voltage spike to sudden changes in load current or input voltage. Second, the continuous-mode has a right-half-plane zero in its transfer function, which makes the feedback control circuit more difficult to design.

The flyback configuration is mostly used in applications with output power below 100 W. It is widely used for high output voltages at relatively low power. The essential attractions of this configuration are its simplicity and low cost. Since no output filter inductor is required for the secondary, there is a significant saving in cost and space, especially for multiple output power supplies. Since there is no output filter inductor, the flyback exhibits high ripple currents in the transformer and at the output. Thus, for higher power applications, the flyback becomes an unsuitable choice. In practice, a small *LC* filter is added after the filter capacitor C_F in order to suppress high-frequency switching noise spikes.

As mentioned previously, the collector voltage of the power transistor must be able to sustain a voltage as defined in Eq. (23.23). In cases where the voltage is too high for the transistor to handle, the double-ended flyback regulator shown in Fig. 23.22 may be used. The regulator uses two transistors that are switched on or off simultaneously. The diodes D_{R1} and D_{R2} are used to restrict the maximum collector voltage to V_i. Therefore, the transistors with a lower voltage rating can be used in the circuit.

23.5.2 Single-ended Isolated Forward Regulators

Although the general appearance of an isolated forward regulator resembles that of its flyback counterpart, their operations are different. The key difference is that the dot on the secondary winding of the transformer is so arranged that the output diode is forward-biased when the voltage across the primary is positive, that is, when the transistor is *on*. Energy is thus not stored in the primary inductance as it was for the flyback. The transformer acts strictly as a transformer. An inductive energy storage element is required at the output for proper and efficient energy transfer.

Unlike the flyback, the forward regulator is very suitable for working in the continuous-mode. In the discontinuous-mode, the forward regulator is more difficult to control because of a

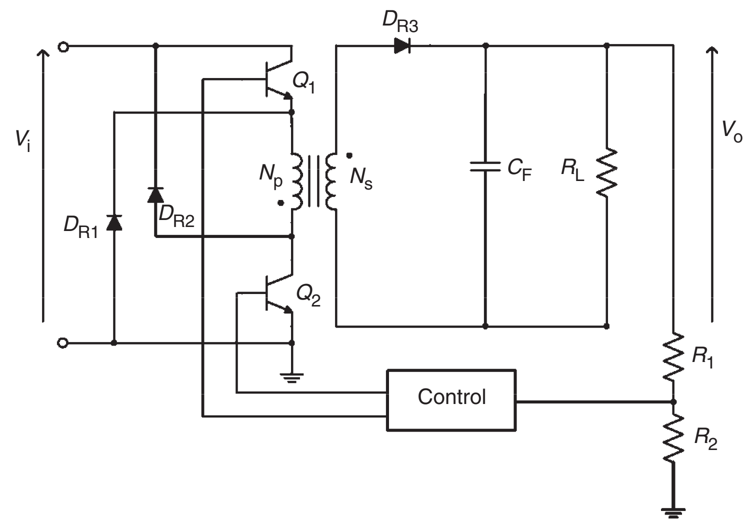


FIGURE 23.22 A double-ended flyback regulator.

double-pole at the output filter. Thus, it is not as much used as the continuous-mode. In view of it, only the continuous-mode will be discussed here.

Figure 23.23 shows a simplified isolated forward regulator and the associated steady-state waveforms for the continuous-mode operation. Again for clarity, the details of the control circuit are omitted from the figure. Under steady-state condition, the operation of the regulator can be explained as follows. When the power switch Q_1 turns on, the primary current I_p starts to build up and stores energy in the primary winding. Because of the same polarity arrangement of the primary and secondary windings, this energy is forward-transferred to the secondary and onto the $L_1 C_F$ filter and the load R_L through the rectifier diode D_{R2}, which is forward-biased. When Q_1 turns off, the polarity of the transformer winding voltage reverses. This causes D_{R2}, to turn off and D_{R1}, and D_{R3}, to turn on. Now D_{R3}, is conducting and delivering energy to R_L through the inductor L_1. During this period, the diode D_{R1}, and the tertiary winding provide a path for the magnetizing current returning to the input.

When the transistor Q_1 is turned on, the voltage across the primary winding is V_i. The secondary winding current is reflected into the primary, and the reaction current I_p, as shown in Fig. 23.24, is given by

$$I_p = \frac{N_s}{N_p} I_s \tag{23.45}$$

The magnetizing current in the primary has a magnitude of I_{mag} and is given by

$$I_{mag} = \frac{V_i t_{on}}{L_p} \tag{23.46}$$

The total primary current I'_p is then

$$\begin{aligned} I'_p &= I_p + I_{mag} \\ &= \frac{N_s}{N_p} I_s + \frac{V_i t_{on}}{L_p} \end{aligned} \tag{23.47}$$

The voltage developed across the secondary winding V_s is

$$V_s = \frac{N_s}{N_p} V_i \tag{23.48}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is $V_s - V_o$. The current in L_1 increases linearly at the rate of

$$I_{L1} = \frac{(V_s - V_o) t_{on}}{L_1} \tag{23.49}$$

At the end of the on-time, the total primary current reaches a peak value equal to $I'_{p(pk)}$ and is given by

$$I'_{p(pk)} = I'_p(0) + \frac{V_i DT}{L_p} \tag{23.50}$$

The output inductor current I_{L1} is

$$I_{L1(pk)} = I_{L1}(0) + \frac{(V_s - V_o) DT}{L_1} \tag{23.51}$$

At the instant of turn on, the amplitude of the secondary current has a value of $I_{s(pk)}$ and is given by

$$\begin{aligned} I_{s(pk)} &= \left(\frac{N_p}{N_s}\right) I'_{p(pk)} \\ &= \left(\frac{N_p}{N_s}\right) \left[I'_p(0) + \frac{V_i DT}{L_p} \right] \end{aligned} \tag{23.52}$$

During the off-time, the current I_{L1} in the output inductor is equal to the current I_{DR3} in the rectifier diode D_{R3} and both decrease linearly at the rate of

$$\begin{aligned} \frac{dI_{L1}}{dt} &= \frac{dI_{DR3}}{dt} \\ &= \frac{V_o}{L_1} \end{aligned} \tag{23.53}$$

The output voltage V_o can be found from the time integral of the secondary winding voltage over a time equal to DT of the switch Q_1. Thus, we have

$$\begin{aligned} V_o &= \frac{1}{T} \int_0^{DT} \frac{N_s}{N_p} V_i \, dt \\ &= \frac{N_s}{N_p} V_i D \end{aligned} \tag{23.54}$$

The maximum collector current $I_{C(\max)}$ at turn on is equal to $I'_{p(pk)}$ and is given by

$$\begin{aligned} I_{C(max)} &= I'_{p(pk)} \\ &= \left(\frac{N_s}{N_p}\right) \left[I'_p(0) + \frac{V_i DT}{L_p} \right] \end{aligned} \tag{23.55}$$

The maximum collector voltage $V_{Q1(max)}$ at turn-off is equal to the maximum input voltage $V_{i(max)}$ plus the maximum voltage $V_{r(max)}$ across the tertiary winding and is given by

$$\begin{aligned} V_{Q1(max)} &= V_{i(max)} + V_{r(max)} \\ &= V_{i(max)} \left(1 + \frac{N_p}{N_r}\right) \end{aligned} \tag{23.56}$$

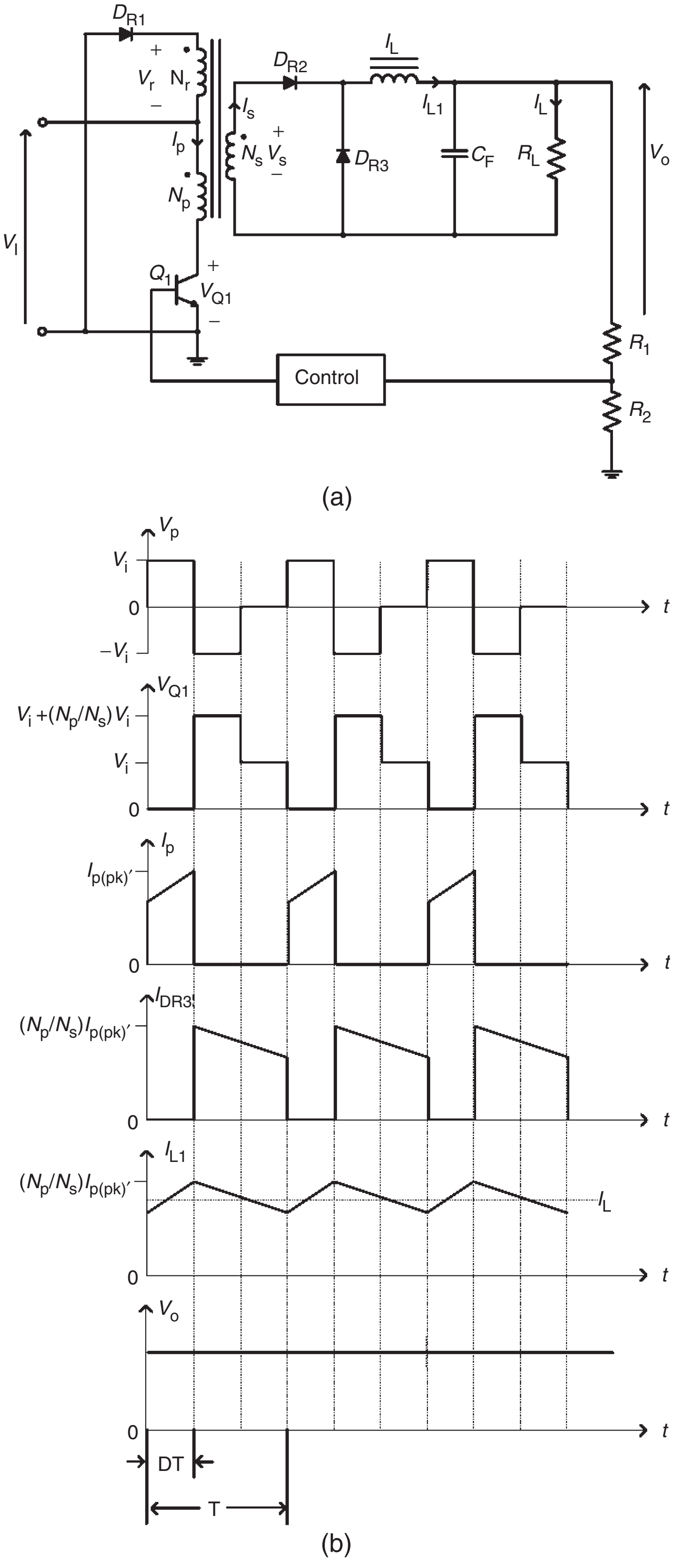


FIGURE 23.23 A simplified isolated forward regulator: (a) circuit and (b) the associated waveforms.

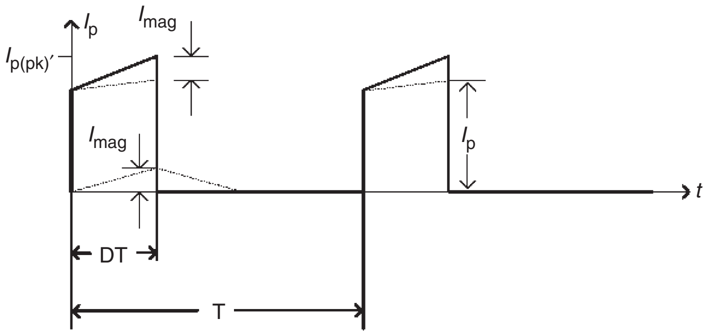


FIGURE 23.24 The current components in the primary winding.

The maximum duty cycle for the forward regulator operated in the continuous-mode can be determined by equating the time integral of the input voltage when Q_1 is on and the clamping voltage V_r when Q_1 is off.

$$\int_0^{DT} V_i\,dt = \int_{DT}^{T} V_r\,dt \tag{23.57}$$

which leads to

$$V_i DT = V_r(1-D)T \tag{23.58}$$

Grouping the D terms in Eq. (23.58) and replacing V_r/V_i with N_r/N_p, we have

$$D_{max} = \frac{1}{1 + N_r/N_p} \tag{23.59}$$

Thus, the maximum duty cycle depends on the turn ratio between the demagnetizing winding and the primary one.

In designing forward regulators, the duty cycle must be kept below the maximum duty cycle D_{max} to avoid saturating the transformer. It should also be noted that the transformer magnetizing current must be reset to zero at the end of each cycle. Failure to do so will drive the transformer into saturation, which can cause damage to the transistor. There are many ways of implementing the resetting function. In the circuit shown in Fig. 23.23(a), a tertiary winding is added to the transformer so that the magnetizing current will return to the input source V_i when the transistor turns off. The primary current always starts at the same value under the steady state condition.

Unlike flyback regulators, forward regulators require a minimum load at the output. Otherwise, excess output voltage will be produced. One commonly used method to avoid this situation is to attach a small load resistance at the output terminals. Of course, with such an arrangement, a certain amount of power will be lost in the resistor.

Because forward regulators do not store energy in their transformers, for the same output power level the transformer can be made smaller than for the flyback type. The output current is reasonably constant owing to the action of the output inductor and the flywheel diode; as a result, the output filter capacitor can be made smaller and its ripple current rating can be much lower than that required for the flybacks.

The forward regulator is widely used with output power below 200 W, though it can be easily constructed with a much higher output power. The limitation comes from the capability of the power transistor to handle the voltage and current stresses if the output power were to increase. In this case, a configuration with more than one transistor can be used to share the burden. Figure 23.25 shows a double-ended forward regulator. Like the double-ended flyback counterpart, the circuit uses two transistors which are switched on and off simultaneously. The diodes are used to restrict the maximum collector voltage to V_i. Therefore, the transistors with low voltage rating can be used in the circuit.

23.5.3 Half-bridge Regulators

The half-bridge regulator is another form of an isolated forward regulator. When the voltage on the power transistor in the single-ended forward regulator becomes too high, the half-bridge regulator is used to reduce the stress on the transistor. In a half-bridge regulator, the voltage stress imposed on the power transistors is subject to only the input voltage and is only half of that in a forward regulator. Thus, the output power of a half-bridge is double to that of a forward regulator for the same semiconductor devices and magnetic core.

Figure 23.26 shows the basic configuration of a half-bridge regulator and the associated steady state waveforms. As seen in Fig. 23.26(a), the half-bridge regulator can be viewed as two back-to-back forward regulators, fed by the same input voltage, each delivering power to the load at each alternate half cycle. The capacitors C_1 and C_2 are placed between the input and ground terminals. As such, the voltage across the primary winding is always half the input voltage. The power switches Q_1 and Q_2 are switched on and off alternatively to produce a square-wave ac at the input of the transformer.

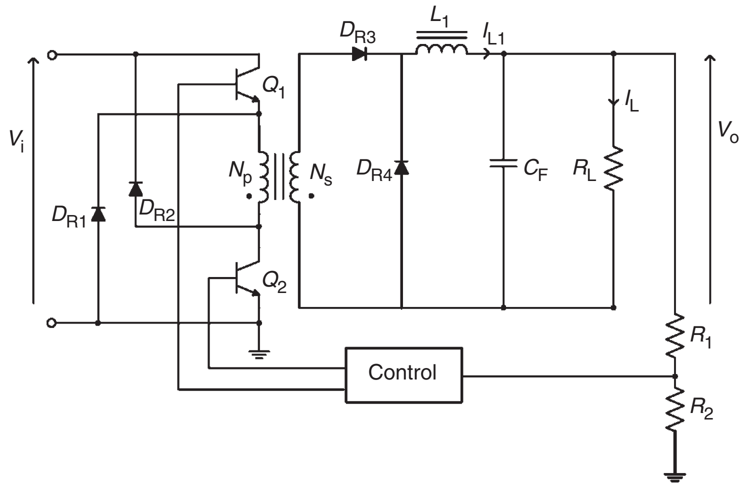


FIGURE 23.25 Double-ended forward regulator.

This square-wave is either stepped down or up by the isolation transformer and then rectified by the diodes D_{R1} and D_{R2}. Subsequently, the rectified voltage is filtered to produce the output voltage V_o.

Under steady state condition, the operation of the regulator can be explained as follows. When Q_1 is on and Q_2 off, D_{R1} conducts and D_{R2} is reverse-biased. The primary voltage V_p is $V_i/2$. The primary current I_p starts to build up and stores energy in the primary winding. This energy is forward-transferred to the secondary and onto the L_1C filter and the load R_L, through the rectifier diode D_{R1}. During the time interval Δ, when both Q_1 and Q_2 are off, D_{R1} and D_{R2} are forced to conduct to carry the magnetizing current that resulted in the interval during which Q_1 is turned on. The inductor current I_{L1} in this interval is equal to the sum of the currents in D_{R1} and D_{R2}. This interval terminates at half of the switching period T, when Q_2 is turned on. When Q_2 is on and Q_1 off, D_{R1} is reverse-biased and D_{R2} conducts. The primary voltage V_p is now $-V_i/2$. The circuit operates in a likewise manner as during the first half cycle.

With Q_1 on, the voltage across the secondary winding is

$$V_{s1} = \frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) \tag{23.60}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is then given by

$$V_{L1} = \frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o \tag{23.61}$$

In this interval, the inductor current I_{L1} increases linearly at the rate of

$$\begin{aligned}\frac{dI_{L1}}{dt} &= \frac{V_{L1}}{L_1}\\ &= \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right]\end{aligned} \tag{23.62}$$

At the end of Q_1 on-time, I_{L1} reaches a value which is given by

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right]DT \tag{23.63}$$

During the interval Δ, I_{L1} is equal to the sum of the rectifier diode currents. Assuming the two secondary windings are identical, I_{L1} is given by

$$I_{L1} = 2I_{DR1} = 2I_{DR2} \tag{23.64}$$

This current decreases linearly at the rate of

$$\frac{dI_{L1}}{dt} = \frac{V_o}{L_1} \tag{23.65}$$

The next half cycle repeats with Q_2 on and for the interval Δ.

The output voltage can be found from the time integral of the inductor voltage over a time equal to T. Thus, we have

$$V_o = 2 \times \frac{1}{T}\left[\int_0^{DT}\left(\frac{N_{s1}}{N_p}\left(\frac{V_i}{2}\right) - V_o\right)dt + \int_{T/2}^{T/2+DT} -V_o\,dt\right] \tag{23.66}$$

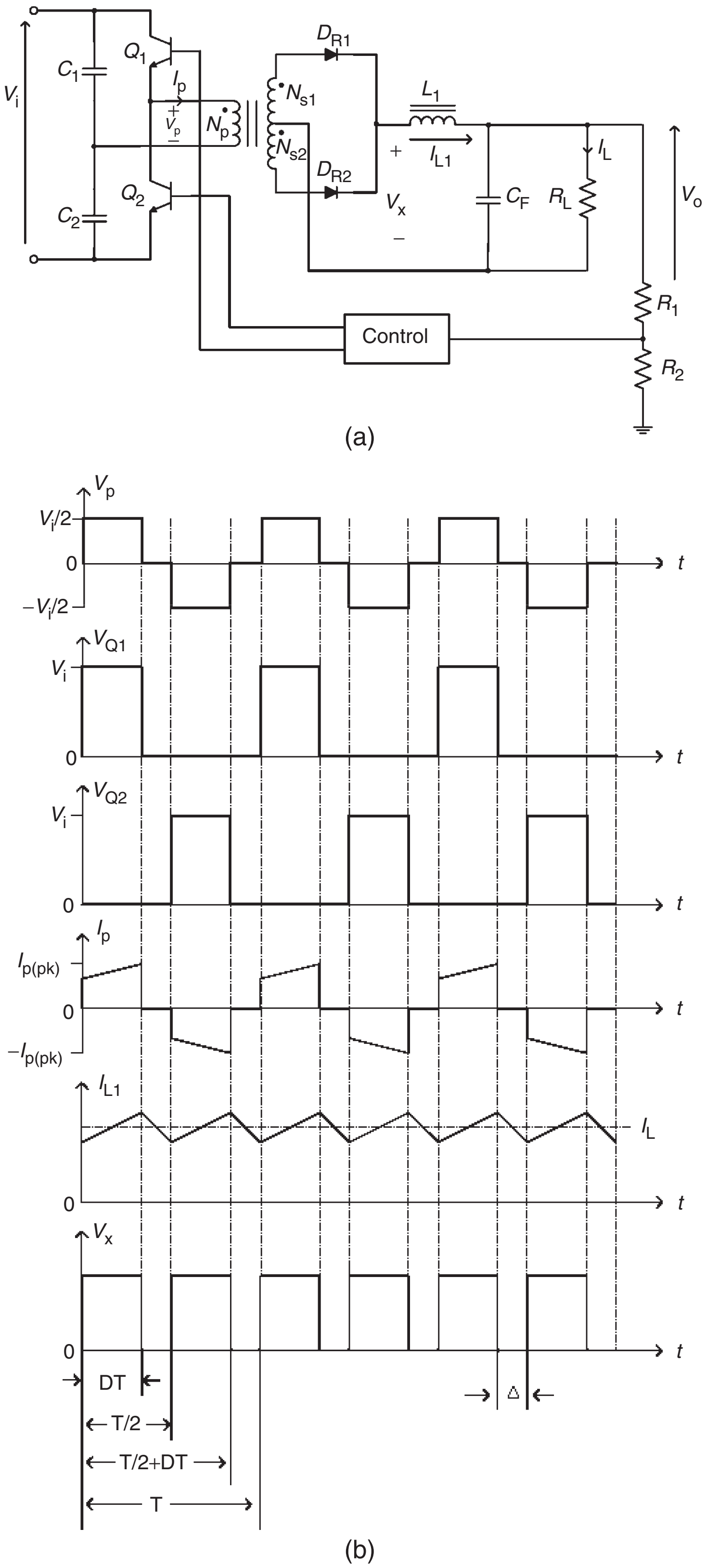


FIGURE 23.26 A simplified half-bridge regulator: (a) circuit and (b) the associated waveforms.

Note that the multiplier of 2 appears in Eq. (23.66) because of the two alternate half cycles. Solving Eq. (23.66) for V_o, we have

$$V_o = \frac{N_{s1}}{N_p} V_i D \tag{23.67}$$

The output power P_o is given by

$$\begin{aligned} P_o &= V_o I_L \\ &= \eta P_{in} \\ &= \eta \frac{V_i I_{p(avg)} D}{2} \end{aligned} \tag{23.68}$$

or

$$I_{p(avg)} = \frac{2P_o}{\eta V_i D} \tag{23.69}$$

where $I_{p(avg)}$ has the value of the primary current at the center of the rising or falling ramp. Assuming the reaction current I'_p reflected from the secondary is much greater than the magnetizing current, then the maximum collector currents for Q_1 and Q_2 are given by

$$\begin{aligned} I_{C(max)} &= I_{p(avg)} \\ &= \frac{2P_o}{\eta V_i D_{max}} \end{aligned} \tag{23.70}$$

As mentioned, the maximum collector voltages for Q_1 and Q_2 at turn off are given by

$$V_{C(max)} = V_{i(max)} \tag{23.71}$$

In designing half-bridge regulators, the maximum duty cycle can never be greater than 50%. When both the transistors are switched on simultaneously, the input voltage is short-circuited to ground. The series capacitors C_1 and C_2 provide a dc bias to balance the volt–second integrals of the two switching intervals. Hence, any mismatch in devices would not easily saturate the core. However, if such a situation arises, a small coupling capacitor can be inserted in series with the primary winding. A dc bias voltage proportional to the volt–second imbalance is developed across the coupling capacitor. This balances the volt–second integrals of the two switching intervals.

One problem in using half-bridge regulators is related to the design of the drivers for the power switches. Specifically, the emitter of Q_1 is not at ground level, but is at a high ac level. The driver must therefore be referenced to this ac level. Typically, transformer-coupled drivers are used to drive both switches, thus solving the grounding problem and allowing the controller to be isolated from the drivers.

The half-bridge regulator is widely used for medium-power applications. Because of its core-balancing feature, the half-bridge becomes the predominant choice for output power ranging from 200 to 400 W. Since the half-bridge is more complex, for application below 200 W, the flyback or forward regulator is considered to be a better choice and more cost-effective. Above 400 W, the primary and switch currents of the half-bridge become very high. Thus, it becomes unsuitable.

23.5.4 Full-bridge Regulators

The full-bridge regulator is yet another form of isolated forward regulator. Its performance is improved over that of the half-bridge regulator because of the reduced peak collector current. The two series capacitors that appeared in half-bridge circuits are now replaced by another pair of transistors of the same type. In each switching interval, two of the switches are turned on and off simultaneously such that the full input voltage appears at the primary winding. The primary and the switch currents are only half that of the half-bridge for the same power level. Thus, the maximum output power of this topology is twice that of the half-bridge.

Figure 23.27 shows the basic configuration of a full-bridge regulator and the associated steady-state waveforms. Four power switches are required in the circuit. The power switches Q_1 and Q_4 turn on and off simultaneously in one of the half cycles. Q_2 and Q_3 also turn on and off simultaneously in the other half cycle, but with opposite phase as Q_1 and Q_4. This produces a square-wave ac with a value of $\pm V_i$ at the primary winding of the transformer. Like the half-bridge, this voltage is stepped down, rectified, and then filtered to produce a dc output voltage. The capacitor C_1 is used to balance the volt-second integrals of the two switching intervals and prevent the transformer from being driven into saturation.

Under steady-state conditions, the operation of the full-bridge is similar to that of the half-bridge. When Q_1 and Q_4 turn on, the voltage across the secondary winding is

$$V_{s1} = \frac{N_{s1}}{N_p} V_i \tag{23.72}$$

Neglecting diode voltage drops and losses, the voltage across the output inductor is then given by

$$V_{L1} = \frac{N_{s1}}{N_p} V_i - V_o \tag{23.73}$$

In this interval, the inductor current I_{L1} increases linearly at the rate of

$$\begin{aligned} \frac{dI_{L1}}{dt} &= \frac{V_{L1}}{L_1} \\ &= \frac{1}{L_1}\left[\frac{N_{s1}}{N_p} V_i - V_o\right] \end{aligned} \tag{23.74}$$

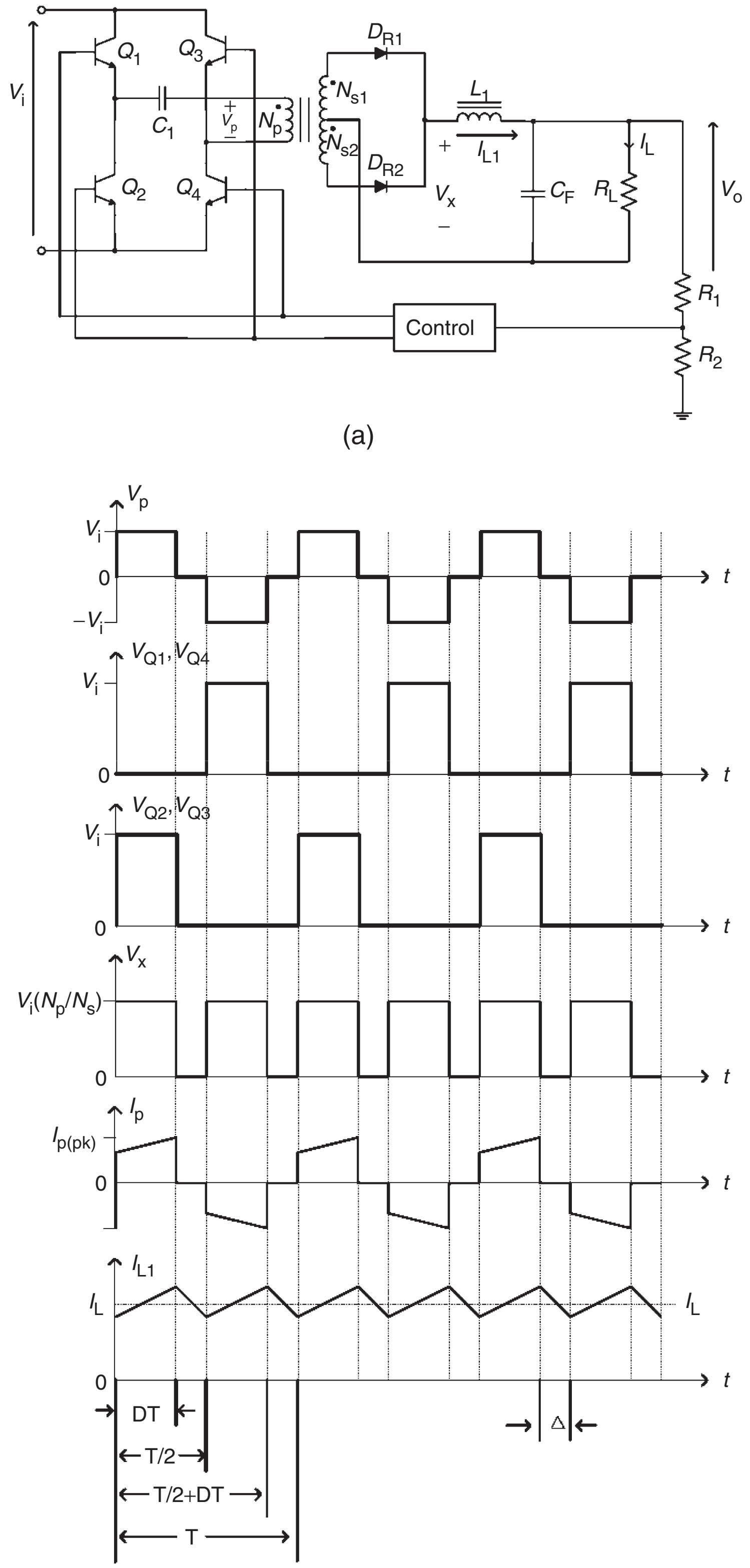


FIGURE 23.27 A simplified full-bridge regulator: (a) circuit and (b) the associated waveforms.

At the end of Q_1 and Q_4 on-time, I_{L1} reaches a value which is given by

$$I_{L1(pk)} = I_{L1}(0) + \frac{1}{L_1}\left[\frac{N_{s1}}{N_p}V_i - V_o\right]DT \tag{23.75}$$

During the interval Δ, I_{L1} decreases linearly at the rate of

$$\frac{dI_{L1}}{dt} = \frac{V_o}{L_1} \tag{23.76}$$

The next half cycle repeats with Q_2 and Q_3 on and the circuit operates in a similar manner as in the first half cycle.

Again, as in the half-bridge, the output voltage can be found from the time integral of the inductor voltage over a time equal to T. Thus, we have

$$V_o = 2 \times \frac{1}{T}\left[\int_0^{DT}\left(\frac{N_{s1}}{N_p}V_i - V_o\right)dt + \int_{T/2}^{T/2+DT} -V_o\,dt\right] \tag{23.77}$$

Solving Eq. (23.77) for V_o, we have

$$V_o = \frac{N_{s1}}{N_p}2V_iD \tag{23.78}$$

The output power P_o is given by

$$\begin{aligned} P_o &= \eta P_{in} \\ &= \eta V_i I_{p(avg)} D \end{aligned} \tag{23.79}$$

or

$$I_{p(avg)} = \frac{P_o}{\eta V_i D} \tag{23.80}$$

where $I_{p(avg)}$ has the same definition as in the half-bridge case.

Comparing Eq. (23.80) with Eq. (23.69), we see that the output power of a full-bridge is twice that of a half-bridge with same input voltage and current. The maximum collector currents for Q_1, Q_2, Q_3, and Q_4 are given by

$$\begin{aligned} I_{C(max)} &= I_{p(avg)} \\ &= \frac{P_o}{\eta V_i D_{max}} \end{aligned} \tag{23.81}$$

Comparing Eq. (23.81) with Eq. (23.70), for the same output power, the maximum collector current is only half that of the half-bridge.

As mentioned, the maximum collector voltage for Q_1 and Q_2 at turn off is given by

$$V_{C(max)} = V_{i(max)} \tag{23.82}$$

The design of the full-bridge is similar to that of the half-bridge. The only difference is the use of four power switches instead of two in the full-bridge. Therefore, additional drivers are required by adding two more secondary windings in the pulse transformer of the driving circuit.

For high power applications ranging from several hundred to thousand kilowatts, the full-bridge regulator is an inevitable choice. It has the most efficient use of magnetic core and semiconductor switches. The full-bridge is complex and therefore expensive to build, and is only justified for high-power applications, typically over 500 W.

23.5.5 Control Circuits and Pulse-width Modulation

In previous subsections, we presented several popular voltage regulators that may be used in a switching mode power supply. This section discusses the control circuits that regulate the output voltage of a switching regulator by constantly adjusting the conduction period t_{on} or duty cycle d of the power switch. Such adjustment is called *pulse-width modulation* (PWM).

The duty cycle is defined as the fraction of the period during which the switch is on, i.e.

$$\begin{aligned} d &= \frac{t_{on}}{T} \\ &= \frac{t_{on}}{t_{on} + t_{off}} \end{aligned} \tag{23.83}$$

where T is the switching period, i.e. $t_{off} = T - t_{on}$. By adjusting either t_{on} or t_{off}, or both, d can be modulated. Thus, PWM controlled regulators can operate at variable frequency as well as fixed frequency.

Among all types of PWM controllers, the fixed frequency controller is by far the most popular choice. There are two main reasons for their popularity. First, low-cost fixed-frequency PWM IC controllers have been developed by various solid-state device manufacturers, and most of these IC controllers have all the features that are needed to build a PWM switching power supply using a minimum number of components. Second, because of their fixed-frequency nature, fixed-frequency controllers do not have the problem of unpredictable noise spectrum associated with variable frequency controllers. This makes EMI control much easier.

There are two types of fixed-frequency PWM controllers, namely, *the voltage-mode controller* and the *current-mode controller*. In its simplified form, a voltage-mode controller consists of four main functional components: an adjustable clock for setting the switching frequency, an output voltage error amplifier for detecting deviation of the output from the nominal value, a ramp generator for providing a sawtooth signal that is synchronized to the clock, and a comparator that compares the output error signal with the sawtooth signal. The output of the comparator is the signal that drives the controlled switch. Figure 23.28 shows a simplified PWM voltage-mode controlled forward regulator operating at fixed frequency and its associated driving signal waveform. As shown, the duration of the on-time t_{on} is determined by the time between the reset of the ramp generator and the intersection of the error voltage with the positive-going ramp signal.

The error voltage v_e is given by

$$v_e = \left(1 + \frac{Z_2}{Z_1}\right) V_{REF} - \frac{Z_2}{Z_1} v_2 \tag{23.84}$$

From Eq. (23.84), the small-signal term can be separated from the dc operating point by

$$\Delta v_e = -\frac{Z_2}{Z_1} \Delta v_2 \tag{23.85}$$

The dc operating point is given by

$$V_e = \left(1 + \frac{Z_2}{Z_1}\right) V_{REF} - \frac{Z_2}{Z_1} V_2 \tag{23.86}$$

Inspecting the waveform of the sawtooth and the error voltage shows that the duty cycle is related to the error voltage by

$$d = \frac{v_e}{V_p} \tag{23.87}$$

where V_p is the peak voltage of the sawtooth.

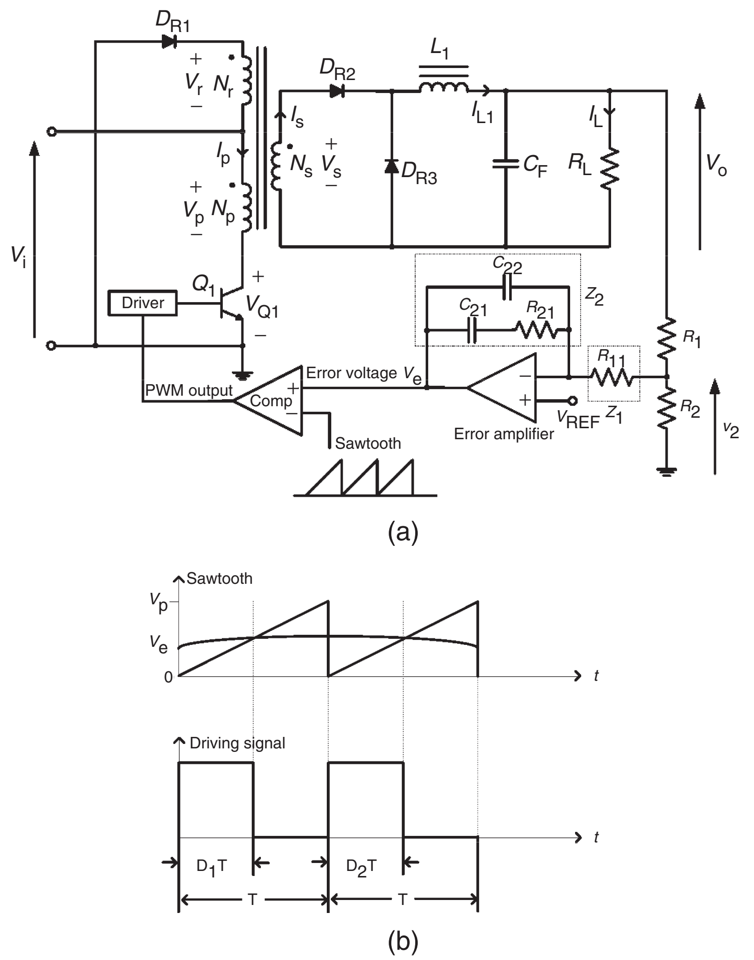


FIGURE 23.28 A simplified voltage-mode controlled forward regulator: (a) circuit and (b) the associated driving signal waveform.

Hence, the small-signal duty cycle is related to the small-signal error voltage by

$$\Delta d = \frac{\Delta v_e}{V_p} \tag{23.88}$$

The operation of the fixed-frequency voltage-mode controller can be explained as follows. When the output is lower than the nominal dc value, a high error voltage is produced. This means that Δv_e is positive. Hence, Δd is positive. The duty cycle is increased to cause a subsequent increase in output voltage. The feedback dynamics (stability and transient response) is determined by the operational amplifier circuit that consists of Z_1 and Z_2. Some of the popular voltage-mode control ICs are SG1524/25/26/27, TL494/5, and MC34060/63.

The current-mode control makes use of the current information in a regulator to achieve output voltage regulation. In its simplest form, current-mode control consists of an inner loop that samples the inductance current value and turns the switches off as soon as the current reaches a certain value set by the outer voltage loop. In this way, the current-mode control achieves faster response than the voltage mode. There are two types of fixed-frequency PWM current-mode control, namely, the *peak current-mode control* and the *average current-mode control.*

In the peak current-mode control, no sawtooth generator is needed. In fact, the inductance current waveform is itself a sawtooth. The voltage analog of the current may be provided by a small resistance, or by a current transformer. Also, in practice, the switch current is used since only the positive-going portion of the inductance current waveform is required. Figure 23.29 shows a peak current-mode controlled flyback regulator.

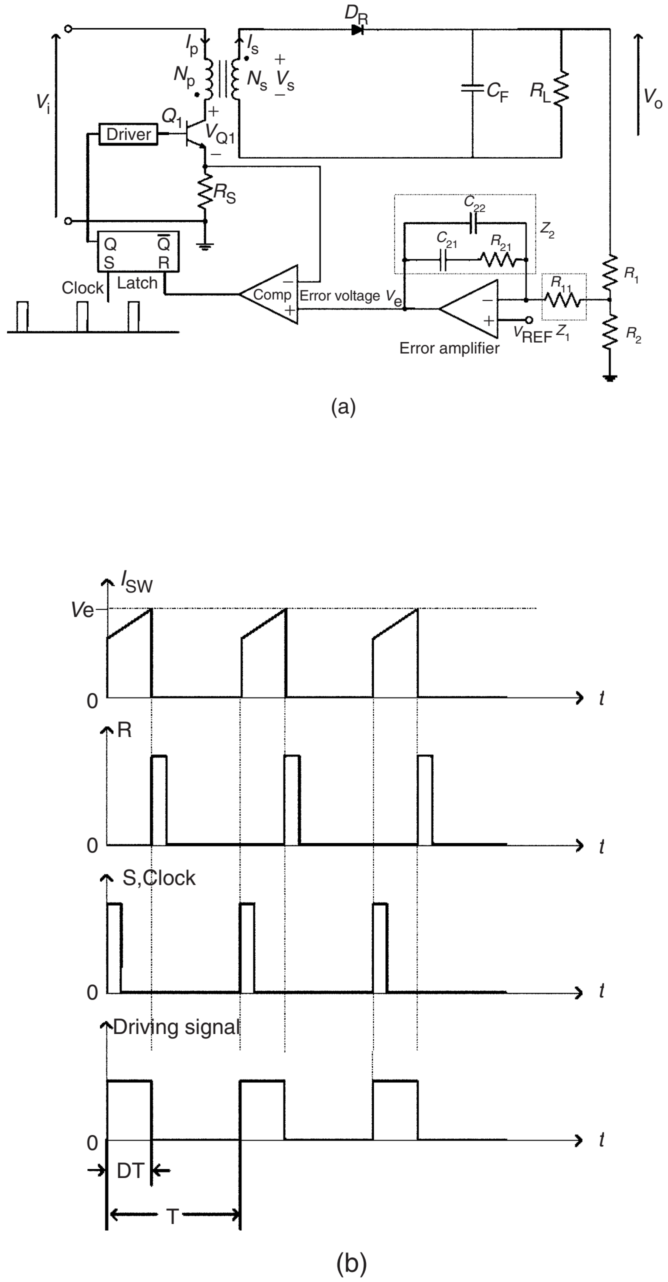


FIGURE 23.29 A simplified peak current-mode controlled flyback regulator: (a) circuit and (b) the associated waveforms.

In Fig. 23.29, the regulator operates at fixed frequency. Turn on is synchronized with the clock pulse, and turn off is determined by the instant at which the input current equals the error voltage V_e.

Because of its inherent peak current-limiting capability, the peak current-mode control can enhance reliability of power switches. The dynamic performance is improved because of the use of the additional current information. One main disadvantage of the peak current-mode control is that it is extremely susceptible to noise, since the current ramp is usually small compared to the reference signal. A second disadvantage is its inherent instability property at duty cycle exceeding 50%, which results in sub-harmonic oscillation. Typically, a compensating ramp is required at the comparator input to eliminate this instability. The third disadvantage is that it has a non-ideal loop response because of the use of the peak, instead of the average current sensing.

Figure 23.30 shows an average current-mode controlled flyback regulator. In the circuit, a PWM modulator (instead of a clocked SR latch in the peak current-mode control) is employed to compare the current error to an externally generated sawtooth signal to formulate the desired control signal. The main advantages of this method over the peak current-control are that it has excellent noise immunity property; it is stable at duty cycle exceeding 50%; and it provides good tracking of average current. However, since there are three compensation networks (Z_1, Z_2, and Z_3), the analysis

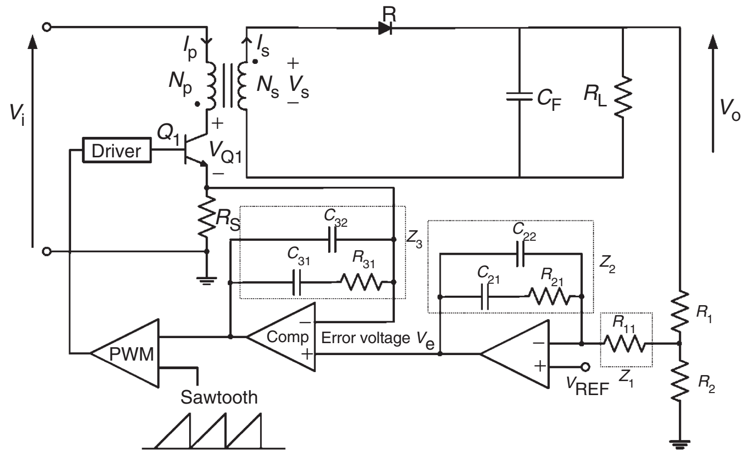


FIGURE 23.30 A simplified average current-mode controlled flyback regulator: (a) circuit and (b) the associated waveforms.

and optimal design of these networks are non-trivial. This is a major obstacle for adopting the average current mode control.

It should be noted that current-mode control is particularly effective for the flyback and boost-type regulators that have an inherent right-half-plane zero. Current-mode control effectively reduces the system to first-order by forcing the inductor current to be related to the output voltage, thus achieving faster response. In the case of the buck-type regulator, current-mode control presents no significant advantage because the current information can be derived from the output voltage, and hence faster response can still be achieved with a proper feedback network. Some of the popular current-mode control ICs are UC3840/2, UC3825, MC34129, and MC34065.

Further Reading

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