9

Static Induction Devices

Bogdan M. Wilamowski, Ph.D.
Alabama Microelectronics Science and Technology Center, Auburn University, Alabama, USA

Summary

Several devices from the static induction family such as: static induction transistor (SIT), static induction diode (SID), static induction thyristor, lateral punch-through transistor (LPTT), static induction transistor logic (SITL), static induction MOS transistor (SIMOS), and space charge limiting load (SCLL) are described. The theory of operation of static induction devices is given for both a current controlled by a potential barrier and a current controlled by space charge. The new concept of a punch-through emitter (PTE), which operates with majority carrier transport, is presented.

9.1 Introduction

Static induction devices were invented in 1975 by J. Nishizawa [1] and for many years Japan was the only country where static induction family devices were successfully fabricated. Static induction transistor can be considered as a short channel junction field effect transistor (JFET) device operating in pre-punch-through region. The number of devices in this family is growing with time. The SIT can operate with the power over 100 kW at 100 kHz; above 150 W at 3 GHz. [2]. These devices may operate upto THz frequencies [3, 4]. Static induction transistor logic had 100 times smaller switching energy than its I^2L competitor [5, 6]. Static induction thyristor has many advantages over the traditional silicon controlled rectifier (SCR), and SID exhibits high switching speed, large reverse voltage, and low forward voltage drops [7].

9.2 Theory of Static Induction Devices

The cross section of the SIT is shown in Fig. 9.1, while its characteristics are shown in Fig. 9.2. An induced electrostatically potential barrier controls the current in static induction devices. The derivations of formulas will be done for an *n*-channel device, but the obtained results, with a little modification can also be applied to *p*-channel devices. For a small electrical field existing in the vicinity of the potential barrier, the drift and diffusion current can be approximated by

$$J_n = -qn(x)\mu_n \frac{d\varphi(x)}{dx} + qD_n \frac{dn(x)}{dx} \tag{9.1}$$

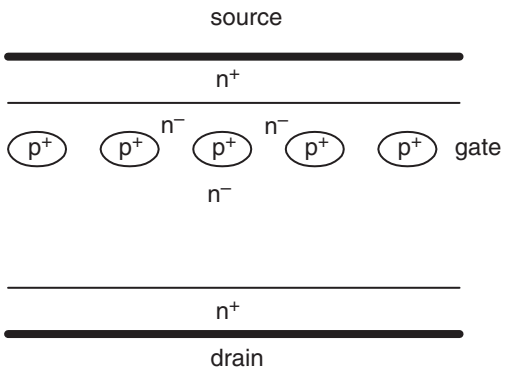

FIGURE 9.1 Cross section of the static induction transistor.

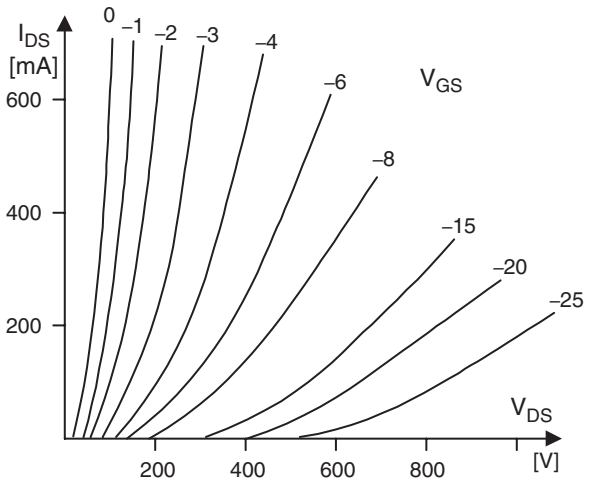

FIGURE 9.2 Characteristics of the early SIT design [1].

where $D_n = \mu_n V_T$ and $V_T = kT/q$. By multiplying both sides of the equation by $\exp\left(-\varphi(x)/V_T\right)$ and rearranging

$$J_n \exp\left(-\frac{\varphi(x)}{V_T}\right) = qD_n \frac{d}{dx}\left[n(x)\exp\left(-\frac{\varphi(x)}{V_T}\right)\right] \tag{9.2}$$

Integrating from x_1 to x_2 one can obtain

$$J_n = qD_n \frac{n(x_2)\exp\left(-\varphi(x_2)/V_T\right) - n(x_1)\exp\left(-\varphi(x_1)/V_T\right)}{\int_{x_1}^{x_2} \exp\left(-\varphi(x)/V_T\right) dx} \tag{9.3}$$

With the following boundary conditions

$$\begin{aligned} \varphi(x_1) &= 0; \qquad n(x_1) = N_S \\ \varphi(x_2) &= V_D; \quad n(x_2) = N_D \end{aligned} \tag{9.4}$$

Eq. (9.3) reduces to

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp\left(-\varphi(x)/V_T\right) dx} \tag{9.5}$$

Note that the above equations derived for SIT can also be used to find current in any devices controlled by a potential barrier, such as a bipolar transistor, MOS transistor operation in subthreshold mode, or in a Schottky diode.

9.3 Characteristics of Static Induction Transistor

Samples of the potential distribution in the SI devices are shown in Fig. 9.3 [7]. The vicinity of the potential barrier can be approximated using parabolic formulas (Fig. 9.4) along and across the channel [8, 9].

$$\varphi(x) = \Phi\left[1 - \left(2\frac{x}{L} - 1\right)^2\right] \tag{9.6}$$

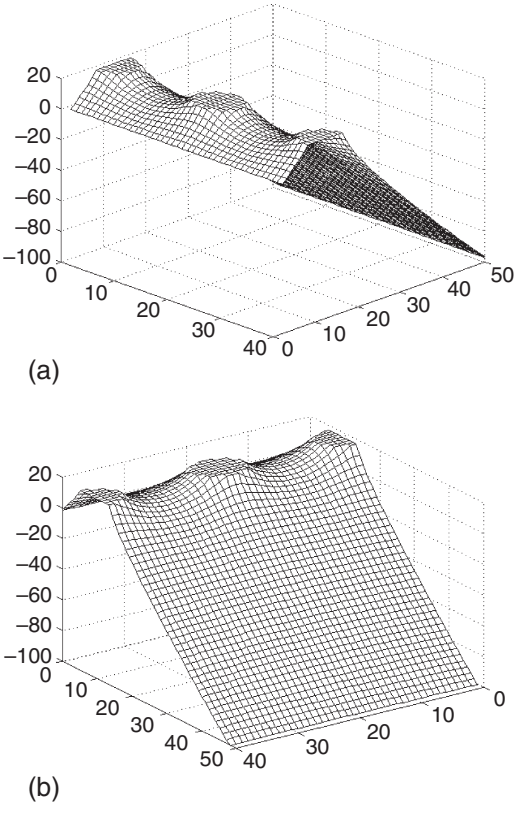

FIGURE 9.3 Potential distribution in SIT: (a) view from the source side and (b) view from the drain side.

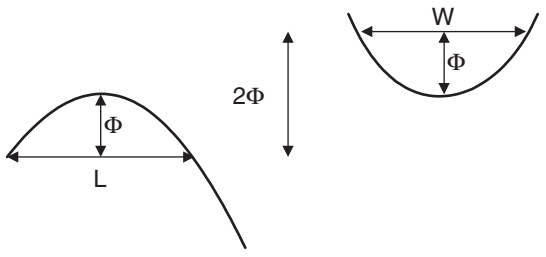

FIGURE 9.4 Potential distribution in the vicinity of the barrier approximated by parabolic shapes.

$$\varphi(y) = \Phi\left[1 - \left(2\frac{y}{W} - 1\right)^2\right] \tag{9.7}$$

Integrating Eq. (9.5) first along the channel and then across the channel, yields a very simple formula for drain currents in *n*-channel SITs

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(\frac{\Phi}{V_T}\right) \tag{9.8}$$

where Φ is the potential barrier height in reference to the source potential, N_S is the electron concentration at the source, W/L ratio describes the shape of the potential saddle in vicinity of the barrier, and Z is the length of the source strip.

Since barrier height Φ can be a linear function of gate and drain voltages; therefore,

$$I_D = qD_pN_SZ\frac{W}{L}\exp\left(a\left(V_{GS} + bV_{DS} + \Phi_0\right)/V_T\right) \tag{9.9}$$

The above equation describes characteristics of SIT for small current range. For large current levels, the device current is controlled by the space charge of moving carriers. In the one-dimensional case, the potential distribution is described by the Poisson equation:

$$\frac{d^2\varphi}{dx_2} = -\frac{\rho(x)}{\varepsilon_{Si}\varepsilon_0} = \frac{I_{DS}}{Av(x)} \tag{9.10}$$

where A is the effective device cross section and $v(x)$ is carrier velocity. For a small electrical field $v(x) = \mu E(x)$ and the solution of Eq. (9.10) is

$$I_{DS} = \frac{9}{8}V_{DS}^2\mu\varepsilon_{Si}\varepsilon_0\frac{A}{L^3} \tag{9.11}$$

and for a large electrical field $v(x) = \text{const}$ and Eq. (9.10) results in:

$$I_{DS} = 2V_{DS}v_{sat}\varepsilon_{Si}\varepsilon_0\frac{A}{L^2} \tag{9.12}$$

where L is the channel length and $v_{sat} \approx 10^{11}\,\mu$m/s is the carrier saturation velocity. In practical devices, the current–voltage relationship is described by an exponential relationship, Eq. (9.9), for small currents, a quadratic relationship, Eq. (9.11), and finally for large voltages by an almost linear relationship, Eq. (9.12). Static induction transistor characteristics drawn in linear and logarithmic scales are shown in Figs. 9.5 and 9.6, respectively.

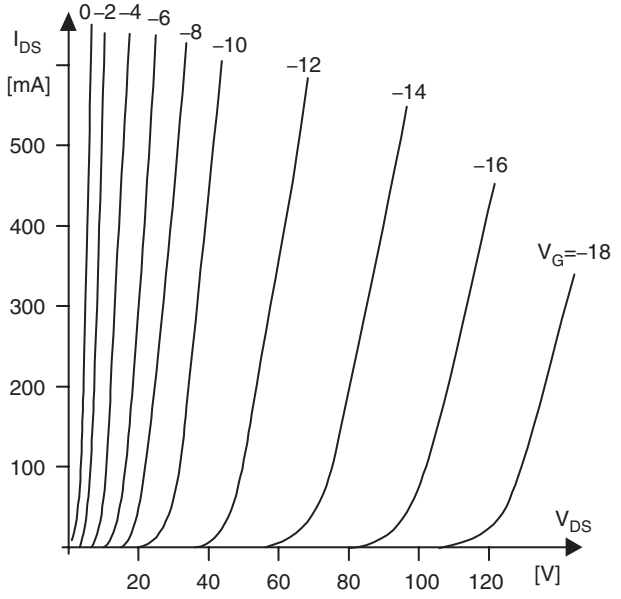

FIGURE 9.5 Characteristics of the SIT drawn in a linear scale.

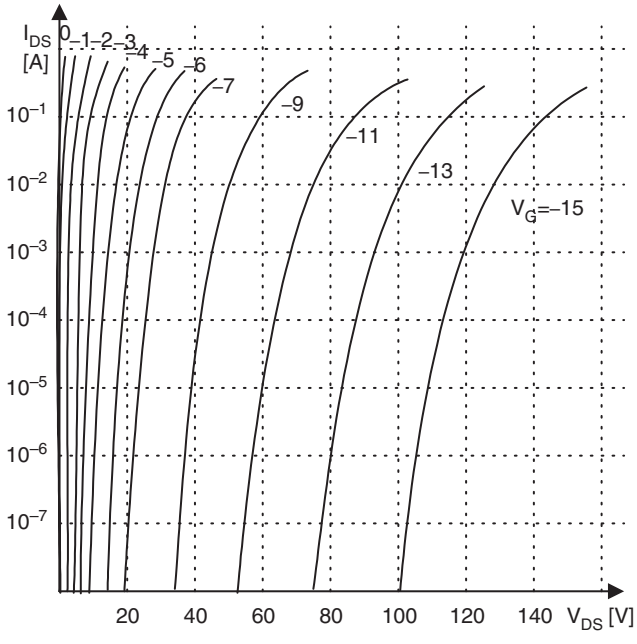

FIGURE 9.6 Characteristics of the SIT drawn in a logarithmic scale.

9.4 Bipolar Mode Operation of SI devices (BSIT)

The bipolar mode of operation of SIT was first reported in 1976 by Nishizawa and Wilamowski [5, 6]. Several complex theories for the bipolar mode of operation were developed [10–14], but actually the simple formula given by Eq. (9.5) works well not only for the typical mode of the SIT operation, but also for the bipolar mode of the SIT operation. Furthermore, the same formula works very well for the classical bipolar transistors. Typical characteristics of the SI transistor operating in normal and in bipolar modes are shown in Figs. 9.7 and 9.8.

A potential barrier controls the current in the SIT and it is given by

$$J_n = \frac{qD_n N_S}{\int_{x_1}^{x_2} \exp\left(-\frac{\varphi(x)}{V_T}\right) dx} \tag{9.13}$$

where $\varphi(x)$ is the profile of the potential barrier along the channel.

For example, in the case of *npn* bipolar transistors, the potential distribution across the base in reference to emitter potential at the reference impurity level $N_E = N_S$ is described by:

$$\varphi(x) = V_T \ln\left(\frac{N_B(x)N_S}{n_i^2}\right) \exp\left(-\frac{V_{BE}}{V_T}\right) \tag{9.14}$$

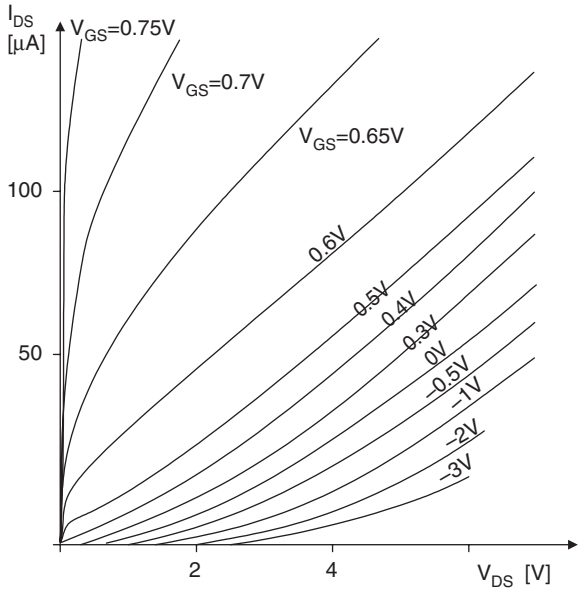

FIGURE 9.7 Small size SIT transistor characteristics, operating in both the normal and bipolar modes, $I_D = f(V_{DS})$ with V_{GS} as a parameter.

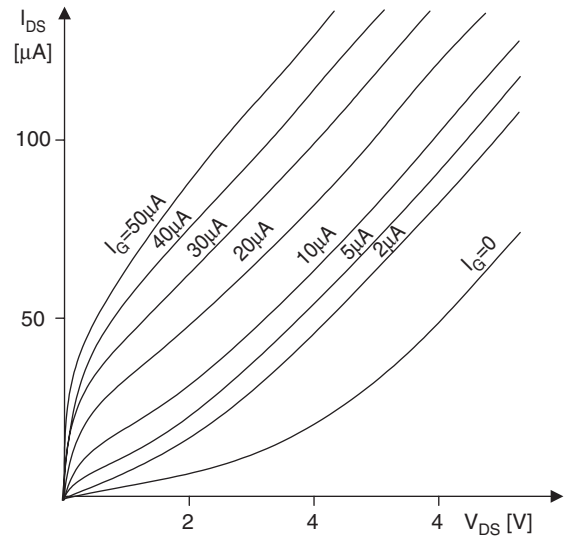

FIGURE 9.8 Small size SIT transistor characteristics, operating in both the normal and bipolar modes, $I_D = f(V_{DS})$ with I_G as a parameter.

After inserting Eq. (9.14) into Eq. (9.13), one can obtain the well-known equation for electron current injected into the base

$$J_n = \frac{qD_n n_i^2}{\int_{x_1}^{x_2} N_B(x)dx} \exp\left(\frac{V_{BE}}{V_T}\right) \tag{9.15}$$

If Eq. (9.13) is valid for SIT and BJT, then one may assume that it is also valid for the bipolar mode of operation of the SIT transistor. This is a well-known equation for the collector current in the bipolar transistor, but this time it was derived using the concept of the current flow through the potential barrier.

9.5 Emitters for Static Induction Devices

One of the disadvantages of the SIT is the relatively flat shape of the potential barrier (Fig. 9.9a). This leads to slow, diffusion-based transport of carriers in the vicinity of the potential barrier. The carrier transit time can be estimated using the formula:

$$t_{transit} = \frac{l_{eff}^2}{D} \tag{9.16}$$

where l_{eff} is the effective length of the channel and $D = \mu V_T$ is the diffusion constant. In the case of a traditional SIT transistor, this channel length is about 2 μm while in the case of SIT transistors with sharper barriers (Fig. 9.9b) the channel length is reduced to about 0.2 μm. The corresponding transient times are 2 ns and 20 ps, respectively.

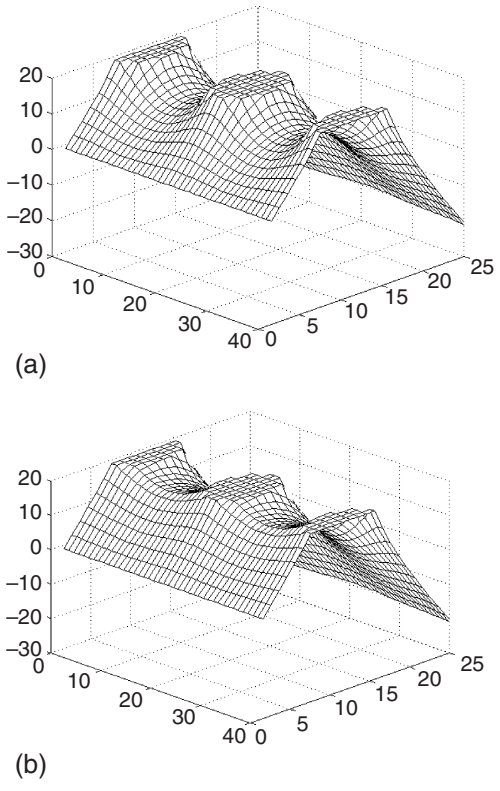

FIGURE 9.9 Potential distributions in SIT: (a) traditional and (b) with sharp potential barrier.

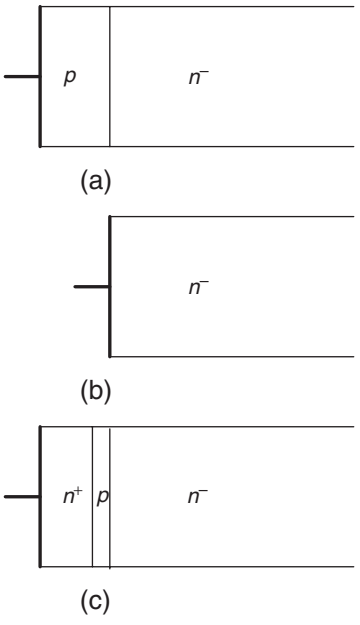

FIGURE 9.10 Various structures of emitters: (a) *p–n* junction including heterostructure with SiGe materials; (b) Schottky junction; and (c) punch-through emitter (in normal operation condition the *p* region is depleted from carriers).

Potential distributions shown in Fig. 9.3 are valid for SIT with an emitter made of a traditional *p–n* junction. A much narrower potential barrier can be obtained when other type of emitter is being used. There are two well-known emitters: (1) *p–n* junction (Fig. 9.10a) and (2) Schottky junction (Fig. 9.10b). For silicon devices, *p–n* junctions have a forward voltage drop of 0.7–0.8 V, while Schottky emitters have 0.2–0.3 V only. Since the Schottky diode is a majority carrier device, the carrier storage effect is negligible.

Another interesting emitter structure is shown in Fig. 9.10c. This emitter has all the advantages of the Schottky diode, with majority carrier injection, even though it is fabricated out of *p–n* junctions.

The concept of static induction devices can be used independently of the type of emitter shown in Fig. 9.10. With Schottky type and punch-through type emitters, the potential barrier is much narrower and this results in faster response time and larger current gain in the bipolar mode of operation.

9.6 Static Induction Diode

The bipolar mode of operation of SIT can also be used to obtain diodes with low forward voltage drop and negligible carrier storage effect [10, 11, 13, 15]. A static induction diode (SID) can be obtained by shorting a gate to the emitter of the SIT [16, 17]. Such diode has all the advantages of the SIT such as thermal stability and short switching time. The cross section of such diode is shown in Fig. 9.11.

The quality of the SID can be further improved with more sophisticated emitters (Figs. 9.10b and c). The SI diode with Schottky emitter was described by Wilamowski in 1983 [18] (Fig. 9.12). A similar structure was later published by Baliga [19].

9.7 Lateral Punch-through Transistor

Fabrications of SI transistors usually require very sophisticated technology. It is much simpler to fabricate a lateral punch-through transistor, which operates on the same principle and has similar characteristics [20] (Fig. 9.14). The cross section of the LPTT is shown in Fig. 9.13.

9.8 Static Induction Transistor Logic

The static induction transistor logic (SITL) was proposed by Nishizawa and Wilamowski [5, 6]. This logic circuit has almost 100 times better power-delay product than its I^2L competitor. Such drastic improvement of the power-delay product is possible because the SITL structure has a significantly smaller junction parasitic capacitance and also the voltage swing

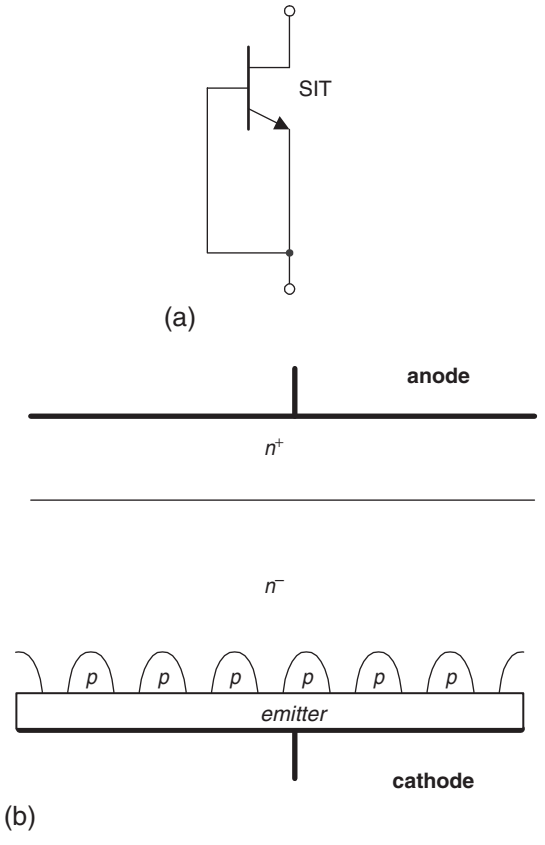

FIGURE 9.11 Static induction diode: (a) circuit diagram and (b) cross section.

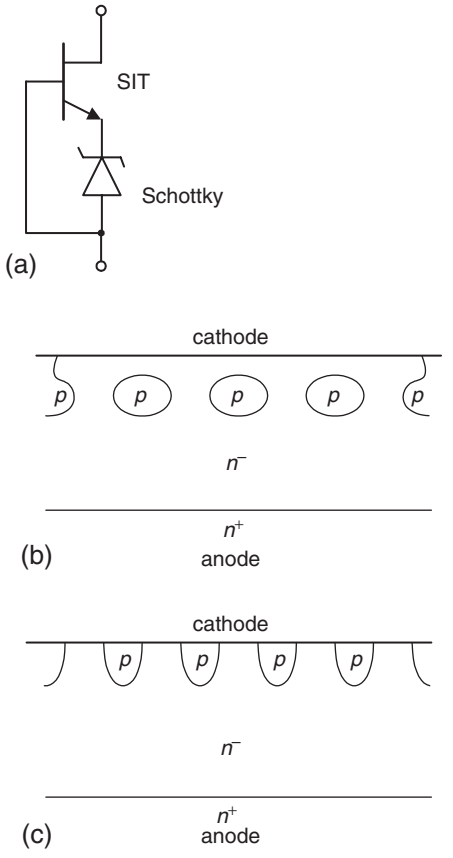

FIGURE 9.12 Schottky diode with enlarged breakdown voltages: (a) circuit diagram; (b) and (c) two cross section of possible implementation.

is reduced. Figs. 9.15 and 9.16 illustrate the concept of SITL. Measured characteristics of *n*-channel transistor of the static induction logic are shown in Fig. 9.17.

9.9 BJT Saturation Protected by SIT

The SI transistor can also be used instead of a Schottky diode to protect a bipolar junction transistor against saturation [21]. This leads to faster switching time. The concept is shown in Figs. 9.18 and 9.19. Note that this approach is advantageous to the solution with Schottky diode, since it does not require additional area on a chip and it does not introduce additional capacitance between the base and the collector. The base collector capacitance is always enlarged by the Miller effect and this leads to slower switching in the case of the solution with the Schottky diode.

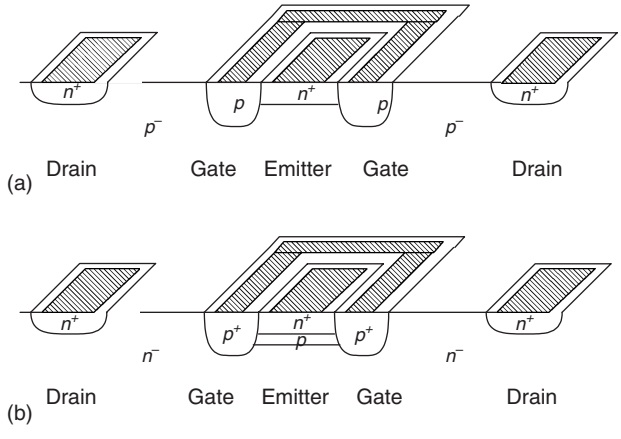

FIGURE 9.13 Structures of the lateral punch-through transistors: (a) simple and (b) with sharper potential barrier.

9.10 Static Induction MOS Transistor

The punch-through transistor with MOS-controlled gate was described in 1983 [22, 23]. In the structure in Fig. 9.20a current can flow in a similar fashion as in the lateral punch-through transistor [20]. In this mode of operation, carriers are moving far from the surface with a velocity close to the saturation velocity. The real advantage of such structure is the very low gate capacitance.

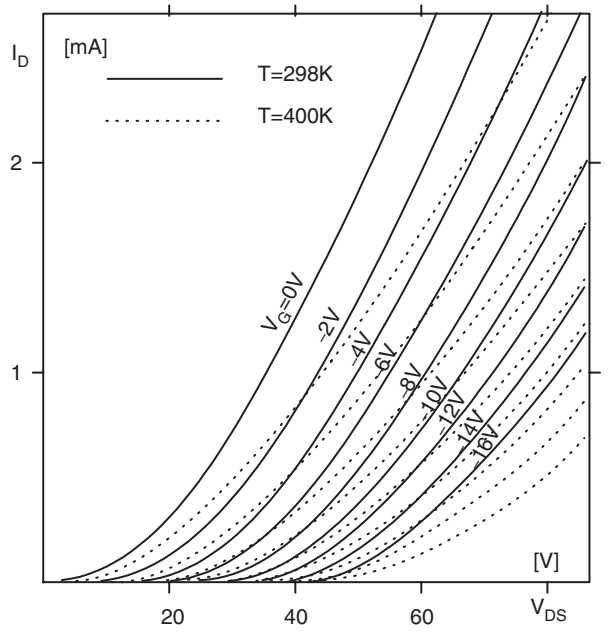

FIGURE 9.14 Characteristics of lateral punch-through transistor.

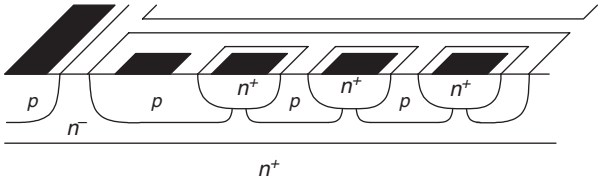

FIGURE 9.15 Cross section of SIT logic.

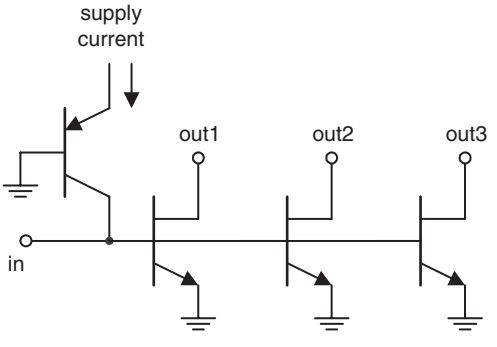

FIGURE 9.16 Diagrams of SIT logic.

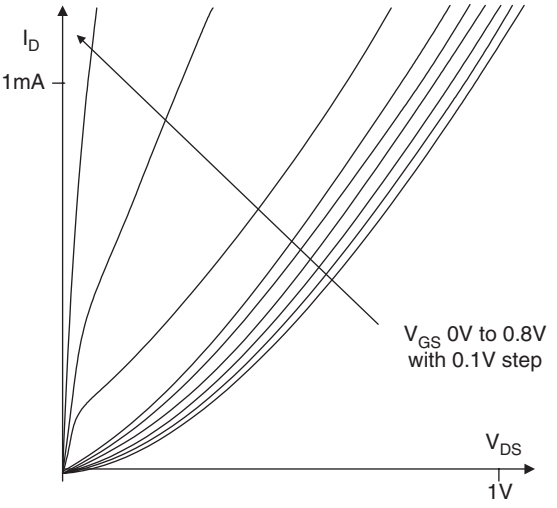

FIGURE 9.17 Measured characteristics of *n*-channel transistor of the logic circuit of Fig. 9.16.

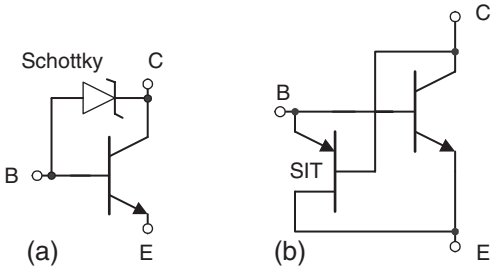

FIGURE 9.18 Protection of bipolar transistor against deep saturation: (a) using Schottky diode and (b) using SIT.

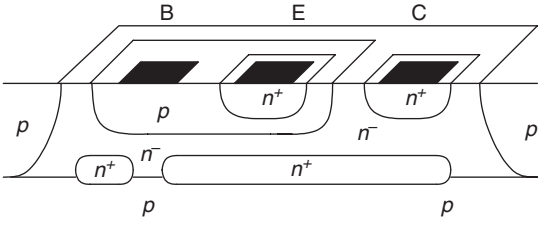

FIGURE 9.19 Cross sections of bipolar transistors protected against deep saturation using SIT.

Another implementation of static induction MOS transistor (SIMOS) is shown in Fig. 9.21. The buried p^+ layer is connected to the substrate, which has a large negative potential. As a result, the potential barrier is high and the emitter–drain current cannot flow. The punch-through current may start to flow when the positive voltage is applied to the gate and in this way the potential barrier is lowered. The *p*-implant layer is depleted and due to the high horizontal electrical field under the gate there is no charge accumulation under this gate. Such a transistor has several advantages over the traditional MOS transistor.

1. The gate capacitance is very small, since there is no accumulation layer under the gate.
2. Carriers are moving with a velocity close to saturation velocity.
3. Much lower substrate doping and the existing depletion layer lead to much smaller drain capacitance.

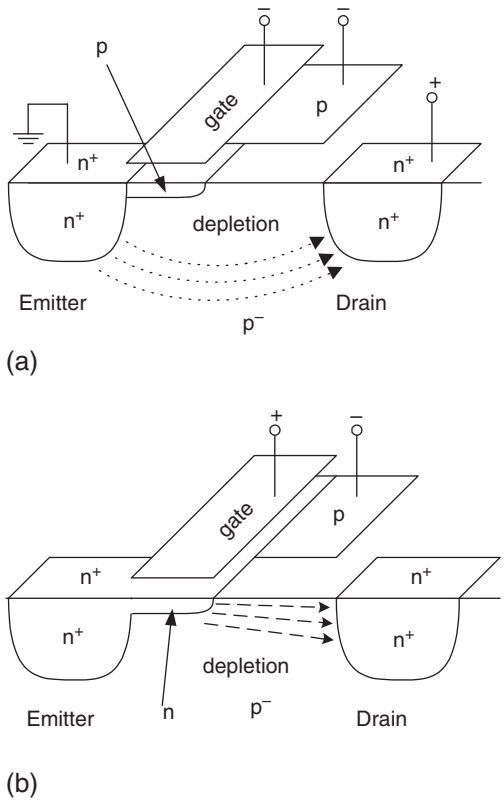

FIGURE 9.20 MOS controlled punch-through transistor: (a) transistor in the punch-through mode for the negative gate potential and (b) transistor in the on-state for the positive gate potential.

The device operates in a similar fashion as MOS transistor in subthreshold conditions, but this process occurs at much higher current levels. Such "bipolar mode" of operation may have many advantages in VLSI applications.

9.11 Space Charge Limiting Load (SCLL)

Using the concept of the space charge limited current flow it is possible to fabricate very large resistors on a very small area. Moreover these resistors have a very small parasitic capacitance. For example, a 50 kΩ resistor requires only several square μm when 2 μm feature size technology is used [7].

Depending on the value of the electrical field, the device current is described by the following two equations. For a small electrical field $v(x) = \mu E(x)$

$$I_{DS} = \frac{9}{8} V_{DS}^2 \mu \varepsilon_{Si} \varepsilon_0 \frac{A}{L^3} \tag{9.17}$$

For a large electrical field $v(x) = \text{const}$

$$I_{DS} = 2 V_{DS} v_{sat} \varepsilon_{Si} \varepsilon_0 \frac{A}{L^2} \tag{9.18}$$

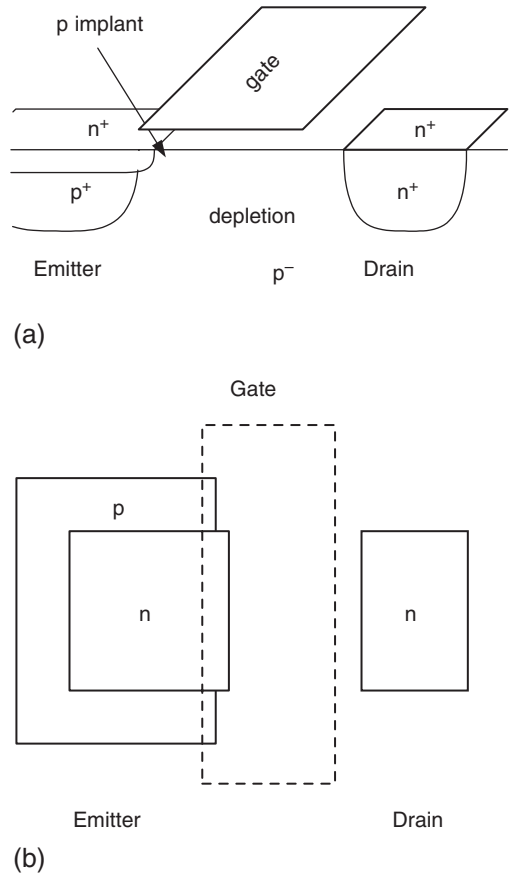

FIGURE 9.21 Static induction MOS structure: (a) cross section and (b) top view.

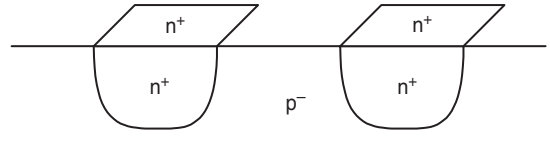

FIGURE 9.22 Space charge limiting load (SCLL).

Moreover these resistors, which are based on the space charge limit flow, have a very small parasitic capacitance.

9.12 Power MOS Transistors

Power MOS transistors are being used for fast switching power supplies and for switching power converters. They can be driven with relatively small power and switching frequencies could be very high. High switching frequencies lead to compact circuit implementations with small inductors and small capacitances. Basically only two technologies, DMOS and VMOS, are used for power MOS devices as shown in Figs. 9.23 and 9.24.

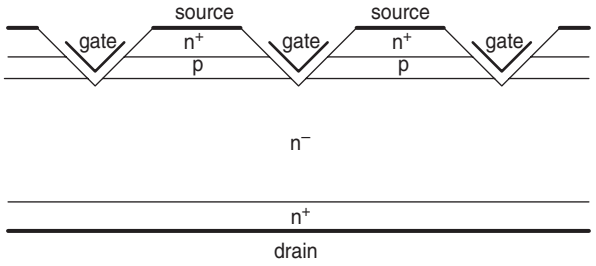

FIGURE 9.23 Cross section of the VMOS transistor.

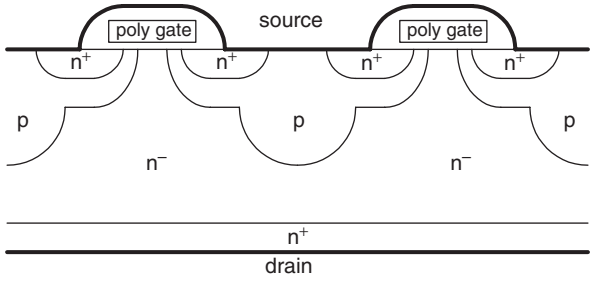

FIGURE 9.24 Cross section of the DMOS transistor.

A more popular structure is the DMOS shown in Fig. 9.24. This structure also uses the SIT concept. Note that for large drain voltages the *n*-region is depleted from carriers and statically induced electrical field in the vicinity of the virtual drain is significantly reduced. As a result this transistor may withstand much larger drain voltages and also the effect of channel length modulation is significantly reduced. The later effect leads to larger output resistances of the transistor. Therefore, the drain current is less sensitive to drain voltage variations. The structure in Fig. 9.24 can be considered as a composition of the MOS transistor and the SIT transistor as is shown in Fig. 9.25.

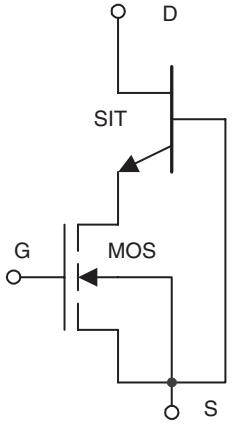

FIGURE 9.25 Equivalent diagram with MOS and SIT of the structure of Fig. 9.24.

The major disadvantage of power MOS transistors is relatively large drain series resistance and much smaller transconductance in comparison to bipolar transistors. Both of these parameters can be improved dramatically by a simple change of the type of drain. In the case of *n*-channel device from *n*-type to *p*-type drain. This way the integrated structure is being built where its equivalent diagram consists MOS transistor integrated with bipolar transistor. Such structure has β times larger transconductance (β is the current gain of bipolar transistor) and much smaller series resistance due to the conductivity modulation effect caused by holes injected into lightly doped drain region. Such device is known as insulated gate bipolar transistors (IGBT) shown in Fig. 9.26. Their main disadvantage is large switching time limited primarily by poor switching performance of bipolar transistor. Another difficulty is related to a possible latch-up action of four layer $n^+pn^-p^+$ structure. This undesired effect could be suppressed by using heavily doped p^+ region in the base of NPN structure, which leads to significant reduction of the current gain of this parasitic transistor. The gain of other PNP transistor must be kept large so the transconductance of the entire device is large too. The IGBT transistor has breakdown voltages up to 1500 V, turn-off times are in range 0.1–0.5 μs. They may operate with currents above 100 A with a forward voltage drop about 3 V.

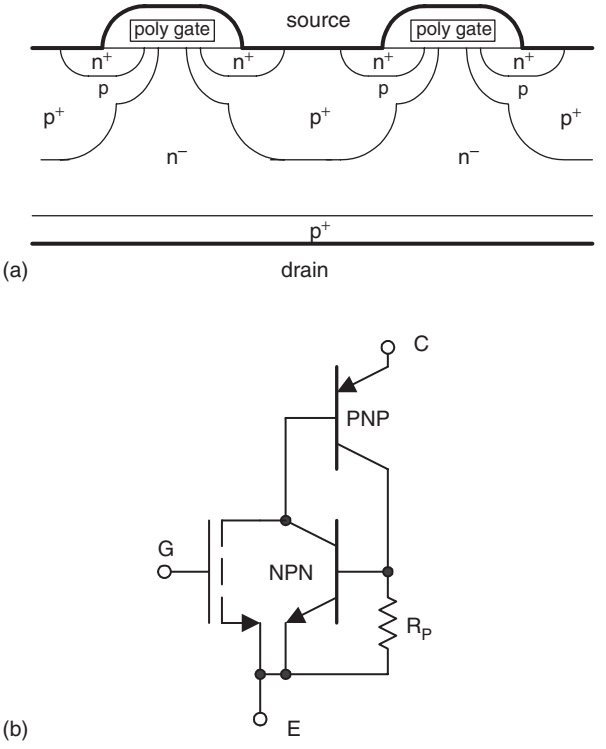

FIGURE 9.26 Insulated gate bipolar transistor (IGBT): (a) cross section and (b) equivalent diagram.

9.13 Static Induction Thyristor

There are several special semiconductor devices dedicated to high power applications. The most popular is thyristor known also as silicon control rectifier (SCR). This device has a four layer structure Fig. 9.27a and it can be considered as two transistors *npn* and *pnp* connected as shown in Fig. 9.27b.

In normal mode of operation (anode has positive potential) only one junction is reverse-biased and it can be represented by capacitance *C*. A spike of anode voltage can therefore get through capacitor *C* and it can trigger SCR. This behavior is not acceptable in practical application and therefore a different device structure is being used as is shown in Fig. 9.28. Note that by shorting gate to cathode by resistor *R* it is much more difficult to trigger the *npn* transistor by spike of anode voltage. This way rapid change of anode voltages is not able to trigger thyristor. Therefore this structure has very large *dv/dt* parameter.

When NPN transistor is replaced with SI transistor parameters of a thyristor can be significantly improved. For example, with breaking voltage in the range of 5 kV and current of 600 A the switching on time can be as short as 100 ns and *dv/dt* parameter can be as large as 50 kV/s [15, 24].

Most of the SCRs sold in the market comprise an integrated structure composed of two or more thyristors. This structure has both large *dv/dt* and *di/dt* parameters. This structure consists of internal thyristor which significantly amplifies the gate signal.

One can notice that the classical thyristor as shown in Fig. 9.27 can be turned off by the gate voltage while integrated SCR shown in Fig. 9.29 can be only turned off by reducing anode current to zero. Most of the SCRs sold in the market have an integrated structure composed of two or more thyristors. This structure has both large *dv/dt* and *di/dt* parameters.

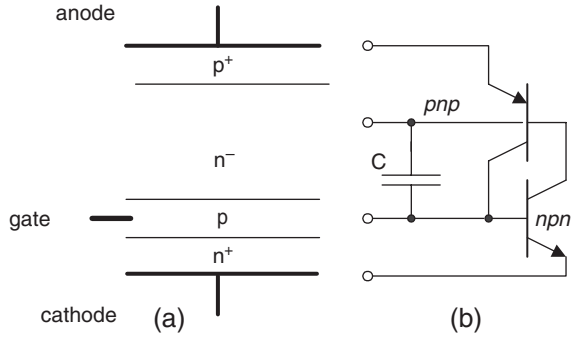

FIGURE 9.27 Silicon control rectifier: (a) cross section and (b) equivalent diagram.

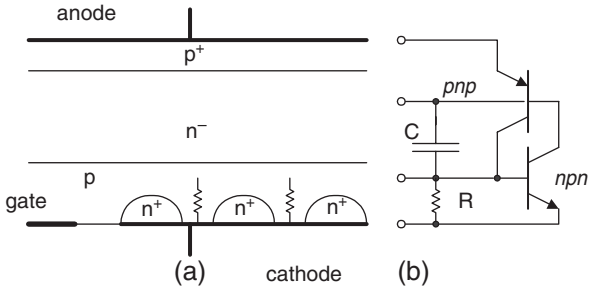

FIGURE 9.28 Silicon control rectifier with larger *dv/dt* parameter: (a) cross section and (b) equivalent diagram.

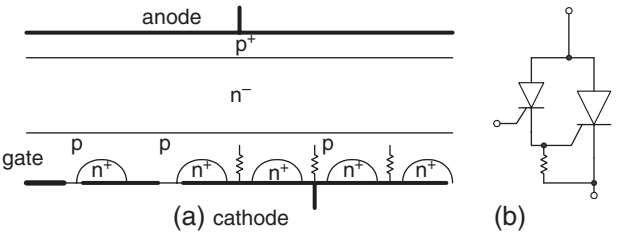

FIGURE 9.29 Integrated structure of silicon control rectifier: (a) cross section and (b) equivalent diagram.

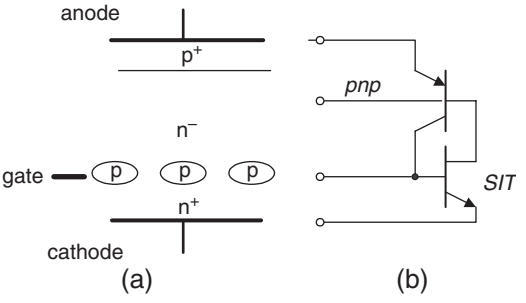

FIGURE 9.30 GTO–SIT: (a) cross section and (b) equivalent diagram.

9.14 Gate Turn Off Thyristor

For the dc operation it is important to have a thyristor which can be turned off by the gate voltage. Such thyristor has a structure similar to the one shown in Fig. 9.27. It is important, however, to have significantly different current gains β for *pnp* and *npn* transistors. The current gain of *npn* transistor should be as large as possible and the current gain of *pnp* transistor should be small. The product of β_{npn} and β_{pnp} should be larger than one. This can be easily implemented using SI structure as shown in Fig. 9.30.

References

1. Nishizawa J., Terasaki T., and Shibata J., "Field-Effect Transistor versus Analog Transistor (Static Induction Transistor)," *IEEE Trans. on Electron Devices*, vol. **22**, No. 4, pp. 185–197, April 1975.

2. Tatsude M., Yamanaka E., and Nishizawa J., "High-Frequency High-Power Static Induction Transistor," *IEEE Industry Application Magazine*, pp. 40–45, March/April 1995.
3. Nishizawa J., Plotka P., and Kurabayashi T., "Ballistic and Tunneling GaAs Static Induction Transistors: Nano-Devices for THz Electronics," *IEEE Trans. on Electron Devices*, vol. **49**, No. 7, pp. 1102–1111, 2002.
4. Nishizawa J., Suto K., and Kurabayashi T., "Recent Advance in Tetrahertz Wave and Material Basis," *Russian Physics Journal*, vol. **46**, No. 6, pp. 615–622, 2003.
5. Nishizawa J. and Wilamowski B. M., "Integrated Logic – State Induction Transistor Logic," *International Solid State Circuit Conference*, Philadelphia USA, pp. 222–223, 1977.
6. Nishizawa J. and Wilamowski B. M., "Static Induction Logic – A Simple Structure with Very Low Switching Energy and Very High Packing Density," *International Conference on Solid State Devices*, Tokyo, Japan, pp. 53–54, 1976 and *Journal of Japanese Soc. Appl. Physics*, vol. **16**, No. 1, pp. 158–162, 1977.
7. Wilamowski B. M., "High Speed, High Voltage, and Energy Efficient Static Induction Devices," *12 Symposium of Static Induction Devices – SSID'99*, (invited speech) Tokyo, Japan, pp. 23–28, April 23, 1999.
8. Plotka P. and Wilamowski B. M., "Interpretation of Exponential Type Drain Characteristics of the SIT," *Solid-State Electronics*, vol. **23**, pp. 693–694, 1980.
9. Plotka P. and Wilamowski B. M., "Temperature Properties of the Static Induction Transistor," *Solid-State Electronics*, vol. **24**, pp. 105–107, 1981.
10. Kim C. W., Kimura M., Yano K., Tanaka, A., and Sukegawa, T., "Bipolar-Mode Static Induction Transistor: Experiment and Two-Dimensional Analysis," *IEEE Trans. on Electron Devices*, vol. **37**, No. 9, pp. 2070–2075, September 1990.
11. Nakamura Y., Tadano H., Takigawa M., Igarashi I., and Nishizawa J., "Experimental Study on Current Gain of BSIT," *IEEE Trans. on Electron Devices*, vol. **33**, No. 6, pp. 810–815, June 1986.
12. Nishizawa J., Ohmi T., and Chen H. L., "Analysis of Static Characteristics of a Bipolar-Mode SIT (BSIT)," *IEEE Trans. on Electron Devices*, vol. **29**, No. 8, pp. 1233–1244, August 1982.
13. Yano K., Henmi I., Kasuga M., and Shimizu A., "High-Power Rectifier Using the BSIT Operation," *IEEE Trans. on Electron Devices*, vol. **45**, No. 2, pp. 563–565, February 1998.
14. Yano K., Masahito M., Moroshima H., Morita J., Kasuga M., and Shimizu A., "Rectifier Characteristics Based on Bipolar-Mode SIT Operation," *IEEE Electron Device Letters*, vol. **15**, No. 9, pp. 321–323, September 1994.
15. Hironaka R., Watanabe M., Hotta E., and Okino A. "Performance of Pulsed Power Generator using High Voltage Static Induction Thyristor," *IEEE Trans. on Plasma Science*, vol. **28**, No. 5, pp. 1524–1527, 2000.
16. Yano K., Honarkhah S., and Salama A., "Lateral SOI Static Induction Rectifiers", *Proc. of 2001 Int. Symp. on Power Semiconductor Devices*, Osaka, pp. 247–250, 2001.
17. Yano K., Hattori N., Yamamoto Y., and Kasuga M., "Impacts of Channel Implantation on Performance of Static Shielding Diodes and Static Induction Rectifiers," *Proc. of 2001 Int. Symp. on Power Semiconductor Devices*, Osaka, pp. 219–222, 2001.
18. Wilamowski B. M., "Schottky Diodes with High Breakdown voltage," *Solid-State Electronics*, vol. **26**, No. 5, pp. 491–493, 1983.
19. Baliga B. J., "The Pinch Rectifier: A Low Forward-Drop, High-Speed Power Diode," *IEEE Electron Device Letters*, vol. **5**, pp. 194–196, 1984.
20. Wilamowski B. M. and Jaeger R. C., "The Lateral Punch-Through Transistor," *IEEE Electron Device Letters*, vol. **3**, No. 10, pp. 277–280, 1982.
21. Wilamowski B. M., Mattson R. H., and Staszak Z. J., "The SIT saturation protected bipolar transistor," *IEEE Electron Device Letters*, vol. **5**, pp. 263–265, 1984.
22. Wilamowski B. M., "The Punch-Through Transistor with MOS Controlled Gate," *Phys. Status Solidi (a)*, vol. **79**, pp. 631–637, 1983.
23. Wilamowski B. M., Jaeger R. C., and Fordemwalt J. N., "Buried MOS Transistor with Punch-Through," *Solid State Electronics*, vol. **27**, No. 8/9, pp. 811–815, 1984.
24. Shimizu N., Sekiya T., Iida K., Imanishi Y., Kimura M., and Nishizawa J., "Over 55kV/us, dv/dt turnoff characteristics of 4kV-Static Induction Thyristor for Pulsed Power Applications," *Proc. of 2004 Int. Symp. on Power Semiconductor Devices,* Kitakyushu, Japan, pp. 281–284, 2004.