16

Resonant and Soft-switching Converters

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16.1 Introduction

Advances in power electronics in the last few decades have led to not just improvements in power devices, but also new concepts in converter topologies and control. In the 1970s, conventional pulse width modulated (PWM) power converters were operated in a switched mode operation. Power switches have to cut off the load current within the turn-on and turn-off times under the hard switching conditions. Hard switching refers to the stressful switching behavior of the power electronic devices. The switching trajectory of a hard-switched power device is shown in Fig. 16.1. During the turn-on and turn-off processes, the power device has to withstand high voltage and current simultaneously, resulting in

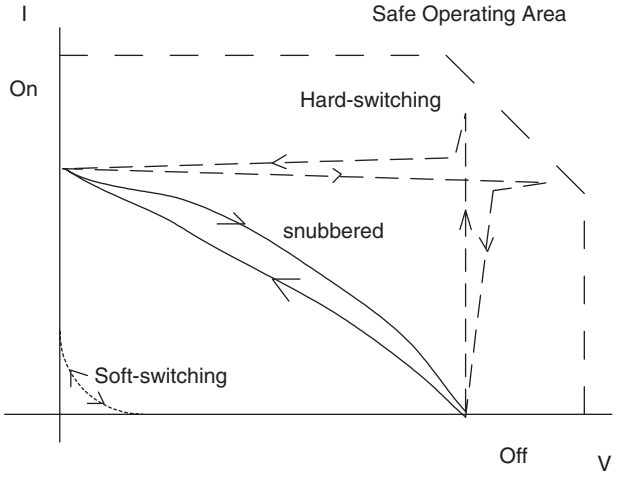


FIGURE 16.1 Typical switching trajectories of power switches.

high switching losses and stress. Dissipative passive snubbers are usually added to the power circuits so that the *dv/dt* and *di/dt* of the power devices could be reduced, and the switching loss and stress be diverted to the passive snubber circuits. However, the switching loss is proportional to the switching frequency, thus limiting the maximum switching frequency of the power converters. Typical converter switching frequency was limited to a few tens of kilo-Hertz (typically 20–50 kHz) in early 1980s. The stray inductive and capacitive components in the power circuits and power devices still cause considerable transient effects, which in turn give rise to electromagnetic interference (EMI) problems. Figure 16.2 shows ideal switching waveforms and typical practical waveforms of the switch voltage. The transient ringing effects are major causes of EMI.

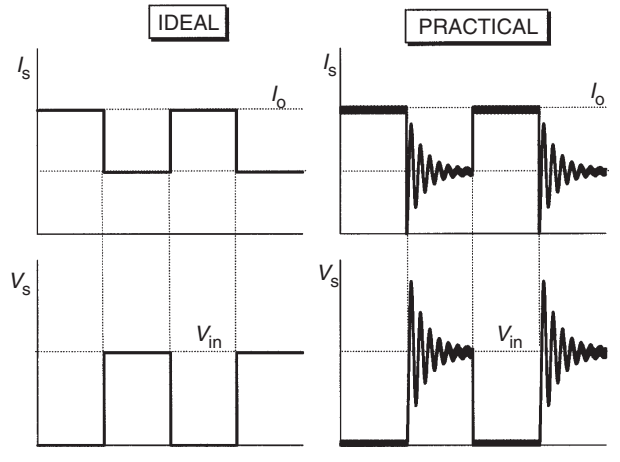
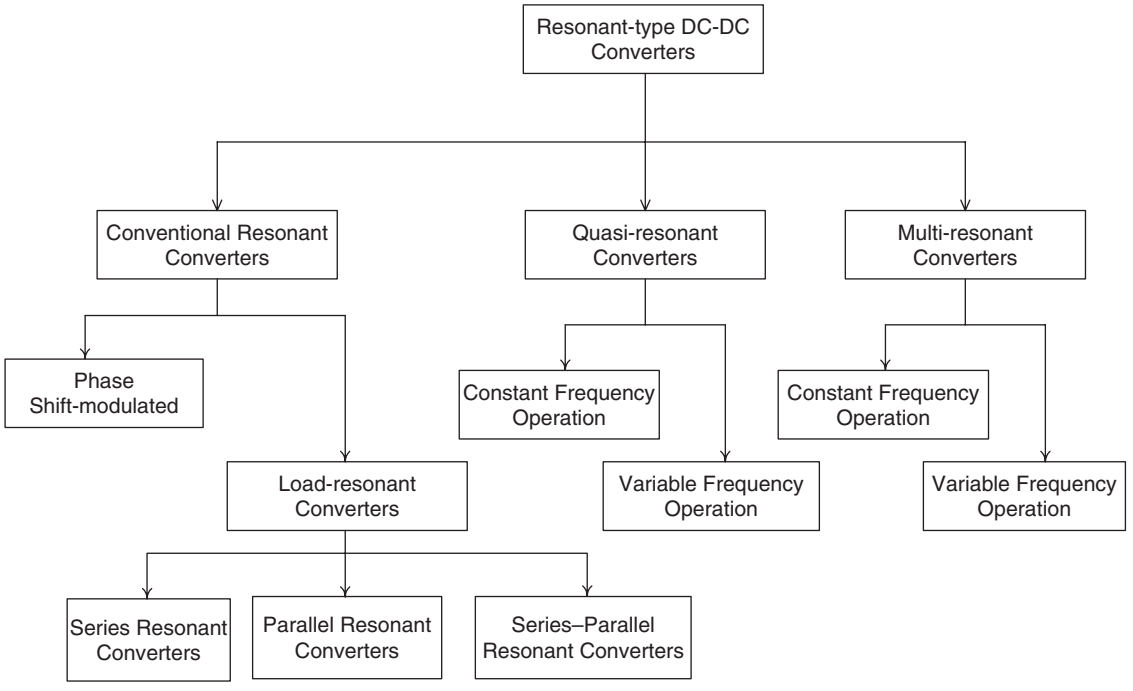


FIGURE 16.2 Typical: (a) ideal and (b) practical switching waveforms.

In the 1980s, lots of research efforts were diverted towards the use of resonant converters. The concept was to incorporate resonant tanks in the converters to create oscillatory (usually sinusoidal) voltage and/or current waveforms so that zero-voltage switching (ZVS) or zero-current switching (ZCS) conditions can be created for the power switches. The reduction of switching loss and the continual improvement of power switches allow the switching frequency of the resonant converters to reach hundreds of kilo-Hertz (typically 100–500 kHz). Consequently, the size of magnetic components can be reduced and the power density of the converters increased. Various forms of resonant converters have been proposed and developed. However, most of the resonant converters suffer several problems. When compared with the conventional PWM converters, the resonant current and the voltage of resonant converters have high peak values, leading to higher conduction loss and higher V and I rating requirements for the power devices. Also, many resonant converters require frequency modulation (FM) for output regulation. Variable switching frequency operation makes the filter design and control more complicated.

In late 1980s and throughout 1990s, further improvements have been made in converter technology. New generations of soft-switched converters that combine the advantages of conventional PWM converters and resonant converters have been developed. These soft-switched converters have switching waveforms similar to those of conventional PWM converters except that the rising and falling edges of the waveforms are "smoothed" with no transient spikes. Unlike the resonant converters, new soft-switched converters usually utilize the resonance in a controlled manner. Resonance is allowed to occur just before and during the turn-on and turn-off processes so as to create ZVS and ZCS conditions. Other than that, they behave just like conventional PWM converters. With simple modifications, many customized control integrated circuits (ICs) designed for conventional converters can be employed for soft-switched converters. Because the switching loss and stress have been reduced, soft-switched converter can be operated at the very high frequency (typically 500 kHz to a few Mega-Hertz). Soft-switching converters also provide an effective solution to suppress EMI and have been applied to DC–DC, AC–DC, and DC–AC converters. This chapter covers the basic technology of resonant and soft-switching converters. Various forms of soft-switching techniques such as ZVS, ZCS, voltage clamping, zero-voltage transition methods, etc. are addressed. The emphasis is placed on the basic operating principle and practicality of the converters without using much mathematical analysis.

16.2 Classification



16.3 Resonant Switch

Prior to the availability of fully controllable power switches, thyristors were the major power devices used in power electronic circuits. Each thyristor requires a commutation circuit, which usually consists of a *LC* resonant circuit, for forcing the current to zero in the turn-off process [1]. This mechanism is in fact a type of zero-current turn-off process. With the recent advancement in semiconductor technology, the voltage and current handling capability, and the switching speed of fully controllable switches have significantly been improved. In many high power applications, controllable switches such as gate turn-offs (GTOs) and insulated gate bipolar transistors (IGBTs) have replaced thyristors [2, 3]. However, the use of resonant circuit for achieving ZCS and/or ZVS [4–8] has also emerged as a new technology for power converters. The concept of resonant switch that replaces conventional power switch is introduced in this section.

A resonant switch is a sub-circuit comprising a semiconductor switch S and resonant elements, L_r and C_r [9–11]. The switch S can be implemented by a unidirectional or bidirectional switch, which determines the operation mode of the resonant switch. Two types of resonant switches [12], including zero-current (ZC) resonant switch and zero-voltage (ZV) resonant switches, are shown in Figs. 16.3 and 16.4, respectively.

16.3.1 ZC Resonant Switch

In a ZC resonant switch, an inductor L_r is connected in series with a power switch S in order to achieve zero-current switching (ZCS). If the switch S is a unidirectional switch, the switch current is allowed to resonate in the positive half cycle only. The resonant switch is said to operate in *half-wave* mode. If a diode is connected in anti-parallel with the unidirectional switch, the switch current can flow in both directions. In this case, the resonant switch can operate in *full-wave* mode. At turn-on, the switch current will rise slowly from zero. It will then oscillate, because of the resonance between L_r and C_r. Finally, the switch can be commutated at the next zero current duration. The objective of this type of switch is to shape the switch current waveform during conduction time in order to create a zero-current condition for the switch to turn off [13].

16.3.2 ZV Resonant Switch

In a ZV resonant switch, a capacitor C_r is connected in parallel with the switch S for achieving zero-voltage switching (ZVS).

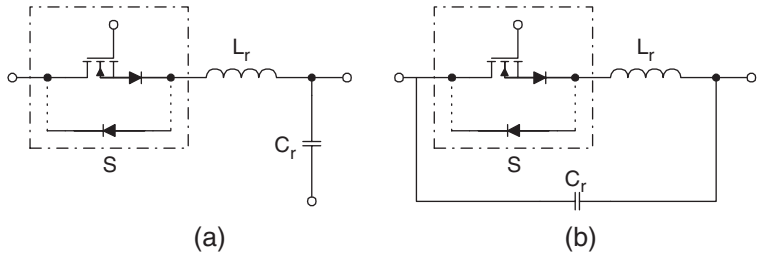


FIGURE 16.3 Zero-current (ZC) resonant switch.

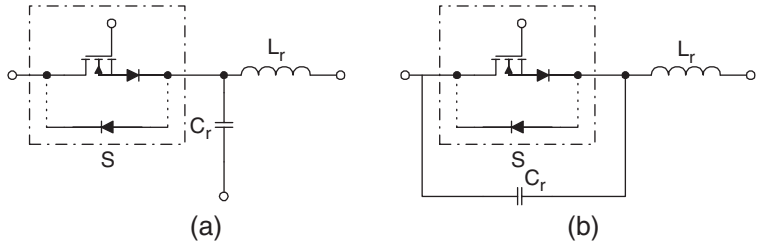


FIGURE 16.4 Zero-voltage (ZV) resonant switch.

If the switch S is a unidirectional switch, the voltage across the capacitor C_r can oscillate freely in both positive and negative half-cycle. Thus, the resonant switch can operate in *full-wave* mode. If a diode is connected in anti-parallel with the unidirectional switch, the resonant capacitor voltage is clamped by the diode to zero during the negative half-cycle. The resonant switch will then operate in *half-wave* mode. The objective of a ZV switch is to use the resonant circuit to shape the switch voltage waveform during the off time in order to create a zero-voltage condition for the switch to turn on [13].

16.4 Quasi-resonant Converters

Quasi-resonant converters (QRCs) can be considered as a hybrid of resonant and PWM converters. The underlying principle is to replace the power switch in PWM converters with the resonant switch. A large family of conventional converter circuits can be transformed into their resonant converter counterparts. The switch current and/or voltage waveforms are forced to oscillate in a quasi-sinusoidal manner, so that ZCS and/or ZVS can be achieved. Both ZCS-QRCs and ZVS-QRCs have *half-wave* and *full-wave* mode of operations [8–10, 12].

16.4.1 ZCS-QRCs

A ZCS-QRC designed for *half-wave* operation is illustrated with a buck type DC–DC converter. The schematic is shown in Fig. 16.5a. It is formed by replacing the power switch in conventional PWM buck converter with the ZC resonant switch in Fig. 16.3a. The circuit waveforms in steady state are shown in Fig. 16.5b. The output filter inductor L_f is sufficiently large so that its current is approximately constant. Prior to turning the switch on, the output current I_o freewheels through the output diode D_f. The resonant capacitor voltage V_{Cr} equals zero. At t_0, the switch is turned on with ZCS. A quasi-sinusoidal current I_S flows through L_r and C_r, the output filter, and the load. S is then softly commutated at t_1 with ZCS again. During and after the gate pulse, the resonant capacitor voltage V_{Cr} rises and then decays at a rate depending on the output current. Output voltage regulation is achieved by controlling the switching frequency. Operation and characteristics of the converter depend mainly on the design of the resonant circuit $L_r C_r$. The following parameters are defined: voltage conversion ratio M, characteristic impedance Z_r, resonant frequency f_r, normalized load resistance r, normalized switching frequency γ.

$$M = \frac{V_o}{V_i} \tag{16.1a}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{16.1b}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{16.1c}$$

$$r = \frac{R_L}{Z_r} \tag{16.1d}$$

$$\gamma = \frac{f_s}{f_r} \tag{16.1e}$$

It can be seen from the waveforms that if $I_o > V_i/Z_r$, I_S will not come back to zero naturally and the switch will have to be

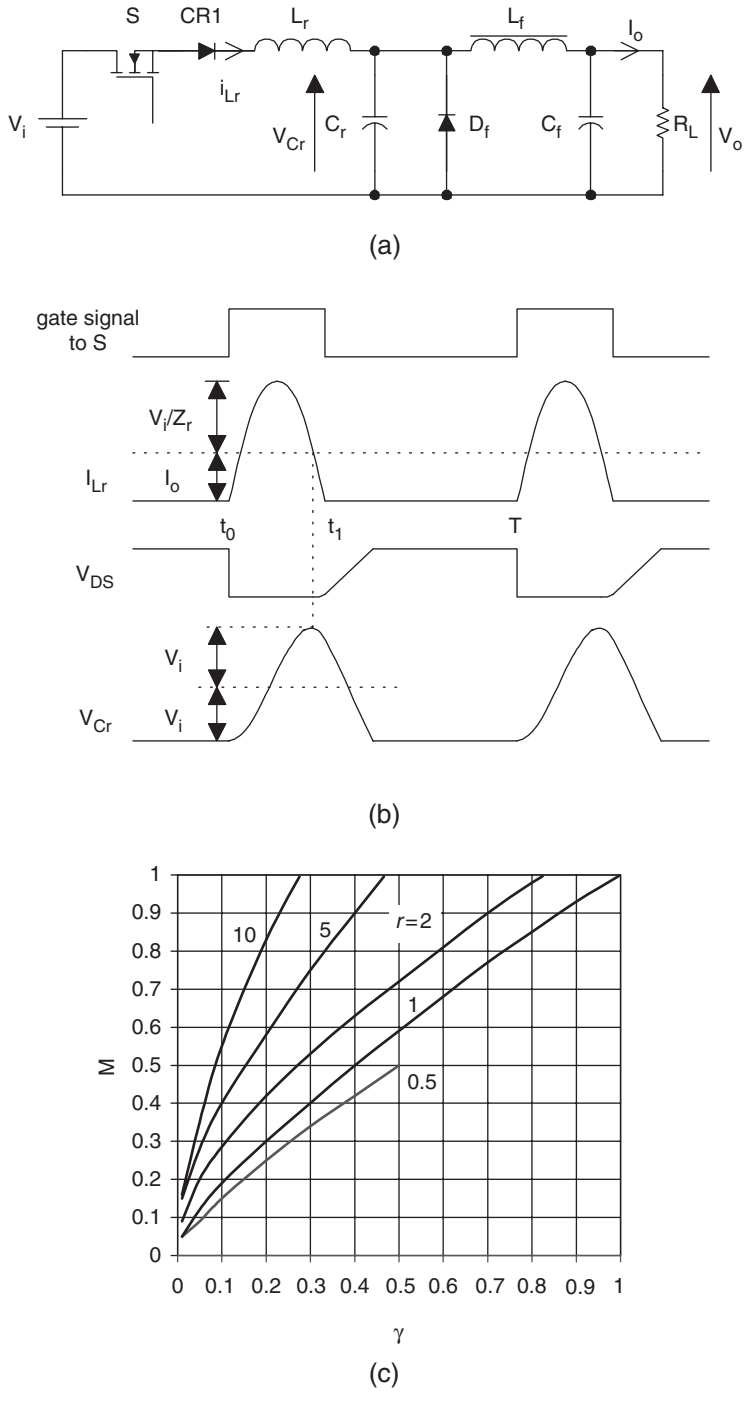


FIGURE 16.5 Half-wave, quasi-resonant buck converter with ZCS: (a) schematic diagram; (b) circuit waveforms; and (c) relationship between M and γ.

forced off, thus resulting in turn-off losses. The relationships between M and γ at different r are shown in Fig. 16.5c. It can be seen that M is sensitive to the load variation. At light load conditions, the unused energy is stored in C_r, leading to an increase in the output voltage. Thus, the switching frequency has to be controlled, in order to regulate the output voltage.

If an anti-parallel diode is connected across the switch, the converter will be operating in *full-wave* mode. The circuit schematic is shown in Fig. 16.6a. The circuit waveforms in steady state are shown in Fig. 16.6b. The operation is similar to the one in *half-wave* mode. However, the inductor current is allowed to reverse through the anti-parallel

diode and the duration for the resonant stage is lengthened. This permits excess energy in the resonant circuit at light loads to be transferred back to the voltage source V_i. This significantly reduces the dependence of V_o on the output load. The relationships between M and γ at different r are shown in Fig. 16.6c. It can be seen that M is insensitive to load variation.

By replacing the switch in the conventional converters, a family of QRC [9] with ZCS is shown in Fig. 16.7.

16.4.2 ZVS-QRC

In these converters, the resonant capacitor provides a zero-voltage condition for the switch to turn on and off.

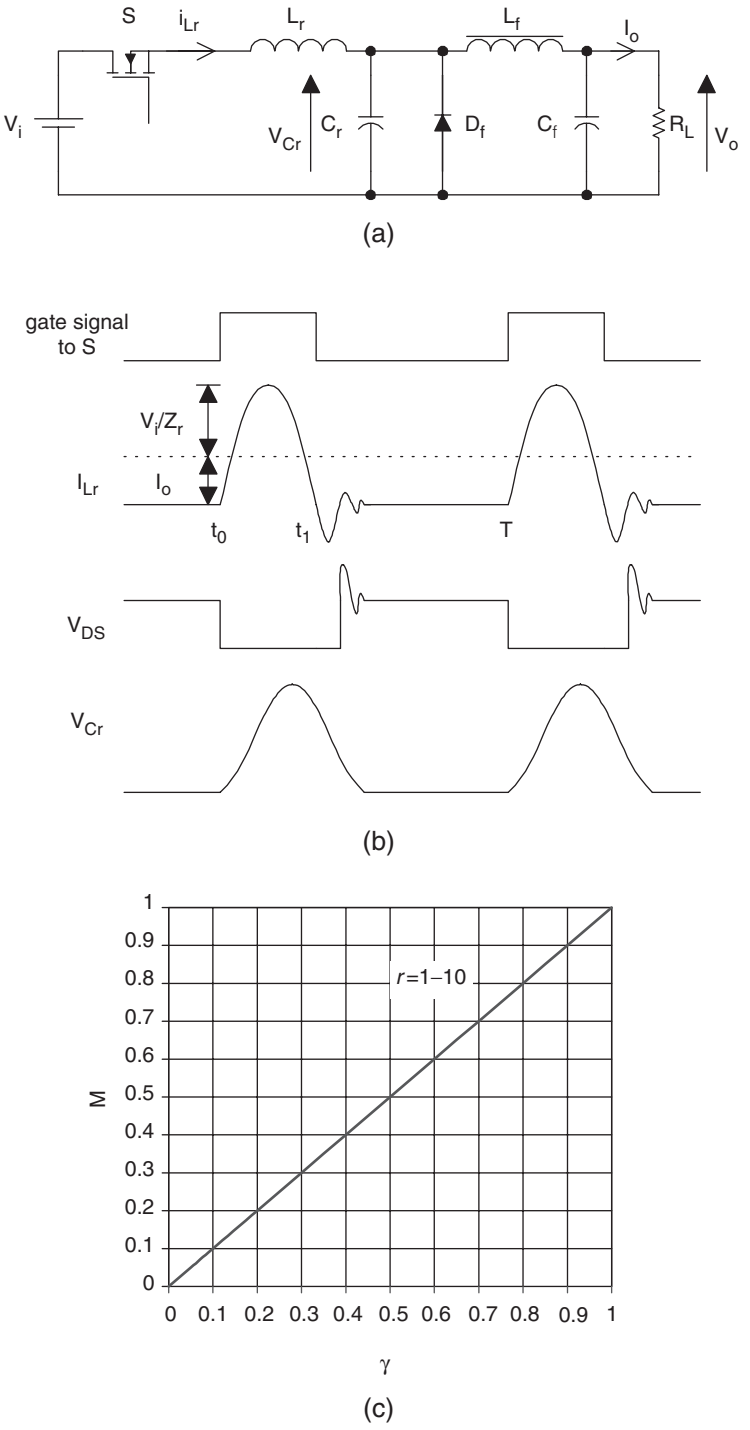


FIGURE 16.6 Full-wave, quasi-resonant buck converter with ZCS: (a) schematic diagram; (b) circuit waveforms; and (c) relationship between M and γ.

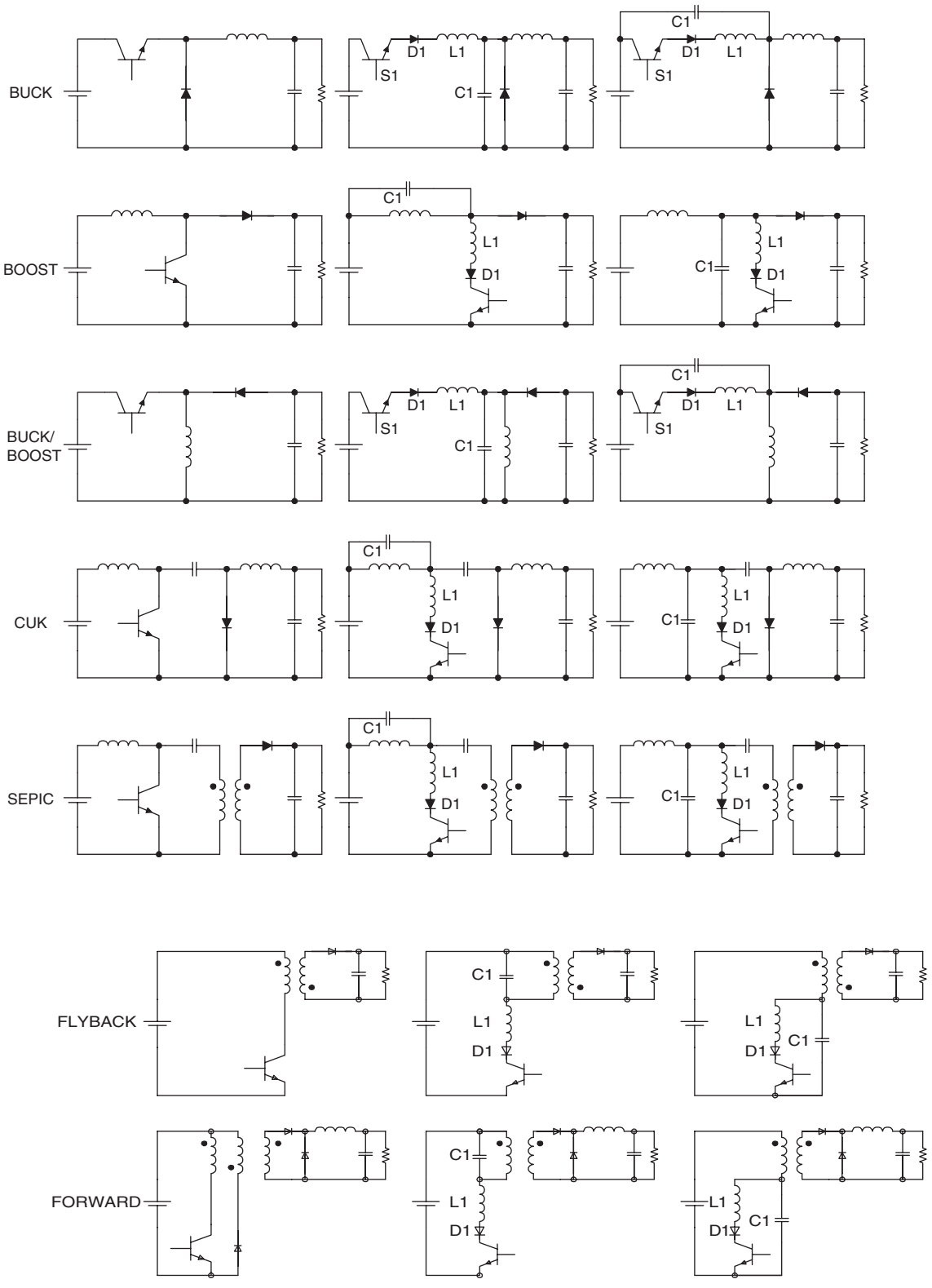


FIGURE 16.7 A family of quasi-resonant converter with ZCS.

A quasi-resonant buck converter designed for *half-wave* operation is shown in Fig. 16.8a – using a ZV resonant switch in Fig. 16.4b. The steady-state circuit waveforms are shown in Fig. 16.8b. Basic relations of ZVS-QRCs are given in Eqs. (16.1a–e). When the switch S is turned on, it carries the output current I_o. The supply voltage V_i reverse biases the diode D_f. When the switch is zero-voltage (ZV) turned off, the output current starts to flow through the resonant capacitor C_r. When the resonant capacitor voltage V_{Cr} is equal to V_i, D_f turns on. This starts the resonant stage. When V_{Cr} equals zero, the anti-parallel diode turns on. The resonant capacitor is shorted and the source voltage is applied to the resonant inductor L_r. The resonant inductor current I_{Lr} increases linearly until it reaches I_o. Then D_f turns off. In order to achieve ZVS, S should be triggered during the time when the anti-parallel diode conducts. It can be seen from the waveforms that the peak amplitude of the resonant capacitor voltage should be greater or equal to the input voltage (i.e. $I_o Z_r > V_{in}$). From Fig. 16.8c, it can be seen that the voltage conversion ratio is load-sensitive. In order to regulate the output voltage for different loads *r*, the switching frequency should also be changed accordingly.

ZVS converters can be operated in *full-wave* mode. The circuit schematic is shown in Fig. 16.9a. The circuit waveforms in steady state are shown in Fig. 16.9b. The operation is similar to *half-wave* mode of operation, except that V_{Cr} can swing between positive and negative voltages. The relationships between M and γ at different r are shown in Fig. 16.9c.

Comparing Fig. 16.8c with Fig. 16.9c, it can be seen that M is load-insensitive in *full-wave* mode. This is a desirable feature. However, as the series diode limits the direction of the switch current, energy will be stored in the output capacitance of the switch and will dissipate in the switch during turn on. Hence, the *full-wave* mode has the problem of capacitive turn-on loss, and is less practical in high frequency operation. In practice, ZVS-QRCs are usually operated in *half-wave* mode rather than *full-wave* mode.

By replacing the ZV resonant switch in the conventional converters, various ZVS-QRCs can be derived. They are shown in Fig. 16.10.

16.4.3 Comparisons between ZCS and ZVS

ZCS can eliminate the switching losses at turn off and reduce the switching losses at turn on. As a relatively large capacitor is connected across the output diode during resonance, the converter operation becomes insensitive to the diode's junction capacitance. When power MOSFETs are zero-current switched on, the energy stored in the device's capacitance will be dissipated. This capacitive turn-on loss is proportional to the switching frequency. During turn on, considerable rate of change of voltage can be coupled to the gate drive circuit through the Miller capacitor, thus increasing switching loss and noise. Another limitation is that the switches are under high current stress, resulting in higher conduction loss. However, it should be noted that ZCS is particularly effective in reducing switching loss for power devices (such as IGBT) with large tail current in the turn-off process.

ZVS eliminates the capacitive turn-on loss. It is suitable for high-frequency operation. For single-ended configuration, the switches could suffer from excessive voltage stress, which is proportional to the load. It will be shown in Section 16.5 that the maximum voltage across switches in half-bridge and full-bridge configurations is clamped to the input voltage.

For both ZCS and ZVS, output regulation of the resonant converters can be achieved by variable frequency control. ZCS operates with constant on-time control, while ZVS operates with constant off-time control. With a wide input and load range, both techniques have to operate with a wide switching frequency range, making it not easy to design resonant converters optimally.

16.5 ZVS in High Frequency Applications

By the nature of the resonant tank and ZCS, the peak switch current in resonant converters is much higher than that in the square-wave counterparts. In addition, a high voltage will be established across the switch in the off state after the resonant stage. When the switch is switched on again, the energy stored in the output capacitor will be discharged through the switch, causing a significant power loss at high frequencies and high voltages. This switching loss can be reduced by using ZVS.

ZVS can be viewed as square-wave power utilizing a constant off-time control. Output regulation is achieved by controlling the on time or switching frequency. During the off time, the resonant tank circuit traverses the voltage across the switch from zero to its peak value and then back to zero again. At that ZV instant, the switch can be reactivated. Apart from the conventional single-ended converters, some other examples of converters with ZVS are illustrated in the following section.

16.5.1 ZVS with Clamped Voltage

The high voltage stress problem in the single-switch configuration with ZVS can be avoided in half-bridge (HB) and full-bridge (FB) configurations [14–17]. The peak switch voltage can be clamped to the dc supply rail, and thus reducing the switch voltage stress. In addition, the series transformer leakage and circuit inductance can form parts of the resonant path. Therefore, these parasitic components, which are undesirable in hard-switched converter become useful components in ZVS ones. Figures 16.11 and 16.12 show the ZVS HB and FB circuits, respectively, together with the circuit waveforms.

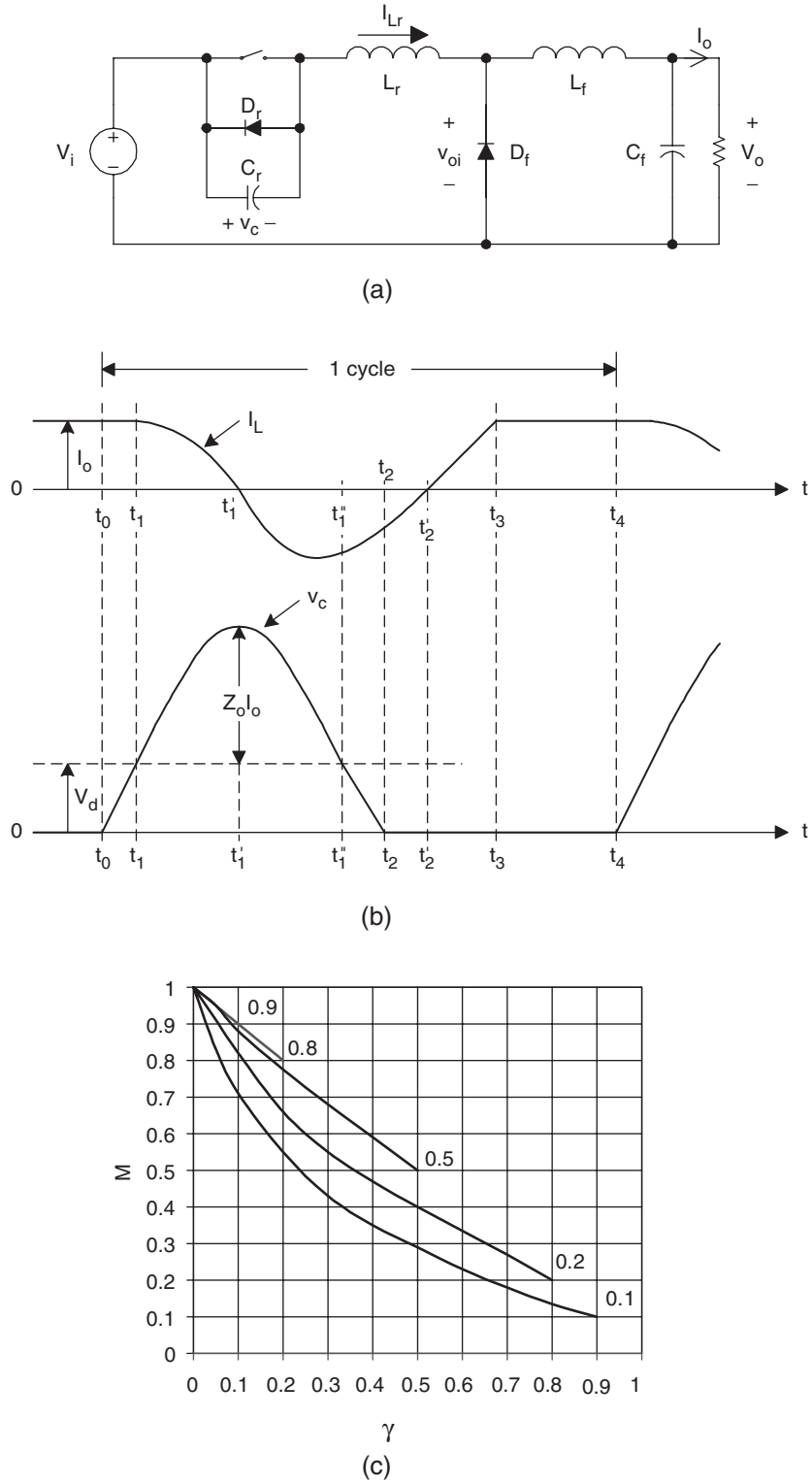


FIGURE 16.8 Half-wave, quasi-resonant buck converter with ZVS: (a) schematic diagram; (b) circuit waveforms; and (c) relationship between M and γ.

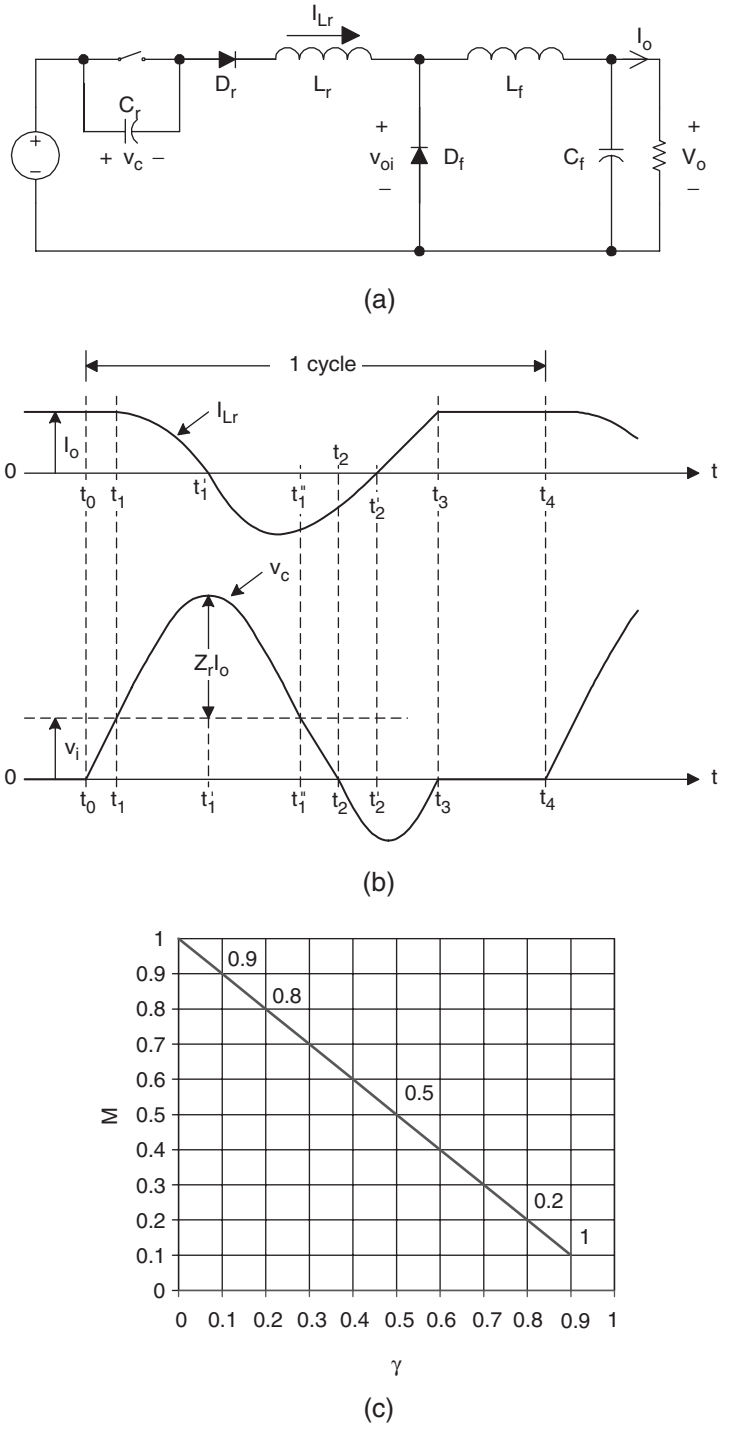


FIGURE 16.9 Full-wave, quasi-resonant buck converter with ZVS: (a) schematic diagram; (b) circuit waveforms; and (c) relationship between M and γ.

The resonant capacitor is equivalent to the parallel connection of the two capacitors ($C_r/2$) across the switches. The off-state voltage of the switches will not exceed the input voltage during resonance because they will be clamped to the supply rail by the anti-parallel diode of the switches.

16.5.2 Phase-shifted Converter with Zero Voltage Transition

In a conventional FB converter, the two diagonal switch pairs are driven alternatively. The output transformer is fed with an

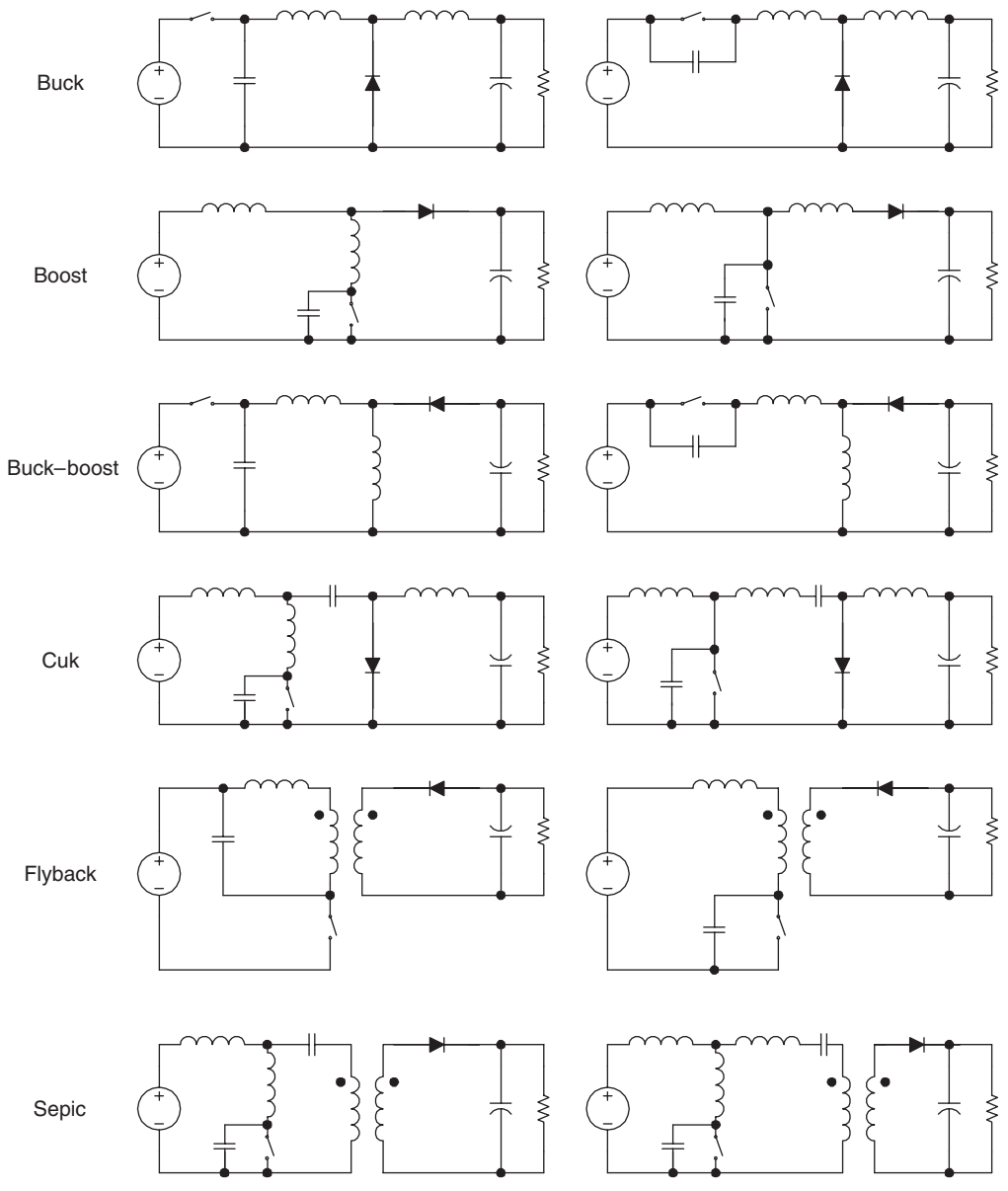


FIGURE 16.10 A family of quasi-resonant converter with ZVS.

ac rectangular voltage. By applying a phase-shifting approach, a deliberate delay can be introduced between the gate signals to the switches [18]. The circuit waveforms are shown in Fig. 16.13. Two upper or lower switches can be conducting (either through the switch or the anti-parallel diode), yet the applied voltage to the transformer is zero. This zero-voltage condition appears in the interval $[t_1, t_2]$ of V_{pri} in Fig. 16.13. This operating stage corresponds to the required off time for that particular switching cycle. When the desired switch is turned off, the primary transformer current flows into the switch output capacitance causing the switch voltage to resonate to the opposite input rail. Effects of the parasitic circuit components are used advantageously to facilitate the resonant transitions. This enables a ZVS condition for turning on the opposite switch. Thus, varying the phase shift controls the effective duty cycle and hence the output power. The resonant circuit is necessary to meet the requirement of providing sufficient inductive energy to drive the capacitors to the opposite bus rail. The resonant transition must be achieved within the designed transition time.

16.6 Multi-resonant Converters (MRC)

The ZCS- and ZVS-QRCs optimize the switching condition for either the active switch or the output diode only, but not

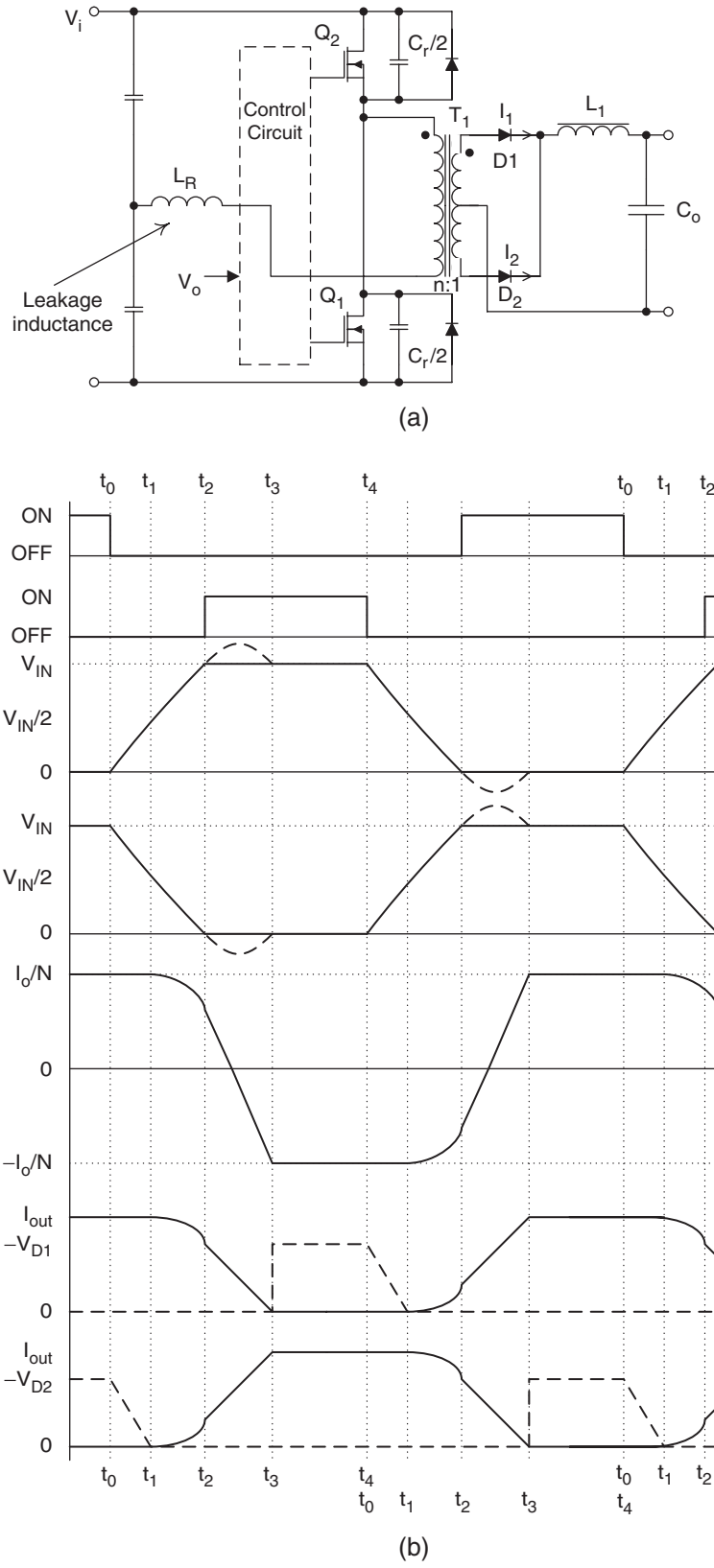


FIGURE 16.11 Half-bridge converter with ZVS: (a) circuit diagram and (b) circuit waveforms.

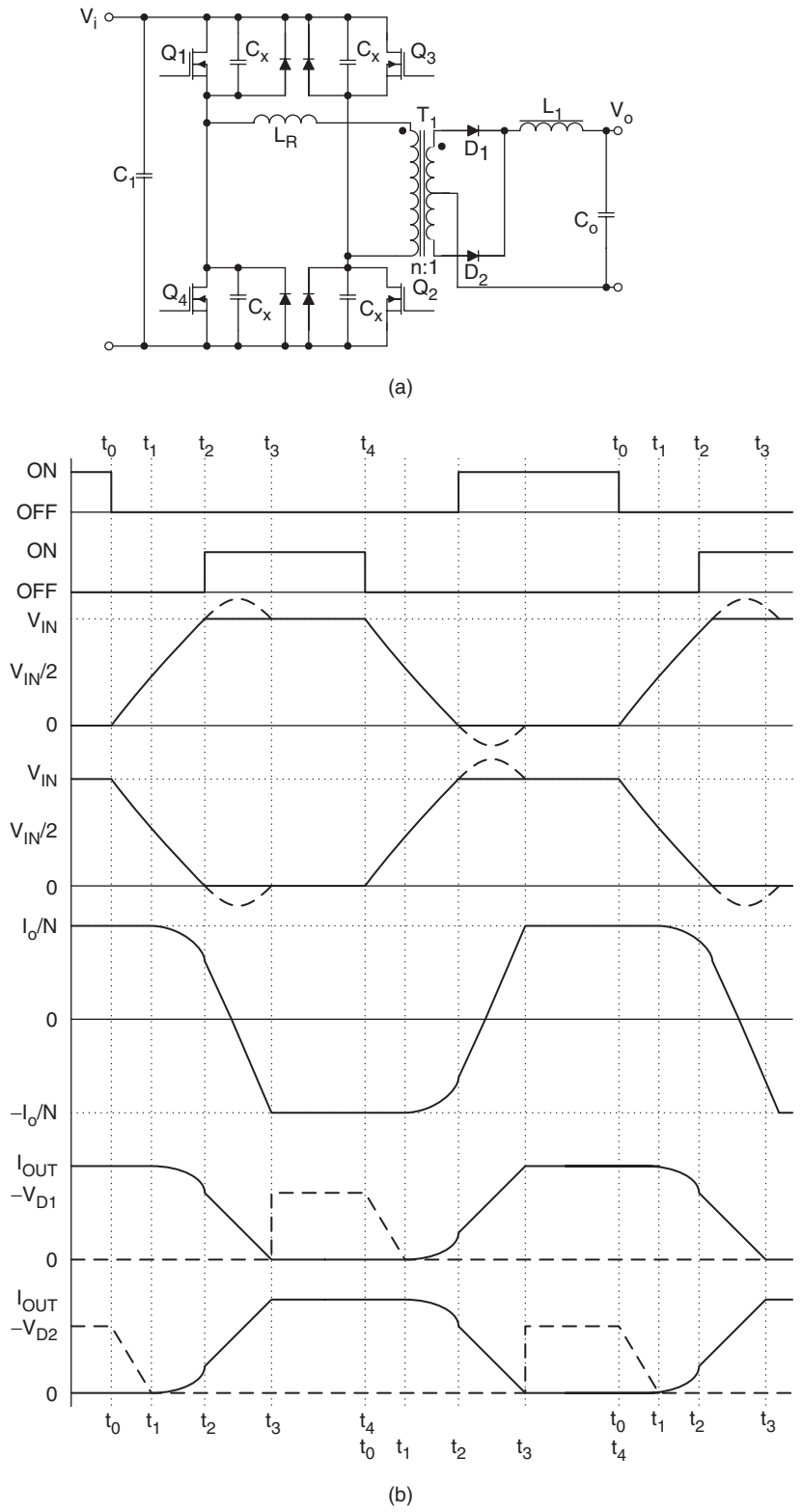


FIGURE 16.12 Full-bridge converter with ZVS: (a) circuit schematics and (b) circuit waveforms.

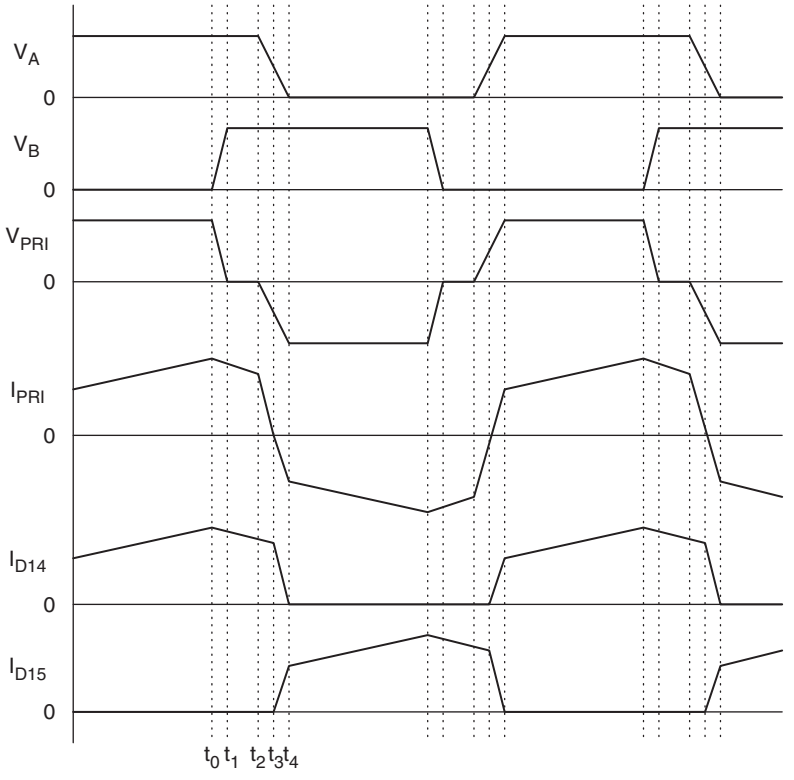


FIGURE 16.13 Circuit waveforms of the phase-shifted, ZVT FB converter.

for both of them simultaneously. Multi-resonant switch concept, which is an extension of the concept of the resonant switch, has been developed to overcome such limitation. The zero-current multi-resonant (ZC-MR) and zero-voltage multi-resonant (ZV-MR) switches [12, 17] are shown in Fig. 16.14.

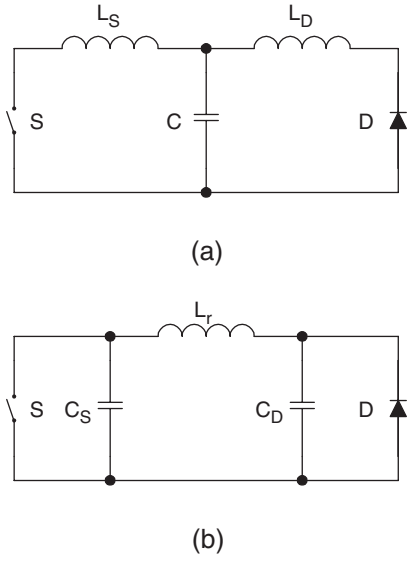


FIGURE 16.14 Multi-resonant switches: (a) ZC-MR switch and (b) ZV-MR switch.

The multi-resonant circuits incorporate all major parasitic components, including switch output capacitance, diode junction capacitance, and transformer leakage inductance into the resonant circuit. In general, ZVS (*half-wave* mode) is more favorable than ZCS in DC–DC converters for high-frequency operation because the parasitic capacitance of the active switch and the diode will form a part of the resonant circuit.

An example of a buck ZVS-MRC is shown in Fig. 16.15. Depending on the ratio of the resonant capacitance C_D/C_S, two possible topological modes, namely mode I and mode II, can be operated [19]. The ratio affects the time at which the voltages across the switch S and the output diode D_f become zero. Their waveforms are shown in Figs. 16.16a and b, respectively. If diode voltage V_D falls to zero earlier than the switch

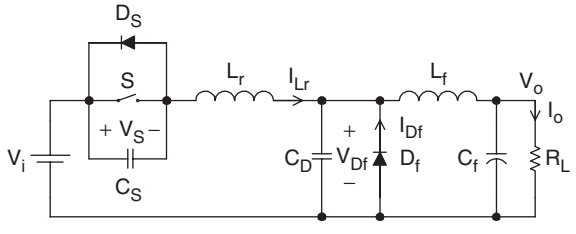


FIGURE 16.15 Buck ZVS-MRC.

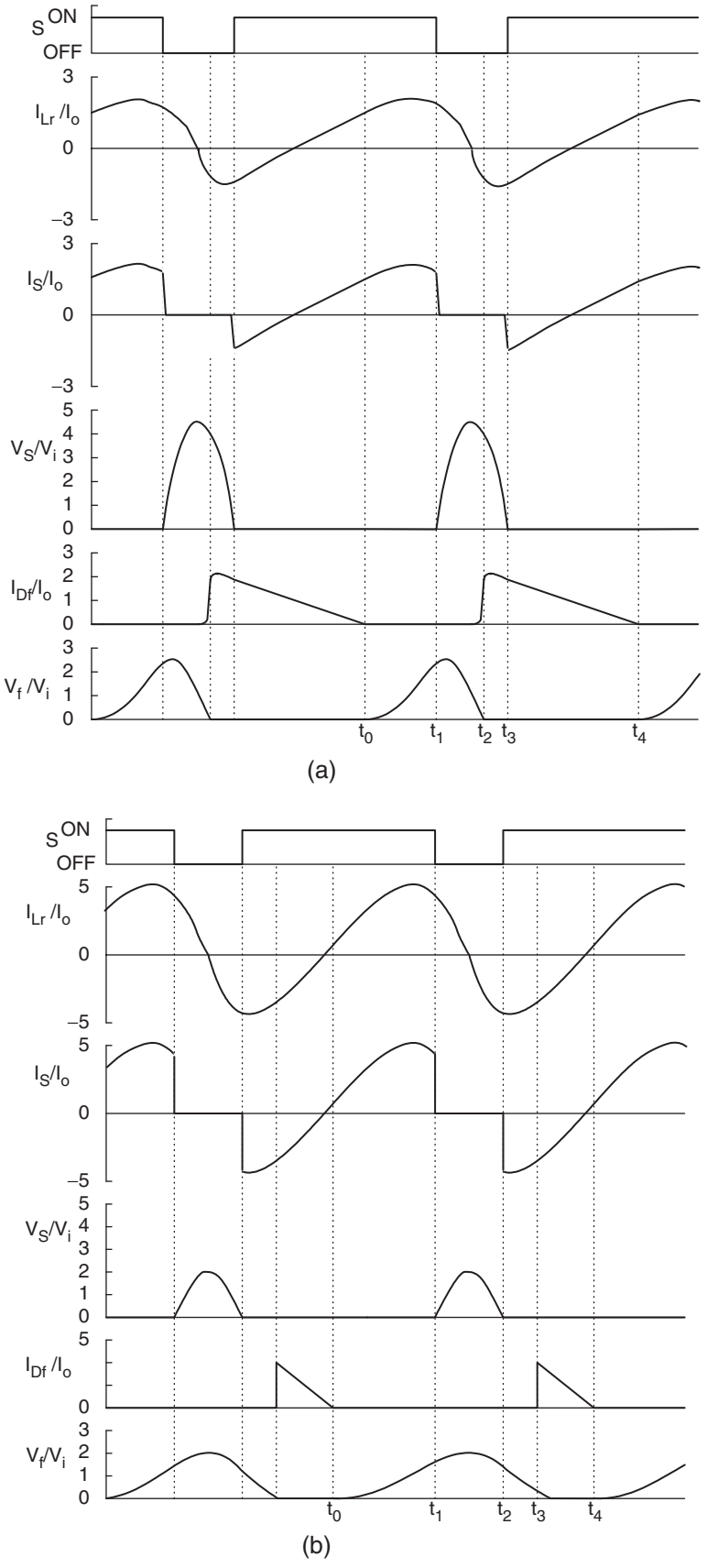


FIGURE 16.16 Possible modes of the buck ZVS-MRC: (a) mode I and (b) mode II.

voltage V_S, the converter will follow mode I. Otherwise, the converter will follow mode II.

Instead of having one resonant stage, there are three in this converter. The mode I operation in Fig. 16.16a is described first. Before the switch S is turned on, the output diode D_f is conducting and the resonant inductor current I_{Lr} is negative (flowing through the anti-parallel diode of S). S is then turned on with ZVS. The resonant inductor current I_{Lr} increases linearly and D_f is still conducting. When I_{Lr} reaches the output current I_o, the first resonant stage starts. The resonant circuit is formed by the resonant inductor L_r and the capacitor C_D across the output diode. This stage ends when S is turned off with ZVS. Then, a second resonant stage starts. The resonant circuit consists of L_r, C_D, and the capacitor across the switch C_s. This stage ends when the output diode becomes forward biased. A third resonant stage will then start. L_r and C_s form the resonant circuit. This stage ends and completes one operation cycle when the diode C_s becomes forward biased.

The only difference between mode I and mode II in Fig. 16.16b is in the third resonant stage, in which the resonant circuit is formed by L_r and C_D. This stage ends when D_f becomes forward biased. The concept of the multi-resonant switch can be applied to conventional converters [19–21]. A family of MRCs are shown in Fig. 16.17.

Although the variation of the switching frequency for regulation in MRCs is smaller than that of QRCs, a wide-band frequency modulation is still required. Hence, the optimal design of magnetic components and the EMI filters in MRCs is not easy. It would be desirable to have a constant switching frequency operation. In order to operate the MRCs with constant switching frequency, the diode in Fig. 16.14 can be replaced with an active switch S_2 [22]. A constant-frequency multi-resonant (CF-MR) switch is shown in Fig. 16.18. The output voltage is regulated by controlling the on-time of the two switches. This concept can be illustrated with the buck converter as shown in Fig. 16.19, together with the gate drive waveforms and operating stages. S_1 and S_2 are turned on during the time when currents flow through the anti-parallel diodes of S_1 and S_2. This stage ends when S_2 is turned off with ZVS. The first resonant stage is then started. L_r and C_{S2} form the resonant circuit. A second resonant stage begins. L_r resonates with C_{S1} and C_{S2}. The voltage across S_1 oscillates to zero. When I_{Lr} becomes negative, S_1 will be turned on with ZVS. Then, L_r resonates with C_{S2}. S_2 will be turned on when current flows through D_{S2}. As the output voltage is the average voltage across S_2, output voltage regulation is achieved by controlling the conduction time of S_2.

All switches in MRCs operate with ZVS, which reduces the switching losses and switching noise and eliminates the oscillation due to the parasitic effects of the components (such as the junction capacitance of the diodes). However, all switches are under high current and voltage stresses, resulting in an increase in the conduction loss.

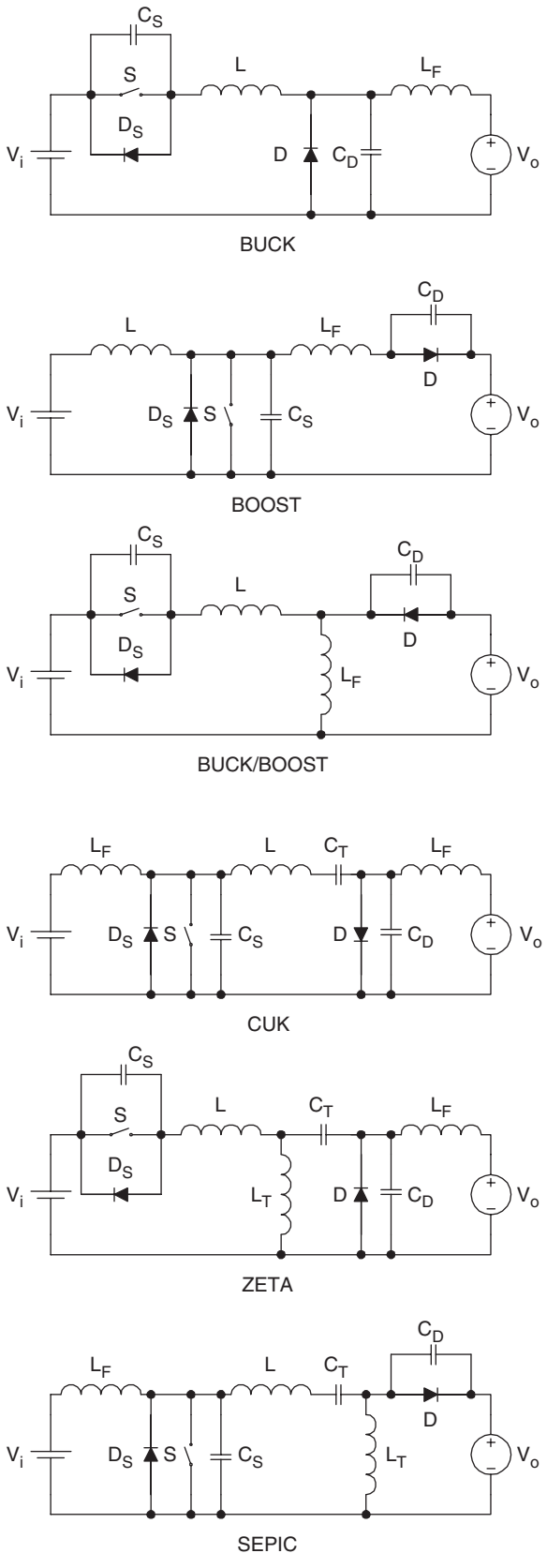


FIGURE 16.17 Use of the multi-resonant switch in conventional PWM converters.

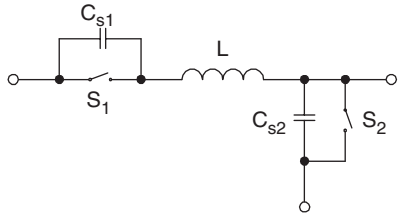


FIGURE 16.18 Constant frequency multi-resonant switch.

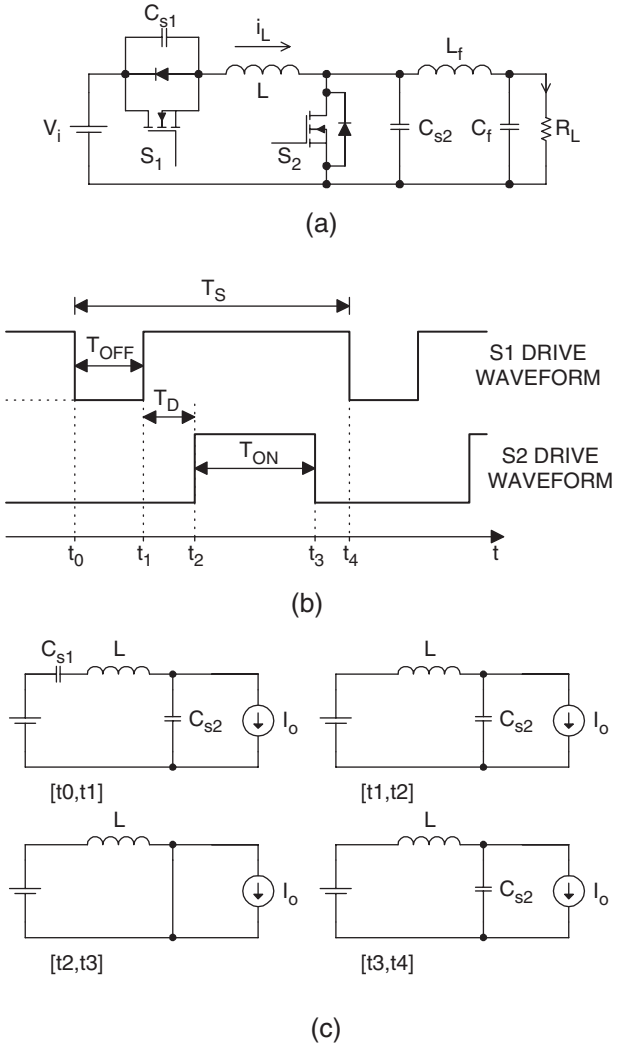


FIGURE 16.19 Constant frequency buck MRC: (a) circuit schematics; (b) gate drive waveforms; and (c) operating stages.

16.7 Zero-voltage-transition (ZVT) Converters

By introducing a resonant circuit in parallel with the switches, the converter can achieve ZVS for both power switch and diode without significantly increasing their voltage and current stresses [23]. Figure 16.20a shows a buck type ZVT-PWM converter and Fig. 16.20b shows the associated waveforms. The converter consists of a main switch S and an auxiliary switch S_1. It can be seen that the voltage and current waveforms of the switches are square-wave-like except during turn-on and turn-off switching intervals, where ZVT takes place. The main switch and the output diode are under ZVS and are subjected to low voltage and current stresses. The auxiliary switch is under ZCS, resulting in low switching loss.

The concept of ZVT can be extended to other PWM circuits by adding the resonant circuit. Some basic ZVT-PWM converters are shown in Fig. 16.21.

16.8 Non-dissipative Active Clamp Network

The active-clamp circuit can utilize the transformer leakage inductance energy and can minimize the the turn-off voltage stress in the isolated converters. The active clamp circuit provides a means of achieving ZVS for the power switch and reducing the rate of change of the diode's reverse recovery current. An example of a flyback converter with active clamp is shown in Fig. 16.22a and the circuit waveforms are shown in Fig. 16.22b. Clamping action is obtained by using a series combination of an active switch (i.e. S_2) and a large capacitor so that the voltage across the main switch (i.e. S_1) is clamped to a minimum value. S_2 is turned on with ZVS. However, S_2 is turned off with finite voltage and current, and has turn-off switching loss. The clamp-mode ZVS-MRCs is discussed in [24–26].

16.9 Load Resonant Converters

Load resonant converters (LRCs) have many distinct features over conventional power converters. Due to the soft commutation of the switches, no turn-off loss or stress is present. LRCs are specially suitable for high-power applications because they allow high-frequency operation for equipment size/weight reduction, without sacrificing the conversion efficiency and imposing extra stress on the switches. Basically, LRCs can be divided into three different configurations, namely series resonant converters, parallel resonant converters, and series–parallel resonant converters.

16.9.1 Series Resonant Converters

Series resonant converters (SRCs) have their load connected in series with the resonant tank circuit, which is formed by L_r and C_r [15, 27–29]. The half-bridge configuration is shown in Fig. 16.23. When the resonant inductor current i_{Lr} is positive, it flows through T_1 if T_1 is on; otherwise it flows through the diode D_2. When i_{Lr} is negative, it flows through T_2 if T_2 is on;

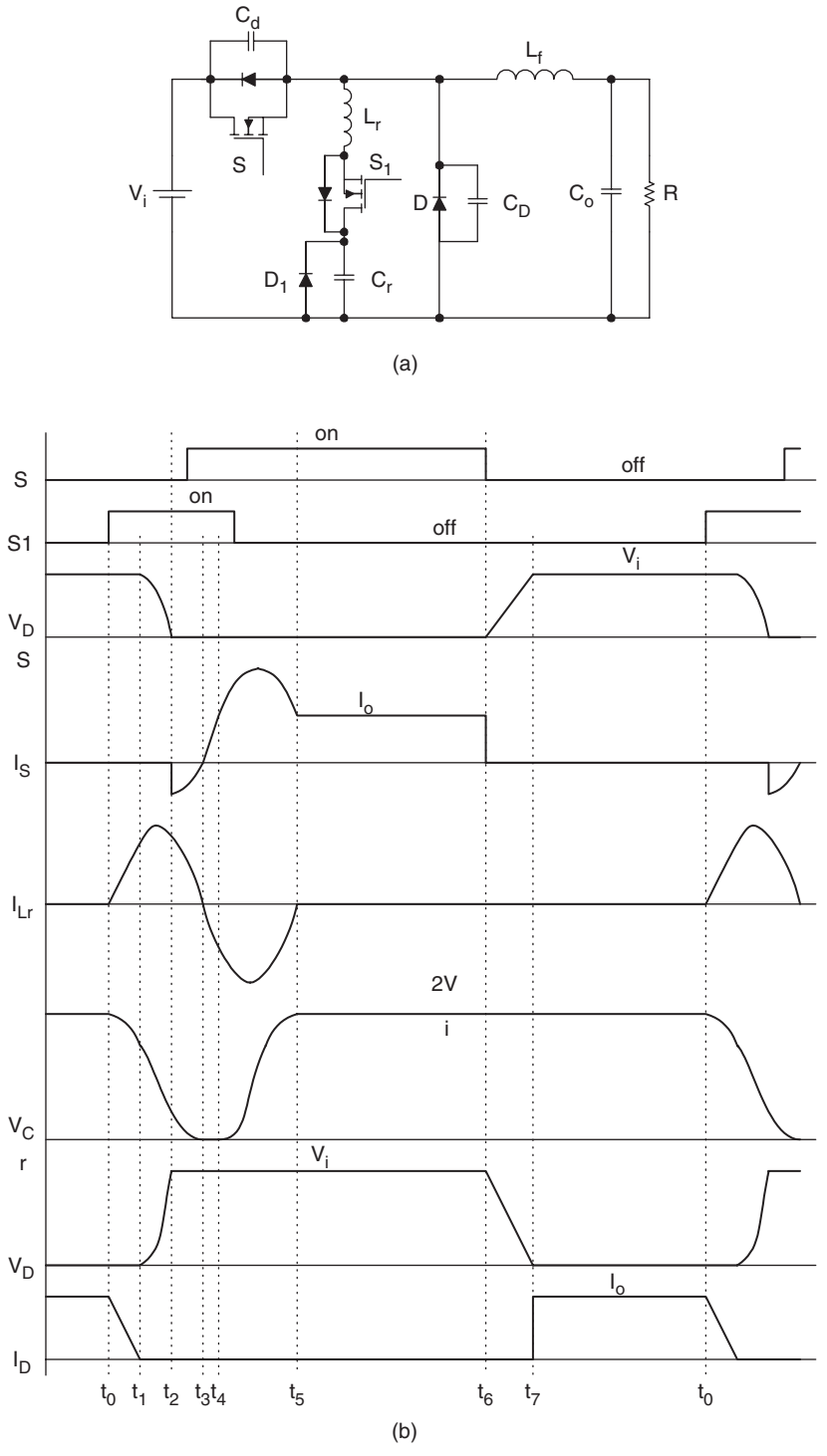


FIGURE 16.20 Buck ZVT-PWM converter: (a) circuit schematics and (b) waveforms.

otherwise it flows through the diode D_1. In the steady-state symmetrical operation, both the active switches are operated in a complementary manner. Depending on the ratio between the switching frequency ω_S and the converter resonant frequency ω_r, the converter has several possible operating modes.

A. Discontinuous Conduction Mode (DCM) with $\omega_S < 0.5\omega_r$

Figure 16.24a shows the waveforms of i_{Lr} and the resonant capacitor voltage v_{Cr} in this mode of operation. From 0 to t_1, T_1 conducts. From t_1 to t_2, the current in T_1reverses its direction. The current flows through D_1 and back to the

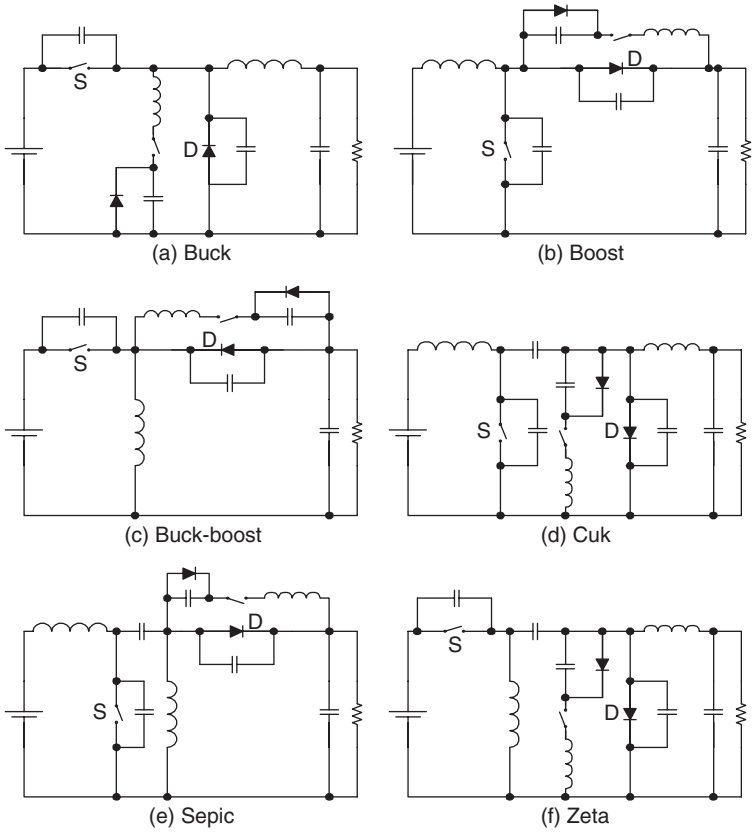


FIGURE 16.21 Conventional ZVT-PWM converters.

supply source. From t_2 to t_3, all switches are in the off state. From t_3 to t_4, T_2 conducts. From t_4 to t_5, the current in T_2 reverses its direction. The current flows through D_2 and back to the supply source. T_1 and T_2 are switched on under ZCS condition and they are switched off under zero-current and zero-voltage conditions. However, the switches are under high current stress in this mode of operation and thus have higher conduction loss.

B. Continuous Conduction Mode (CCM) with $0.5\omega_r < \omega_S < \omega_r$

Figure 16.24b shows the circuit waveforms. From 0 to t_1, i_{Lr} transfers from D_2 to T_1. T_1 is switched on with finite switch current and voltage, resulting in turn-on switching loss. Moreover, the diodes must have good reverse recovery characteristics in order to reduce the reverse recovery current. From t_1 to t_2, D_1 conducts and T_1 is turned off softly with zero voltage and zero current. From t_2 to t_3, T_2 is switched on with finite switch current and voltage. At t_3, T_2 is turned off softly and D_2 conducts until t_4.

C. Continuous Conduction Mode (CCM) with $\omega_r < \omega_S$

Figure 16.24c shows the circuit waveforms. From 0 to t_1, i_{Lr} transfers from D_1 to T_1. Thus, T_1 is switched on with zero current and zero voltage. At t_1, T_1 is switched off with finite voltage and current, resulting in turn-off switching loss. From t_1 to t_2, D_2 conducts. From t_2 to t_3, T_2 is switched on with zero current and zero voltage. At t_3, T_2 is switched off. i_{Lr} transfers from T_2 to D_1. As the switches are turned on with ZVS, lossless snubber capacitors can be added across the switches.

The following parameters are defined: voltage conversion ratio M, characteristic impedance Z_r, resonant frequency f_r, normalized load resistance r, normalized switching frequency γ.

$$M = nV_o/V_{in} \tag{16.2a}$$

$$Z_r = \sqrt{L_r/C_r} \tag{16.2b}$$

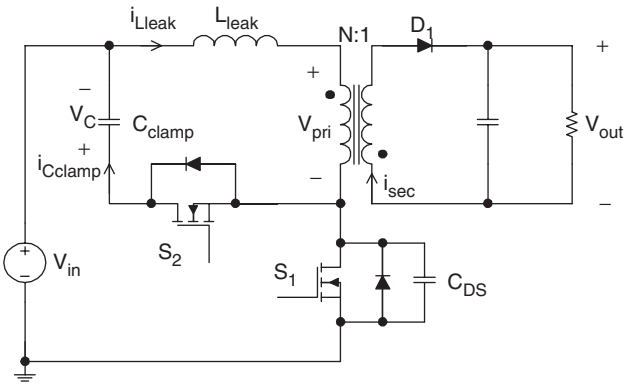
$$f_r = 1/\left(2\pi\sqrt{L_r C_r}\right) \tag{16.2c}$$

$$r = n^2 R_L/Z_r \tag{16.2d}$$

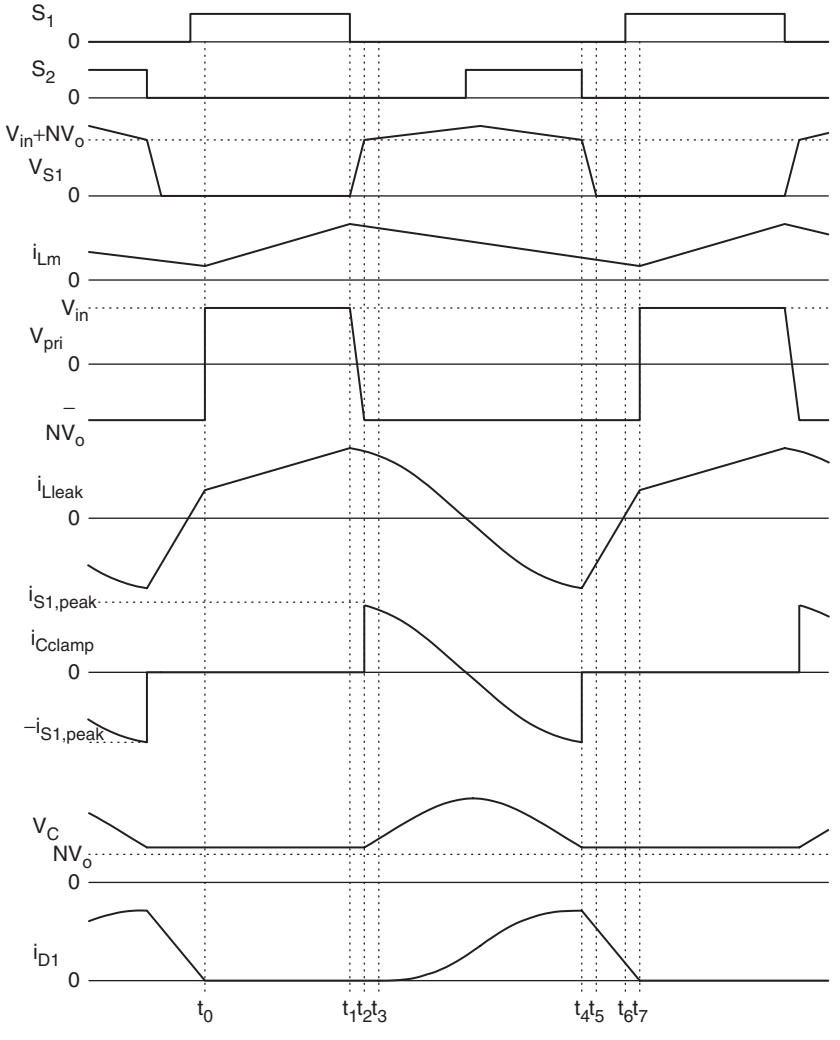
$$\gamma = f_s/f_r \tag{16.2e}$$

$$M = 1\Big/\sqrt{(\gamma - 1/\gamma)^2/(r^2+1)} \tag{16.2f}$$

The relationships between M and γ for different value of r are shown in Fig. 16.25. The boundary between CCM and DCM



(a)



(b)

FIGURE 16.22 Active-clamp flyback converter: (a) circuit schematics and (b) circuit waveforms.

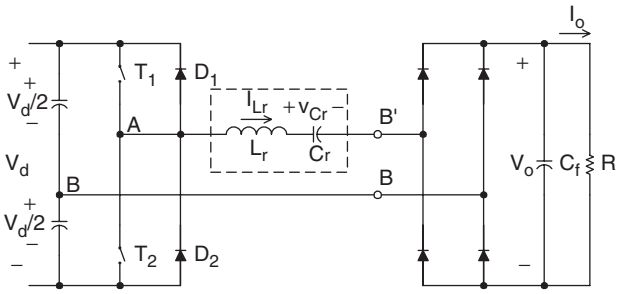


FIGURE 16.23 SRC half-bridge configuration.

is at $r = 1.27\gamma$. When the converter is operating in DCM and $0.2 < \gamma < 0.5$, $M = 1.27\ r\gamma$.

The SRC has the following advantages. Transformer saturation can be avoided since the series capacitor can block the dc component. The light load efficiency is high because the device current and conduction loss are low. However, the major disadvantages are that there is difficulty in regulating the output voltage under light load and no load conditions. Moreover, the output dc filter capacitor has to carry high ripple current, which could be a major problem in low-output voltage and high-output current applications [29].

16.9.2 Parallel Resonant Converters

Parallel resonant converters (PRCs) have their load connected in parallel with the resonant tank capacitor C_r [27–30]. The half-bridge configuration is shown in Fig. 16.26. SRC behaves as a current source, whereas the PRC acts as a voltage source. For voltage regulation, PRC requires a smaller operating frequency range than the SRC to compensate for load variation.

A. Discontinuous Conduction Mode (DCM)

The steady-state waveforms of the resonant inductor current i_{Lr} and the resonant capacitor voltage v_{Cr} are shown in Fig. 16.27a. Initially both i_{Lr} and v_{Cr} are zero. From 0 to t_2, T_1 conducts and is turned on with zero current. When i_{Lr} is less than the output current I_o, i_{Lr} increases linearly from 0 to t_1 and the output current circulates through the diode bridge. From t_1 to t_3, L_r resonates with C_r. Starting from t_2, i_{Lr} reverses its direction and flows through D_1. T_1 is then turned off with zero current and zero voltage. From t_3 to t_4, v_{Cr} decreases linearly due to the relatively constant value of I_o. At t_4, when v_{Cr} equals zero, the output current circulates through the diode bridge again. Both i_{Lr} and v_{Cr} will stay at zero for an interval. From t_5 to t_9, the above operations will be repeated for T_2 and D_2. The output voltage is controlled by adjusting the time interval of $[t_4, t_5]$.

B. Continuous Conduction Mode $\omega_S < \omega_r$

This mode is similar to the operation in the DCM, but with a higher switching frequency. Both i_{Lr} and v_{Cr} become continuous. The waveforms are shown in Fig. 16.27b. The switches T_1 and T_2 are hard turned on with finite voltage and current and are soft turned off with ZVS.

C. Continuous Conduction Mode $\omega_S > \omega_r$

If the switching frequency is higher than ω_r (Fig. 16.27c), the anti-parallel diode of the switch will be turned on before the switch is triggered. Thus, the switches are turned on with ZVS. However, the switches are hard turned off with finite current and voltage.

The parameters defined in Eq. (16.2) are applicable. The relationships between M and γ for various values of r are shown in Fig. 16.28. During the DCM (i.e. $\gamma < 0.5$), M is in linear relationship with γ. Output voltage regulation can be achieved easily. The output voltage is independent on the output current. The converter shows a good voltage source characteristics. It is also possible to step up and step down the input voltage.

The PRC has the advantages that the load can be short-circuited and the circuit is suitable for low-output voltage, high-output current applications. However, the major disadvantage of the PRC is the high device current. Moreover, since the device current do not decrease with the load, the efficiency drops with a decrease in the load [29].

16.9.3 Series–Parallel Resonant Converter

Series–Parallel Resonant Converter (SPRC) combines the advantages of the SRC and PRC. The SPRC has an additional capacitor or inductor connected in the resonant tank circuit [29–31]. Figure 16.29a shows an LCC-type SPRC, in which an additional capacitor is placed in series with the resonant inductor. Figure 16.29b shows an LLC-type SPRC, in which an additional inductor is connected in parallel with the resonant capacitor in the SRC. However, there are many possible combinations of the resonant tank circuit. Detailed analysis can be found in [31].

16.10 Control Circuits for Resonant Converters

Since the 1985s, various control integrated circuits (ICs) for resonant converters have been developed. Some common ICs for different converters are described in this section.

16.10.1 QRCs and MRCs

Output regulations in many resonant-type converters, such as QRCs and MRCs, are achieved by controlling the

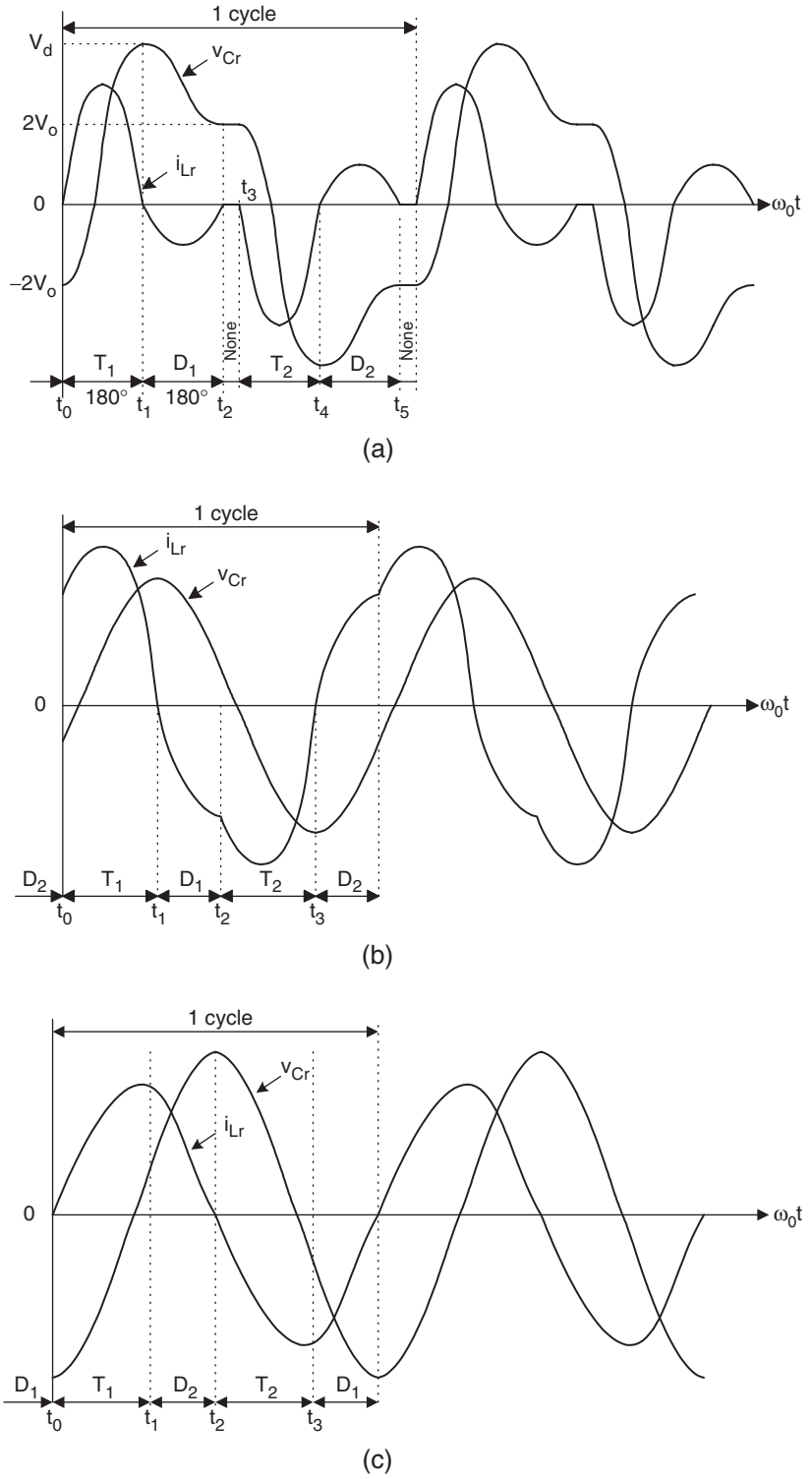


FIGURE 16.24 Circuit waveforms under different operating conditions: (a) $\omega_S < 0.5\ \omega_r$; (b) $0.5\ \omega_r < \omega_S < \omega$; and (c) $\omega_r < \omega_S$.

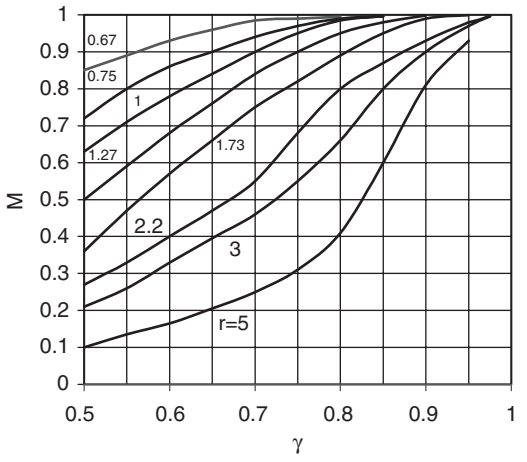


FIGURE 16.25 M vs γ in SRC.

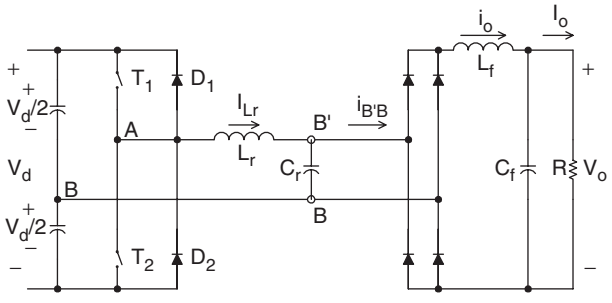


FIGURE 16.26 PRC half-bridge configuration.

switching frequency. ZCS applications require controlled switch-on times while ZVS applications require controlled switch-off times. The fundamental control blocks in the IC include an error amplifier, voltage controlled oscillator (VCO), one shot generator with a zero wave-crossing detection comparator, and an output stage to drive the active switch. Typical ICs include UC1861–UC1864 for ZVS applications and UC 1865–UC 1868 for ZCS applications [32]. Figure 16.30 shows the controller block diagram of UC 1864.

The maximum and minimum switching frequencies (i.e. f_{max} and f_{min}) are controlled by the resistors R_{ange} and R_{min} and the capacitor C_{vco}. f_{max} and f_{min} can be expressed as

$$f_{max} = \frac{3.6}{(R_{ange}//R_{min})C_{VCO}} \quad \text{and} \quad f_{min} = \frac{3.6}{R_{min}C_{VCO}} \tag{16.3}$$

The frequency range Δf is then equal to

$$\Delta f = f_{max} - f_{min} = \frac{3.6}{R_{ange}C_{VCO}} \tag{16.4}$$

The frequency range of the ICs is from 10 kHz to 1 MHz. The output frequency of the oscillator is controlled by the error amplifier (E/A) output. An example of a ZVS-MR forward converter is shown in Fig. 16.31.

16.10.2 Phase-shifted, ZVT FB Circuit

The UCC3895 is a phase shift PWM controller that can generate a phase shifting pattern of one half-bridge with respect to the other. The application diagram is shown in Fig. 16.32.

The four outputs "OUTA," "OUTB," "OUTC," and "OUTD" are used to drive the MOSFETs in the full-bridge. The dead time between "OUTA" and "OUTB" is controlled by "DELAB" and the dead time between "OUTC" and "OUTD" is controlled by "DELCD." Separate delays are provided for the two half-bridges to accommodate differences in resonant capacitor charging currents. The delay in each set is approximated by

$$t_{DELAY} = \frac{25 \times 10^{-12} R_{DEL}}{0.75(V_{CS} - V_{ADS}) + 0.5} + 25\ ns \tag{16.5}$$

where R_{DEL} is the resistor value connected between "DELAB" or "DELCD" to ground.

The oscillator period is determined by R_T and C_T. It is defined as

$$t_{OSC} = \frac{5R_T C_T}{48} + 120\ ns \tag{16.6}$$

The maximum operating frequency is 1 MHz. The phase shift between the two sets of signals is controlled by the ramp voltage and the error amplifier output having a 7 MHz bandwidth.

16.11 Extended-period Quasi-resonant (EP-QR) Converters

Generally, resonant and quasi-resonant converters operate with frequency control. The extended-period quasi-resonant converters proposed by Barbi [33] offer a simple solution to modify existing hard-switched converters into soft-switched ones with constant frequency operation. This makes both output filter design and control simple. Figure 16.33 shows a standard hard-switched boost type PFC converter. In this hard-switched circuit, the main switch SW1 could be subject to significant switching stress because the reverse recovery current of the diode D_F could be excessive when SW1 is turned on. In practice, a small saturable inductor may be added in series with the power diode D_F in order to reduce the di/dt of the reverse-recovery current. In addition, an optional R–C snubber may be added across SW1 to reduce the dv/dt of SW1. These extra reactance components can in fact be used in the EP-QR circuit to achieve soft switching, as shown in Fig. 16.34. The resonant components L_r and C_r are of small

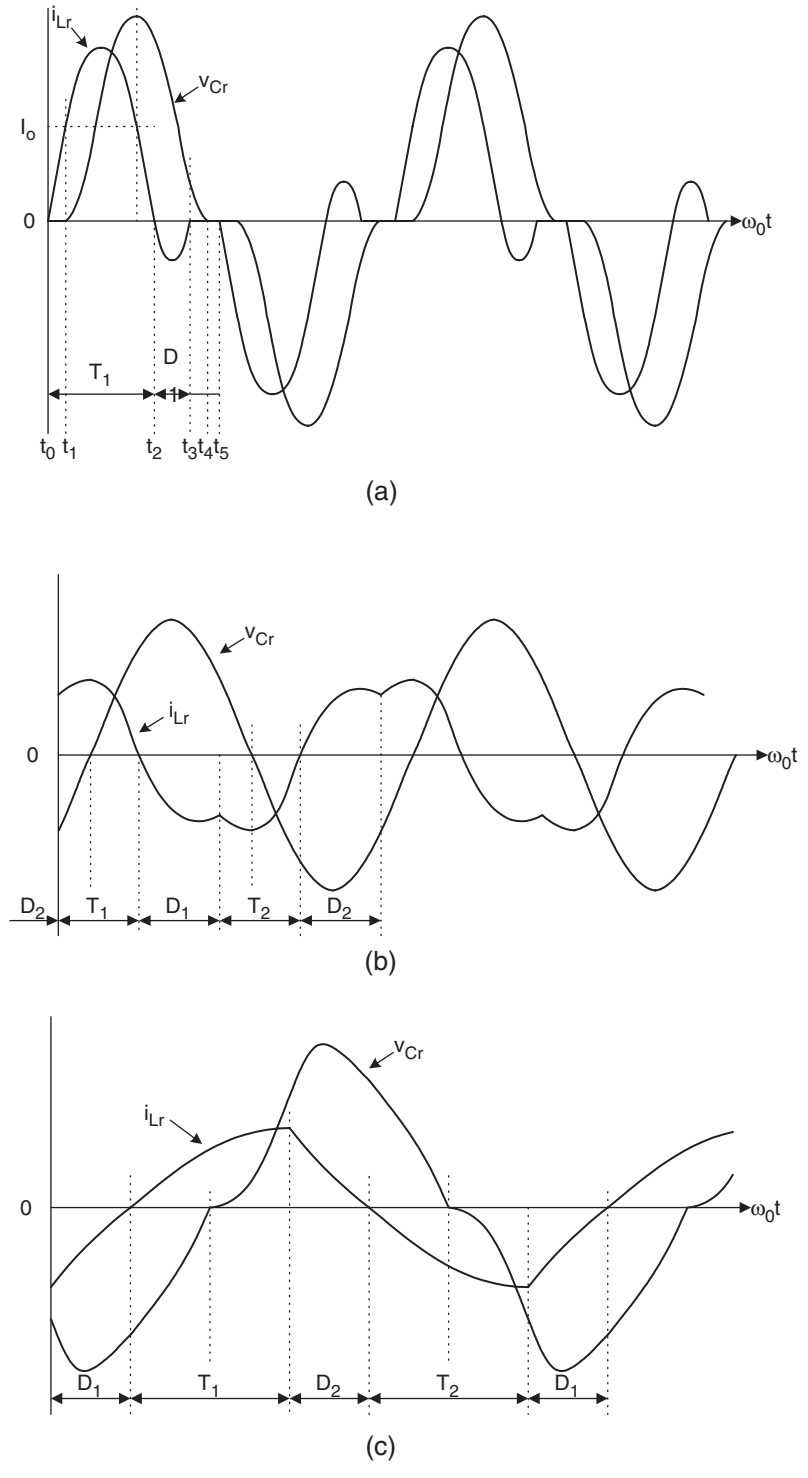


FIGURE 16.27 Circuit waveforms under different operating conditions: (a) discontinuous conduction mode; (b) continuous conduction mode $\omega_S < \omega_r$; and (c) continuous conduction mode $\omega_S > \omega_r$.

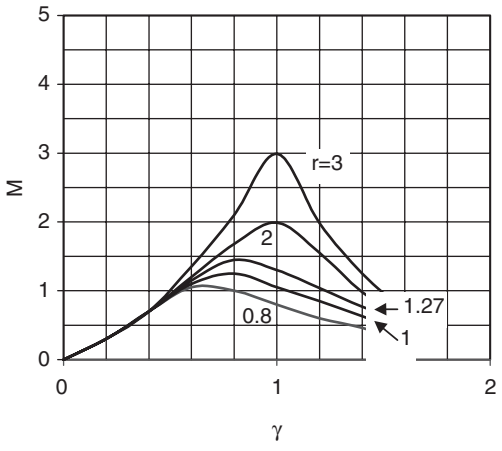


FIGURE 16.28 M vs γ in PRC.

values and can come from the snubber circuits of a standard hard-switched converter. Thus, the only additional component is the auxiliary switch Q2. The small resonant inductor is put in series with the main switch SW1 so that SW1 can be switched on under ZC condition and the *di*/*dt* problem of the reverse-recovery current be eliminated. The resonant capacitor C_r is used to store energy for creating condition for soft switching. Q2 is used to control the resonance during the main switch transition. It should be noted that all power devices including SW1, Q1 and main power diode D_F are turned on and off under ZV and/or ZC conditions. Therefore, the large *di*/*dt* problem due to the reverse recovery of the power diode can be eliminated. The soft-switching method is an effective technique for EMI suppression.

Together with power factor correction technique, soft-switching converters offer a complete solution to meet EMI regulations for both conducted and radiated EMI. The operation of the EP-QR boost PFC circuit [34, 35] can be described in six modes as shown in Fig. 16.35. The corresponding idealized waveforms are included in Fig. 16.36.

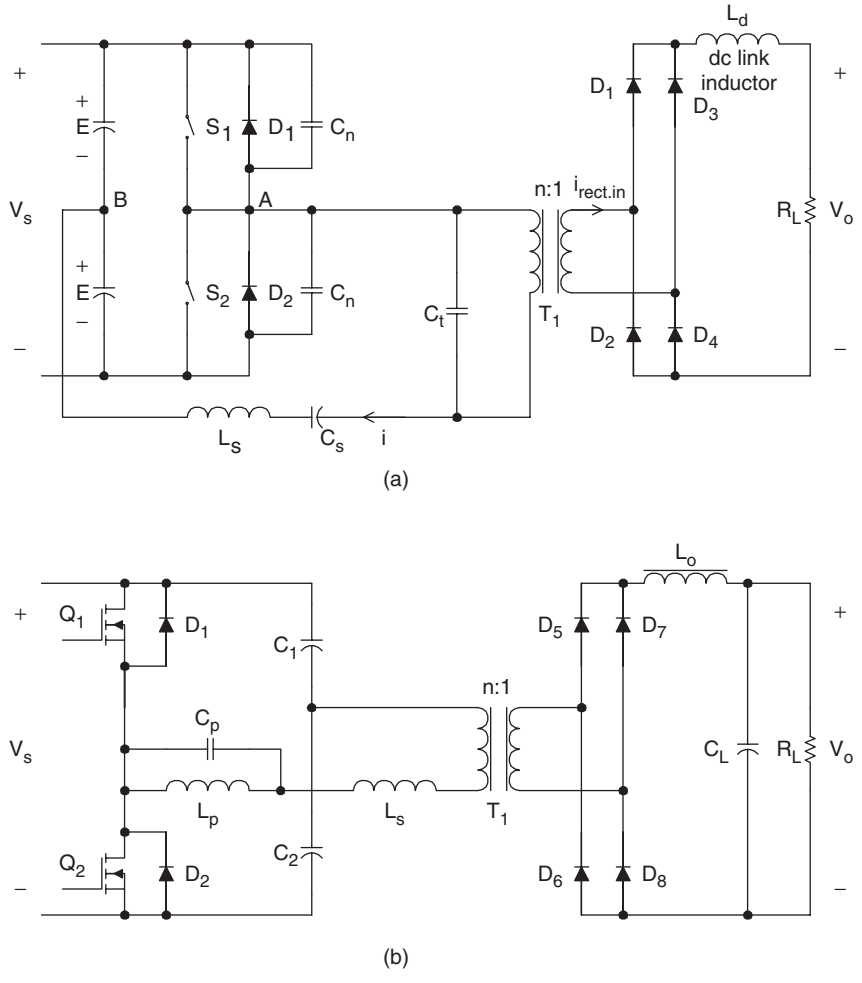


FIGURE 16.29 Different types of SPRC: (a) LCC-type and (b) LLC-type.

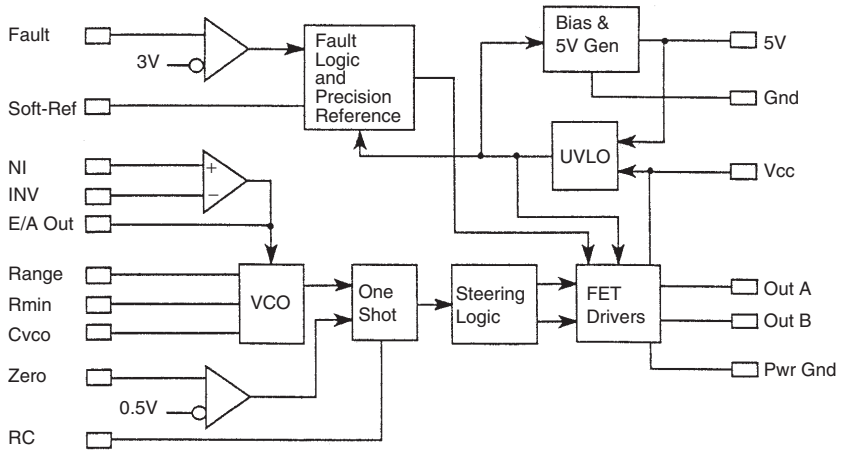


FIGURE 16.30 Controller block diagram of UC1864 (Courtesy of Unitrode Corp. and Texas Instruments).

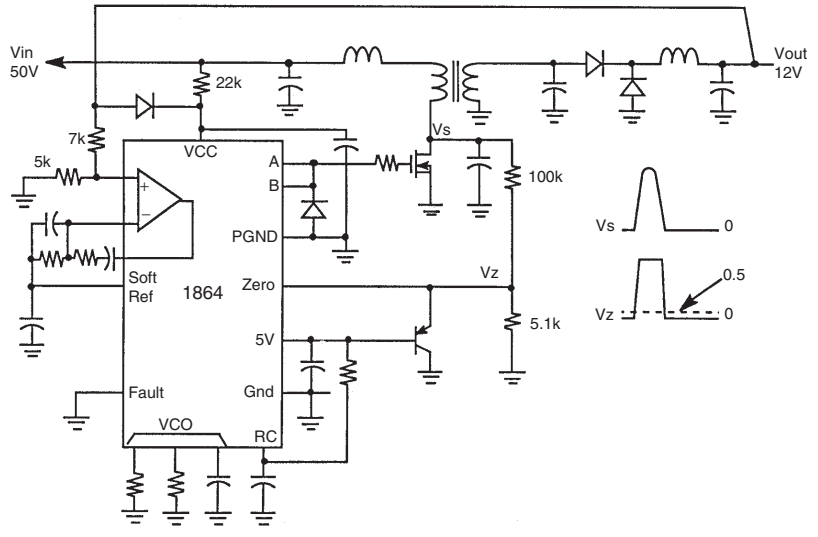


FIGURE 16.31 ZV-MR forward converter (Courtesy of Unitrode Corp. and Texas Instruments).

A. Circuit Operation

Interval I: (t_0–t_1) Due to the resonant inductor L_r which limits the di/dt of the switch current, switch SW1 is turned on at zero-current condition with a positive gating signal V_{GS1} to start a switching cycle at $t = t_0$. Current in D_F is diverted to inductor L_r. Because D_F is still conducting during this short period, D_{S2} is still reverse biased and is thus not conducting. The equivalent circuit topology for the conducting paths is shown in Fig. 16.35a. Resonant switch Q_2 remains off in this interval.

Interval II: (t_1–t_a) When D_F regains its blocking state, D_{S2} becomes forward biased. The first half of the resonance cycle occurs and resonant capacitor C_r starts to discharge and current flows in the loop C_r–Q_2–L_r–SW_1. The resonance half-cycle stops at time $t = t_a$ because D_{S2} prevents the loop current i_{Cr} from flowing in the opposition direction. The voltage across C_r is reversed at the end of this interval. The equivalent circuit is shown in Fig. 16.35b.

Interval III: (t_a–t_b) Between t_a and t_b, current in L_F and L_r continues to build up. This interval is the extended-period for the resonance during which energy is pumped into L_r. The corresponding equivalent circuit is showed in Fig. 16.35c.

Interval IV: (t_b–t_2) Figure 16.35d shows the equivalent circuit for this operating mode. Before SW_1 is turned off, the second half of the resonant cycle needs to take place in order that a zero-voltage condition can be created for the turn-off process of SW_1. The second half of the resonant cycle starts when auxiliary switch Q_2 is turned on at $t = t_b$. Resonant current then flows through the loop L_r–Q_2–C_r-anti-parallel diode

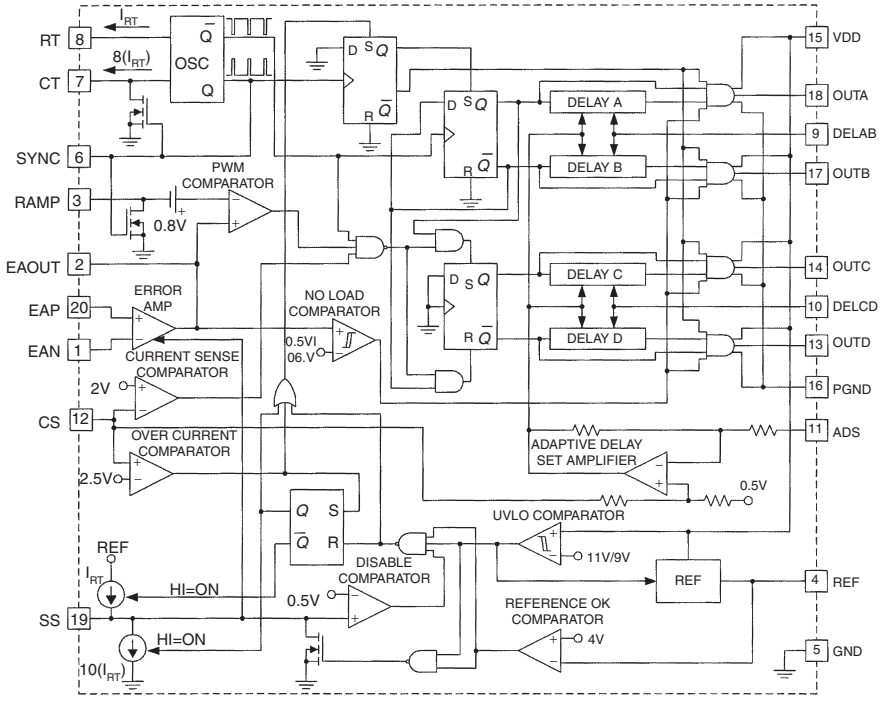


FIGURE 16.32 Application diagram of UCC3895 (Courtesy of Unitrode Corp. and Texas Instruments).

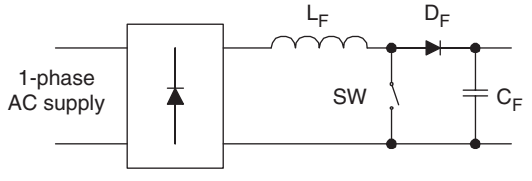


FIGURE 16.33 Boost-type AC–DC power factor correction circuit.

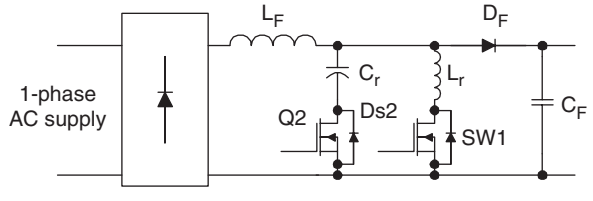


FIGURE 16.34 EP-QR boost-type AC–DC power factor correction circuit.

of SW_1. This current is limited by L_r and thus Q_2 is turned on under zero-current condition. Since the anti-parallel diode of SW_1 is conducting, the voltage across SW_1 is clamped to the on-state voltage of the anti-parallel diode. SW_1 can therefore be turned off at (near) zero-voltage condition before $t = t_2$ at which the second half of the resonant cycle ends.

Interval V: (t_2–t_3) During this interval, the voltage across C_r is less than the output voltage V_o. Therefore D_F is still reverse biased. Inductor current I_s flows into C_r until V_{Cr} reaches V_o at $t = t_3$. The equivalent circuit is represented in Fig. 16.35e.

Interval VI: (t_3–t_4) During this period, the resonant circuit is not in action and the inductor current I_s charges the output capacitor C_F via D_F, as in the case of a classical boost-type PFC circuit. C_r is charged to V_o, therefore Q_2 can be turned off at zero-voltage and zero-current conditions. Figure 16.35f shows the equivalent topology of this operating mode.

In summary, SW1, Q2, and D_F are fully soft-switched. Since the two resonance half-cycles take place within a closed loop outside the main inductor, the high resonant pulse will not occur in the inductor current, thus making a well-established averaged current mode control technique applicable for such QR circuit. For full soft-switching in the turn-off process, the resonant components need to be designed so that the peak resonant current exceeds the maximum value of the inductor current. Typical measured switching waveforms and trajectories of SW1, Q2 and D_F are shown in Figs. 16.37, 16.38, and 16.39, respectively.

B. Design Procedure

Given: Input AC voltage = V_s (V)
Peak AC voltage = $V_s(max)$ (V)
Nominal output DC voltage = V_o (V)
Switching frequency = f_{sw} (Hz)
Output power = P_o (W)

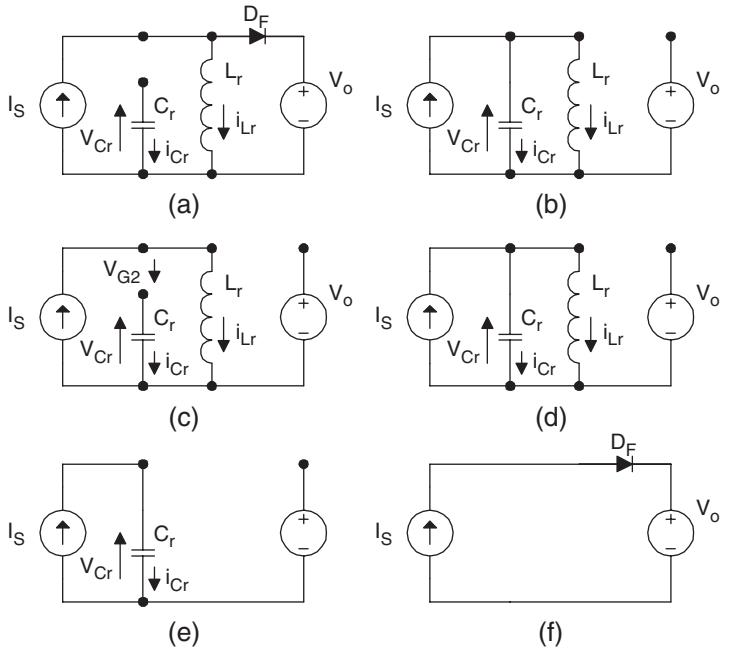


FIGURE 16.35 Operating modes of EP-QR boost-type AC–DC power factor correction circuit.

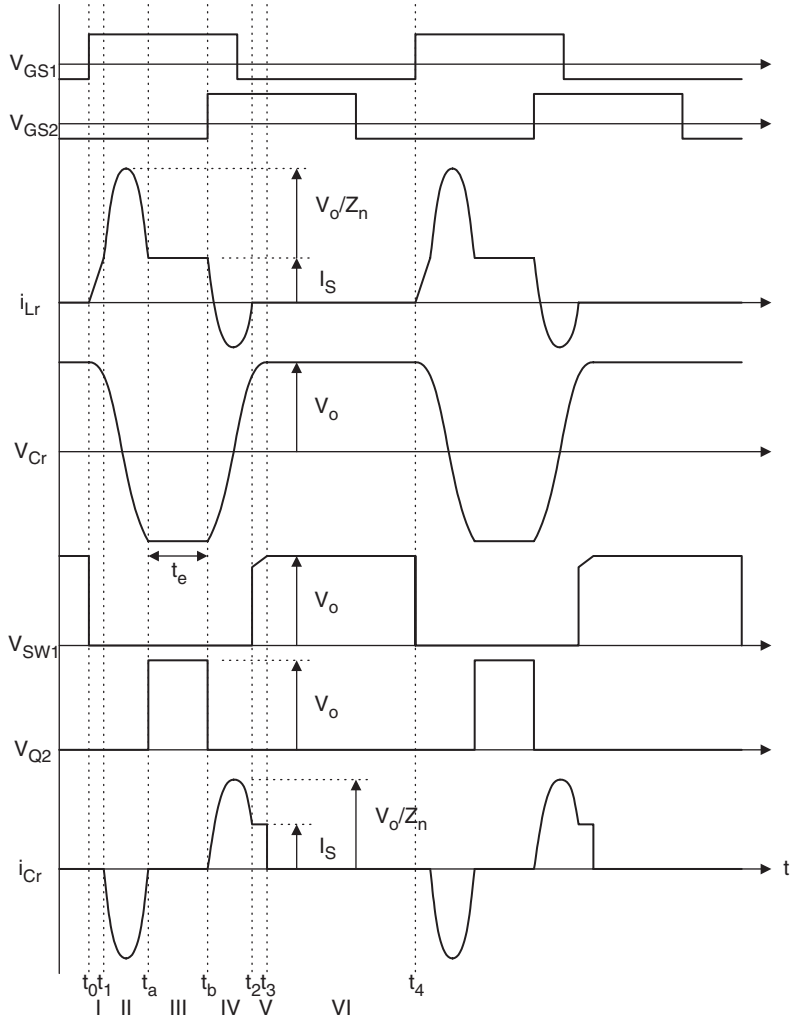


FIGURE 16.36 Idealized waveforms of EP-QR boost-type AC–DC power factor correction circuit.

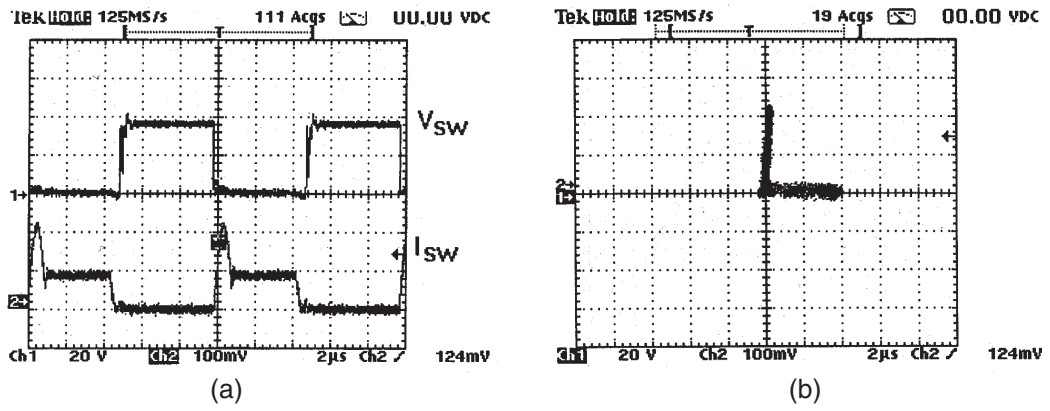


FIGURE 16.37 (a) Drain-source voltage and current of SW1 and (b) switching locus of SW1.

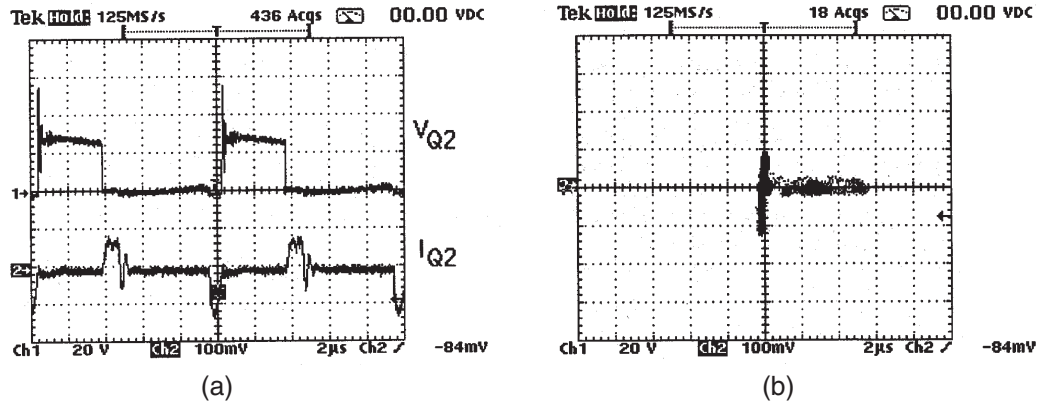


FIGURE 16.38 (a) Drain-source voltage and current of Q2 and (b) switching locus of Q2.

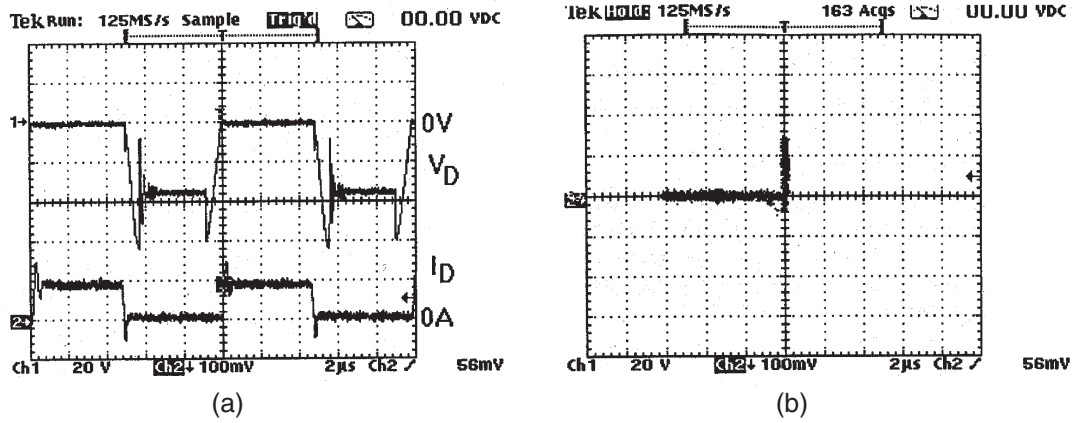


FIGURE 16.39 (a) Diode voltage and current and (b) switching locus of diode.

Input current ripple $= \Delta I$ (A)
Output voltage ripple $= \Delta V$ (V)

(I) Resonant tank design:
Step 1: Because the peak resonant current must be greater than the peak inductor current (same as peak input line current) in order to achieve soft-turn-off, it is necessary to determine the peak input current $I_s(max)$. Assuming lossless AC–DC power conversion, $I_s(max)$ can be estimated from the following equation

$$I_{s(max)} \approx \frac{2V_oI_o}{V_{s(max)}} \tag{16.7}$$

where $I_o = P_o/V_o$ is the maximum output current.
Step 2: Soft-switching criterion is

$$Z_r \leq \frac{V_o}{I_{s(max)}} \tag{16.8}$$

where $Z_r = \sqrt{\frac{L_r}{C_r}}$ is the impedance of the resonant tank.

For a chosen resonant frequency f_r, L_r, and C_r can be obtained from:

$$2\pi f_r = \frac{1}{\sqrt{L_rC_r}} \tag{16.9}$$

(II) Filter component design:
The minimum conversion ratio is

$$M_{(min)} = \frac{V_o}{V_{s(max)}} = \frac{1}{1-\left(\frac{f_{sw}}{f_r}+\frac{t_e}{T_{sw}}\right)} \tag{16.10}$$

where $T_{sw} = 1/f_{sw}$ and t_e is the extended period. From Eq. (16.10), minimum t_e can be estimated.

The turn-on period of the SW1 is

$$T_{on}(sw1) = t_e + 1/f_r \tag{16.11}$$

Inductor value L is obtained from:

$$L \geq \left(\frac{T_{on(sw1)}}{\Delta I}\right) V_{s(max)} \tag{16.12}$$

The filter capacitor value C can be determined from:

$$C\left(\frac{\Delta V}{\frac{T_s}{\pi}\sin^{-1}\left(\frac{I_o}{I_{s(max)}}\right)}\right) = I_o \tag{16.13}$$

where $T_s = 1/f_s$ is the period of the AC voltage supply frequency.

16.11.1 Soft-switched DC–DC Flyback Converter

A simple approach that can turn an existing hard-switched converter design into a soft-switched one is shown in Fig. 16.40. The key advantage of the proposal is that many well proven and reliable hard-switched converter designs can be kept. The modification required is the addition of a simple circuit (consisting an auxiliary winding, a switch, and a small capacitor) to an existing isolated converter [36]. This principle, which is the modified version of the EPQR technique for isolated converter, is demonstrated in an isolated soft-switched flyback converter with multiple outputs. Other advantageous features of the proposal are:

- All switches and diodes of the converter are 'fully' soft-switched, i.e. soft-switched at both turn-on and turn-off transitions under zero-voltage and/or zero-current conditions.
- The leakage inductance of each winding in the flyback transformer forms part of the resonant circuit for achieving ZVS and ZCS of all switches and diodes.
- The control technique is simply PWM-based as in standard hard-switched converters.
- The soft-switched technique is a proven method for EMI reduction [37].

16.11.2 A ZCS Bidirectional Flyback DC–DC Converter

A bi-directional flyback dc–dc converter that uses one auxiliary circuit for both power flow directions is proposed in Fig. 16.41 [38]. The methodology is based on extending the unidirectional soft-switched flyback converter in [36] and replacing the output diode with a controlled switch, which acts as either a rectifier [39] or a power control switch in the corresponding power flow direction. An auxiliary circuit that consists of a winding in the coupled inductor, a switch, and a capacitor converts the hard-switched design into a soft-switched one. The operation is the same as [36] in the forward mode. An extended-period resonant stage [34] is introduced when the power control switch is on. Conversely, in the reverse mode, a complete resonant stage is initiated before the main switch is off. In both the power flow operations, the leakage inductance of the coupled inductor is used to create zero-current switching conditions for all switches.

16.12 Soft-switching and EMI Suppression

A family of EP-QR converters are displayed in Fig. 16.42. Their radiated EMI emission have been compared with that from their hard-switched counterparts [37]. Figures 16.43a, b show the conducted EMI emission from a hard-switched flyback

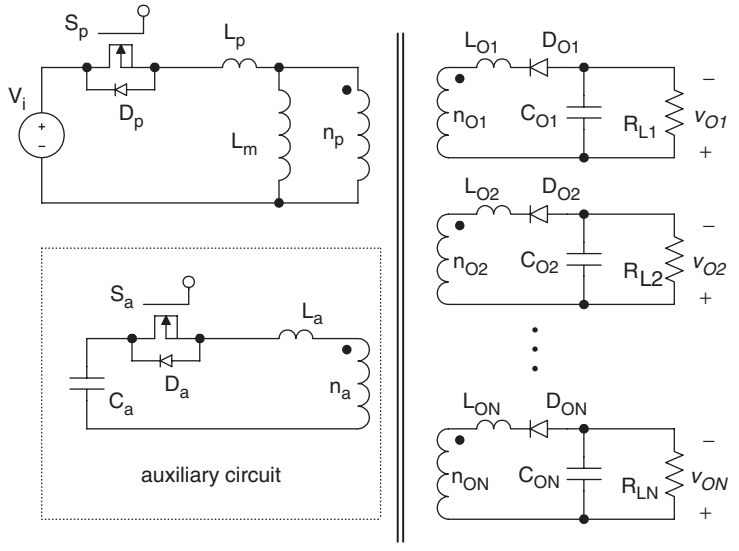


FIGURE 16.40 Fully soft-switched isolated flyback converter.

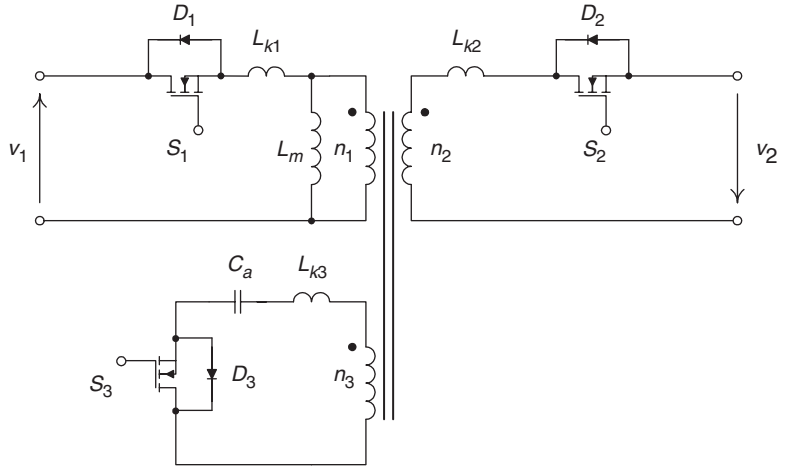


FIGURE 16.41 Bidirectional soft-switched isolated flyback converter.

converter and a soft-switched one, respectively. Their radiated EMI emissions are included in Fig. 16.44. Both converters are tested at an output power of 50 W. No special filtering or shielding measures have been taken during the measurement. It is clear from the measurements that soft-switching is an effective means to EMI suppression.

16.13 Snubbers and Soft-switching for High Power Devices

Today, most of the medium power (up to 200 kVA) and medium voltage (up to 800 V) inverter are hard-switched. Compared with low-power switched mode power supplies, the high voltage involved in the power inverters makes the *dv/dt*, *di/dt*, and the switching stress problems more serious. In addition, the reverse recovery of power diodes in the inverter leg may cause very sharp current spike, leading to severe EMI problem. It should be noted that some high power devices such as GTO thyristors do not have a square safe operating area (SOA). It is therefore essential that the switching stress they undergone must be within their limits. Commonly used protective measures are to use snubber circuits for protecting high power devices.

Among various snubbers, two snubber circuits are most well-known for applications in power inverters. They are the Undeland snubber [40] (Fig. 16.45) and McMurray snubber circuits [41] (Fig. 16.46). The Undeland snubber is an asymmetric snubber circuit with one turn-on inductor and one turn-off capacitor. The turn-off snubber capacitor C_s is clamped by another capacitor C_c. At the end of each switching

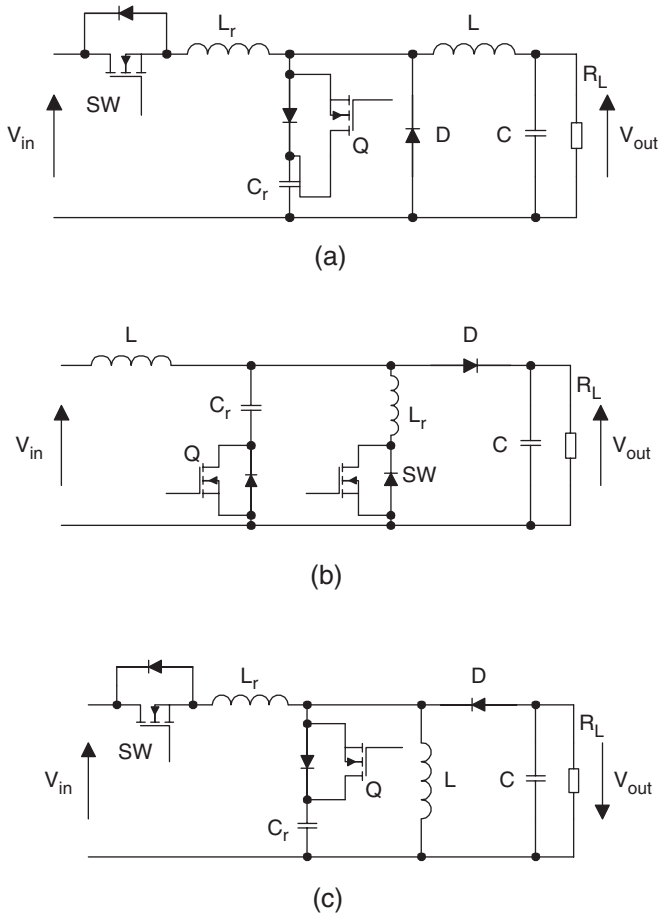


FIGURE 16.42 A family of EP-QR converters: (a) buck converter; (b) boost converter; and (c) flyback converter.

cycle, the snubber energy is dumped into C_c and then discharged into the dc bus via a discharge resistor. In order to reduce the snubber loss, the discharge resistor can be replaced by a switched mode circuit. In this way, the Undeland snubber can become a snubber with energy recovery. The McMurray snubber is symmetrical. Both the turn-off snubber capacitors share current in parallel during turn off. The voltage transient is limited by the capacitor closest to the turning-off device because the stray inductance to the other capacitor will prevent instantaneous current sharing. The turn-on inductors require mid-point connection. Snubber energy is dissipated into the snubber resistor. Like the Undeland snubber, the McMurray snubber can be modified into an energy recovery snubber. By using an energy recovery transformer as shown in Fig. 16.47, this snubber becomes a regenerative one. Although other regenerative circuits have been proposed, their complexity makes them unattractive in industrial applications. Also, they do not necessarily solve the power diode reverse-recovery problems.

Although the use of snubber circuits can reduce the switching stress in the power devices, the switching loss is actually damped into the snubber resistors unless regenerative snubbers are used. The switching loss is still a limiting factor to the high frequency operation of power inverters. However, the advent of soft-switching techniques opens a new way to high-frequency inverter operation. Because the switching trajectory of a soft-switched switch is close to the voltage and current axis, faster power electronic devices with smaller SOAs can in principle be used. In general, both ZVS and ZCS can reduce switching loss in high-power power switches. However, for power switches with tail currents, such as IGBT, ZCS is more effective than ZVS.

16.14 Soft-switching DC–AC Power Inverters

Soft-switching technique not only offers a reduction in switching loss and thermal requirement, but also allows the possibility of high frequency and snubberless operation. Improved circuit performance and efficiency, and reduction of EMI emission can be achieved. For zero-voltage switching (ZVS) inverter applications, two major approaches which enable

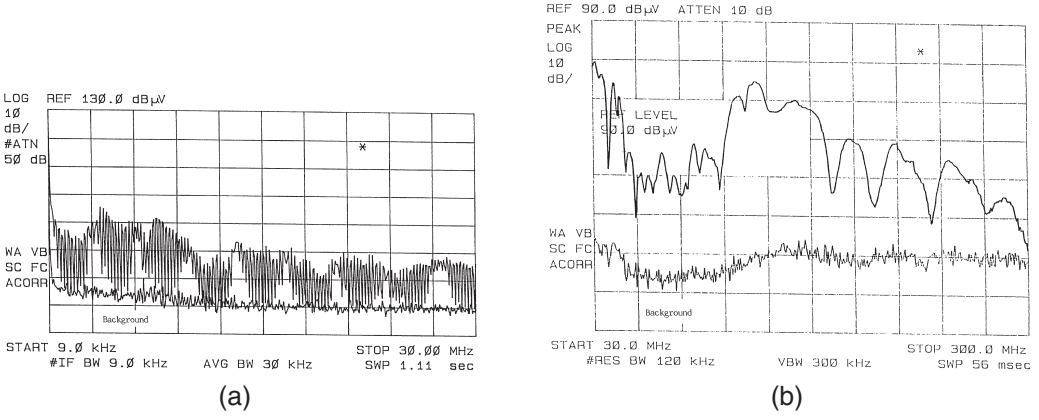


FIGURE 16.43 (a) Conducted EMI from hard-switched flyback converter and (b) radiated EMI from hard-switched flyback converter.

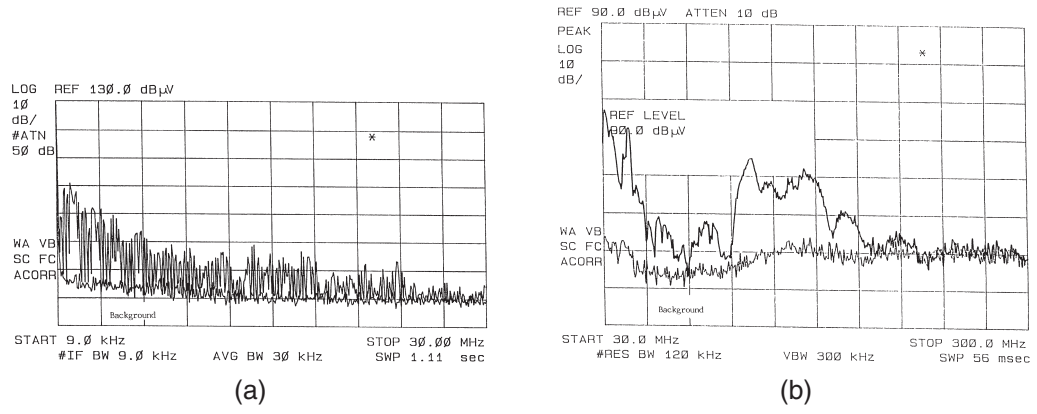


FIGURE 16.44 (a) Conducted EMI from soft-switched flyback converter and (b) radiated EMI from soft-switched flyback converter.

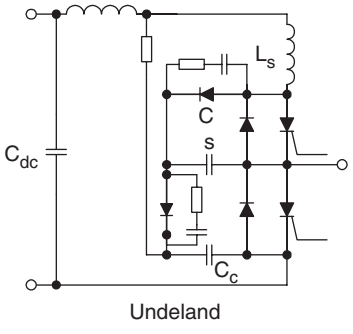


FIGURE 16.45 Undeland snubber.

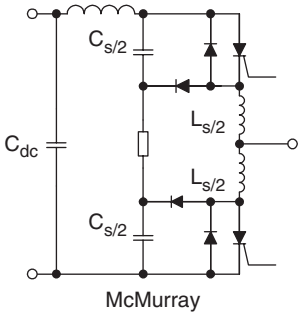


FIGURE 16.46 McMurray snubber.

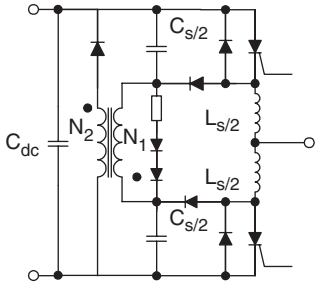


FIGURE 16.47 McMurray snubber with energy recovery.

inverters to be soft-switched have been proposed. The first approach pulls the dc link voltage to zero momentarily so that the inverter's switches can be turned on and off with ZVS. Resonant dc link and quasi-resonant inverters belong to this category. The second approach uses the resonant pole idea. By incorporating the filter components into the inverter operation, resonance condition and thus zero voltage/current conditions can be created for the inverter switches.

In this section, the following soft-switched inverters are described.

Approach 1: Resonant dc link inverters

1. Resonant (pulsating) dc link inverters
2. Actively-clamped resonant dc link inverters
3. Resonant inverters with minimum voltage stress
4. Quasi-resonant soft-switched inverter
5. Parallel resonant dc link inverter.

Approach 2: Resonant pole inverters

1. Resonant pole inverters
2. Auxiliary resonant pole inverters
3. Auxiliary resonant commutated pole inverters.

Type 1 is the resonant dc link inverter [42–44] which sets the dc link voltage into oscillation so that the zero-voltage instants are created periodically for ZVS. Despite the potential advantages that this soft-switching approach can offer, a recent review on existing resonant link topologies for inverters [45] concludes that the resonant dc link system results in an increase in circuit complexity and the frequency spectrum is restricted by the need of using integral pulse density modulation (IPDM) when compared with a standard hard-switched inverter. In addition, the peak pulsating link voltage of resonant link inverters is twice the dc link voltage in a standard hard-switched inverter. Although clamp circuits (Type 2) can be used to limit the peak voltage to 1.3–1.5 per unit [44], power devices with higher than normal voltage ratings have to be used.

Circuits of Type 3–5 employ a switched mode front stage circuit which pulls the dc link voltage to zero momentarily whenever inverter switching is required. This soft-switching approach does not cause extra voltage stress to the inverter and hence the voltage rating of the power devices is only 1 per unit. As ZVS conditions can be created at any time, there is virtually no restriction in the PWM strategies. Therefore, well established PWM schemes developed in the last two decades can be employed. In some ways, this approach is similar to some dc-side commutation techniques proposed in the past for thyristor inverters [46, 47], although these dc-side commutation techniques were used for turning off thyristors in the inverter bridge and were not primarily developed for soft-switching.

Circuits of Type 6–8 retain the use of a constant dc link voltage. They incorporate the use of the resonant components and/or filter components into the inverter circuit operation. This approach is particularly useful for inverter applications in which output filters are required. Examples include uninterruptible power supplies (UPS) and inverters with output filters for motor drives. The LC filter components can form the auxiliary resonant circuits that create the soft-switching conditions. However, these tend to have high power device count and require complex control strategy.

16.14.1 Resonant (Pulsating) DC Link Inverter

Resonant DC link converter for DC–AC power conversion was proposed in 1986 [42]. Instead of using a nominally constant DC link voltage, a resonant circuit is added to cause the DC link voltage to be pulsating at a high frequency. This resonant circuit theoretically creates periodic zero-voltage duration at which the inverter switches can be turned on or off. Figure 16.48 shows the schematics of the pulsating link inverter. Typical dc link voltage, inverter's phase voltage and the line voltages are shown in Fig. 16.49. Because the inverter switching can only occur at zero voltage duration, integral pulse density modulation (IPDM) has to be adopted in the switching strategy.

Analysis of the resonant dc link converter can be simplified by considering that the inverter system is highly inductive. The equivalent circuit is shown in Fig. 16.50.

The link current I_x may vary with the changing load condition, but can be considered constant during the short resonant cycle. If switch S is turned on when the inductor current is I_{Lo}, the resonant dc link voltage can be expressed as

$$V_c(t) = V_s + e^{-\alpha t}\left[-V_s \cos(\omega t) + \omega L I_M \sin(\omega t)\right] \quad (16.14)$$

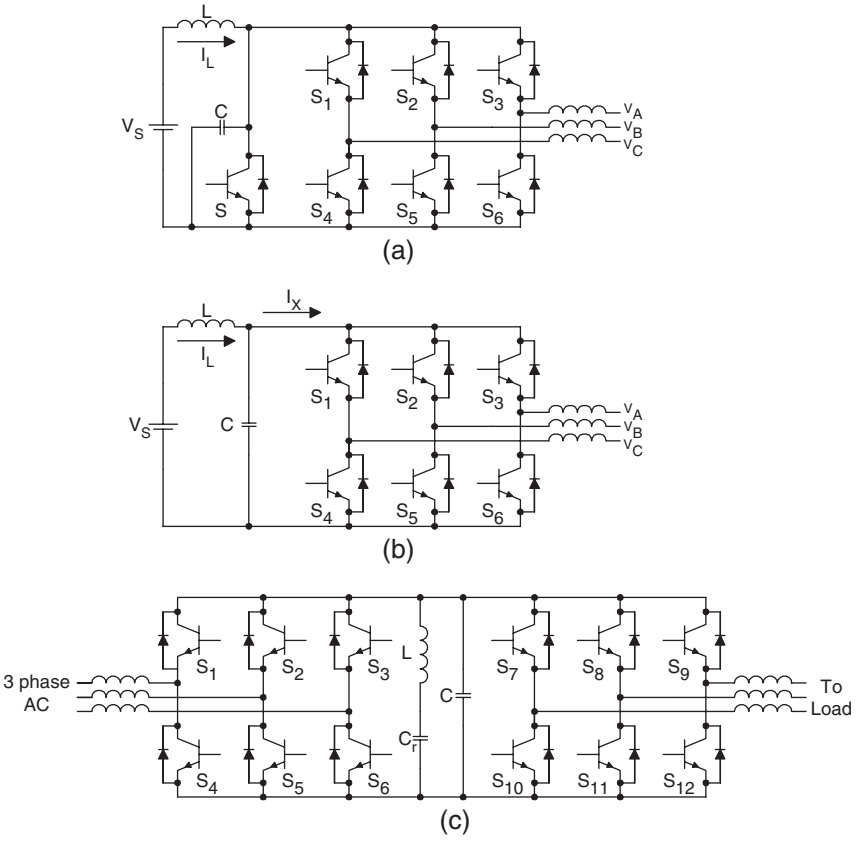


FIGURE 16.48 Resonant-link inverters.

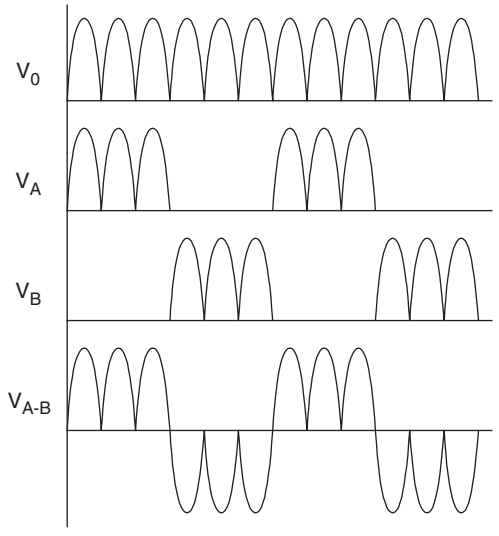


FIGURE 16.49 Typical dc link voltage (V_0), phase voltages (V_A,V_B), and line voltage (V_{AB}) of resonant link inverters.

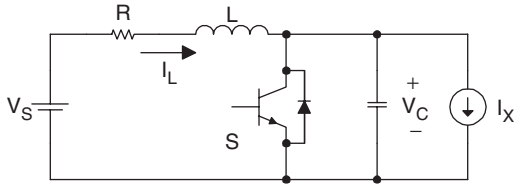


FIGURE 16.50 Equivalent circuit of resonant link inverter.

and inductor current i_L is

$$i_L(t) \approx I_x + e^{-\alpha t}\left[I_M \cos(\omega t) + \frac{V_s}{\omega L}\sin(\omega t)\right] \quad (16.15)$$

where $$\alpha = \frac{R}{2L} \quad (16.16)$$

$$\omega_o = (LC)^{-0.5} \quad (16.17)$$

$$\omega = \left(\omega_o^2 - \alpha^2\right)^{0.5} \quad (16.18)$$

and $$I_M = I_{Lo} - I_x \quad (16.19)$$

The resistance in the inductor could affect the resonant behavior because it dissipates some energy. In practice, $(i_L - I_x)$ has to be monitored when S is conducting. S can be turned on when $(i_L - I_x)$ equal to a desired value. The objective is to ensure that the dc link voltage can be resonated to zero voltage level in the next cycle.

The pulsating dc link inverter has the following advantages:

- Reduction of switching loss.
- Snubberless operation.
- High switching frequency (> 18 kHz) operation becomes possible, leading to the reduction of acoustic noise in inverter equipment.
- Reduction of heatsink requirements and thus improvement of power density.

This approach has the following limitations:

- The peak dc pulsating link voltage (2.0 per unit) is higher than the nominal dc voltage value of a conventional inverter. This implies that power devices and circuit components of higher voltage ratings must be used. This could be a serious drawback because power components of higher voltage ratings are not only more expensive, but usually have inferior switching performance than their low-voltage counterparts.
- Although voltage clamp can be used to reduce the peak dc link voltage, the peak voltage value is still higher than normal and the additional clamping circuit makes the control more complicated.
- Integral pulse-density modulation has to be used. Many well-established PWM techniques cannot be employed.

Despite these advantages, this resonant converter concept has paved the way for other soft-switched converters to develop.

16.14.2 Active-clamped Resonant DC Link Inverter

In order to solve the high voltage requirement in the basic pulsating dc link inverters, active clamping techniques (Fig. 16.51) have been proposed. The active clamp can reduce the per-unit peak voltage from 2.0 to about 1.3–1.5 [44]. It has been reported that operating frequency in the range of 60–100 kHz has been achieved [48] with an energy efficiency of 97% for a 50 kVA drive system.

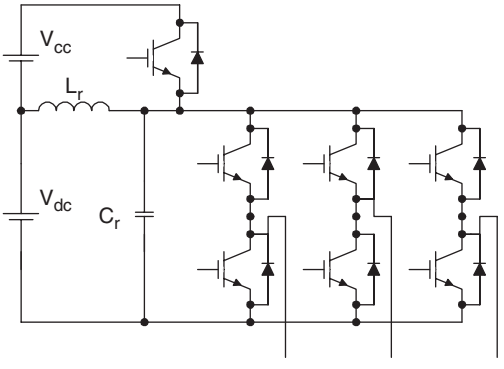


FIGURE 16.51 Active-clamp resonant link inverter.

The design equations for active-clamped resonant link inverter are

$$T_L = \frac{1}{f_L} = 2\sqrt{L_r C_r}\left(\cos^{-1}(1-k) + \frac{\sqrt{k(2-k)}}{k-1}\right) \quad (16.20)$$

where T_L is the minimum link period, f_L is the maximum link frequency, and k is the clamping ratio. For the active-clamped resonant inverter, k is typically 1.3–1.4 per unit.

The rate of rise of the current in the clamping device is

$$\frac{di}{dt} = \frac{(k-1)\,V_s}{L_r} \quad (16.21)$$

The peak clamping current required to ensure that the dc bus return to zero volt is

$$I_{sp} = V_s\sqrt{\frac{k(2-k)\,C_r}{L_r}} \quad (16.22)$$

In summary, resonant (pulsating) dc link inverters offer significant advantages such as:

- High switching frequency operation.
- Low dv/dt for power devices.
- ZVS with reduced switching loss.
- Suitable for 1–250 kW.
- Rugged operation with few failure mode.

16.14.3 Resonant DC Link Inverter with Low Voltage Stress [49]

A resonant dc link inverter with low voltage stress is shown in Fig. 16.52. It consists of a front-end resonant converter that can pull the dc link voltage down just before any inverter switching. This resonant dc circuit serves as an interface between the dc power supply and the inverter. It essentially retains all the advantages of the resonant (pulsating) dc link inverters. But it offers extra advantages such as:

- No increase in the dc link voltage when compared with conventional hard-switched inverter. That is, the dc link voltage is 1.0 per unit.
- The zero voltage condition can be created at any time. The ZVS is not restricted to the periodic zero-voltage instants as in resonant dc link inverter.
- Well-established PWM techniques can be employed.
- Power devices of standard voltage ratings can be used.

The timing program and the six operating modes of this resonant circuit are as shown in Figs. 16.53 and 16.54, respectively.

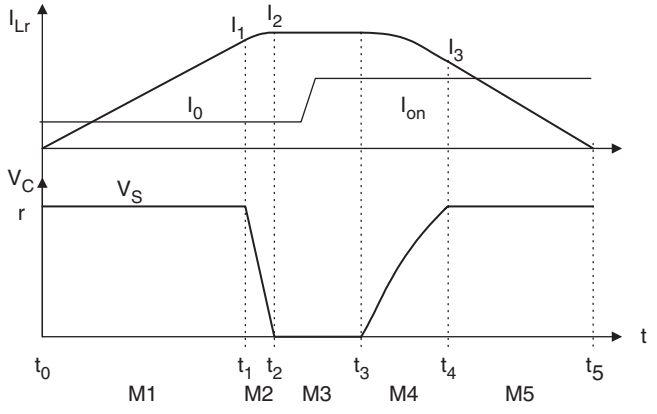


FIGURE 16.53 Timing diagram of resonant link inverter with minimum voltage stress.

(1) *Normal mode:*
This is the standard PWM inverter mode. The resonant inductor current $i_{Lr}(t)$ and the resonant voltage $V_{cr}(t)$ are given by

$$i_{Lr}(t) = 0$$

$$v_{Cr}(t) = V_s$$

where V_s is the nominal dc link voltage.

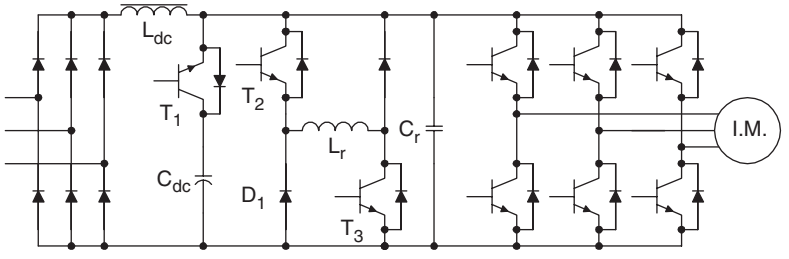


FIGURE 16.52 Resonant DC link inverter with low voltage stress.

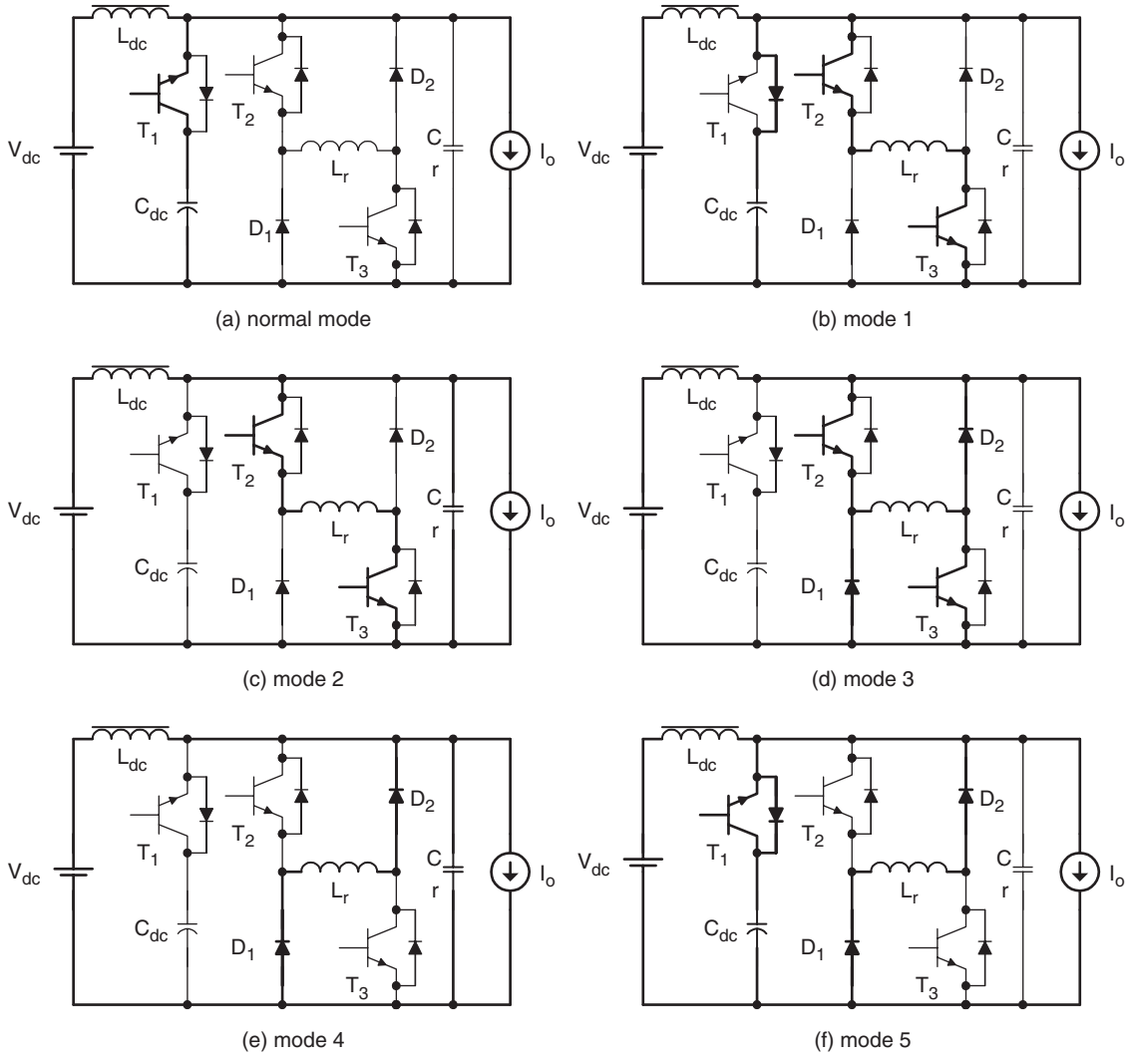


FIGURE 16.54 Operating modes of resonant link inverter with minimum voltage stress.

(2) *Mode 1 (initiating mode): ($t_0 - t_1$)*
At t_0, mode 1 begins by switching on T2 and T3 on with zero current. $i_{Lr}(t)$ increases linearly with a di/dt of V_s/L_r. If $i_{Lr}(t)$ is equal to the initialized current I_i, T1 is zero-voltage turned off. If $(I_s - I_o) < I_i$, then the initialization is ended when $i_{Lr}(t)$ is equal to I_i, where I_s is the current flowing into the dc inductor L_{dc}. If $(I_s - I_o) > I_i$, then this mode continues until $i_{Lr}(t)$ is equal to $(I_s - I_o)$. The equations in this interval are

$$i_{Lr}(t) = \frac{V_s}{L_r} t$$

$$v_{Cr}(t) = V_s$$

$$i_{Lr}(t_1) = \frac{V_s}{L_r} t_1 = I_i$$

(3) *Mode 2 (Resonant mode): ($t_1 - t_2$)*
After T1 is turned off under ZVS condition, resonance between L_r and C_r occurs. $V_{cr}(t)$ decreases from V_s to 0. At t_2, $i_{Lr}(t)$ reaches the peak value in this interval. The equations are:

$$i_{Lr}(t) = \frac{V_s}{Z_r} \sin(\omega_r t) + [I_1 + (I_o - I_s)] \cos(\omega_r t) - (I_o - I_s)$$

$$V_{Cr}(t) = -V_s \cos(\omega_r t) - [I_1 + (I_o - I_s)] Z_r \sin(\omega_r t)$$

$$i_{Lr}(t_2) = I_2 = I_{Lr,peak}$$

$$V_{Cr}(t_2) = 0$$

where

$$Z_r = \sqrt{\frac{L_r}{C_r}} \text{ and } \omega_r = \frac{1}{\sqrt{L_r C_r}}$$

(4) *Mode 3 (Freewheeling mode): ($t_2 - t_3$)*
The resonant inductor current flows through two freewheeling paths (T2-Lr-D2 and T3-D1-Lr). This duration is the zero voltage period created for ZVS of the inverter, and should be longer than the minimum on and off times of the inverter's power switches.

$$i_{Lr}(t) = I_2$$

$$v_{Cr}(t) = 0$$

(5) *Mode 4 (Resonant mode): ($t_3 - t_4$)*
This mode begins when T2 and T3 are switched off under ZVS. The second half of the resonance between L_r and C_r starts again. The capacitor voltage $V_{cr}(t)$ increases back from 0 to V_s and is clamped to V_s. The relevant equations in this mode are

$$i_{Lr}(t) = [I_2 - (I_{on} - I_s)]\cos(\omega_r t) - (I_{on} - I_s)$$

$$V_{Cr}(t) = [I_2 - (I_{on} - I_s)]\, Z_r \sin(\omega_r t)$$

$$i_{Lr}(t_4) = I_3$$

$$V_{Cr}(t_4) = V_s$$

where I_{on} is the load current after the switching state.
(6) *Mode 5 (Discharging mode): ($t_4 - t_5$)*
In this period, T1 is switched on under ZV condition because $V_{cr}(t) = V_s$. The inductor current decreases linearly. This mode finishes when $i_{Lr}(t)$ becomes zero.

$$i_{Lr}(t) = -\frac{V_s}{L_r}t + I_3$$

$$v_{Cr}(t) = V_s$$

$$i_{Lr}(t_5) = 0$$

16.14.4 Quasi-resonant Soft-switched Inverter [50]

(A) Circuit Operation
Consider an inverter fed by a dc voltage source vs a front-stage interface circuit shown in Fig. 16.55, can be added between the dc voltage source and the inverter. The front-stage circuit consists of a quasi-resonant circuit in which the first half of the resonance cycle is set to occur to create the zero-voltage condition whenever inverter switching is needed. After inverter switching has been completed, the second half of the resonance cycle takes place so that the dc link voltage is set back to its normal level. To avoid excessive losses in the resonant circuit, a small capacitor C_{r1} is normally used to provide the dc link voltage whilst the large smoothing dc link capacitor C_1 is isolated from the resonant circuit just before the zero-voltage

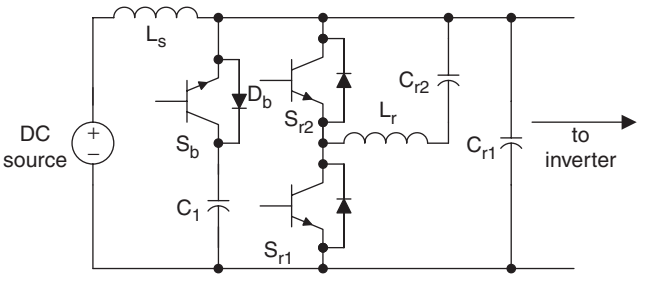


FIGURE 16.55 Quasi-resonant circuit for soft-switched inverter.

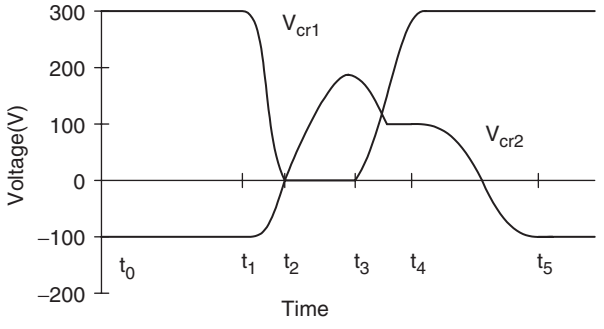


FIGURE 16.56 Typical waveforms for V_{cr1} and V_{cr2}.

duration. This method avoids the requirement for pulling the dc voltage of the bulk capacitor to zero.

The period for this mode is from t_0 to t_1 in Fig. 16.56. In this mode, switch S_b is turned on and switches S_{r1} and S_{r2} are turned off. The inverter in Fig. 16.55 works like a conventional dc link inverter. In this mode, $V_{cr1} = V_{c1}$. The voltage across switch S_b is zero. Before an inverter switching takes place, when switch S_{r1} is triggered at t_1 to discharge C_{r1}. This operating mode ends at t_2 when V_{cr1} approaches zero. The equivalent circuit in this mode is shown in Fig. 16.57a. The switch S_b must be turned off at zero voltage when switch S_{r1} is triggered. After S_{r1} is triggered, C_{r1} will be discharged via the loop C_{r1}, C_{r2}, L_r, and S_{r1}. Under conditions of $V_{cr2} \leq 0$ and $C_{r1} \leq C_{r2}$, the energy stored in C_{r1} will be transferred to C_{r2} and V_{cr1} falls to zero in the first half of the resonant cycle in the equivalent circuit of Fig. 16.57a. V_{cr1} will be clamped to zero by the freewheel diodes in the inverter bridge and will not become negative. Thus, V_{cr1} can be pulled down to zero for zero-voltage switching. When the current in inductor L_r becomes zero, switch S_{r1} can be turned off at zero current.

Inverter switching can take place in the period from t_2 to t_3 in which V_{cr1} remains zero. This period must be longer than the turn-on and turn-off times of the switches. When inverter switching has been completed, it is necessary to reset the voltage of capacitor C_{r1}. The equivalent circuit in this mode is shown in Fig. 16.57b. The current in inductor L_r reaches zero at t_3. Due to the voltage in V_{cr2} and the presence

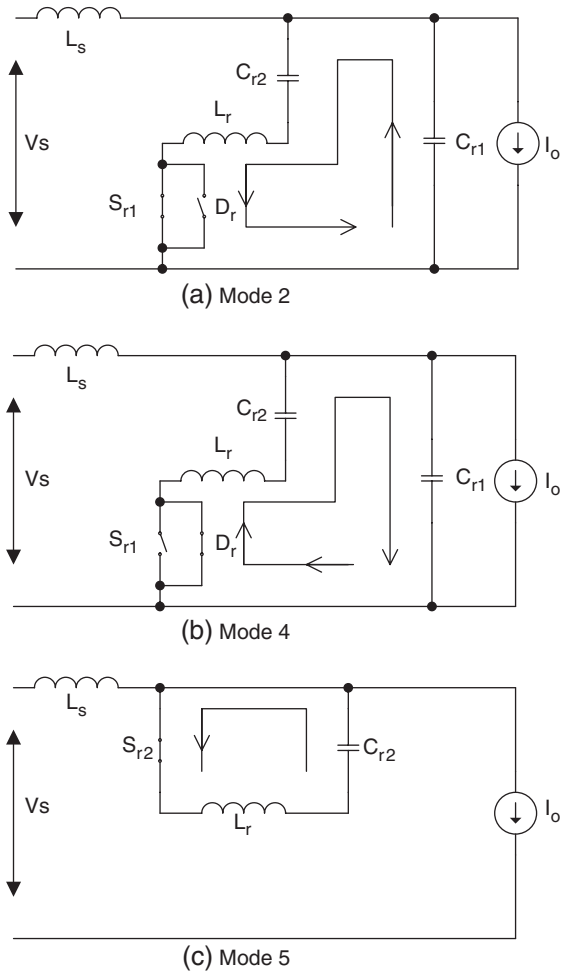


FIGURE 16.57 Equivalent circuits of the quasi-resonant circuit for different modes.

of diode D_r, this current then flows in the opposite direction. C_{r1} will be recharged via L_r, C_{r2}, C_{r1}, and D_r. The diode D_r turns off when the current in L_r becomes zero. V_{cr1} will not go beyond 1 per unit because C_{r1} is clamped to supply voltage by diode D_b. The switch S_b can be turned on again at zero-voltage condition when V_{cr1} returns to normal dc supply voltage. After D_r turns off, V_{cr2} may not be zero. Some positive residual capacitor voltage remains in C_2 at t_4, as shown in Fig. 16.56. In case V_{cr2} is positive, V_{cr1} cannot be pulled down to zero again in the next switching cycle. Therefore, S_{r2} should be triggered after t_4 to reverse the residual voltage in C_{r2}. At time t_5, Sr_2 turns off at zero-current condition and V_{cr2} is now reversed to negative. The equivalent circuit in this mode is shown in Fig. 16.57c. When $V_{cr2} \leq 0$ and $C_{r1} \leq C_{r2}$, V_{cr1} can be pulled down to zero again before the next inverter switching. The operation can then be repeated in next switching cycle.

(B) Design Considerations

(1) C_{r1} and C_{r2}

The criterion for getting zero capacitor voltages V_{cr1} is:

$$(C_{r1} - C_{r2})V_s + 2C_{r2}V_{o2} - \Delta I\pi\sqrt{L_r C_e} \leq 0 \qquad (16.23)$$

where

- V_{o1} is the initial voltage of C_{r1};
- V_{o2} is the initial voltage of C_{r2};
- i_{L0} is the initial current of inductor L_r;
- $\Delta I = I_o - I_s$, which is the difference between load current and supply current. It is assumed to be a constant within a resonant cycle;
- R_r is the equivalent resistance in the resonant circuit.
- $C_e = \dfrac{C_{r1}C_{r2}}{C_{r1} + C_{r2}}$

When $\Delta I \geq 0$, the above criterion is always true under conditions of:

$$C_{r1} \leq C_{r2}, \quad V_{o2} \leq 0$$

The criterion for recharging voltage V_{cr1} to 1 per unit dc link voltage is:

$$\frac{2C_{r2}}{C_{r1} + C_{r2}}V_{o2} - \frac{\Delta I}{C_{r1} + C_{r2}}\pi\sqrt{L_r C_e} \geq V_s \qquad (16.24)$$

(2) Inductor L_r

The inductor L_r should be small so that the dc link voltage can be decreased to zero quickly. However, a small L_r could result in large peak resonant current and therefore requirement of power devices with large current pulse ratings. An increase in the inductance of L_r can limit the peak current in the quasi-resonant circuit. Because the resonant frequency depends on both the inductor and the capacitor, therefore, the selection of L_r can be considered together with the capacitors C_{r1} and C_{r2} and with other factors such as the current ratings of power devices, the zero-voltage duration and the switching frequency required in the soft-switching circuit.

(3) Triggering instants of the switches

The correct triggering instants for the switches are essential for the successful operation of this soft-switched inverter. For the inverter switches, the triggering instants are determined from a PWM modulation. Let T_s be the time at which the inverter switches change states. To get the zero-voltage inverter switching, switch S_{r1} should be turned on half resonant cycle before the inverter switching instant. The turn-on instant of S_{r1}, which is t_1 in Fig. 16.56, can be written as:

$$t_1 = T_s - \frac{\pi}{\omega} \qquad (16.25)$$

where $\omega = \sqrt{\omega_0^2 - \alpha^2}$, $\alpha = \frac{R_r}{2L_r}$, $\omega_0 = \sqrt{\frac{1}{L_r C_e}}$. The switch S_b is turned off at t_1.

S_{r1} may be turned off during its zero current period when diode D_r is conducting. For easy implementation, its turn-off time can be selected as $T_s + \pi/\omega$. Because the dc link voltage can be pulled down to zero in less than half resonant cycle, T_s should occur between t_2 and t_3.

At time t_3 (the exact instant depends on the ΔI), the diode D_r turns on in the second half of the resonant cycle to recharge C_{r1}. At t_4, V_{cr1} reaches 1 per unit and diode D_b clamps V_{cr1} to 1 per unit. The switch S_b can be turned on again at t_4, which is half resonant cycle after the start of t_3:

$$t_4 \approx t_3 + \frac{\pi}{\omega} \tag{16.26}$$

As t_3 cannot be determined accurately, a voltage sensor in principle can be used to provide information for t_4 so that S_b can be turned on to reconnect C_1 to the inverter. In practice, however, S_b can be turned on a few microseconds (longer than $T_s + \pi/\omega$) after t_2 without using a voltage sensor (because it is not critical for S_b to be on exactly at the moment V_{cr} reaches the nominal voltage). As for switch S_{r2}, it can be turned on a few microseconds after t_4. It will be turned off half of resonant cycle ($\pi\sqrt{L_r C_{r2}}$) in the $L_r - C_{r2}$ circuit later. In practice, the timing of S_{r1}, S_{r2}, and S_b can be adjusted in a simple tuning procedure for a given set of parameters. Figure 16.58 shows the measured gating signals of S_{r1}, S_{r2}, and S_b with the dc link voltage V_{cr1} in a 20 kHz switching inverter. Figures 16.59 and 16.60 show the measured waveforms of I_s, I_o, and V_{cr1} under no load condition and loaded condition, respectively.

(C) Control of Quasi-resonant Soft-switched Inverter Using Digital Time Control (DTC) [51]

Based on the zero-average-current error (ZACE) control concept, a digital time control method has been developed for a current-controlled quasi-resonant soft-switched inverter. The basic ZACE concept is shown in Fig. 16.61. The current error is obtained from the difference of a reference current and the sensed current. The idea is to make the areas of each transition (A1 and A2) equal. If the switching frequency is significantly greater than the fundamental frequency of the reference signal,

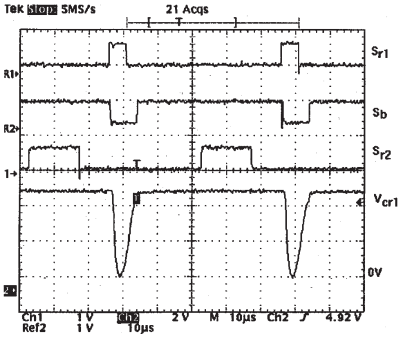


FIGURE 16.58 Gating signals for S_{r1}, S_{r2}, and S_b with V_{cr1}.

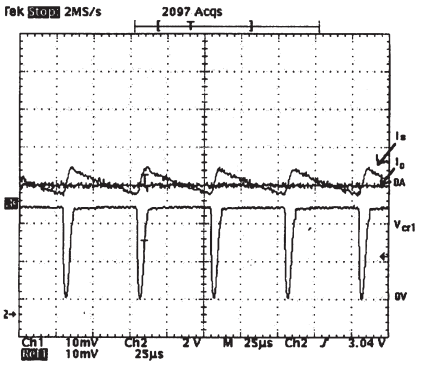


FIGURE 16.59 Typical I_s, I_o, and V_{cr1} under no-load condition.

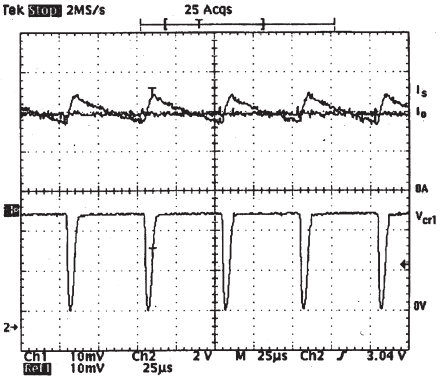


FIGURE 16.60 Typical I_s, I_o, and V_{cr1} under loaded condition.

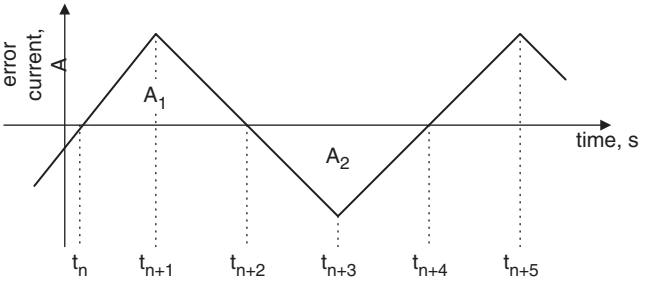


FIGURE 16.61 Zero-average-current error (ZACE) control concept.

the rising and falling current segments can be assumed to be linear. The following simplified equation can be established.

$$\Delta t_{n+1} = t_{n+1} - t_n \tag{16.27}$$

The control algorithm for the inverter is

$$\Delta t_{n+3} = \Delta t_{n+2} + D\left[\frac{T_{sw}}{2} - (t_{n+2} - t_n)\right] \tag{16.28}$$

where $D = \dfrac{\Delta t_{n+2}}{t_{n+2} - t_n}$ and $T_{sw} = t_{n+4} - t_n$.

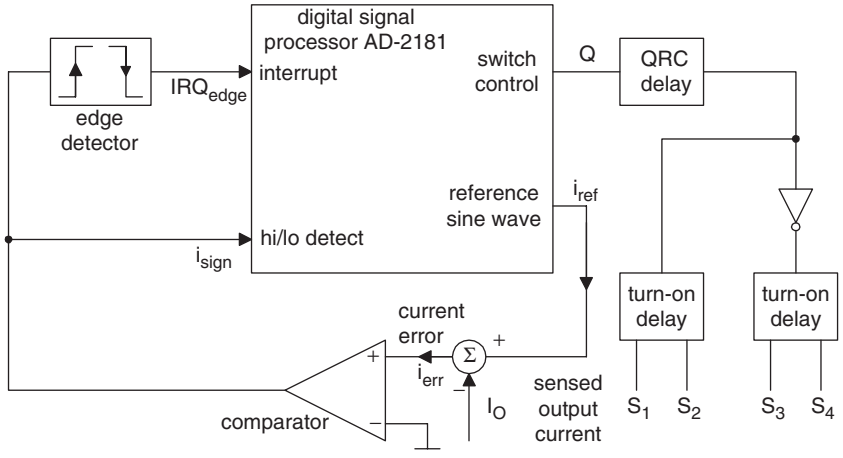


FIGURE 16.62 Implementation of DTC.

The schematic of a digital signal processor (DSP) based controller for the DTC method is shown in Fig. 16.62. The duty cycle can be approximated from the reference sine wave by level shifting and scaling it between 0 and 1. The time $t_{n+2} - t_n$ is the sum of Δt_{n+1} and Δt_{n+2}. These data provide information for the calculation of the next switching time Δt_{n+1}.

The switches are triggered by the changing edge of the switch control Q. Approximate delays are added to the individual switching signals for both the inverter switches and the quasi-resonant switches. Typical gating waveforms are shown in Fig. 16.63. The use of the quasi-resonant soft-switched inverter is a very effective way in suppressing switching transient and EMI emission. Figures 16.64a,b show the inverter switch voltage waveforms of a standard hard-switched inverter and a quasi-resonant soft-switched inverter, respectively. It is clear that the soft-switched waveform has much less transient than the hard-switched waveform.

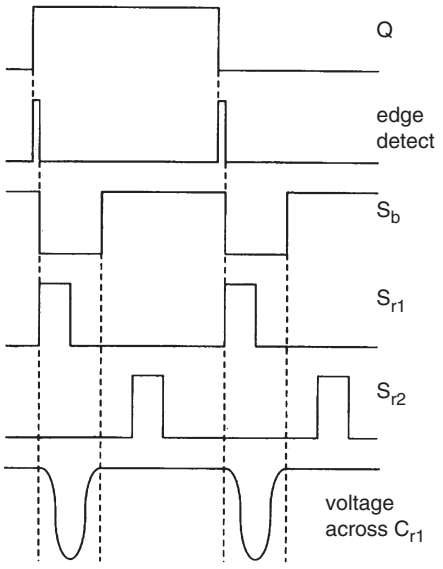


FIGURE 16.63 Timing diagrams for the gating signals.

16.14.5 Resonant Pole Inverter (RPI) and Auxiliary Resonant Commutated Pole Inverter (ARCPI)

The resonant pole inverter integrates the resonant components with the output filter components L_f and C_f. The load

FIGURE 16.64 (a) Typical switch voltage under hard turn-off and (b) typical switch voltage under soft turn-off.

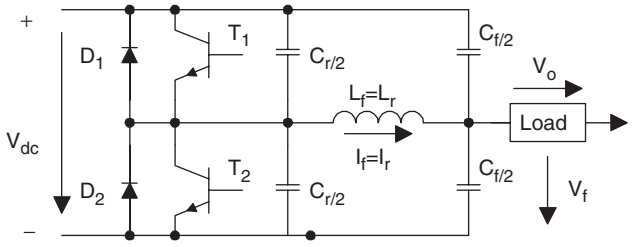


FIGURE 16.65 One leg of a resonant pole inverter.

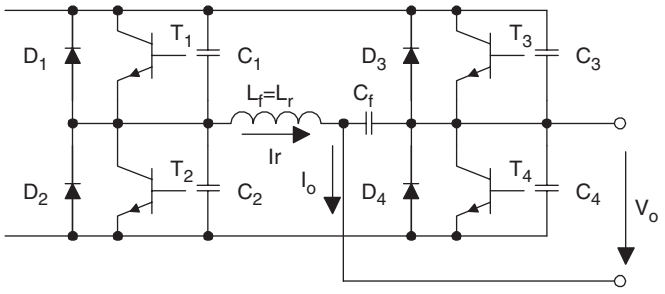


FIGURE 16.66 Single-phase resonant pole inverter.

is connected to the mid-point of the dc bus capacitors as shown in Fig. 16.65. It should however be noted that the RPI can be described as a resonant inverter. Figure 16.66 shows a single-phase RPI. Its operation can be described with the timing diagram in Fig. 16.67. The operating modes are included in Fig. 16.68. The RPI provides soft-switching for all power switches. But it has two disadvantages. First, the power devices have to be switched continuously at the resonant frequency determined by the resonant components. Second, the power devices in the RPI circuit require a 2.2–2.5 p.u. current turn-off capability.

An improved version of the RPI is the auxiliary resonant commutated pole inverter (ARCPI). The ARCPI for one inverter leg is shown in Fig. 16.69. Unlike the basic RPI, the ARCPI allows the switching frequency to be controlled. Each of the primary switches is closely paralleled with a snubber capacitor to ensure ZV turn off. Auxiliary switches are connected in series with an inductor, ensuring that they operate under ZC conditions. For each leg, an auxiliary circuit comprising two extra switches A1 and A2, two freewheeling diodes, and a resonant inductor L_r is required. This doubles the number of power switches when compared with hard-switched inverters. Figure 16.70 shows the three-phase ARCPI system. Depending on the load conditions, three commutation modes are generally needed. The commutation methods at low and high current are different. This makes the control of the ARCPI very complex. The increase in control and circuit complexity represents a considerable cost penalty [52, 53].

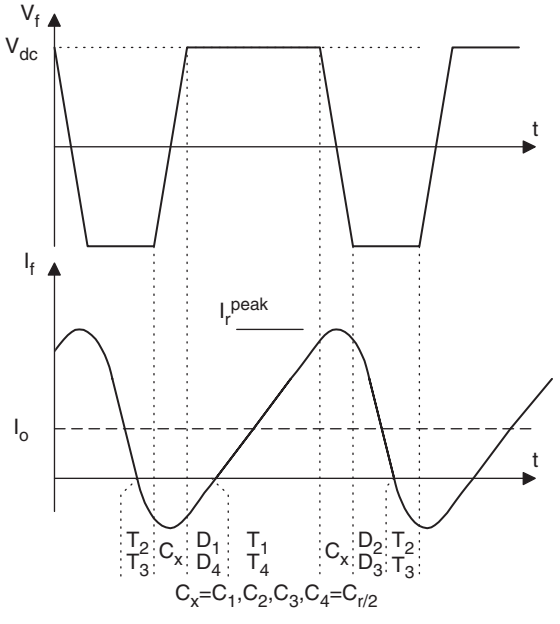


FIGURE 16.67 Timing diagram for a single-phase resonant pole inverter.

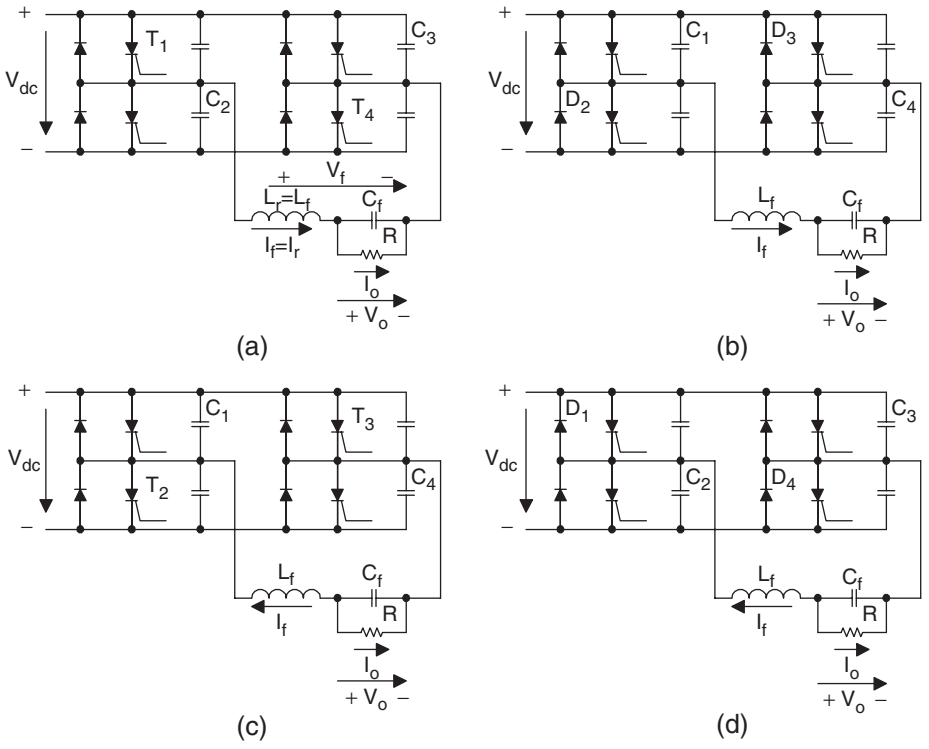


FIGURE 16.68 Operating modes of a single-phase resonant pole inverter.

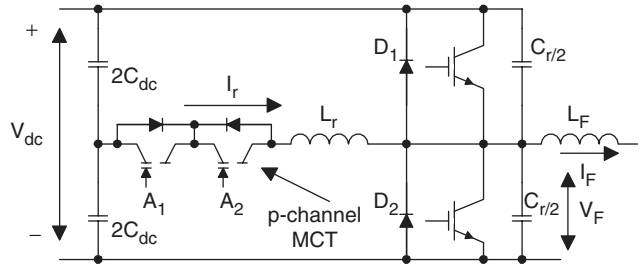


FIGURE 16.69 Improved resonant pole inverter leg.

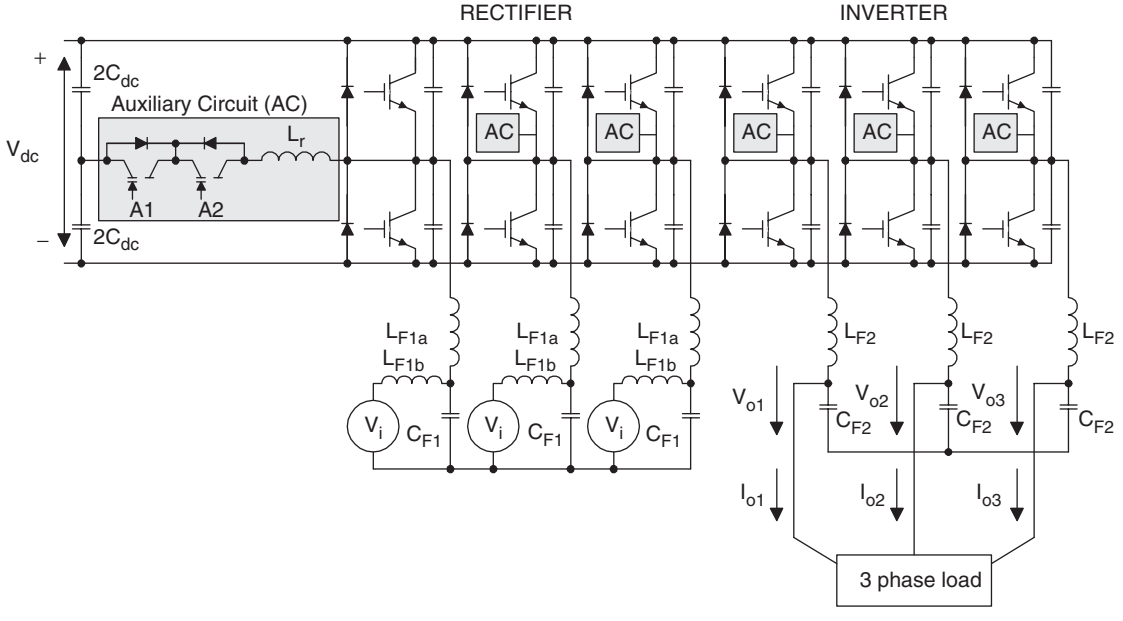


FIGURE 16.70 Three-phase auxiliary resonant commutated pole inverter (ARCPI).

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