5

Insulated Gate Bipolar Transistor

S. Abedinpour, Ph.D. and K. Shenai, Ph.D.
Department of Electrical Engineering and Computer Science, University of Illinois at Chicago, 851, South Morgan Street (M/C 154), Chicago, Illinois, USA

5.1 Introduction

The insulated gate bipolar transistor (IGBT), which was introduced in early 1980s, is becoming a successful device because of its superior characteristics. IGBT is a three-terminal power semiconductor switch used to control the electrical energy. Many new applications would not be economically feasible without IGBTs. Prior to the advent of IGBT, power bipolar junction transistors (BJT) and power metal oxide field effect transistors (MOSFET) were widely used in low to medium power and high-frequency applications, where the speed of gate turn-off thyristors was not adequate. Power BJTs have good on-state characteristics but have long switching times especially at turn-off. They are current-controlled devices with small current gain because of high-level injection effects and wide base width required to prevent reach-through breakdown for high blocking voltage capability. Therefore, they require complex base drive circuits to provide the base current during on-state, which increases the power loss in the control electrode.

On the other hand power MOSFETs are voltage-controlled devices, which require very small current during switching period and hence have simple gate drive requirements. Power MOSFETs are majority carrier devices, which exhibit very high switching speeds. But the unipolar nature of the power MOSFETs causes inferior conduction characteristics as the voltage rating is increased above 200 V. Therefore their on-state resistance increases with increasing breakdown voltage. Furthermore, as the voltage rating increases the inherent body diode shows inferior reverse recovery characteristics, which leads to higher switching losses.

In order to improve the power device performance, it is advantageous to have the low on-state resistance of power BJTs with an insulated gate input like that of a power MOSFET. The Darlington configuration of the two devices shown in Fig. 5.1 has superior characteristics as compared to the two discrete devices. This hybrid device could be gated like a power MOSFET with low on-state resistance because the majority of the output current is handled by the BJT. Because of the low current gain of BJT, a MOSFET of equal size is required as a driver. A more powerful approach to obtain the maximum benefits of the MOS gate control and bipolar current conduction is to integrate the physics of MOSFET and BJT within the same semiconductor region. This concept gave rise to the commercially available IGBTs with superior on-state characteristics, good switching speed and excellent safe operating area. Compared to power MOSFETs the absence of the integral body diode can be considered as an advantage or disadvantage depending on the switching speed and current requirements. An external fast recovery diode or a diode in the same package

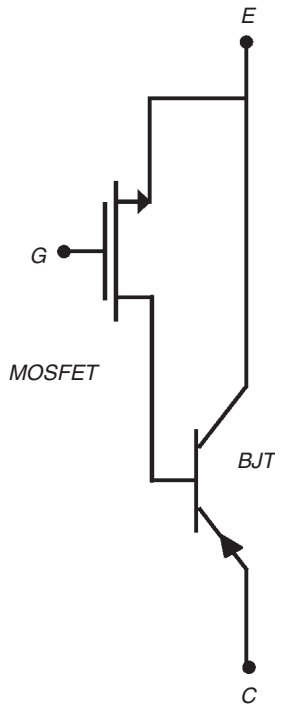

FIGURE 5.1 Hybrid Darlington configuration of MOSFET and BJT.

can be used for specific applications. The IGBTs are replacing MOSFETs in high-voltage applications with lower conduction losses. They have on-state voltage and current density comparable to a power BJT with higher switching frequency. Although they exhibit fast turn-on, their turn-off is slower than a MOSFET because of current fall time. The IGBTs have considerably less silicon area than similar rated power MOSFETs. Therefore by replacing power MOSFETs with IGBTs, the efficiency is improved and cost is reduced. IGBT is also known as conductivity modulated FET (COMFET), insulated gate transistor (IGT), and bipolar-mode MOSFET.

As soft switching topologies offer numerous advantages over the hard switching topologies, their use is increasing in the industry. By the use of soft-switching techniques, IGBTs can operate at frequencies up to hundreds of kilohertz. The IGBTs behave differently under soft switching condition as opposed to hard switching conditions. Therefore, the device tradeoffs involved in soft switching circuits are different than those in hard switching case. Application of IGBTs in high power converters subjects them to high-transient electrical stress such as short circuit and turn-off under clamped inductive load and therefore robustness of IGBTs under stress conditions is an important requirement. Traditionally, there has been limited interaction between device manufacturers and power electronic circuit designers. Therefore, shortcomings of device reliability are observed only after the devices are used in actual circuits. This significantly slows down the process of power electronic system optimization. The development time can be significantly reduced if all issues of device performance and reliability are taken into consideration at the design stage. As high stress conditions are quite frequent in circuit applications, it is extremely cost efficient and pertinent to model the IGBT performance under these conditions. However, development of the model can follow only after the physics of device operation under stress conditions imposed by the circuit is properly understood. Physically based process and device simulations are a quick and cheap way of optimizing the IGBT. The emergence of mixed mode circuit simulators in which semiconductor carrier dynamics is optimized within the constraints of circuit level switching is a key design tool for this task.

5.2 Basic Structure and Operation

The vertical cross section of a half cell of one of the parallel cells of an n-channel IGBT shown in Fig. 5.2 is similar to that of a double diffused power MOSFET (DMOS) except for a p^+ layer at the bottom. This layer forms the IGBT collector and a pn junction with n^- drift region, where conductivity modulation occurs by injecting minority carriers into the drain drift region of the vertical MOSFET. Therefore, the current density is much greater than a power MOSFET and the forward voltage drop is reduced. The p^+ substrate, n^- drift layer, and p^+ emitter constitute a BJT with a wide base region and hence small current gain. The device operation can be explained by a BJT with its base current controlled by the voltage applied to the MOS gate. For simplicity, it is assumed that the emitter terminal is connected to the ground potential. By applying a negative voltage to the collector, the pn junction between the p^+ substrate

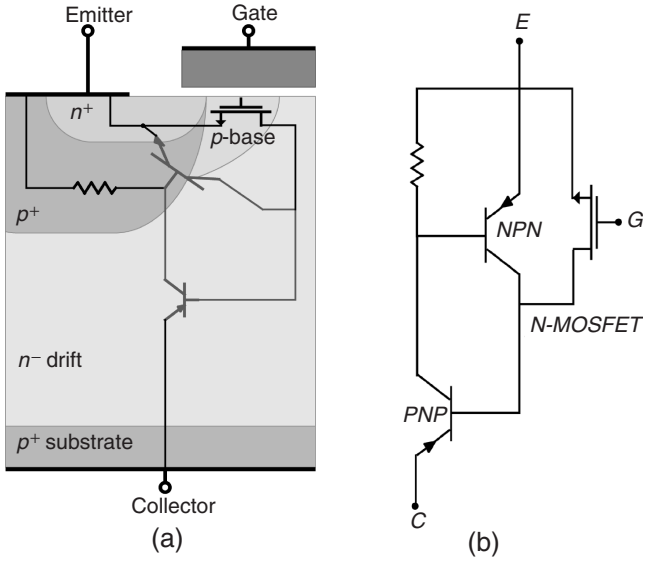

FIGURE 5.2 IGBT: (a) half-cell vertical cross section and (b) equivalent circuit model.

and the n^- drift region is reverse biased which prevents any current flow and the device is in its reverse blocking state. If the gate terminal is kept at ground potential but a positive potential is applied to the collector, the pn junction between the p-base and n^- drift region is reverse biased. This prevents any current flow and the device is in its forward blocking state until the open base breakdown of the pnp transistor is reached.

When a positive potential is applied to the gate and exceeds the threshold voltage required to invert the MOS region under the gate an n channel is formed, which provides a path for electrons to flow into the n^- drift region. The pn junction between the p^+ substrate and n^- drift region is forward biased and holes are injected into the drift region. The electrons in the drift region recombine with these holes to maintain space charge neutrality and the remaining holes are collected at the emitter, causing a vertical current flow between the emitter and collector. For small values of collector potential and a gate voltage larger than the threshold voltage the on-state characteristics can be defined by a wide base power BJT. As the current density increases, the injected carrier density exceeds the low doping of the base region and becomes much larger than the background doping. This conductivity modulation decreases the resistance of the drift region, and therefore IGBT has a much greater current density than a power MOSFET with reduced forward voltage drop. The base–collector junction of the pnp BJT cannot be forward biased, and therefore this transistor will not operate in saturation. But when the potential drop across the inversion layer becomes comparable to the difference between the gate voltage and threshold voltage, channel pinch-off occurs. The pinch-off limits the electron current and as a result the holes injected from the p^+ layer. Therefore, base current saturation causes the collector current to saturate.

Typical forward characteristics of an IGBT as a function of gate potential and IGBT transfer characteristics are shown in Fig. 5.3. The transfer characteristics of IGBT and MOSFET are similar. The IGBT is in the off-state if the gate–emitter potential is below the threshold voltage. For gate voltages greater than the threshold voltage, the transfer curve is linear over most of the drain current range. Gate-oxide breakdown and the maximum IGBT drain current limit the maximum gate–emitter voltage.

To turn-off the IGBT, gate is shorted to the emitter to remove the MOS channel and the base current of the pnp transistor. The collector current is suddenly reduced because the electron current from channel is removed. Then the excess carriers in the n^- drift region decay by electron–hole recombination, which causes a gradual collector current decay. In order to keep the on-state voltage drop low, the excess carrier lifetime must be kept large. Therefore, similar to the other minority carrier devices there is a tradeoff between on-state losses and faster turn-off switching times. In the punch-through (PT) IGBT structure of Fig. 5.4 the switching time is reduced by use of a heavily doped n buffer layer in the drift region near the collector. Because of much higher doping density in the buffer layer, the injection efficiency of the collector junction and the minority carrier lifetime in the base region is reduced. The smaller excess carrier lifetime in the buffer layer sinks the excess holes. This speeds up the removal of holes from the drift region and therefore decreases the turn-off time. Non-punch-through (NPT) IGBTs have higher carrier lifetimes and low doped shallow collector region, which affect their electrical characteristics. In order to prevent punch through, NPT IGBTs have a thicker drift region, which results in a higher base transit time. Therefore in NPT structure carrier lifetime is kept more than that of a PT structure, which causes conductivity modulation of the drift region and reduces the on-state voltage drop.

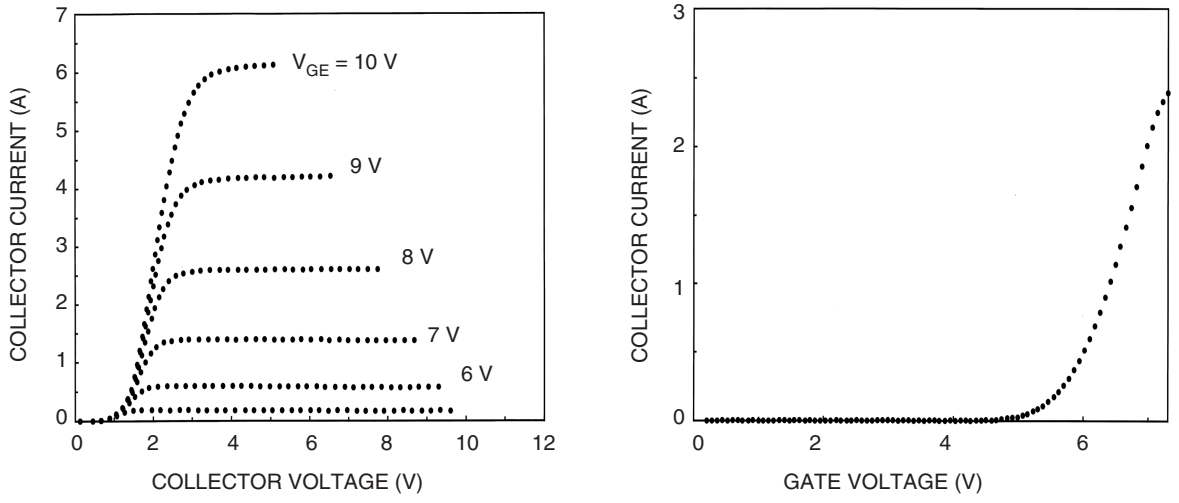

FIGURE 5.3 IGBT: (a) forward characteristics and (b) transfer characteristics.

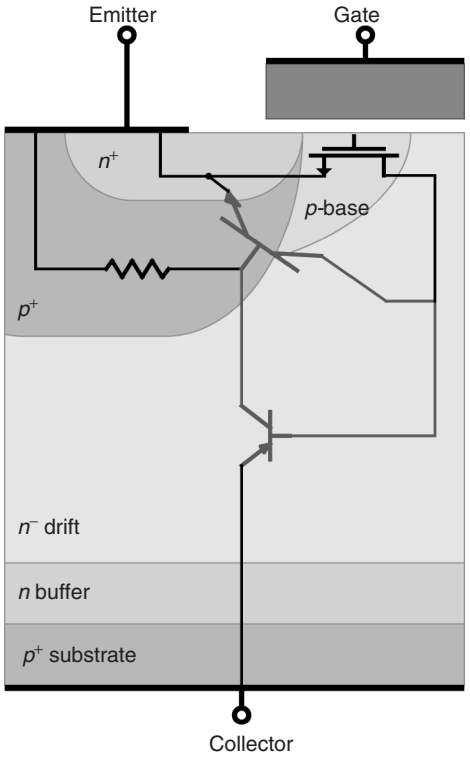

FIGURE 5.4 Punch-through (PT) IGBT structure.

5.3 Static Characteristics

In the IGBT structure of Fig. 5.2, if a negative voltage is applied to the collector, the junction between the p^+ substrate and n^- drift region becomes reverse biased. The drift region is lightly doped and the depletion layer extends principally into the drift region. An open base transistor exists between the p^+ substrate, n^- drift region, and the p-base region. The doping concentration (N_D) and thickness of the n^- drift region (W_D) are designed to avoid the breakdown of this structure. The width of the drift region affects the forward voltage drop and therefore, should be optimized for a desired breakdown voltage. The thickness of the drift region (W_D) is chosen equal to the sum of one diffusion length (L_p) and the width of the depletion layer at maximum applied voltage (V_{max}).

$$W_D = \sqrt{\frac{2\varepsilon_s V_{max}}{qN_D}} + L_P \tag{5.1}$$

When the gate is shorted to the emitter, no channel exists under the gate. Therefore, if a positive voltage is applied to the collector the junction between the p-base and n^- drift region is reverse biased and only a small leakage current flows through IGBT. Similar to a MOSFET the depletion layer extends into the p-base and n^- drift region. The p-base doping concentration, which also controls the threshold voltage is chosen to avoid punch through of the p-base to n^+ emitter. In ac circuit applications, which require identical forward and reverse blocking capability the drift region thickness of the symmetrical IGBT shown in Fig. 5.2 is designed by use of Eq. (5.1) to avoid reach through of the depletion layer to the junction between the p^+ collector and the n^- drift region. When IGBT is used in dc circuits, which do not require reverse blocking capability a highly doped n buffer layer is added to the drift region near the collector junction to form a PT IGBT. In this structure, the depletion layer occupies the entire drift region and the n buffer layer prevents reach through of the depletion layer to the p^+ collector layer. Therefore the required thickness of the drift region is reduced, which reduces the on-state losses. But the highly doped n buffer layer and p^+ collector layer degrade the reverse blocking capability to a very low value. Therefore on-state characteristics of a PT IGBT can be optimized for a required forward blocking capability while the reverse blocking capability is neglected.

When a positive voltage is applied to the gate of an IGBT, an MOS channel is formed between the n^+ emitter and the n^- drift region. Therefore a base current is provided for the parasitic pnp BJT. By applying a positive voltage between the collector and emitter electrodes of an n type IGBT, minority carriers (holes) are injected into the drift region. The injected minority carriers reduce the resistivity of the drift region and reduce the on-state voltage drop resulting in a much higher current density compared to a power MOSFET.

If the shorting resistance between the base and emitter of the npn transistor is small, the n^+ emitter p-base junction does not become forward biased and therefore the parasitic npn transistor is not active and can be deleted from the equivalent IGBT circuit. The analysis of the forward conduction characteristics of an IGBT is possible by the use of two equivalent circuit approaches. The model based on a PiN rectifier in series with a MOSFET, shown in Fig. 5.5b is easy to analyze and gives a reasonable understanding of the IGBT operation. But this model does not account for the hole current component flowing into the p-base region. The junction between the p-base and the n^- drift region is reverse biased. This requires that the free carrier density be zero at this junction, and therefore results in a different boundary condition for IGBT compared to those for PiN rectifier. The IGBT conductivity modulation in the drift region is identical to the PiN rectifier near the collector junction, but it is less than a PiN rectifier near the p-base junction. Therefore, the model based on a bipolar pnp transistor driven by a MOSFET in Fig. 5.5a gives a more complete description of the conduction characteristics.

Analyzing the IGBT operation by the use of these models shows that IGBT has one diode drop due to the parasitic diode. Below the diode knee voltage, there is negligible current flow due to the lack of minority carrier injection from the collector. Also by increasing the applied voltage between the gate and emitter, the base of the internal bipolar transistor is supplied by more base current, which results in an increase in the collector

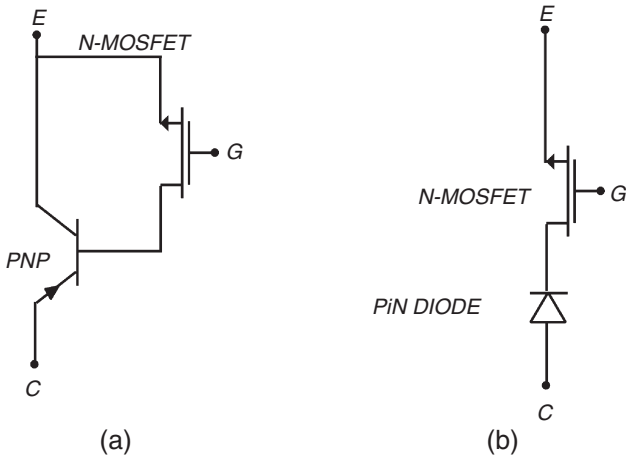

FIGURE 5.5 IGBT equivalent circuits: (a) BJT/MOSFET and (b) PiN/MOSFET.

current. The IGBT current shows saturation due to the pinch-off of the MOS channel. This limits the input base current of the bipolar transistor. The MOS channel of the IGBT reverse biases the collector–base junction and forces the bipolar pnp transistor to operate in its active region. The drift region is in high-level injection at the required current densities and wider n^- drift region results in higher breakdown voltage.

Because of the very low gain of the pnp BJT, the driver MOSFET in the equivalent circuit of the IGBT carries a major portion of the total collector current. Therefore, the IGBT on-state voltage drop as is shown in Fig. 5.6 consists of voltage drop across the collector junction, drift region, and MOSFET portion. The low value of the drift region conductivity modulation near the p-base junction causes a substantial drop across the junction field effect transistor (JFET) resistance of the MOSFET (V_{JFET}) in addition to the voltage drop across the channel resistance (V_{ch}) and the accumulation layer resistance (V_{acc}).

$$V_{CE(on)} = V_{p^+n} + V_{drift} + V_{MOSFET} \tag{5.2}$$

$$V_{MOSFET} = V_{ch} + V_{JFET} + V_{acc} \tag{5.3}$$

When the lifetime in the n^- drift region is large, the gain of the pnp bipolar transistor is high and its collector current is much larger than the MOSFET current and therefore, the voltage drop across the MOSFET component of IGBT is a small fraction of the total voltage drop. When lifetime control techniques are used to increase the switching speed, the current gain of the bipolar transistor is reduced and a greater portion of the current flows through the MOSFET channel and therefore the voltage drop across the MOSFET increases. In order to decrease the resistance of the MOSFET current path, trench IGBTs can be used as shown in Fig. 5.7. Extending the trench gate below the p-base and n^- drift region junction forms a channel between the n^+ emitter and the n^- drift region. This eliminates the JFET and accumulation layer resistance

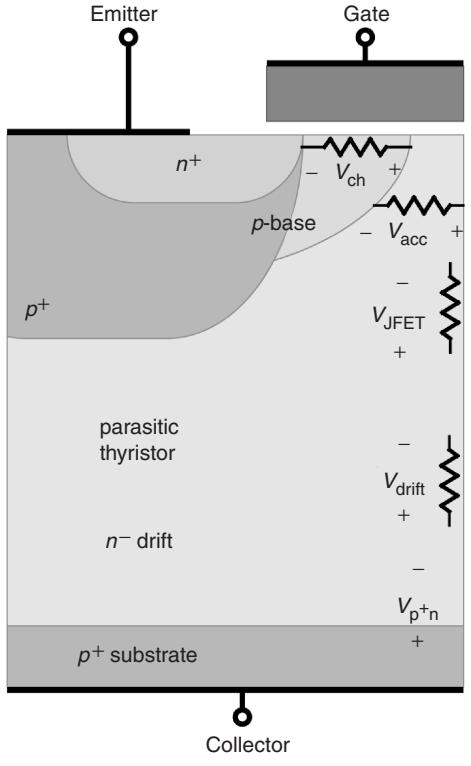

FIGURE 5.6 Components of on-state voltage drop within the IGBT structure.

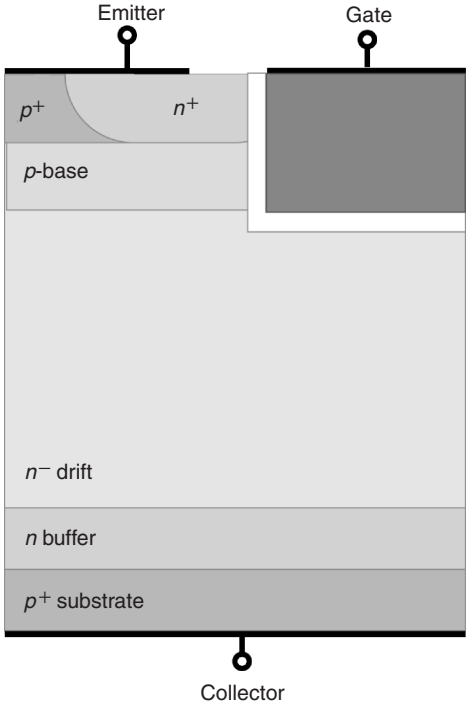

FIGURE 5.7 Trench IGBT structure.

and therefore reduces the voltage drop across the MOSFET component of IGBT, which results in a superior conduction characteristics. By the use of trench structure, the IGBT cell density and latching current density are also improved.

5.4 Dynamic Switching Characteristics

5.4.1 Turn-on Characteristics

The switching waveforms of an IGBT in a clamped inductive circuit are shown in Fig. 5.8. The L/R time constant of the inductive load is assumed to be large compared to the switching frequency and therefore, can be considered as a constant current source I_{on}. The IGBT turn-on switching performance is dominated by its MOS structure. During $t_{d(on)}$, the gate current charges the constant input capacitance with a constant slope until the gate–emitter voltage reaches the threshold voltage $V_{GE(th)}$ of the device. During t_{ri}, load current is transferred from the diode into the device and increases to its steady-state value.

The gate voltage rise time and IGBT transconductance determine the current slope and results as t_{ri}. When the gate–emitter voltage reaches $V_{GE(Ion)}$, which will support the steady-state collector current, collector–emitter voltage starts to decrease. After this there are two distinct intervals, during

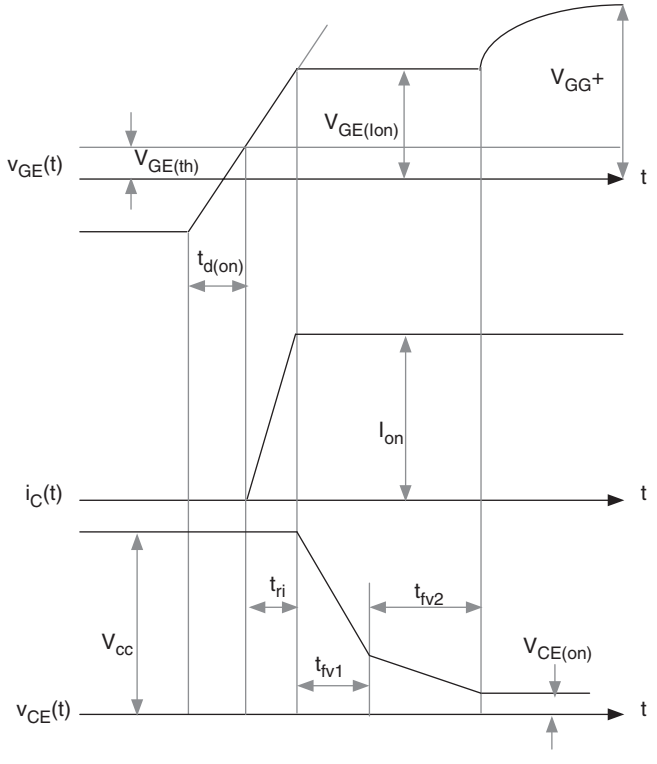

FIGURE 5.8 IGBT turn-on waveforms in a clamped inductive load circuit.

IGBT turn-on. In the first interval, the collector to emitter voltage drops rapidly as the gate–drain capacitance C_{gd} of the MOSFET portion of IGBT discharges. At low collector–emitter voltage C_{gd} increases. A finite time is required for high-level injection conditions to set in the drift region. The pnp transistor portion of IGBT has a slower transition to its on-state than the MOSFET. The gate voltage starts rising again only after the transistor comes out of its saturation region into the linear region, when complete conductivity modulation occurs and the collector–emitter voltage reaches its final on-state value.

5.4.2 Turn-off Characteristics

Turn-off begins by removing the gate–emitter voltage. Voltage and current remain constant until the gate voltage reaches $V_{GE(Ion)}$, required to maintain the collector steady-state current as shown in Fig. 5.9. After this delay time ($t_{d(off)}$) the collector voltage rises, while the current is held constant. The gate resistance determines the rate of collector voltage rise. As the MOS channel turns off, collector current decreases sharply during t_{fi1}. The MOSFET portion of IGBT determines the turn-off delay time $t_{d(off)}$ and the voltage rise time t_{rv}. When the collector voltage reaches the bus voltage, the freewheeling diode starts to conduct.

However the excess stored charge in the n^- drift region during on-state conduction, must be removed for the device to turn-off. The high minority carrier concentration stored in the n^- drift region supports the collector current after the MOS channel is turned off. Recombination of the minority carriers in the wide base region gradually decreases the collector current and results in a current tail. Since there is no access to the base of the pnp transistor, the excess minority carriers cannot be removed by reverse biasing the gate. The t_{fi2} interval is long because the excess carrier lifetime in this region is normally kept high to reduce the on-state voltage drop. Since the collector–emitter voltage has reached the bus voltage in this interval, a significant power loss occurs which increases with frequency. Therefore, the current tail limits the IGBT operating frequency and there is a tradeoff between the on-state losses and faster switching times. For an on-state current of I_{on}, the magnitude of the current tail, and the time required for the collector current to decrease to 10% of its on-state value, turn-off (t_{off}) time, are approximated as:

$$I_c(t) = \alpha_{pnp} I_{on} \mathrm{e}^{-t/\tau_{HL}} \tag{5.4}$$

$$t_{off} = \tau_{HL} \ln(10\alpha_{pnp}) \tag{5.5}$$

where

$$\alpha_{pnp} = \sec h\left(\frac{l}{L_a}\right) \tag{5.6}$$

is the gain of the bipolar pnp transistor, l is the undepleted base width, and L_a is the ambipolar diffusion length and it

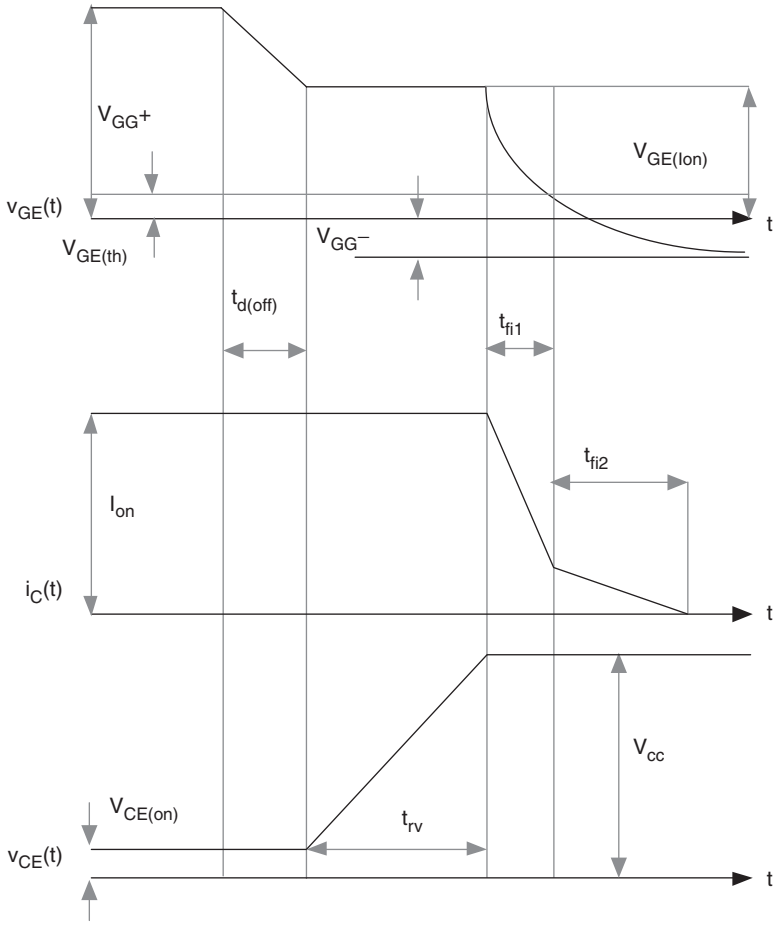

FIGURE 5.9 Switching waveforms during IGBT clamped inductive load turn-off.

is assumed that the high level lifetime (τ_{HL}) is independent of the minority carrier injection during the collector current decay.

Lifetime-control techniques are used to reduce the lifetime (τ_{HL}) and the gain of the bipolar transistor (α_{pnp}). As a result, the magnitude of the current tail and t_{off} decrease. But the conductivity modulation decreases, which increases the on-state voltage drop in the drift region. Therefore, higher speed IGBTs have a lower current rating. Thermal diffusion of impurities such as gold and platinum introduces recombination centers, which reduce the lifetime. The device can also be irradiated with high-energy electrons to generate recombination centers. Electron irradiation introduces a uniform distribution of defects, which results in reduction of lifetime in the entire wafer and affects the conduction properties of the device. Another method of lifetime control is proton implantation, which can place defects at a specific depth. Therefore, it is possible to have a localized control of lifetime to improve the tradeoff between the on-state voltage and switching speed of the device. The turn-off loss can be minimized by curtailing the current tail as a result of speeding up the recombination process in the portion of the drift region, which is not swept by the reverse bias.

5.4.3 Latch-up of Parasitic Thyristor

A portion of minority carriers injected into the drift region from the collector of an IGBT flows directly to the emitter terminal. The negative charge of electrons in the inversion layer attracts the majority of holes and generates the lateral component of hole current through the p-type body layer as shown in Fig. 5.10. This lateral current flow develops a voltage drop across the spreading resistance of the p-base region, which forward biases the base–emitter junction of the npn parasitic BJT. By designing a small spreading resistance, the voltage drop is lower than the built-in potential and therefore the parasitic thyristor between the p^+ collector region, n^- drift region, p-base region, and n^+ emitter does not latch-up. Larger values of on-state current density produce a larger voltage drop, which causes injection of electrons from the emitter region into the p-base region and hence turns on the npn transistor. When this occurs the pnp transistor will turn-on,

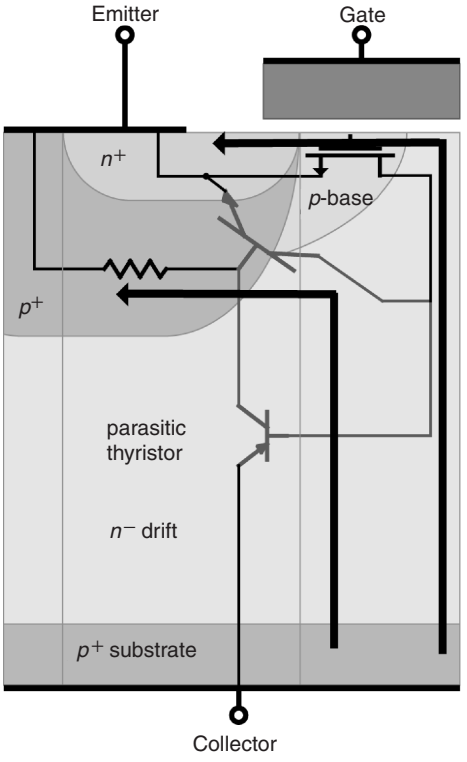

FIGURE 5.10 On-state current flow paths in an IGBT structure.

therefore the parasitic thyristor will latch-up and the gate loses control over the collector current.

Under dynamic turn-off conditions the magnitude of the lateral hole current flow increases and latch-up can occur at lower on-state currents compared to the static condition. The parasitic thyristor latches up when the sum of the current gains of the npn and pnp transistors exceeds one. When the gate voltage is removed from IGBT with a clamped inductive load, its MOSFET component turns off and reduces the MOSFET current to zero very rapidly. As a result the drain–source voltage rises rapidly and is supported by the junction between the n^- drift region and the p-base region. The drift region has a lower doping and therefore the depletion layer extends more in the drift region. As a result the current gain of the pnp transistor portion, α_{pnp} increases and a greater portion of the injected holes into the drift region will be collected at the junction of p-base and n^- drift regions. Therefore, the magnitude of the lateral hole current increases, which increases the lateral voltage drop. As a result the parasitic thyristor will latch-up even if the on-state current is less than the static latch-up value.

Reducing the gain of the npn or pnp transistors can prevent the parasitic thyristor latch-up. A reduction in the gain of the pnp transistor increases the IGBT on-state voltage drop. Therefore in order to prevent the parasitic thyristor latch-up, it is better to reduce the gain of the npn transistor component of IGBT. Reduction of carrier lifetime, use of buffer layer, and use of deep p^+ diffusion improve the latch-up immunity of IGBT. But inadequate extent of the p^+ region may fail to prevent the device from latch-up. Also care should be taken that the p^+ diffusion does not extend into the MOS channel because this causes an increase in the MOS threshold voltage.

5.5 IGBT Performance Parameters

The IGBTs are characterized by certain performance parameters. The manufacturers specify these parameters, which are described below, in the IGBT data sheet. The important ratings of IGBTs are values, which establish either a minimum or maximum limiting capability or limiting condition. The IGBTs cannot be operated beyond the maximum or minimum rating's value, which are determined for a specified operating point and environment condition.

Collector–Emitter blocking voltage (BV_{CES}): This parameter specifies the maximum off-state collector–emitter voltage when the gate and emitter are shorted. Breakdown is specified at a specific leakage current and varies with temperature by a positive temperature coefficient.

Emitter–Collector blocking voltage (BV_{ECS}): This parameter specifies the reverse breakdown of the collector–base junction of the pnp transistor component of IGBT.

Gate–Emitter voltage (V_{GES}): This parameter determines the maximum allowable gate–emitter voltage, when collector is shorted to emitter. The thickness and characteristics of the gate-oxide layer determine this voltage. The gate voltage should be limited to a much lower value to limit the collector current under fault conditions.

Continuous collector current (I_C): This parameter represents the value of the dc current required to raise the junction to its maximum temperature, from a specified case temperature. This rating is specified at a case temperature of 25°C and maximum junction temperature of 150°C. Since normal operating condition cause higher case temperatures, a plot is given to show the variation of this rating with case temperature.

Peak collector repetitive current (I_{CM}): Under transient conditions, the IGBT can withstand higher peak currents compared to its maximum continuous current, which is described by this parameter.

Maximum power dissipation (P_D): This parameter represents the power dissipation required to raise the junction temperature to its maximum value of 150°C, at a case temperature of 25°C. Normally a plot is provided to show the variation of this rating with temperature.

Junction temperature (T_j): Specifies the allowable range of the IGBT junction temperature during its operation.

Clamped inductive load current (I_{LM}): This parameter specifies the maximum repetitive current that IGBT can turn-off under a clamped inductive load. During IGBT turn-on, the reverse recovery current of the freewheeling diode in parallel with the inductive load increases the IGBT turn-on switching loss.

Collector–Emitter leakage current (I_{CES}): This parameter determines the leakage current at the rated voltage and specific temperature when the gate is shorted to emitter.

Gate–Emitter threshold voltage ($V_{GE(th)}$): This parameter specifies the gate–emitter voltage range, where the IGBT is turned on to conduct the collector current. The threshold voltage has a negative temperature coefficient. Threshold voltage increases linearly with gate-oxide thickness and as the square root of the p-base doping concentration. Fixed surface charge at the oxide–silicon interface and mobile ions in the oxide shift the threshold voltage.

Collector–Emitter saturation voltage ($V_{CE(SAT)}$): This parameter specifies the collector–emitter forward voltage drop and is a function of collector current, gate voltage, and temperature. Reducing the resistance of the MOSFET channel and JFET region, and increasing the gain of the pnp bipolar transistor can minimize the on-state voltage drop. The voltage drop across the MOSFET component of IGBT, which provides the base current of the pnp transistor is reduced by a larger channel width, shorter channel length, lower threshold voltage, and wider gate length. Higher minority carrier lifetime and a thin n-epi region cause high carrier injection and reduce the voltage drop in the drift region.

Forward transconductance (g_{FE}): Forward transconductance is measured with a small variation on the gate voltage, which linearly increases the IGBT collector current to its rated current at 100°C. The transconductance of an IGBT is reduced at currents much higher than its thermal handling capability. Therefore, unlike the bipolar transistors, the current handling capability of IGBTs is limited by thermal consideration and not by its gain. At higher temperatures, the transconductance starts to decrease at lower collector currents. Therefore, these features of transconductance protects the IGBT under short circuit operation.

Total gate charge (Q_G): This parameter helps to design a suitable size gate drive circuit and approximately calculate its losses. Because of the minority carrier behavior of device, the switching times cannot be approximately calculated by the use of gate charge value. This parameter varies as a function of the gate–emitter voltage.

Turn-on delay time (t_d): It is defined as the time between 10% of gate voltage and 10% of the final collector current.

Rise time (t_r): It is the time required for the collector current to increase to 90% of its final value from 10% of its final value.

Turn-off delay time ($t_{d(off)}$): It is the time between 90% of gate voltage and 10% of final collector voltage.

Fall time (t_f): It is the time required for the collector current to drop from 90% of its initial value to 10% of its initial value.

Input capacitance (C_{ies}): It is the measured gate–emitter capacitance when collector is shorted to emitter. The input capacitance is the sum of the gate–emitter and the miller capacitance. The gate–emitter capacitance is much larger than the miller capacitance.

Output capacitance (C_{oes}): It is the capacitance between collector and emitter when gate is shorted to the emitter, which has the typical pn junction voltage dependency.

Reverse transfer capacitance (C_{res}): It is the miller capacitance between gate and collector, which has a complex voltage dependency.

Safe operating area (SOA): The safe operating area determines the current and voltage boundary within which the IGBT can be operated without destructive failure. At low currents the maximum IGBT voltage is limited by the open base transistor breakdown. The parasitic thyristor latch-up limits the maximum collector current at low voltages. The IGBTs immune to static latch-up may be vulnerable to dynamic latch-up. Operation in short circuit and inductive load switching are conditions that would subject an IGBT to a combined voltage and current stress. Forward biased safe operating area (FBSOA) is defined during the turn-on transient of the inductive load switching when both electron and hole current flow in the IGBT in the presence of high voltage across the device. The reverse biased safe operating area (RBSOA) is defined during the turn-off transient, where only hole current flows in the IGBT with high voltage across it.

If the time duration of simultaneous high voltage and high current is long enough, the IGBT failure will occur because of thermal breakdown. But if this time duration is short, the temperature rise due to power dissipation will not be enough to cause thermal breakdown. Under this condition the avalanche breakdown occurs at voltage levels lower than the breakdown voltage of the device. Compared to the steady-state forward blocking condition the much larger charge in the drift region causes a higher electric field and narrower depletion region at the p-base and n^- drift junction. Under RBSOA conditions there is no electron in the space charge region, and therefore there is a larger increase in electric field than the FBSOA condition.

The IGBT SOA is indicated in Fig. 5.11. Under short-switching times the rectangular SOA shrinks by increase in

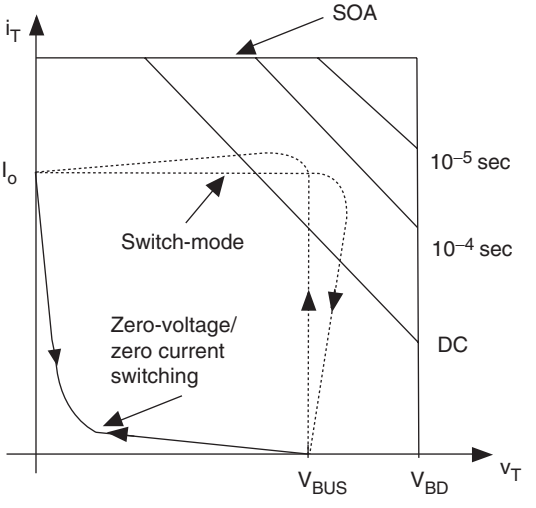

FIGURE 5.11 IGBT safe operating area (SOA).

the duration of on-time. Thermal limitation is the reason for smaller SOA and the lower limit is set by dc operating conditions. The device switching loci under hard switching (dashed lines) and zero voltage or zero current switching (solid lines) is also indicated in Fig. 5.11. The excursion is much wider for switch-mode hard-switching applications than for the soft-switching case, and therefore a much wider SOA is required for hard-switching applications. Presently IGBTs are optimized for hard-switching applications. In soft-switching applications the conduction losses of IGBT can be optimized at the cost of smaller SOA. In this case the p-base doping can be adjusted to result in a much lower threshold voltage and hence forward voltage drop. But in hard-switching applications, the SOA requirements dominate over forward voltage drop and switching time. Therefore, the p-base resistance should be reduced, which causes a higher threshold voltage. As a result, the channel resistance and forward voltage drop will increase.

5.6 Gate Drive Requirements

The gate drive circuit acts as an interface between the logic signals of the controller and the gate signals of the IGBT, which reproduces the commanded switching function at a higher power level. Non-idealities of the IGBT such as finite voltage and current rise and fall times, turn-on delay, voltage and current overshoots, and parasitic components of the circuit cause differences between the commanded and real waveforms. Gate drive characteristics affect the IGBT non-idealities. The MOSFET portion of the IGBT drives the base of the pnp transistor and therefore the turn-on transient and losses is greatly affected by the gate drive.

Due to lower switching losses, soft-switched power converters require gate drives with higher power ratings. The IGBT gate drive must have sufficient peak current capability to provide the required gate charge for zero current switching and zero voltage switching. The delay of the input signal to the gate drive should be small compared to the IGBT switching period and therefore, the gate drive speed should be designed properly to be able to use the advantages of faster switching speeds of the new generation IGBTs.

5.6.1 Conventional Gate Drives

The first IGBT gate drives used fixed passive components and were similar to MOSFET gate drives. Conventional gate drive circuits use a fixed gate resistance for turn-on and turn-off as shown in Fig. 5.12. The turn-on gate resistor R_{gon} limits the maximum collector current during turn-on, and the turn-off gate resistor R_{goff} limits the maximum collector–emitter voltage. In order to decouple the dv_{ce}/dt and di_c/dt control, an external capacitance C_g can be used at the gate, which increases the time constant of the gate circuit and reduces the di_c/dt as shown in Fig. 5.13. But C_g does not affect the dv_{ce}/dt

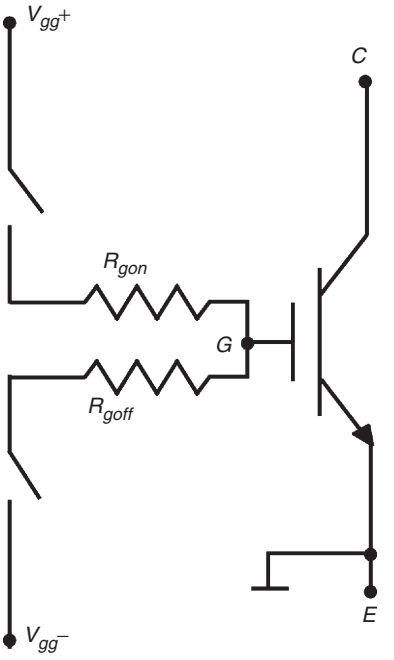

FIGURE 5.12 Gate drive circuit with independent turn-on and turn-off resistors.

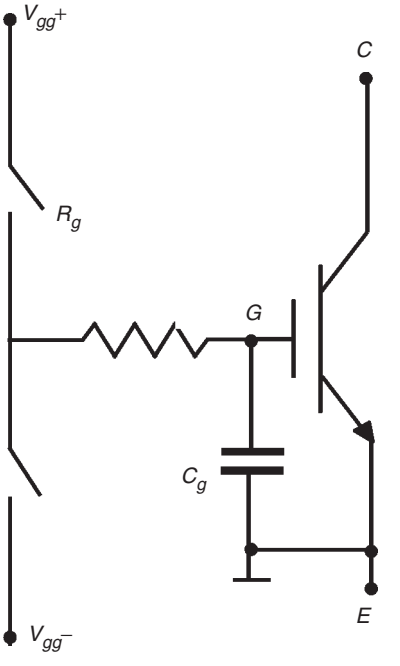

FIGURE 5.13 External gate capacitor for decoupling dv_{ce}/dt and di_c/dt during switching transient.

transient, which occurs during the miller plateau region of the gate voltage.

5.6.2 New Gate Drive Circuits

In order to reduce the delay time required for the gate voltage to increase from V_{gg-} to $V_{ge}(th)$, the external gate capacitor can be introduced in the circuit only after V_{ge} reaches $V_{ge}(th)$ as is shown in Fig. 5.14, where the collector current rise occurs. The voltage tail during turn-on transient is not affected by this method. In order to prevent shoot through caused by accidental turn-on of IGBT due to noise, a negative gate voltage is required during off-state. Low gate impedance reduces the effect of noise on gate.

During the first slope of the gate voltage turn-on transient, the rate of charge supply to the gate determines the collector current slope. During the miller effect zone of the turn-on transient the rate of charge supply to the gate determines the collector voltage slope. Therefore, the slope of the collector current, which is controlled by the gate resistance, strongly affects the turn-on power loss. Reduction in switching power loss requires low gate resistance. But the collector current slope also determines the amplitude of the conducted electromagnetic interference (EMI) during turn-on switching transient. Lower EMI generation requires higher values of gate resistance. Therefore, in conventional gate drive circuits by selecting an optimum value for R_g, there is a tradeoff between lower switching losses and lower EMI generation.

But the turn-off switching of IGBT depends on the bipolar characteristics. Carrier lifetime determines the rate at which the minority carriers stored in the drift region recombine. The charge removed from the gate during turn-off has small influence on minority carrier recombination. The tail current and di/dt during turn-off, which determine the turn-off losses, depend mostly on the amount of stored charge and the minority carriers lifetime. Therefore, the gate drive circuit has a minor influence on turn-off losses of the IGBT, while it affects the turn-on switching losses.

The turn-on transient is improved by use of the circuit shown in Fig. 5.15. The additional current source increases the gate current during the tail voltage time, and therefore reduces the turn-on loss. The initial gate current is determined by $V_{gg}+$ and R_{gon}, which are chosen to satisfy device electrical specifications and EMI requirements. After the collector current reaches its maximum value, the miller effect occurs and the controlled current source is enabled to increase the gate current to increase the rate of collector voltage fall. This reduces the turn-on switching loss. Turn-off losses can only be reduced during the miller effect and MOS turn-off portion of the turn-off transient, by reducing the gate resistance. But this increases the rate of change of collector voltage, which strongly affects the IGBT latching current and RBSOA. During the turn-off

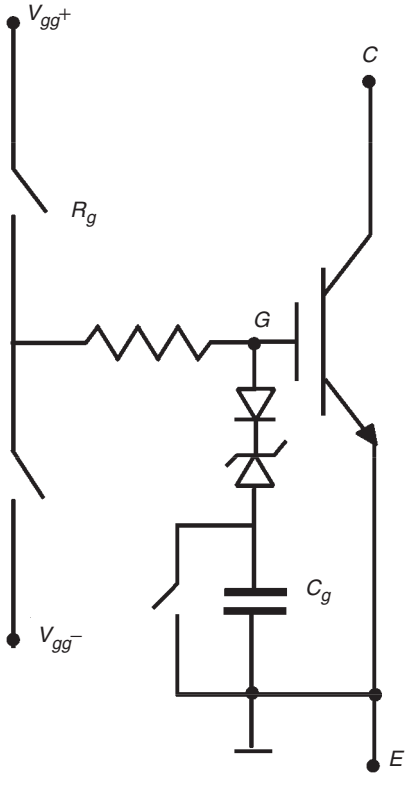

FIGURE 5.14 A circuit for reducing the turn-on delay.

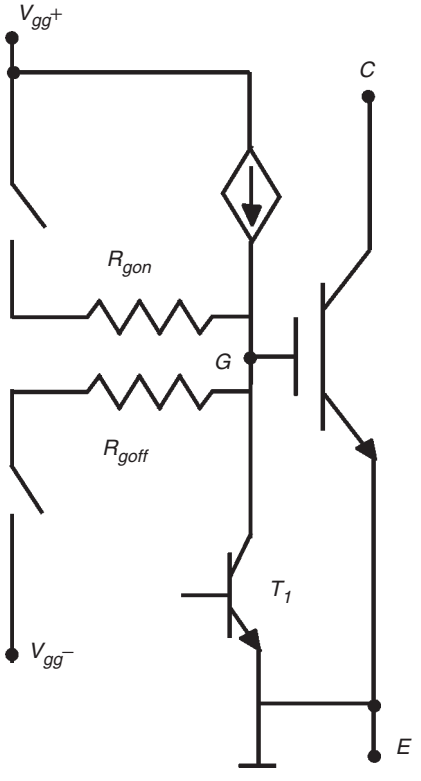

FIGURE 5.15 Schematic circuit of an IGBT gate drive circuit.

period, the turn-off gate resistor R_{goff} determines the maximum rate of collector voltage change. After the device turns off, turning on transistor T_1 prevents the spurious turn-on of IGBT by preventing the gate voltage to reach the threshold voltage.

5.6.3 Protection

Gate drive circuits can also provide fault protection of IGBT in the circuit. The fault protection methods used in IGBT converters are different from their gate turn-off thyristor (GTO) counterparts. In a GTO converter, a crowbar is used for protection and as a result there is no current limiting. When the short circuit is detected the control circuit turns on all the GTO switches in the converter, which results in the opening of a fuse or circuit breaker on the dc input. Therefore, series di/dt snubbers are required to prevent rapid increase of the fault current and the snubber inductor has to be rated for large currents in the fault condition. But IGBT has an important ability to intrinsically limit the current under over-current and short circuit fault conditions. However, the value of the fault current can be much larger than the nominal IGBT current. Therefore, IGBT has to be turned off rapidly after the fault occurs. The magnitude of the fault current depends on the positive gate bias voltage V_{gg+}. A higher V_{gg+} is required to reduce conduction loss in the device, but this leads to larger fault currents. In order to decouple the tradeoff limitation between conduction loss and fault current level, a protection circuit can reduce the gate voltage when a fault occurs. But this does not limit the peak value of the fault current, and therefore, a fast fault detection circuit is required to limit the peak value of the fault current. Fast integrated sensors in the gate drive circuit are essential for proper IGBT protection.

Various methods have been studied to protect IGBTs under fault conditions. One of the techniques uses a capacitor to reduce the gate voltage when the fault occurs. But depending on the initial condition of the capacitor and its value the IGBT current may reduce to zero and then turned on again. Another method is to softly turn-off the IGBT after the fault and to reduce the over-voltage due to di_c/dt. Therefore the over-voltage on IGBT caused by the parasitic inductance is limited while turning off large currents. The most common method of IGBT protection is the collector voltage monitoring or desat detection. The monitored parameter is the collector–emitter voltage, which makes fault detection easier compared to measuring the device current. But voltage detection can be activated only after the complete turn-on of IGBT. If the fault current increases slowly due to large fault inductance, the fault detection is difficult because the collector–emitter voltage will not change significantly. In order to determine whether the current that is being turned off is over-current or nominal current, the miller voltage plateau level can be used. This method can be used to initiate soft turn-off and reduce the over-voltage during over-currents.

Special sense IGBTs have been introduced at low power levels with a sense terminal to provide a current signal proportional to the IGBT collector current. A few active device cells are used to mirror the current carried by the other cells. But unfortunately, sense IGBTs are not available at high power levels and there are problems related to the higher conduction losses in the sense device. The most reliable method to detect an over-current fault condition is to introduce a current sensor in series with the IGBT. The additional current sensor makes the power circuit more complex and may lead to parasitic bus inductance, which results in higher over-voltages during turn-off.

After the fault occurs, the IGBT has to be safely turned off. Due to large di_c/dt during turn-off, the over-voltage can be very large. Therefore, many techniques have been investigated to obtain soft turn-off. The most common method is to use large turn-off gate resistor when the fault occurs. Another method to reduce the turn-off over-voltage is to lower the fault current level by reducing the gate voltage before initiating the turn-off. A resistive voltage divider can be used to reduce the gate voltage during fault turn-off. For example, the gate voltage reduction can be obtained by turning on simultaneously R_{goff} and R_{gon} in the circuit of Fig. 5.12. Another method is to switch a capacitor into the gate and rapidly discharge the gate during the occurrence of a fault. To prevent the capacitor from charging back up to the nominal on-state gate voltage, a large capacitor should be used, which may cause a rapid gate discharge. Also a zener can be used in the gate to reduce the gate voltage after a fault occurs. But the slow transient behavior of the zener leads to large initial peak fault current. The power dissipation during a fault determines the time duration that the fault current can flow in the IGBT without damaging it. Therefore, the IGBT fault endurance capability is improved by the use of fault current limiting circuits to reduce the power dissipation in the IGBT under fault conditions.

5.7 Circuit Models

High-quality IGBT model for circuit simulation is essential for improving the efficiency and reliability in the design of power electronic circuits. Conventional models for power semiconductor devices simply described an abrupt or linear switching behavior and a fixed resistance during the conduction state. Low switching frequencies of power circuits made it possible to use these approximate models. But moving to higher switching frequencies to reduce the size of a power electronic system requires high-quality power semiconductor device models for circuit simulation.

The n-channel IGBT consists of a pnp bipolar transistor whose base current is provided by an n-channel MOSFET, as is shown in Fig. 5.1. Therefore, the IGBT behavior is determined by the physics of the bipolar and MOSFET devices.

Several effects dominate the static and dynamic device characteristics. The influence of these effects on low-power semiconductor device is negligible and therefore they cannot be described by standard device models. The conventional circuit models were developed to describe the behavior of low power devices, and therefore were not adequate to be modified for IGBT. The reason is that the bipolar transistor and MOSFET in the IGBT have a different behavior compared to their low-power counterparts and have different structures.

The present available models have different levels of accuracy at the expense of speed. Circuit issues such as switching losses and reliability are strongly dependent on the device and require accurate device models. But simpler models are only adequate for system oriented issues such as the behavior of an electric motor driven by a pulse width modulation (PWM) converter. Finite element models have high accuracy, but are slow and require internal device structure details. Macro models are fast but have low accuracy, which depends on the operating point. Recently commercial circuit simulators have introduced one-dimensional physics-based models, which offer a compromise between the finite element models and macro models. The Hefner model and the Kraus model are such examples that have been implemented in Saber and there has been some effort to implement them in PSPICE. The Hefner model depends on the redistribution of charge in the drift region during transients. The Kraus model depends on the extraction of charge from the drift region by the electric field and emitter back injection.

The internal BJT of the IGBT has a wide base, which is lightly doped to support the depletion region to have high blocking voltages. The excess carrier lifetime in the base region is low to have fast turn-off. But low power bipolar transistors have high excess carrier lifetime in the base, narrow base, and high current gain. A finite base transit time is required for a change in the injected base charge to change the collector current. Therefore, quasi-static approximation cannot be used at high speeds and the transport of carriers in the base should be described by ambipolar transport theory.

5.7.1 Input and Output Characteristics

The bipolar and MOSFET components of a symmetric IGBT are shown in Fig. 5.16. The components between the emitter (e), base (b), and collector (c) terminals correspond to the bipolar transistor and those between gate (g), source (s), and drain (d) are associated with MOSFET. The combination of the drain–source and gate–drain depletion capacitances is identical to the base–collector depletion capacitance, and therefore they are shown for the MOSFET components. The gate-oxide capacitance of the source overlap (C_{oxs}) and source metallization capacitance (C_m) form the gate–source capacitance (C_{gs}). When the MOSFET is in its linear region the gate-oxide capacitance of the drain overlap (C_{oxd}) forms the gate–drain capacitance (C_{gd}). In the saturation region of

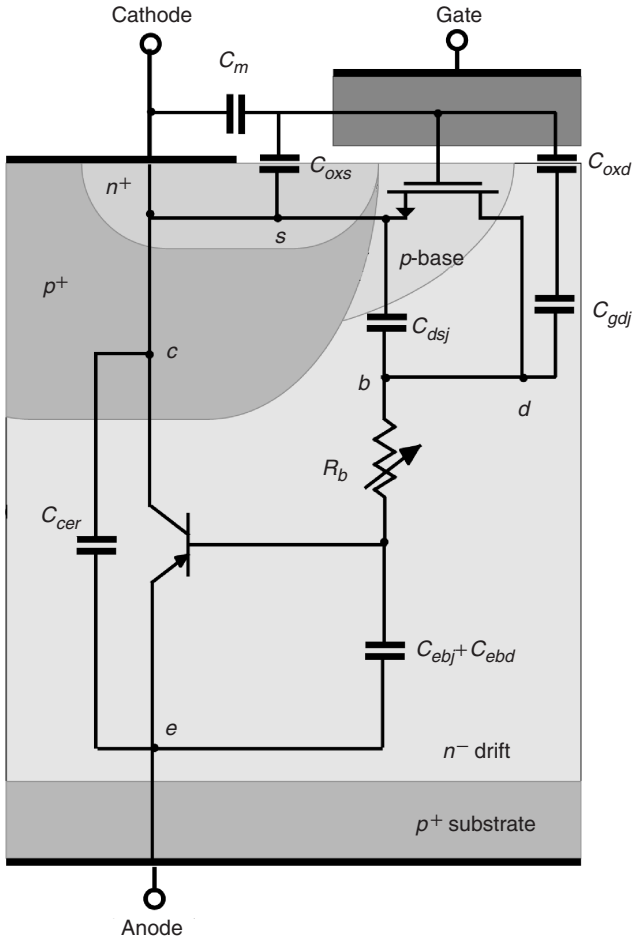

FIGURE 5.16 Symmetric IGBT half cell.

MOSFET the equivalent series connection of gate–drain overlap oxide capacitance and the depletion capacitance of the gate–drain overlap (C_{gdj}) forms the gate–drain miller capacitance. The gate–drain depletion width and the drain–source depletion width are voltage dependent, which has the same effect on the corresponding capacitances.

The most important capacitance in IGBT is the capacitance between the input terminal (g) and output terminal (a), because the switching characteristics is affected by this feedback.

$$C_{ga}\frac{dQ_g}{dv_{ga}} = C_{ox}\frac{dv_{ox}}{dv_{ga}} \tag{5.7}$$

C_{ox} is determined by the oxide thickness and device area. The accumulation, depletion, and inversion states below the gate cause different states of charge and therefore different capacitance values.

The stored charge in the lightly doped wide base of the bipolar component of IGBT causes switching delays and switching losses. The standard quasi-static charge description

is not adequate for IGBT because it assumes that the charge distribution is a function of the IGBT terminal voltage. But the stored charge density ($P(x,t)$) changes with time and position and therefore the ambipolar diffusion equation must be used to describe the charge variation.

$$\frac{dP(x,t)}{dt} = -\frac{P(x,t)}{\tau_a} + D_a \frac{d^2P(x,t)}{dx^2} \tag{5.8}$$

The slope of the charge carrier distribution determines the sum of electron and hole currents. The non-quasi-static behavior of the stored charge in the base of the bipolar component of IGBT results in the collector–emitter redistribution capacitance (C_{cer}). This capacitance dominates the output capacitance of IGBT during turn-off and describes the rate of change of base–collector depletion layer with the rate of change of base–collector voltage. But the base–collector displacement current is determined by the gate–drain (C_{gdj}) and drain–source (C_{dsj}) capacitance of the MOSFET component.

5.7.2 Implementing the IGBT Model into a Circuit Simulator

Usually a netlist is used in a circuit simulator such as Saber to describe an electrical circuit. Each component of the circuit is defined by a model template with the component terminal connection and the model parameters values. While Saber libraries provide some standard component models, the models can be generated by implementing the model equations in a defined saber template. Electrical component models of IGBT are defined by the current through each component element as a function of component variables, such as terminal and internal node voltages and explicitly defined variables. The circuit simulator uses the Kirchhoff's current law to solve for electrical component variables such that the total current into each node is equal to zero, while satisfying the explicitly defined component variables needed to describe the state of the device.

The IGBT circuit model is generated by defining the currents between terminal nodes as a non-linear function of component variables and their rate of change. An IGBT circuit model is shown in Fig. 5.17. Compared to Fig. 5.16, the bipolar transistor is replaced by the two base and collector current sources. There is a distributed voltage drop due to diffusion and drift in the base regions. The drift terms in the ambipolar diffusion equation depends on base and collector currents. Therefore, both of these currents generate the resistive voltage drop V_{ae} and R_b is placed at the emitter-terminal in the IGBT circuit model. The capacitance of the emitter–base junction (C_{eb}) is implicitly defined by the emitter–base voltage as a function of base charge. I_{ceb} is the emitter–base capacitor current which defines the rate of change of the base charge. The current through the collector–emitter redistribution capacitance (I_{ccer}) is part of the collector current, which in contrast

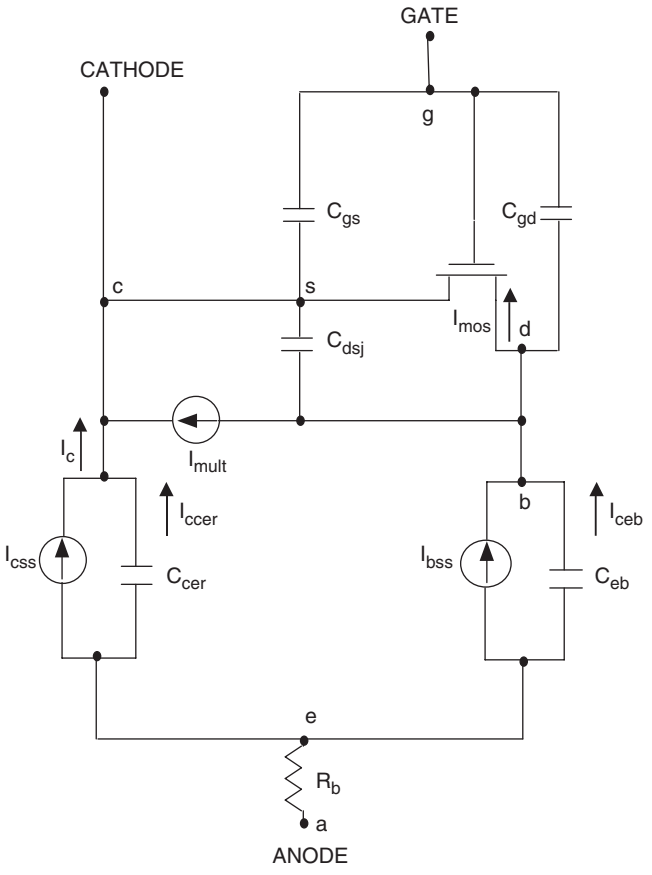

FIGURE 5.17 IGBT circuit model.

to I_{css} depends on the rate of change of the base–emitter voltage. I_{bss} is part of the base current that does not flow through C_{eb} and does not depend on rate of change of base–collector voltage.

Impact ionization causes carrier multiplication in the high electric field of the base–collector depletion region. This carrier multiplication generates an additional base–collector current component (I_{mult}), which is proportional to I_c, I_{mos}, and the multiplication factor. The resulting Saber IGBT model should be able to describe accurately the experimental results for the range of static and dynamic conditions where IGBT operates. Therefore, the model can be used to describe the steady-state and dynamic characteristics under various circuit conditions.

The present available models have different levels of accuracy at the expense of speed. Circuit issues such as switching losses and reliability are strongly dependent on the device and require accurate device models. But simpler models are adequate for system oriented issues such as the behavior of an electric motor driven by a PWM converter. Finite element models have high accuracy, but are slow and require internal device structure details. Macro models are fast but have low accuracy, which depends on the operating point. Recently commercial circuit simulators have introduced one-dimensional

physics-based models, which offer a compromise between the finite element models and macro models.

5.8 Applications

Power electronics evolution is a result of the evolution of power semiconductor devices. Applications of power electronics are still expanding in industrial and utility systems. A major challenge in designing power electronic systems is a simultaneous operation at high power and high-switching frequency. The advent of IGBTs has revolutionized power electronics by extending the power and frequency boundary. During the last decade, the conduction and switching losses of IGBTs has been reduced in the process of transition from the first to the third generation IGBTs. The improved charcteristics of the IGBTs have resulted in higher switching speed and lower energy losses. High voltage IGBTs are expected to take the place of high voltage GTO thyristor converters in the near future. To advance the performance beyond the third generation IGBTs, the fourth generation devices will require exploiting fine-line lithographic technology and employing the trench technology used to produce power MOSFETs with very low on-state resistance. Intelligent IGBT or intelligent power module (IPM) is an attractive power device integrated with circuits to protect against over-current, over-voltage, and over-heat. The main application of IGBT is for use as a switching component in inverter circuits, which are used in both power supply and motor-drive applications. The advantages of using IGBT in these converters are simplicity and modularity of the converter, simple gate drive, elimination of snubber circuits due to the square SOA, lower switching loss, improved protection characteristics in case of over-current and short circuit fault, galvanic isolation of the modules, and simpler mechanical construction of the power converter. These advantages have made the IGBT the preferred switching device in the power range below 1 MW.

Power supply applications of IGBTs include uninterruptible power supplies (UPS) as is shown in Fig. 5.18, constant voltage, constant frequency power supplies, induction heating systems, switch mode power supplies, welders (Fig. 5.19), cutters, traction power supplies, and medical equipment (CT, X-ray). Low noise operation, small size, low cost, and high accuracy are chracteristics of the IGBT converters in these applications. Examples of motor-drive applications include variable voltage, variable frequency inverter as is shown in Fig. 5.20. The IGBTS have been recently introduced at high voltage and current levels, which has enabled their use in high power converters utilized for medium voltage motor drives. The improved characteristics of the IGBTs have introduced power converters in megawatt power applications such as traction drives. One of the critical issues in realizing high power

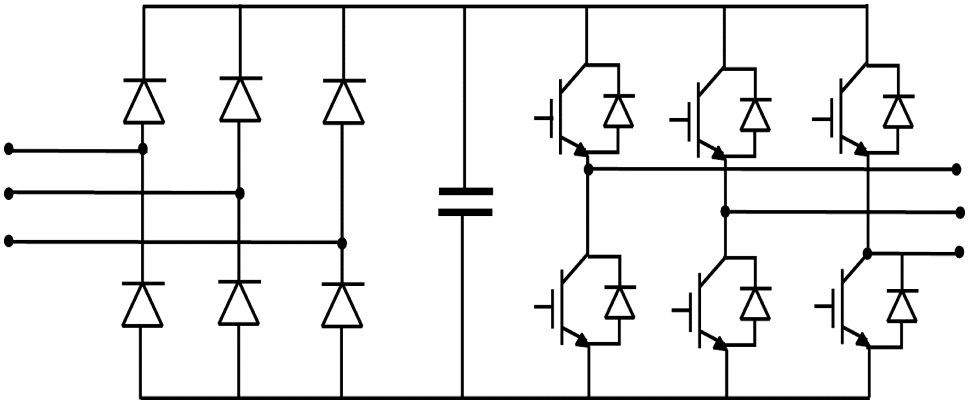

FIGURE 5.18 Constant voltage, constant frequency inverter (UPS).

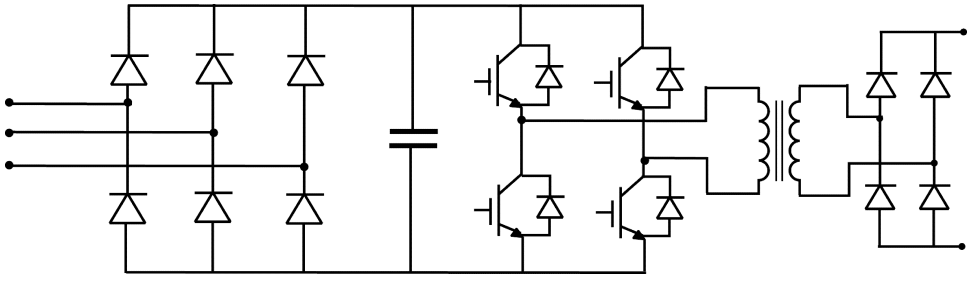

FIGURE 5.19 IGBT welder.

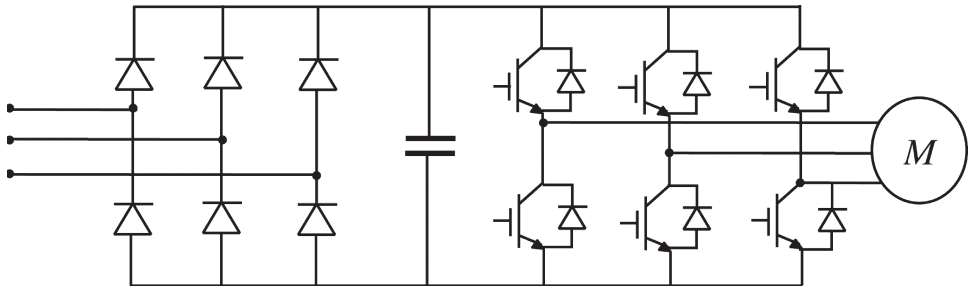

FIGURE 5.20 Variable voltage, variable frequency inverter (PWM).

converters is the reliability of the power switches. The devices used in these applications must be robust and capable of withstanding faults long enough for a protection scheme to be activated. The hard switching voltage source power converter is the most commonly used topology. In this switch-mode operation, the switches are subjected to high switching stresses and high switching power loss that increases linearly with the switching frequency of the PWM. The resulting switching loci in the v_t–i_t plane is shown by the dotted lines in Fig. 5.11. Because of simultaneous large switch voltage and large switch current, the switch must be capable of withstanding high switching stresses with a large SOA. The requirement of being able to withstand large stresses results in design compromises in other characteristics of the power semiconductor device. Often forward voltage drop and switching speed are sacrificed for enhanced short circuit capability. Process parameters of the IGBT such as threshold voltage, carrier lifetime, and the device thickness can be varied to obtain various combinations of SOA, on-state voltage, and switching time. However, there is very little overlap in the optimum combination for more than one performance parameter. Therefore, improved performance in one parameter is achieved at the cost of other parameters.

In order to reduce the size, the weight, and the cost of circuit components used in a power electronics converter very high-switching frequencies of the order of few megahertz are being contemplated. In order to be able to increase the switching frequency, the problems of switch stresses, switching losses, and the EMI associated with switch-mode applications need to be overcome. Use of soft-switching converters reduces the problems of high dv/dt and high di/dt by the use of external inductive and capacitive components to shape the switching trajectory of device. The device switching loci resulting from soft switching is shown in Fig. 5.11, where significant reduction in switching stress can be noticed. The traditional snubber circuits achieves this goal without the added control complexity, but the power dissipation in these snubber circuits can be large and limit the switching frequency of the converter. Also passive components significantly add to the size, weight, and cost of the converter at high power levels. Soft switching uses lossless resonant circuits, which overcomes the problem of power loss in the snubber circuit, but increases the conduction loss. Resonant transition circuits eliminate the problem of high peak device stress in the soft-switched converters. The main drawback of these circuits is the increased control complexity required to obtain the resonant switching transition. The large number of circuit variables that have to be sensed in such power converters can affect their reliability. Short circuit capability no longer being the primary concern, designers can push the performance envelope for their circuits until the device becomes the limiting factor once again.

The transient response of the conventional volts/hertz induction motor drive is sluggish, because both torque and flux are functions of stator voltage and frequency. Use of vector or field oriented control methods makes the performance of the induction motor drive almost identical to that of a separately excited dc motor. Therefore, the transient response is like a dc machine, where torque and flux can be controlled in a decoupled manner. Vector controlled induction motors with shaft encoders or speed sensors have been widely applied in combination with voltage source PWM inverters using IGBT modules. According to the specification of the new products, vector controlled induction motor drive systems ranging from kilowatts to megawatts provide a broad range of speed control, constant torque operation, and high starting torque.

Because of their simple gate drives and modular packaging, IGBTs lead to simpler construction of power electronic circuits. This feature has lead to a trend to standardize and modularize power electronic circuits. Simplification of the overall system design and construction and significant cost reduction are the main implications of this approach. With these goals the power electronics building block (PEBB) program has been introduced, where the entire power electronic converter system is reduced to a single block. Similar modular power electronic blocks are commercially available at low power levels in the form of power integrated circuits. At higher power levels, these blocks have been realized in the form of intelligent power modules and power blocks. But these high power modules do not encompass the entire power electronic systems like motor drives and UPS. The aim of the PEBB program is to realize the whole power handling system within standardized blocks. A PEBB is a universal power processor

that changes any electrical power input to any desired form of voltage, current, and frequency output. A PEBB is a single package with a multi-function controller that replaces the complex power electronic circuits with a single device and therefore reduces the development and design costs of the complex power circuits and simplifies the development and design of large electric power systems.

The applications of power electronics are varied and various applications have their own specific design requirement. There is a wide choice of available power devices. Because of physical, material, and design limitations, none of the presently available devices behave as an ideal switch, which should block arbitrarily large forward and reverse voltages with zero current in the off-state, conduct arbitrarily large currents with zero voltage drop in the on-state, and have negligible switching time and power loss. Therefore, power electronic circuits should be designed by considering the capabilities and limitations of available devices. Traditionally there has been limited interaction between device manufacturers and circuit designers. Therefore, manufacturers have been fabricating generic power semiconductor devices with inadequate consideration of the specific applications where the devices are used. The diverse nature of power electronics does not allow the use of generic power semiconductor devices in all applications as it leads to non-optimal systems. Therefore, the devices and circuits need to be optimized at the application level. Soft-switching topologies offer numerous advantages over conventional hard-switching applications such as reduced switching stress and EMI, and higher switching speed at reduced power loss. The IGBTs behave dissimilarly in the two circuit conditions. As a result, devices optimized for hard switching conditions do not necessarily give the best possible performance when used in soft switching circuits. In order to extract maximum system performance, it is necessary to develop IGBTs suited for specific applications. These optimized devices need to be manufacturable and cost effective in order to be commercially viable.

Further Reading

1. Adler, M. S., Owyang, K. W., Baliga, B. J., and Kokosa, R. A., "The evolution of power device technology," *IEEE Trans. Electron. Devices* **ED-31**: 1570–1591 (1984).
2. Akagi, H., "The state-of-the-art of power electronics in Japan," *IEEE Trans. Power Electron.* **13**: 345–356 (1998).
3. Baliga, B. J., Adler, M. S., Love, R. P., Gray, P. V., and Zommer, N., "The insulated gate transistor: a new three-terminal MOS controlled bipolar power device," *IEEE Trans. Electron. Devices* **ED-31**: 821–828 (1984).
4. Baliga B. J., *Power Semiconductor Devices*, PWS Publishing, Boston, MA, 1996.
5. Blaabjerg, F. and Pedersen, J. K., "An optimum drive and clamp circuit design with controlled switching for a snubberless PWM-VSI-IGBT inverterleg," in *IEEE Power Electronics Specialists Conference Records*, pp. 289–297, 1992.
6. Chokhawala, R. and Castino, G., "IGBT fault current limiting circuits," in *IEEE Industry Applications Society Annual Meeting Records*, pp. 1339–1345, 1993.
7. Clemente, S. *et al.*, *IGBT Characteristics*, IR Applications note AN-983A.
8. Divan, D. M. and Skibinski, G., "Zero-switching-loss inverters for high power applications," *IEEE Trans. Industry Applications* **25**: 634–643 (1989).
9. Elasser, A., Parthasarathy, V., and Torrey, D., "A study of the internal device dynamics of punch-through and non punch-through IGBTs under zero-current switching," *IEEE Trans. Power Electron.* **12**: 21–35 (1997).
10. Ghandi, S. K., *Semiconductor Power Devices*, John Wiley & Sons, NY, 1977.
11. Hefner, A. R., "An improved understanding for the transient operation of the insulated gate bipolar transistor (IGBT)," *IEEE Trans. Power Electron.* **5**: 459–468 (1990).
12. Hefner, A. R. and Blackburn, D. L., "An analytical model for the steady-state and transient characteristics of the power insulated gate bipolar transistor," *Solid-State Electron.* **31**: 1513–1532 (1988).
13. Hefner, A. R., "An investigation of the drive circuit requirements for the power insulated gate bipolar transistor (IGBT)," *IEEE Trans. Power Electron.* **6**: 208–219 (1991).
14. Jahns, T.M. "Designing intelligent muscle into industrial motion control," in *Industrial Electronics Conference Records*, pp. 1–14, 1989.
15. John, V., Suh, B. S., and Lipo, T. A., "Fast clamped short circuit protection of IGBTs," in *IEEE Applied Power Electronics Conference Records*, pp. 724–730, 1998.
16. Kassakian, J. G., Schlecht, M. F., and Verghese, G. C., *Principles of Power Electronics*, Addison Wesley, Reading, MA, 1991.
17. Kraus, R. and Hoffman, K., "An analytical model of IGBTs with low emitter efficiency," in *ISPSD'93*, pp. 30–34.
18. Lee, H. G., Lee, Y. H., Suh, B. S., and Lee, J. W., "A new intelligent gate control scheme to drive and protect high power IGBTs," in *European Power Electronics Conference Records*, pp. 1.400–1.405, 1997.
19. Licitra, C., Musumeci, S., Raciti, A., Galluzzo, A. U., and Letor, R., "A new driving circuit for IGBT devices," *IEEE Trans. Power Electron.* **10**: 373–378 (1995).
20. McMurray, W., "Resonant snubbers with auxiliary switches," *IEEE Trans. Industry Applications* **29**: 355–362 (1993).
21. Mohan, N., Undeland, T., and Robbins, W., *Power Electronics – Design, Converters and Applications*, John Wiley & Sons, NY, 1996.
22. Penharkar, S. and Shenai, K., "Zero voltage switching behavior of punchthrough and nonpunchthrough insulated gate bipolar transistors (IGBTs)," *IEEE Trans. Electron. Devices* **45**: 1826–1835 (1998).
23. Powerex IGBTMOD and intellimod – *Intelligent Power Modules Applications and Technical Data Book*, 1994.
24. Sze, S. M., *Physics of Semiconductor Devices*, John Wiley & Sons, NY, 1981.
25. Sze, S. M., *Modern Semiconductor Device Physics*, John Wiley & Sons, NY, 1998.
26. Trivedi, M., Pendharkar, S., and Shenai, K., "Switching charcteristics of IGBTs and MCTs in power converters," *IEEE Trans. Electron. Devices* **43**: 1994–2003 (1996).
27. Trivedi, M. and Shenai, K., "Modeling the turn-off of IGBTs in hard- and soft-switching applications," *IEEE Trans. Electron. Devices* **44**: 887–893 (1997).

28. Trivedi, M. and Shenai, K., "Internal dynamics of IGBT under zero-voltage and zero-current switching conditions," *IEEE Trans. Electron. Devices* **46:** 1274–1282 (1999).
29. Trivedi, M. and Shenai, K., "Failure mechanisms of IGBTs under short-circuit and clamped inductive switching stress," *IEEE Trans. Power Electron.* **14**: 108–116 (1999).
30. Undeland, T., Jenset, F., Steinbakk, A., Ronge, T., and Hernes, M., "A snubber configuration for both power transistor and GTO PWM inverters," in *IEEE Power Electronics Specialists Conference Records*, pp. 42–53, 1984.
31. Venkatesan, V., Eshaghi, M., Borras, R., and Deuty, S., "IGBT turn-off characteristics explained through measurements and device simulation," in *IEEE Applied Power Electronics Conference Records*, pp. 175–178, 1997.
32. Widjaja, I., Kurnia, A., Shenai, K., and Divan, D., "Switching dynamics of IGBTs in soft-switching converters," *IEEE Trans. Electron. Devices* **42**: 445–454 (1995).