34

Control Methods for Switching Power Converters

J. Fernando Silva, Ph.D. and Sónia Ferreira Pinto, Ph.D.

Instituto Superior Técnico, DEEC, A.C. Energia, Laboratório de Máquinas Eléctricas e Electrónica de Potência, Centro de Automática da Universidade Técnica de Lisboa, AV. Rorisco Pais 1, 1049-001 Lisboa, Portugal

34.1 Introduction

Switching power converters must be suitably designed and controlled in order to supply the voltages, currents, or frequency ranges needed for the load and to guarantee the requested dynamics [1–4]. Furthermore, they can be designed to serve as "clean" interfaces between most loads and the electrical utility system. Thereafter, the set switching converter plus load behaves as an almost pure electrical utility resistive load.

This chapter provides basic and some advanced skills to control electronic power converters, taking into account that the control of switching power converters is a vast and interdisciplinary subject. Control designers for switching converters should know the static and dynamic behavior of the electronic power converter and how to design its elements for the intended operating modes. Designers must be experts on control techniques, especially the nonlinear ones, since switching converters are nonlinear, time-variant, discrete systems, and designers must be capable of analog or digital implementation of the derived modulators, regulators, or compensators. Powerful modeling methodologies and sophisticated control processes must be used to obtain stable-controlled switching converters, not only with satisfactory static and dynamic performance, but also with low sensitivity against load or line disturbances or, preferably, robustness.

In Section 34.2, the techniques to obtain suitable nonlinear and linear state-space models, for most switching converters, are presented and illustrated through examples. The derived linear models are used to create equivalent circuits, and to design linear feedback controllers for converters operating in the continuous or discontinuous mode. The classical linear time-invariant systems control theory, based on Laplace transform, transfer function concepts, Bode plots or root locus, is best used with state-space averaged models, or derived circuits, and well-known triangular wave modulators for generating the switching variables or the trigger signals for the power semiconductors.

Nonlinear state-space models and sliding-mode controllers, presented in Section 34.3, provide a more consistent way of handling the control problem of switching converters, since sliding mode is aimed at variable structure systems, as are switching power converters. Chattering, a characteristic of sliding mode, is inherent to switching power converters, even if they are controlled with linear methods. Chattering is very hard to remove and is acceptable in certain converter variables. The described sliding-mode methodology defines exactly the variables that need to be measured, while providing the necessary equations (control law and switching law) whose implementation gives the robust modulator and compensator low-level hardware (or software). Therefore, the sliding-mode control integrates the design of the switching converter modulator and controller electronics, reducing the needed designer expertise. This approach requires measurement of the state variables, but eliminates conventional modulators and linear feedback compensators, enabling better performance and robustness. It also reduces the converter cost, control complexity, volume, and weight (increasing power density). The so-called main drawback of sliding mode, variable switching frequency, is also addressed, providing fixed-frequency auxiliary functions and suitable augmented control laws to null steady-state errors due to the use of constant switching frequency.

Fuzzy control of switching converters (Section 34.4) is a control technique needing no converter models, parameters, or operating conditions, but only an expert knowledge of the converter dynamics. Fuzzy controllers can be used in a diverse array of switching converters with only small adaptations, since the controllers, based on fuzzy sets, are obtained simply from the knowledge of the system dynamics, using a model reference adaptive control philosophy. Obtained fuzzy control rules can be built into a decision-lookup table, in which the control processor simply picks up the control input corresponding to the sampled measurements. Fuzzy controllers are almost immune to system parameter fluctuations, since they do not take into account their values. The steps to obtain a fuzzy controller are described, and the example provided compares the fuzzy controller performance to the current-mode control.

34.2 Switching Power Converter Control Using State-space Averaged Models

34.2.1 Introduction

State-space models provide a general and strong basis for dynamic modeling of various systems including switching converters. State-space models are useful to design the needed linear control loops, and can also be used to computer simulate the steady state, as well as the dynamic behavior, of the switching converter, fitted with the designed feedback control loops and subjected to external perturbations. Furthermore, state-space models are the basis for applying powerful nonlinear control methods such as sliding mode. State-space averaging and linearization provides an elegant solution for the application of widely known linear control techniques to most switching converters.

34.2.2 State-space Modeling

Consider a switching converter with sets of power semiconductor structures, each one with two different circuit configurations, according to the state of the respective semiconductors, and operating in the continuous mode of conduction. Supposing the power semiconductors as controlled ideal switches (zero on-state voltage drops, zero off-state currents, and instantaneous commutation between the on- and off-states), the time (t) behavior of the circuit, over period T, can be represented by the general form of the state-space model (34.1):

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ \mathbf{y} &= \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \end{aligned} \tag{34.1}$$

where $\mathbf{x}$ is the state vector, $\dot{\mathbf{x}} = \mathrm{d}\mathbf{x}/\mathrm{d}t$, $\mathbf{u}$ is the input or control vector, and $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, $\mathbf{D}$ are respectively the dynamics (or state), the input, the output, and the direct transmission (or feedforward) matrices.

Since the power semiconductors will either be conducting or blocking, a time-dependent switching variable $\delta(t)$ can be used to describe the allowed switch states of each structure (i.e. $\delta(t) = 1$ for the on-state circuit and $\delta(t) = 0$ for the off-state circuit). Then, two subintervals must be considered: subinterval 1 for $0 \le t \le \delta_1 T$, where $\delta(t) = 1$ and subinterval 2 for $\delta_1 T \le t \le T$ where $\delta(t) = 0$. The state equations of the circuit, in each of the circuit configurations, can be written as:

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}_1\mathbf{x} + \mathbf{B}_1\mathbf{u} \\ \mathbf{y} &= \mathbf{C}_1\mathbf{x} + \mathbf{D}_1\mathbf{u} \end{aligned} \quad \text{for} \quad 0 \le t \le \delta_1 T \quad \text{where} \quad \delta(t) = 1 \tag{34.2}$$

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}_2\mathbf{x} + \mathbf{B}_2\mathbf{u} \\ \mathbf{y} &= \mathbf{C}_2\mathbf{x} + \mathbf{D}_2\mathbf{u} \end{aligned} \quad \text{for} \quad \delta_1 T \le t \le T \quad \text{where} \quad \delta(t) = 0 \tag{34.3}$$

34.2.2.1 Switched State-space Model

Given the two binary values of the switching variable $\delta(t)$, Eqs. (34.2) and (34.3) can be combined to obtain the nonlinear and time-variant switched state-space model of the switching

converter circuit, Eq. (34.4) or (34.5):

$$\dot{\mathbf{x}} = [\mathbf{A}_1\delta(t) + \mathbf{A}_2(1-\delta(t))]\mathbf{x} + [\mathbf{B}_1\delta(t) + \mathbf{B}_2(1-\delta(t))]\mathbf{u}$$
$$\mathbf{y} = [\mathbf{C}_1\delta(t) + \mathbf{C}_2(1-\delta(t))]\mathbf{x} + [\mathbf{D}_1\delta(t) + \mathbf{D}_2(1-\delta(t))]\mathbf{u} \tag{34.4}$$

$$\dot{\mathbf{x}} = \mathbf{A}_S\,\mathbf{x} + \mathbf{B}_S\,\mathbf{u}$$
$$\mathbf{y} = \mathbf{C}_S\,\mathbf{x} + \mathbf{D}_S\,\mathbf{u} \tag{34.5}$$

where $\mathbf{A}_S = [\mathbf{A}_1\delta(t) + \mathbf{A}_2(1-\delta(t))]$, $\mathbf{B}_S = [\mathbf{B}_1\delta(t) + \mathbf{B}_2(1-\delta(t))]$, $\mathbf{C}_S = [\mathbf{C}_1\delta(t) + \mathbf{C}_2(1-\delta(t))]$, and $\mathbf{D}_S = [\mathbf{D}_1\delta(t) + \mathbf{D}_2(1-\delta(t))]$.

34.2.2.2 State-space Averaged Model

Since the state variables of the $\mathbf{x}$ vector are continuous, using Eq. (34.4), with the initial conditions $\mathbf{x}_1(0) = \mathbf{x}_2(T)$, $\mathbf{x}_2(\delta_1 T) = \mathbf{x}_1(\delta_1 T)$, and considering the duty cycle δ_1 as the average value of $\delta(t)$, the time evolution of the converter state variables can be obtained, integrating Eq. (34.4) over the intervals $0 \le t \le \delta_1 T$ and $\delta_1 T \le t \le T$, although it often requires excessive calculation effort. However, a convenient approximation can be devised, considering λ_{max}, the maximum of the absolute values of all eigenvalues of $\mathbf{A}$ (usually λ_{max} is related to the cutoff frequency f_c of an equivalent low-pass filter with $f_c \ll 1/T$). For $\lambda_{max} T \ll 1$, the exponential matrix (or state transition matrix) $e^{\mathbf{A}t} = \mathbf{I} + \mathbf{A}t + \mathbf{A}^2t^2/2 + \cdots + \mathbf{A}^n t^n/n!$, where $\mathbf{I}$ is the identity or unity matrix, can be approximated by $e^{\mathbf{A}t} \approx \mathbf{I} + \mathbf{A}t$. Therefore, $e^{\mathbf{A}_1\delta_1 t} \cdot e^{\mathbf{A}_2(1-\delta_1)t} \approx \mathbf{I} + [\mathbf{A}_1\delta_1 + \mathbf{A}_2(1-\delta_1)]t$. Hence, the solution over the period T, for the system represented by Eq. (34.4), is found to be:

$$\mathbf{x}(T) \cong e^{[\mathbf{A}_1\delta_1 + \mathbf{A}_2(1-\delta_1)]T}\mathbf{x}_1(0) + \int_0^T e^{[\mathbf{A}_1\delta_1 + \mathbf{A}_2(1-\delta_1)](T-\tau)}\,[\mathbf{B}_1\delta_1 + \mathbf{B}_2(1-\delta_1)]\,\mathbf{u}\,d\tau \tag{34.6}$$

This approximate response of Eq. (34.4) is identical to the exact response obtained from the nonlinear continuous time-invariant state-space model (34.7), supposing that the average values of $\mathbf{x}$, denoted $\bar{\mathbf{x}}$, are the new state variables, and considering $\delta_2 = 1 - \delta_1$. Moreover, if $\mathbf{A}_1\,\mathbf{A}_2 = \mathbf{A}_2\,\mathbf{A}_1$, the approximation is exact.

$$\dot{\bar{\mathbf{x}}} = [\mathbf{A}_1\delta_1 + \mathbf{A}_2\delta_2]\;\bar{\mathbf{x}} + [\mathbf{B}_1\delta_1 + \mathbf{B}_2\delta_2]\;\bar{\mathbf{u}}$$
$$\bar{\mathbf{y}} = [\mathbf{C}_1\delta_1 + \mathbf{C}_2\delta_2]\;\bar{\mathbf{x}} + [\mathbf{D}_1\delta_1 + \mathbf{D}_2\delta_2]\;\bar{\mathbf{u}} \tag{34.7}$$

For $\lambda_{max} T \ll 1$, the model (34.7), often referred to as the state-space averaged model, is also said to be obtained by "averaging" Eq. (34.4) over one period, under small ripple and slow variations, as the average of products is approximated by products of the averages. Comparing Eq. (34.7) to Eq. (34.1), the relations (34.8), defining the state-space averaged model, are obtained.

$$\mathbf{A} = [\mathbf{A}_1\delta_1 + \mathbf{A}_2\delta_2]; \quad \mathbf{B} = [\mathbf{B}_1\delta_1 + \mathbf{B}_2\delta_2];$$
$$\mathbf{C} = [\mathbf{C}_1\delta_1 + \mathbf{C}_2\delta_2]; \quad \mathbf{D} = [\mathbf{D}_1\delta_1 + \mathbf{D}_2\delta_2] \tag{34.8}$$

EXAMPLE 34.1 State-space models for the buck–boost dc/dc converter

Consider the simplified circuitry of the buck–boost converter of Fig. 34.1 switching at $f_s = 20\,\text{kHz}$ ($T = 50\,\mu\text{s}$) with $V_{DCmax} = 28\,\text{V}$, $V_{DCmin} = 22\,\text{V}$, $V_o = 24\,\text{V}$, $L_i = 400\,\mu\text{H}$, $C_o = 2700\,\mu\text{F}$, $R_o = 2\,\Omega$.

The differential equations governing the dynamics of the state vector $\mathbf{x} = [i_L,\ v_o]^T$ (^{T} denotes the transpose of vectors or matrices) are:

$$L_i\frac{di_L}{dt} = V_{DC}$$
$$C_o\frac{dv_o}{dt} = -\frac{v_o}{R_o}$$
for $0 \le t \le \delta_1 T$ ($\delta(t) = 1$, Q_1 is on and D_1 is off) (34.9)

$$L_i\frac{di_L}{dt} = -v_o$$
$$C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o}$$
for $\delta_1 T \le t \le T$ ($\delta(t) = 1$, Q_1 is off and D_1 is on) (34.10)

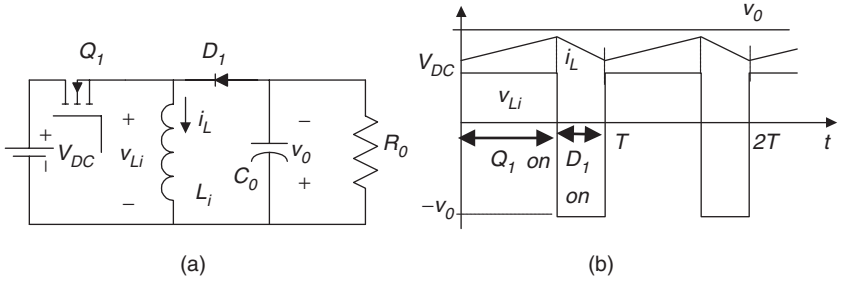


FIGURE 34.1 (a) Basic circuit of the buck–boost dc/dc converter and (b) ideal waveforms.

Comparing Eqs. (34.9) and (34.10) to Eqs. (34.2) and (34.3) and considering $\mathbf{y} = [v_o,\ i_L]^T$, the following matrices can be identified:

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 \\ 0 & -1/(R_o C_o) \end{bmatrix}; \quad \mathbf{A}_2 = \begin{bmatrix} 0 & -1/L_i \\ 1/C_o & -1/(R_o C_o) \end{bmatrix};$$

$$\mathbf{B}_1 = [1/L_i,\ 0]^T; \quad \mathbf{B}_2 = [0,\ 0]^T; \quad \mathbf{u} = [V_{DC}];$$

$$\mathbf{C}_1 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}; \quad \mathbf{C}_2 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix};$$

$$\mathbf{D}_1 = [0,\ 0]^T; \quad \mathbf{D}_2 = [0,\ 0]^T$$

From Eqs. (34.4) and (34.5), the switched state-space model of this switching converter is

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_o \end{bmatrix} = \begin{bmatrix} 0 & -\big(1-\delta(t)\big)/L_i \\ \big(1-\delta(t)\big)/C_o & -1/(R_o C_o) \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \delta(t)/L_i \\ 0 \end{bmatrix} V_{DC}$$

$$\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [V_{DC}] \tag{34.11}$$

Now, applying Eq. (34.7), Eqs. (34.12) and (34.13) can be obtained:

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_o \end{bmatrix} = \left[\begin{bmatrix} 0 & 0 \\ 0 & -1/R_o C_o \end{bmatrix} \delta_1 + \begin{bmatrix} 0 & -1/L_i \\ 1/C_o & -1/R_o C_o \end{bmatrix} \delta_2 \right] \times \begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} + \left[\begin{bmatrix} 1/L_i \\ 0 \end{bmatrix} \delta_1 + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \delta_2 \right] \left[\bar{V}_{DC} \right] \tag{34.12}$$

$$\begin{bmatrix} \bar{v}_o \\ \bar{i}_L \end{bmatrix} = \left[\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \delta_1 + \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \delta_2 \right] \begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} + \left[\begin{bmatrix} 0 \\ 0 \end{bmatrix} \delta_1 + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \delta_2 \right] \left[\bar{V}_{DC} \right] \tag{34.13}$$

From Eqs. (34.12) and (34.13), the state-space averaged model, written as a function of δ_1, is

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_o \end{bmatrix} = \begin{bmatrix} 0 & -1-\delta_1/L_i \\ 1-\delta_1/C_o & -1/R_o C_o \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} + \begin{bmatrix} \delta_1/L_i \\ 0 \end{bmatrix} \left[\bar{V}_{DC} \right] \tag{34.14}$$

$$\begin{bmatrix} \bar{v}_o \\ \bar{i}_L \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \left[\bar{V}_{DC} \right] \tag{34.15}$$

The eigenvalues $s_{bb_{1,2}}$, or characteristic roots of $\mathbf{A}$, are the roots of $|s\mathbf{I}-\mathbf{A}|$. Therefore:

$$s_{bb_{1,2}} = \frac{-1}{2R_o C_o} \pm \sqrt{\frac{1}{4\,(R_o C_o)^2} - \frac{(1-\delta_1)^2}{L_i C_o}} \tag{34.16}$$

Since λ_{max} is the maximum of the absolute values of all the eigenvalues of $\mathbf{A}$, the model (34.14, 34.15) is valid for switching frequencies f_s ($f_s = 1/T$) that verify $\lambda_{max} T \ll 1$. Therefore, as $T \ll 1/\lambda_{max}$, the values of T that approximately verify this restriction are $T \ll 1/max(|s_{bb_{1,2}}|)$. Given this buck–boost converter data, $T \ll 2$ ms is obtained. Therefore, the converter switching frequency must obey $f_s \gg \max(|s_{f\,1,2}|)$, implying switching frequencies above, say, 5 kHz. Consequently, the buck–boost switching frequency, the inductor value, and the capacitor value were chosen accordingly.

This restriction can be further used to discuss the maximum frequency ω_{max} for which the state-space averaged model is still valid, given a certain switching frequency. As λ_{max} can be regarded as a frequency, the preceding constraint brings $\omega_{max} \ll 2\pi f_s$, say $\omega_{max} < 2\pi f_s/10$, which means that the state-space averaged model is a good approximation at frequencies under one-tenth of the power converter switching frequency.

The state-space averaged model (34.14, 34.15) is also the state-space model of the circuit represented in Fig. 34.2. Hence, this circuit is often named "the averaged equivalent circuit" of the buck–boost converter and allows the determination, under small ripple and slow variations, of the average equivalent circuit of the converter switching cell (power transistor plus diode).

The average equivalent circuit of the switching cell (Fig. 34.3a) is represented in Fig. 34.3b and emerges directly from the state-space averaged model (34.14, 34.15). This equivalent circuit can be viewed as the model of an "ideal transformer" (Fig. 34.3c), whose primary to secondary ratio (v_1/v_2) can be calculated applying Kirchhoff's voltage law to obtain $-v_1 + v_s - v_2 = 0$. As $v_2 = \delta_1 v_s$, it follows that $v_1 = v_s(1-\delta_1)$, giving $(v_1/v_2) = (1-\delta_1)/\delta_1$. The same ratio could be obtained beginning with $i_L = i_1 + i_2$, and $i_1 = \delta_1 i_L$ (Fig. 34.3b) which gives $i_2 = i_L(1-\delta_1)$ and $(i_2/i_1) = \delta_2/\delta_1$.

The average equivalent circuit concept, obtained from Eq. (34.7) or Eqs. (34.14) and (34.15), can be applied to other switching converters, with or without a similar switching cell, to obtain transfer functions or to computer simulate

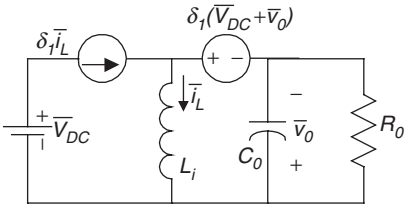


FIGURE 34.2 Equivalent circuit of the averaged state-space model of the buck–boost converter.

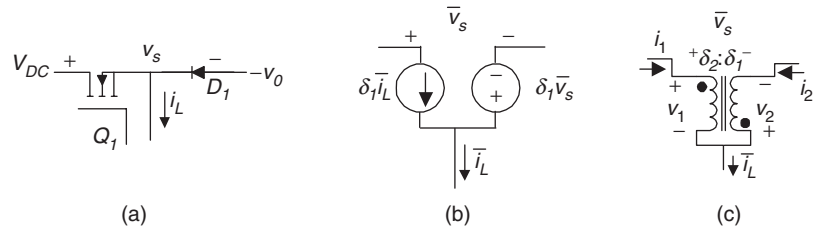


FIGURE 34.3 Average equivalent circuit of the switching cell: (a) switching cell; (b) average equivalent circuit; and (c) average equivalent circuit using an ideal transformer.

the converter average behavior. The average equivalent circuit of the switching cell can be applied to converters with the same switching cell operating in the continuous conduction mode. However, note that the state variables of Eq. (34.7) or Eqs. (34.14) and (34.15) are the mean values of the converter instantaneous variables and, therefore, do not represent their ripple components. The inputs of the state-space averaged model are the mean values of the converter inputs over one switching period.

34.2.2.3 Linearized State-space Averaged Model

Since the converter outputs $\bar{\mathbf{y}}$ must be regulated actuating on the duty cycle $\delta(t)$, and the converter inputs $\bar{\mathbf{u}}$ usually present perturbations due to the load and power supply variations. State variables are decomposed in small ac perturbations (denoted by "$\sim$") and dc steady-state quantities (represented by uppercase letters). Therefore:

$$\begin{aligned}\bar{\mathbf{x}} &= \mathbf{X} + \tilde{\mathbf{x}}\\ \bar{\mathbf{y}} &= \mathbf{Y} + \tilde{\mathbf{y}}\\ \bar{\mathbf{u}} &= \mathbf{U} + \tilde{\mathbf{u}}\\ \delta_1 &= \Delta_1 + \tilde{\delta}\\ \delta_2 &= \Delta_2 - \tilde{\delta}\end{aligned} \tag{34.17}$$

Using Eq. (34.17) in Eq. (34.7) and rearranging terms, we obtain:

$$\begin{aligned}\dot{\tilde{\mathbf{x}}} = {} & [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\,\mathbf{X} + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\,\mathbf{U}\\ & + [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\,\tilde{\mathbf{x}} + [(\mathbf{A}_1 - \mathbf{A}_2)\,\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\,\mathbf{U}]\,\tilde{\delta}\\ & + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\,\tilde{\mathbf{u}} + [(\mathbf{A}_1 - \mathbf{A}_2)\,\tilde{\mathbf{x}} + (\mathbf{B}_1 - \mathbf{B}_2)\,\tilde{\mathbf{u}}]\,\tilde{\delta}\end{aligned} \tag{34.18}$$

$$\begin{aligned}\mathbf{Y} + \tilde{\mathbf{y}} = {} & [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\,\mathbf{X} + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\,\mathbf{U}\\ & + [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\,\tilde{\mathbf{x}} + [(\mathbf{C}_1 - \mathbf{C}_2)\,\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\,\mathbf{U}]\,\tilde{\delta}\\ & + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\,\tilde{\mathbf{u}} + [(C_1 - C_2)\,\tilde{\mathbf{x}} + (\mathbf{D}_1 - \mathbf{D}_2)\,\tilde{\mathbf{u}}]\,\tilde{\delta}\end{aligned} \tag{34.19}$$

The terms $[\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\,\mathbf{X} + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\,\mathbf{U}$ and $[\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\,\mathbf{X} + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\,\mathbf{U}$, respectively from Eqs. (34.18) and (34.19), represent the steady-state behavior of the system. As in steady state $\dot{\mathbf{X}} = \mathbf{0}$, the following relationships hold:

$$\mathbf{0} = [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\,\mathbf{X} + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\,\mathbf{U} \tag{34.20}$$

$$\mathbf{Y} = [C_1\Delta_1 + \mathbf{C}_2\Delta_2]\,\mathbf{X} + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\,\mathbf{U} \tag{34.21}$$

Neglecting higher order terms ($[(\mathbf{A}_1 - \mathbf{A}_2)\,\tilde{\mathbf{x}} + (\mathbf{B}_1 - \mathbf{B}_2)\,\tilde{\mathbf{u}}]\,\tilde{\delta} \approx 0$) of Eqs. (34.18) and (34.19), the linearized small-signal state-space averaged model is

$$\begin{aligned}\dot{\tilde{\mathbf{x}}} = {} & [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\,\tilde{\mathbf{x}} + [(\mathbf{A}_1 - \mathbf{A}_2)\,\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\,\mathbf{U}]\,\tilde{\delta}\\ & + [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\,\tilde{\mathbf{u}}\\ \tilde{\mathbf{y}} = {} & [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\,\tilde{\mathbf{x}} + [(\mathbf{C}_1 - \mathbf{C}_2)\,\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\,\mathbf{U}]\,\tilde{\delta}\\ & + [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\,\tilde{\mathbf{u}}\end{aligned} \tag{34.22}$$

or

$$\begin{aligned}\dot{\tilde{\mathbf{x}}} &= \mathbf{A}_{av}\,\tilde{\mathbf{x}} + \mathbf{B}_{av}\,\tilde{\mathbf{u}} + [(\mathbf{A}_1 - \mathbf{A}_2)\,\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\,\mathbf{U}]\,\tilde{\delta}\\ \tilde{\mathbf{y}} &= \mathbf{C}_{av}\,\tilde{\mathbf{x}} + \mathbf{D}_{av}\,\tilde{\mathbf{u}} + [(\mathbf{C}_1 - \mathbf{C}_2)\,\mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\,\mathbf{U}]\,\tilde{\delta}\end{aligned} \tag{34.23}$$

with

$$\begin{aligned}\mathbf{A}_{av} &= [\mathbf{A}_1\Delta_1 + \mathbf{A}_2\Delta_2]\\ \mathbf{B}_{av} &= [\mathbf{B}_1\Delta_1 + \mathbf{B}_2\Delta_2]\\ \mathbf{C}_{av} &= [\mathbf{C}_1\Delta_1 + \mathbf{C}_2\Delta_2]\\ \mathbf{D}_{av} &= [\mathbf{D}_1\Delta_1 + \mathbf{D}_2\Delta_2]\end{aligned} \tag{34.24}$$

34.2.3 Converter Transfer Functions

Using Eq. (34.20) in Eq. (34.21), the input $\mathbf{U}$ to output $\mathbf{Y}$ steady-state relations (34.25), needed for open-loop and feedforward control, can be obtained.

$$\frac{\mathbf{Y}}{\mathbf{U}} = -\mathbf{C}_{av}\mathbf{A}_{av}^{-1}\mathbf{B}_{av} + \mathbf{D}_{av} \tag{34.25}$$

Applying Laplace transforms to Eq. (34.23) with zero initial conditions, and using the superposition theorem, the small-signal duty-cycle $\tilde{\delta}$ to output $\tilde{\mathbf{y}}$ transfer functions (34.26) can be obtained considering zero line perturbations ($\tilde{u} = 0$).

$$\frac{\tilde{\mathbf{y}}(s)}{\tilde{\delta}(s)} = \mathbf{C}_{av}\left[s\mathbf{I} - \mathbf{A}_{av}\right]^{-1}\left[(\mathbf{A}_1 - \mathbf{A}_2)\ \mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\ \mathbf{U}\right] + \left[(\mathbf{C}_1 - \mathbf{C}_2)\ \mathbf{X} + (\mathbf{D}_1 - \mathbf{D}_2)\ \mathbf{U}\right] \tag{34.26}$$

The line to output transfer function (or audio susceptibility transfer function) (34.27) is derived using the same method, considering now zero small-signal duty-cycle perturbations ($\tilde{\delta} = 0$).

$$\frac{\tilde{\mathbf{y}}(s)}{\tilde{\mathbf{u}}(s)} = \mathbf{C}_{av}\left[s\mathbf{I} - \mathbf{A}_{av}\right]^{-1}\mathbf{B}_{av} + \mathbf{D}_{av} \tag{34.27}$$

Example 34.2 Buck–Boost dc/dc converter transfer functions

From Eqs. (34.14) and (34.15) of Example 34.1 and Eq. (34.23), making $\mathbf{X} = [I_L,\ V_o]^T$, $\mathbf{Y} = [V_o,\ I_L]^T$, and $\mathbf{U} = [V_{DC}]$, the linearized state-space model of the buck–boost converter is

$$\begin{bmatrix}\dot{\tilde{i}}_L\\ \dot{\tilde{v}}_o\end{bmatrix} = \begin{bmatrix}0 & -1-\Delta_1/L_i\\ 1-\Delta_1/C_o & -1/R_oC_o\end{bmatrix}\begin{bmatrix}\tilde{i}_L\\ \tilde{v}_o\end{bmatrix} + \begin{bmatrix}\Delta_1/L_i\\ 0\end{bmatrix}[\tilde{v}_{DC}] + \begin{bmatrix}0 & \tilde{\delta}/L_i\\ -\tilde{\delta}/C_o & 0\end{bmatrix}\begin{bmatrix}I_L\\ V_o\end{bmatrix} + \begin{bmatrix}V_{DC}/L_i\\ 0\end{bmatrix}[\tilde{\delta}]$$

$$\begin{bmatrix}\tilde{v}_o\\ \tilde{i}_L\end{bmatrix} = \begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\tilde{i}_L\\ \tilde{v}_o\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}[\tilde{v}_{DC}] \tag{34.28}$$

From Eqs. (34.24) and (34.28), the following matrices are identified:

$$\mathbf{A}_{av} = \begin{bmatrix}0 & -(1-\Delta_1)/L_i\\ 1-\Delta_1/C_o & -1/R_oC_o\end{bmatrix};\quad \mathbf{B}_{av} = \begin{bmatrix}\Delta_1/L_i\\ 0\end{bmatrix};$$

$$\mathbf{C}_{av} = \begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix};\quad \mathbf{D}_{av} = \begin{bmatrix}0\\ 0\end{bmatrix} \tag{34.29}$$

The averaged linear equivalent circuit, resulting from Eq. (34.28) or from the linearization of the averaged equivalent circuit (Fig. 34.2) derived from Eqs. (34.14) and (34.15), now includes the small-signal current source $\tilde{\delta}I_L$ in parallel with the current source $\Delta_1\tilde{i}_L$, and the small-signal voltage source $\tilde{\delta}\,(V_{DC} + V_o)$ in series with the voltage source $\Delta_1(\tilde{v}_{dc} + \tilde{v}_o)$. The supply voltage source $\bar{V}_{DC}$ is replaced by the voltage source $\tilde{v}_{DC}$.

Using Eq. (34.29) in Eq. (34.25), the *input U to output Y steady-state relations* are:

$$\frac{I_L}{V_{DC}} = \frac{\Delta_1}{R_o\,(\Delta_1 - 1)^2} \tag{34.30}$$

$$\frac{V_o}{V_{DC}} = \frac{\Delta_1}{1 - \Delta_1} \tag{34.31}$$

These relations are the well-known steady-state transfer relationships of the buck–boost converter [2, 5, 6]. For open-loop control of the V_o output, knowing the nominal value of the power supply V_{DC} and the required V_o, the value of Δ_1 can be off-line calculated from Eq. (34.31) ($\Delta_1 = V_o/(V_o + V_{DC})$). A modulator such as that described in Section 34.2.4, with the modulation signal proportional to Δ_1, would generate the signal $\delta(t)$. The open-loop control for fixed output voltages is possible, if the power supply V_{DC} is almost constant and the converter load does not change significantly. If the V_{DC} value presents disturbances, then the feedforward control can be used, calculating Δ_1 on-line, so that its value will always be in accordance with Eq. (34.31). The correct V_o value will be attained at steady state, despite input-voltage variations. However, because of converter parasitic reactances, not modeled here (see Example 34.3), in practice a steady-state error would appear. Moreover, the transient dynamics imposed by the converter would present overshoots, being often not suited for demanding applications.

From Eq. (34.27), the *line to output transfer functions* are:

$$\frac{\tilde{i}_L(s)}{\tilde{v}_{DC}(s)} = \frac{\Delta_1\,(1 + sC_oR_o)}{s^2L_iC_oR_o + sL_i + R_o\,(1 - \Delta_1)^2} \tag{34.32}$$

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{DC}(s)} = \frac{R_o\Delta_1\,(1 - \Delta_1)}{s^2L_iC_oR_o + sL_i + R_o\,(1 - \Delta_1)^2} \tag{34.33}$$

From Eq. (34.26), *the small-signal duty-cycle $\tilde{\delta}$ to output $\tilde{y}$ transfer functions* are:

$$\frac{\tilde{i}_L(s)}{\tilde{\delta}(s)} = \frac{V_{DC}(1 + \Delta_1 + sC_oR_o)/(1 - \Delta_1)}{s^2L_iC_oR_o + sL_i + R_o\,(1 - \Delta_1)^2} \tag{34.34}$$

$$\frac{\tilde{v}_o(s)}{\tilde{\delta}(s)} = \frac{V_{DC}\left(R_o - sL_i\Delta_1/(1 - \Delta_1)^2\right)}{s^2L_iC_oR_o + sL_i + R_o\,(1 - \Delta_1)^2} \tag{34.35}$$

These transfer functions enable the choice and feedback-loop design of the compensation network. Note the positive zero in $\tilde{v}_o(s)/\tilde{\delta}(s)$, pointing out a

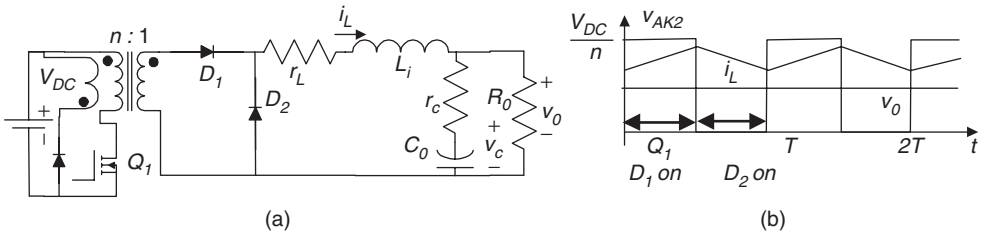


FIGURE 34.4 (a) Basic circuit of the forward dc/dc converter and (b) circuit main waveforms.

nonminimum-phase system. These equations could also be obtained using the small-signal equivalent circuit derived from Eq. (34.28), or from the linearized model of the switching cell Fig. 34.3b, substituting the current source $\delta_1 \bar{i}_L$ by the current sources $\Delta_1 \tilde{i}_L$ and $\tilde{\delta} I_L$ in parallel, and the voltage source $\delta_1 \bar{v}_s$ by the voltage sources $\Delta_1 \left(\tilde{v}_{DC} + \tilde{v}_o\right)$ and $\tilde{\delta}\left(V_{DC} + V_o\right)$ in series.

EXAMPLE 34.3 Transfer functions of the forward dc/dc converter

Consider the forward (buck derived) converter of Fig. 34.4 switching at $f_s = 100\,\text{kHz}$ ($T = 10\,\mu\text{s}$) with $V_{DC} = 300\,\text{V}$, $n = 30$, $V_o = 5\,\text{V}$, $L_i = 20\,\mu\text{H}$, $r_L = 0.01\,\Omega$, $C_o = 2200\,\mu\text{F}$, $r_C = 0.005\,\Omega$, $R_o = 0.1\,\Omega$.

Assuming $\mathbf{x} = [i_L,\ v_C]^T$, $\delta(t) = 1$ when both Q_1, D_1 are on and D_2 is off ($0 \le t \le \delta_1 T$), $\delta(t) = 0$ when both Q_1, D_1 are off and D_2 is on ($\delta_1 T \le t \le T$), the switched state-space model of the forward converter, considering as output vector $\mathbf{y} = [i_L,\ v_o]^T$, is

$$\begin{aligned}
\frac{\mathrm{d}i_L}{\mathrm{d}t} &= -\frac{(R_o r_C + R_o r_L + r_L r_C)}{L_i\,(R_o + r_C)} i_L \\
&\quad - \frac{R_o}{L_i\,(R_o + r_C)} v_c + \frac{\delta(t)}{n} V_{DC} \\
\frac{dv_C}{dt} &= \frac{R_o}{(R_o + r_C)\,C_o} i_L - \frac{1}{(R_o + r_C)\,C_o} v_C \\
v_o &= \frac{r_C}{1 + r_C/R_o} i_L + \frac{1}{1 + r_C/R_o} v_C
\end{aligned} \tag{34.36}$$

Making $r_{cm} = r_C/(1 + r_C/R_o)$, $R_{oc} = R_o + r_C$, $k_{oc} = R_o/R_{oc}$, $r_P = r_L + r_{cm}$ and comparing Eq. (34.36) to Eqs. (34.2) and (34.3), the following matrices can be identified:

$$\mathbf{A}_1 = \mathbf{A}_2 = \begin{bmatrix} -r_P/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc} C_o) \end{bmatrix};$$

$$\mathbf{B}_1 = [1/(nL_i),\ 0]^T; \quad \mathbf{B}_2 = [0,\ 0]^T; \quad \mathbf{u} = [V_{DC}]$$

$$\mathbf{C}_1 = \mathbf{C}_2 = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix}; \quad \mathbf{D}_1 = \mathbf{D}_2 = [0,\ 0]^T$$

Now, applying Eq. (34.7), the exact (since $\mathbf{A}_1 = \mathbf{A}_2$) state-space averaged model (34.37, 34.38) is obtained:

$$\begin{bmatrix} \dot{\bar{i}}_L \\ \dot{\bar{v}}_C \end{bmatrix} = \begin{bmatrix} -r_P/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc} C_o) \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_C \end{bmatrix} + \begin{bmatrix} \frac{\delta_1}{nL_i} \\ 0 \end{bmatrix} \left[\bar{V}_{DC}\right] \tag{34.37}$$

$$\begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix} \begin{bmatrix} \bar{i}_L \\ \bar{v}_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \left[\bar{V}_{DC}\right] \tag{34.38}$$

Since $\mathbf{A}_1 = \mathbf{A}_2$, this model is valid for $\omega_{max} < 2\pi f_s$. The converter eigenvalues $s_{f1,2}$, are:

$$s_{f1,2} = -\frac{L_i + C_o R_{oc} r_P \pm \sqrt{-4 R_{oc} L_i C_o \left(R_{oc} k_{oc}^2 + r_P\right) + \left(L_i + C_o R_{oc} r_P\right)^2}}{2 R_{oc} L_i C_o} \tag{34.39}$$

The equivalent circuit arising from Eqs. (34.37) and (34.38) is represented in Fig. 34.5. It could also be obtained with the concept of the switching cell equivalent circuit Fig. 34.3 of Example (34.1).

Making $\mathbf{X} = [I_L,\ V_C]^T$, $\mathbf{Y} = [I_L,\ V_o]^T$ and $\mathbf{U} = [V_{DC}]$, from Eq. (34.23) the small-signal state-space averaged model is

$$\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{\tilde{v}}_C \end{bmatrix} = \begin{bmatrix} -r_P/L_i & -k_{oc}/L_i \\ k_{oc}/C_o & -1/(R_{oc} C_o) \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} \Delta_1/nL_i \\ 0 \end{bmatrix} \left[\tilde{v}_{DC}\right] + \begin{bmatrix} V_{DC}/nL_i \\ 0 \end{bmatrix} \left[\tilde{\delta}\right] \tag{34.40}$$

$$\begin{bmatrix} \tilde{i}_L \\ \tilde{v}_o \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ r_{cm} & k_{oc} \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} \left[\tilde{v}_{DC}\right] \tag{34.41}$$

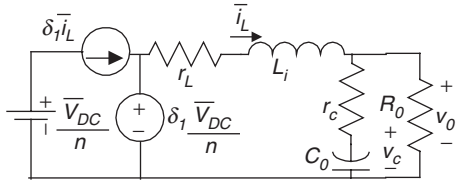


FIGURE 34.5 Equivalent circuit of the averaged state-space model of the forward converter.

From Eq. (34.25), the input **U** to output **Y** steady-state relations are:

$$\frac{I_L}{V_{DC}} = \frac{\Delta_1}{n\left(k_{oc}^2 R_{oc} + r_P\right)} \tag{34.42}$$

$$\frac{V_o}{V_{DC}} = \frac{\Delta_1\left(k_{oc}^2 R_{oc} + r_{cm}\right)}{n\left(k_{oc}^2 R_{oc} + r_P\right)} \tag{34.43}$$

Making $r_C = 0$, $r_L = 0$ and $n = 1$, the former relations give the well-known dc transfer relationships of the buck dc/dc converter. Relations (34.42, 34.43) allow the open-loop and feedforward control of the converter, as discussed in Example 34.2, provided that all the modeled parameters are time-invariant and accurate enough.

From Eq. (34.27), the line to output transfer functions are derived:

$$\frac{\tilde{i}_L(s)}{\tilde{v}_{DC}(s)} = \frac{(\Delta_1/n)\,(1 + sC_oR_{oc})}{s^2L_iC_oR_{oc} + s\,(L_i + C_oR_{oc}r_P) + k_{oc}^2R_{oc} + r_P} \tag{34.44}$$

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{DC}(s)} = \frac{(\Delta_1/n)\left(k_{oc}^2R_{oc} + r_{cm} + sC_oR_{oc}r_{cm}\right)}{s^2L_iC_oR_{oc} + s\,(L_i + C_oR_{oc}r_P) + k_{oc}^2R_{oc} + r_P} \tag{34.45}$$

Using Eq. (34.26), the small-signal duty-cycle $\tilde{\delta}$ to output $\tilde{\mathbf{y}}$ transfer functions are:

$$\frac{\tilde{i}_L(s)}{\delta(s)} = \frac{(V_{DC}/n)\,(1 + sC_oR_{oc})}{s^2L_iC_oR_{oc} + s\,(L_i + C_oR_{oc}r_P) + k_{oc}^2R_{oc} + r_P} \tag{34.46}$$

$$\frac{\tilde{v}_o(s)}{\delta(s)} = \frac{(V_{DC}/n)\left(k_{oc}^2R_{oc} + r_{cm} + sC_oR_{oc}r_{cm}\right)}{s^2L_iC_oR_{oc} + s\,(L_i + C_oR_{oc}r_P) + k_{oc}^2R_{oc} + r_P} \tag{34.47}$$

The real zero of Eq. (34.47) is due to r_C, the equivalent series resistance (ESR) of the output capacitor. A similar zero would occur in the buck–boost converter (Example 34.2), if the ESR of the output capacitor had been included in the modeling.

34.2.4 Pulse Width Modulator Transfer Functions

In what is often referred to as the pulse width modulation (PWM) voltage mode control, the output voltage $u_c(t)$ of the error (between desired and actual output) amplifier plus regulator, processed if needed, is compared to a repetitive or carrier waveform $r(t)$, to obtain the switching variable $\delta(t)$ (Fig. 34.6a). This function controls the power switch, turning it on at the beginning of the period and turning it off when the ramp exceeds the $u_c(t)$ voltage. In Fig. 34.6b the opposite occurs (turn-off at the end of the period, turn-on when the $u_c(t)$ voltage exceeds the ramp).

Considering $r(t)$ as represented in Fig. 34.6a ($r(t) = u_{cmax}t/T$), δ_k is obtained equating $r(t) = u_c$ giving $\delta_k = u_c(t)/u_{cmax}$ or $\delta_k/u_c(t) = G_M$ (G_M=$1/u_{cmax}$). In Fig. 34.6b, the switching-on angle α_k is obtained from $r(t) = u_{cmax} - 2u_{cmax}\omega t/\pi$, $u_c(t) = u_{cmax} - 2u_{cmax}\,\alpha_k/\pi$, giving $\alpha_k = (\pi/2)\times(1 - u_c/u_{cmax})$ and $G_M = \partial\alpha_k/\partial u_c = -\pi/(2u_{cmax})$.

Since, after turn-off or turn-on, any control action variation of $u_c(t)$ will only affect the converter duty cycle in the next period, a time delay is introduced in the control loop. For simplicity, with small-signal perturbations around the operating point, this delay is assumed almost constant and equal to its mean value ($T/2$). Then, the transfer function of the PWM

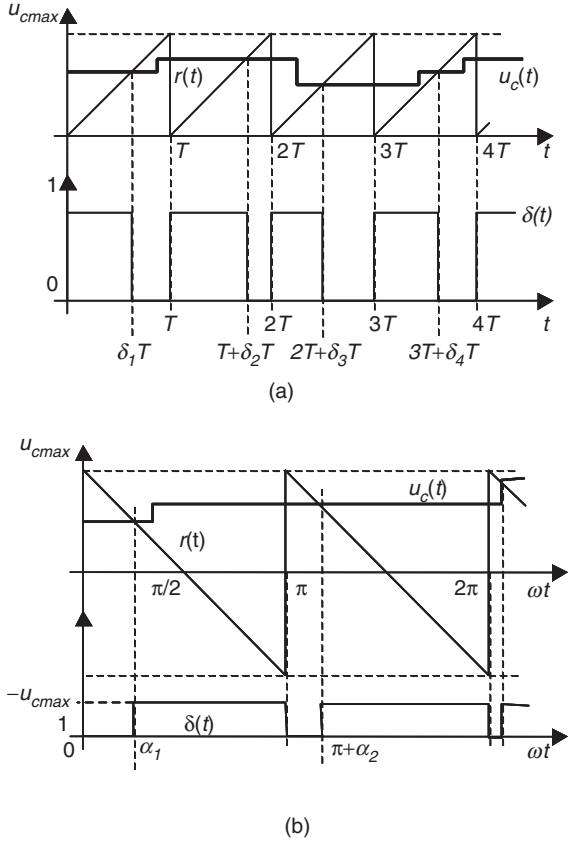


FIGURE 34.6 Waveforms of pulse width modulators showing the variable time delays of the modulator response: (a) $r(t) = u_{cmax}t/T$ and (b) $r(t) = u_{cmax} - 2u_{cmax}\omega t/\pi$.

modulator is

$$\frac{\tilde{\delta}(s)}{\tilde{u}_c(s)} = G_M e^{-sT/2} = \frac{G_M}{e^{s(T/2)}} = \frac{G_M}{1 + s\frac{T}{2} + \frac{s^2}{2!}\left(\frac{T}{2}\right)^2 + \cdots + \frac{s^j}{j!}\left(\frac{T}{2}\right)^2 + \cdots} \approx \frac{G_M}{1 + s\frac{T}{2}} \tag{34.48}$$

The final approximation of Eq. (34.48), valid for $\omega T/2 < \sqrt{2}/2$, [7] suggests that the PWM modulator can be considered as an amplifier with gain G_M and a dominant pole. Notice that this pole occurs at a frequency doubling the switching frequency, and most state-space averaged models are valid only for frequencies below one-tenth of the switching frequency. Therefore, in most situations this modulator pole can be neglected, being simply $\delta(s) = G_M u_c(s)$, as the dominant pole of Eq. (34.48) stays at least one decade to the left of the dominant poles of the converter.

34.2.5 Linear Feedback Design Ensuring Stability

In the application of classical linear feedback control to switching converters, Bode plots and root locus are, usually, suitable methods to assess system performance and stability. General rules for the design of the compensated open-loop transfer function are as follows:

(i) The low-frequency gain should be high enough to minimize output steady-state errors;
(ii) The frequency of 0 dB gain (unity gain), ω_{0dB}, should be placed close to the maximum allowed by the modeling approximations ($\lambda_{max} T \ll 1$), to allow fast response to transients. In practice, this frequency should be almost an order of magnitude lower than the switching frequency;
(iii) To ensure stability, the phase margin, defined as the additional phase shift needed to render the system unstable without gain changes (or the difference between the open-loop system phase at ω_{0dB} and $-180°$), must be positive and in general greater than 30° (45°−70° is desirable). In the root locus, no poles should enter the right-half of the complex plane;
(iv) To increase stability, the gain should be less than −30 dB at the frequency where the phase reaches −180° (gain margin greater than 30 dB).

Transient behavior and stability margins are related: the obtained damping factor is generally 0.01 times the phase margin (in degrees), and overshoot (in percent) is given approximately by 75° minus the phase margin. The product of the rise time (in seconds) and the closed-loop bandwidth (in rad/s) is close to 2.8.

To guarantee gain and phase margins, the following series compensation transfer functions (usually implemented with operational amplifiers) are often used [8]:

34.2.5.1 Types of Compensation

Lag or lead compensation

Lag compensation should be used in converters with good stability margin but poor steady-state accuracy. If the frequencies $1/T_p$ and $1/T_z$ of Eq. (34.49) with $1/T_p < 1/T_z$ are chosen well below the unity gain frequency, lag–lead compensation lowers the loop gain at high frequency but maintains the phase unchanged for $\omega \gg 1/T_z$. Then, the dc gain can be increased to reduce the steady-state error without significantly decreasing the phase margin.

$$C_{LL}(s) = k_{LL}\frac{1 + sT_z}{1 + sT_p} = k_{LL}\frac{T_z}{T_p}\frac{s + 1/T_z}{s + 1/T_p} \tag{34.49}$$

Lead compensation can be used in converters with good steady-state accuracy but poor stability margin. If the frequencies $1/T_p$ and $1/T_z$ of Eq. (34.49) with $1/T_p > 1/T_z$ are chosen below the unity gain frequency, lead–lag compensation increases the phase margin without significantly affecting the steady-state error. The T_p and T_z values are chosen to increase the phase margin, fastening the transient response and increasing the bandwidth.

Proportional–Integral compensation

Proportional–integral (PI) compensators (34.50) are used to guarantee null steady-state error with acceptable rise times. The PI compensators are a particular case of lag–lead compensators, therefore suitable for converters with good stability margin but poor steady-state accuracy.

$$C_{PI}(s) = \frac{1 + sT_z}{sT_p} = \frac{T_z}{T_p} + \frac{1}{sT_p} = K_p + \frac{K_i}{s} = K_p\left(1 + \frac{K_i}{K_p s}\right) = K_p\left(1 + \frac{1}{sT_z}\right) = \frac{1 + sT_z}{sT_z/K_p} \tag{34.50}$$

Proportional–Integral plus high-frequency pole compensation

This integral plus zero-pole compensation (34.51) combines the advantages of a PI with lead or lag compensation. It can be used in converters with good stability margin but poor steady-state accuracy. If the frequencies $1/T_M$ and $1/T_z$ ($1/T_z < 1/T_M$) are carefully chosen, compensation lowers the loop gain at high frequency, while only slightly lowering the phase to achieve the desired phase margin.

$$C_{ILD}(s) = \frac{1 + sT_z}{sT_p(1 + sT_M)} = \frac{T_z}{T_p T_M}\frac{s + 1/T_z}{s(s + 1/T_M)} = W_{cp}\frac{s + \omega_z}{s(s + \omega_M)} \tag{34.51}$$

Proportional–Integral derivative (PID), plus high-frequency poles

The PID notch filter type (34.52) scheme is used in converters with two lightly damped complex poles, to increase the response speed, while ensuring zero steady-state error. In most switching converters, the two complex zeros are selected to have a damping factor greater than the converter complex poles and slightly smaller oscillating frequency. The high-frequency pole is placed to achieve the needed phase margin [9]. The design is correct if the complex pole loci, heading to the complex zeros in the system root locus, never enter the right half-plane.

$$C_{PIDnf}(s) = T_{cp}\frac{s^2 + 2\xi_{cp}\omega_{0cp}s + \omega_{0cp}^2}{s\left(1 + s/\omega_{p1}\right)} = \frac{T_{cp}s}{1 + s/\omega_{p1}} + \frac{2T_{cp}\xi_{cp}\omega_{0cp}}{1 + s/\omega_{p1}} + \frac{T_{cp}\omega_{0cp}^2}{s\left(1 + s/\omega_{p1}\right)} = \frac{T_{cp}s}{1 + s/\omega_{p1}} + \frac{T_{cp}\omega_{0pc}^2\left(1 + 2s\xi_{cp}/\omega_{0cp}\right)}{s\left(1 + s/\omega_{p1}\right)} \quad (34.52)$$

For systems with a high-frequency zero placed at least one decade above the two lightly damped complex poles, the compensator (34.53), with $\omega_{z1} \approx \omega_{z2} < \omega_p$, can be used. Usually, the two real zeros present frequencies slightly lower than the frequency of the converter complex poles. The two high-frequency poles are placed to obtain the desired phase margin [9]. The obtained overall performance will often be inferior to that of the PID type notch filter.

$$C_{PID}(s) = W_{cp}\frac{(1 + s/\omega_{z1})(1 + s/\omega_{z2})}{s\left(1 + s/\omega_p\right)^2} \quad (34.53)$$

34.2.5.2 Compensator Selection and Design

The procedure to select the compensator and to design its parameters can be outlined as follows:

1. Compensator selection: In general, since V_{DC} perturbations exist, null steady-state error guarantee is needed. High-frequency poles are usually necessary, if the transfer function shows a −6 dB/octave roll-off due to high frequency left plane zeros. Therefore, in general, two types of compensation schemes with integral action (34.51 or 34.50), and (34.52 or 34.53) can be tried. Compensator (34.52) is usually convenient for systems with lightly damped complex poles;
2. Unity gain frequency ω_{0dB} choice:
   - If the selected compensator has no complex zeros, it is better to be conservative, choosing ω_{0dB} well below the frequency of the lightly damped poles of the converter (or the frequency of the right half plane zeros if lower). However, because of the resonant peak of most converter transfer functions, the phase margin can be obtained at a frequency near the resonance. If the phase margin is not enough, the compensator gain must be lowered;
   - If the selected compensator has complex zeros, ω_{0dB} can be chosen slightly above the frequency of the lightly damped poles;
3. Desired phase margin (ϕ_M) specification $\phi_M \geq 30°$ (preferably between 45° and 70°);
4. Compensator zero-pole placement to achieve the desired phase margin:
   - With the integral plus zero-pole compensation type (34.51), the compensator phase ϕ_{cp}, at the maximum frequency of unity gain (often ω_{0dB}), equals the phase margin (ϕ_M) minus 180° and minus the converter phase ϕ_{cv}, ($\phi_{cp} = \phi_M - 180° - \phi_{cv}$). The zero-pole position can be obtained calculating the factor $f_{ct} = tg(\pi/2 + \phi_{cp}/2)$ being $\omega_z = \omega_{0dB}/f_{ct}$ and $\omega_M = \omega_{0dB}f_{ct}$.
   - With the PID notch filter type (34.52) controller, the two complex zeros are placed to have a damping factor equal to two times the damping of the converter complex poles, and oscillating frequency ω_{0cp} 30% smaller. The high-frequency pole ω_{p1} is placed to achieve the needed phase margin ($\omega_{p1} \approx (\omega_{0cp}\cdot\omega_{0dB})^{1/2}f_{ct}^2$ with $f_{ct} = tg(\pi/2+\phi_{cp}/2)$ and $\phi_{cp} = \phi_M - 180° - \phi_{cv}$ [5]).
5. Compensator gain calculation (the product of the converter and compensator gains at the ω_{0dB} frequency must be one).
6. Stability margins verification using Bode plots and root locus.
7. Results evaluation. Restarting the compensator selection and design, if the attained results are still not good enough.

34.2.6 Examples: Buck–Boost DC/DC Converter, Forward DC/DC Converter, 12 Pulse Rectifiers, Buck–Boost DC/DC Converter in the Discontinuous Mode (Voltage and Current Mode), Three-phase PWM Inverters

EXAMPLE 34.4 Feedback design for the buck–boost dc/dc converter

Consider the converter output voltage v_o (Fig. 34.1) to be the controlled output. From Example 34.2 and Eqs. (34.33) and (34.35), the block diagram of Fig. 34.7 is obtained. The modulator transfer function is considered a pure gain ($G_M = 0.1$). The magnitude and phase of the

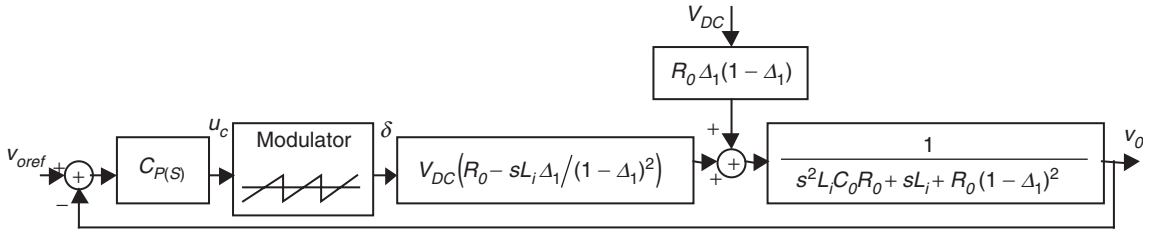


FIGURE 34.7 Block diagram of the linearized model of the closed loop buck–boost converter.

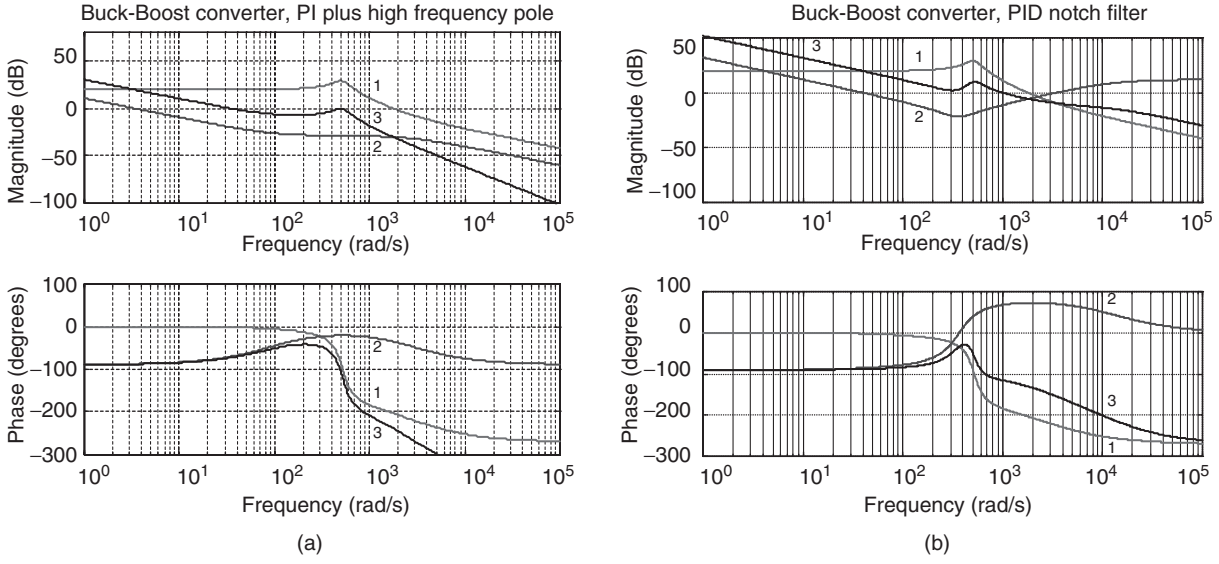


FIGURE 34.8 Bode plots for the buck–boost converter. Trace 1 – switching converter magnitude and phase; trace 2 – compensator magnitude and phase; trace 3 – resulting magnitude and phase of the compensated converter: (a) PI plus high-frequency pole compensation with 60° phase margin, $\omega_{0dB} = 500$ rad/s and (b) PID notch filter compensation with 65° phase margin, $\omega_{0dB} = 1000$ rad/s.

open-loop transfer function v_o/u_c (Fig. 34.8a trace 1), shows a resonant peak due to the two lightly damped complex poles and the associated −12 dB/octave roll-off. The right half-plane zero changes the roll-off to −6 dB/octave and adds −90° to the converter phase (nonminimum-phase converter).

Compensator selection. As V_{DC} perturbations exist null steady-state error guarantee is needed. High-frequency poles are needed given the −6 dB/octave final slope of the transfer function. Therefore, two compensation schemes (34.51 and 34.52) with integral action are tried here. The buck–boost converter controlled with integral plus zero-pole compensation presents, in closed-loop, two complex poles closer to the imaginary axes than in open-loop. These poles should not dominate the converter dynamics. Instead, the real pole resulting from the open-loop pole placed at the origin should be almost the dominant one, thus slightly lowering the calculated compensator gain. If the ω_{0dB} frequency is chosen too low, the integral plus zero-pole compensation turns into a pure integral compensator ($\omega_z = \omega_M = \omega_{0dB}$). However, the obtained gains are too low, leading to very slow transient responses.

Results showing the transient responses to v_{oref} and V_{DC} step changes, using the selected compensators and converter Bode plots (Fig. 34.8), are shown (Fig. 34.9). The compensated real converter transient behavior occurs in the buck and in the boost regions. Notice the nonminimum-phase behavior of the converter (mainly in Fig. 34.9b), the superior performance of the PID notch filter compensator and the unacceptable behavior of the PI with high-frequency pole. Care should be taken with load changes, when using this compensator, since instability can easily occur.

The compensator critical values, obtained with the root-locus studies, are $W_{cpcrit} = 700\,\mathrm{s}^{-1}$ for the integral plus zero-pole compensator, $T_{cpcrit} = 0.0012$ s for the PID notch filter, and $W_{Icpcrit} = 18\,\mathrm{s}^{-1}$ for the integral compensation derived from the integral plus zero-pole compensator ($\omega_z = \omega_M$). This confirms the Bode-plot design and allows stability estimation with changing loads and power supply.

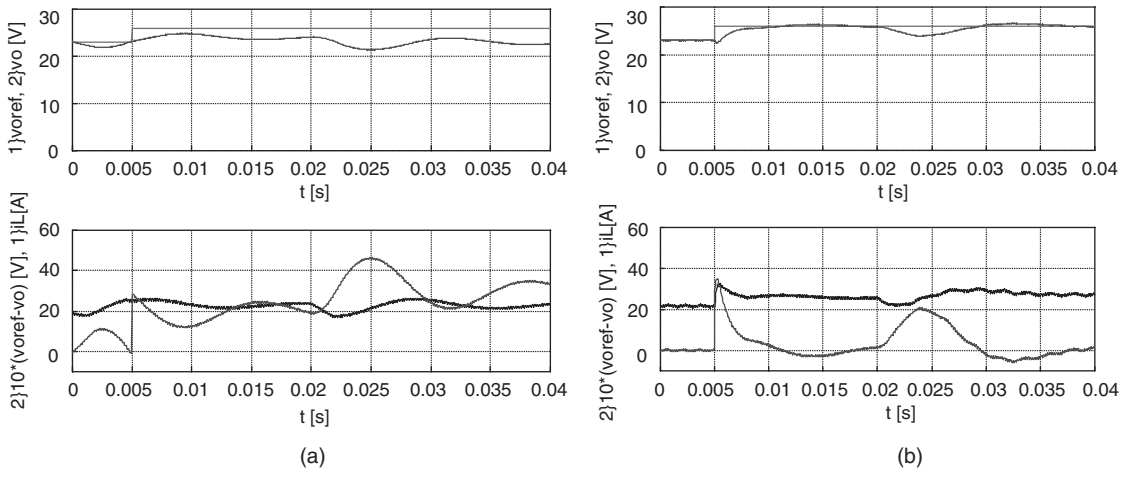


FIGURE 34.9 Transient responses of the compensated buck–boost converter. At $t = 0.005\,\text{s}$, v_{oref} step from 23 to 26 V. At $t = 0.02\,\text{s}$, V_{DC} step from 26 to 23 V. Top graphs: step reference v_{oref} and output voltage v_o. Bottom graphs: trace starting at 20 is i_L current; trace starting at zero is $10 \times (v_{oref} - v_o)$: (a) PI plus high-frequency pole compensation with 60° phase margin and $\omega_{0dB} = 500$ rad/s and (b) PID notch filter compensation with 64° phase margin and $\omega_{0dB} = 1000$ rad/s.

EXAMPLE 34.5 Feedback design for the forward dc/dc converter

Consider the output voltage v_o of the forward converter (Fig. 34.4a) to be the controlled output. From Example 34.3 and Eqs. (34.45) and (34.47), the block diagram of Fig. 34.10 is obtained. As in Example 34.4, the modulator transfer function is considered as a pure gain ($G_M = 0.1$). The magnitude and phase of the open-loop transfer function v_o/u_c (Fig. 34.11a, trace 1), shows an open-loop stable system. Since integral action is needed to have some disturbance rejection of the voltage source V_{DC}, the compensation schemes used in Example 34.4, obtained using the same procedure (Fig. 34.11), were also tested.

Results, showing the transient responses to v_{oref} and V_{DC} step changes, are shown (Fig. 34.12). Both compensators (34.51) and (34.52) are easier to design than the ones for the buck–boost converter, and both have acceptable performances. Moreover, the PID notch filter presents a much faster response.

Alternatively, a PID feedback controller such as Eq. (34.53) can be easily hand-adjusted, starting with the proportional, integral, and derivative gains all set to zero. In the first step, the proportional gain is increased until the output presents an oscillatory response with nearly 50% overshoot. Next, the derivative gain is slowly increased until the overshoot is eliminated. Finally, the integral gain is increased to eliminate the steady-state error as quickly as possible.

EXAMPLE 34.6 Feedback design for phase controlled rectifiers in the continuous mode

Phase controlled, p pulse ($p > 1$), thyristor rectifiers (Fig. 34.13a), operating in the continuous mode, present an output voltage with p identical segments within the mains period T. Given this cyclic waveform, the **A**, **B**, **C**, and **D** matrices for all these p intervals can be written with the same form, inspite of the topological variation. Hence, the state-space averaged model is obtained simply by averaging all the variables within the period T/p. Assuming small variations, the mean value of the rectifier output voltage U_{DC} can be written [10]:

$$U_{DC} = U_p \frac{p}{\pi} \sin\left(\frac{\pi}{p}\right) \cos\alpha \tag{34.54}$$

where α is the triggering angle of the thyristors, and U_p the maximum peak value of the rectifier output voltage, determined by the rectifier topology and the ac supply voltage. The α value can be obtained ($\alpha = (\pi/2) \times (1 - u_c/u_{cmax})$) using the modulator of Fig. 34.6b, where $\omega = 2\pi/T$ is the mains frequency. From Eq. (34.54), the incremental gain K_R of the modulator plus rectifier yields:

$$K_R = \frac{\partial U_{DC}}{\partial u_c} = U_p \frac{p}{2u_{cmax}} \sin\left(\frac{\pi}{p}\right) \cos\left(\frac{\pi u_c}{2u_{cmax}}\right) \tag{34.55}$$

For a given rectifier, this gain depends on u_c, and should be calculated for a certain quiescent point. However, for feedback design purposes, keeping in mind that the rectifier could be required to be stable in all operating

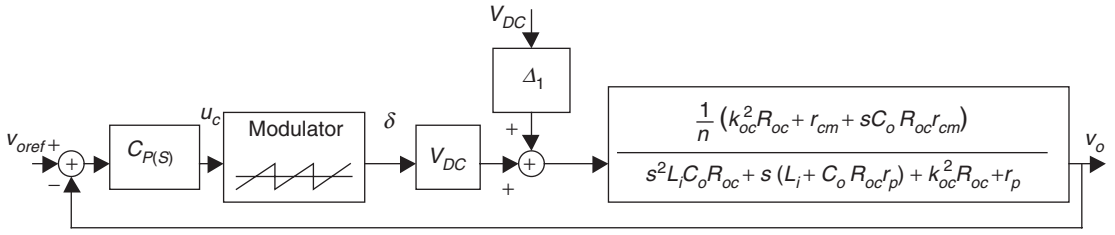


FIGURE 34.10 Block diagram of the linearized model of the closed-loop controlled forward converter.

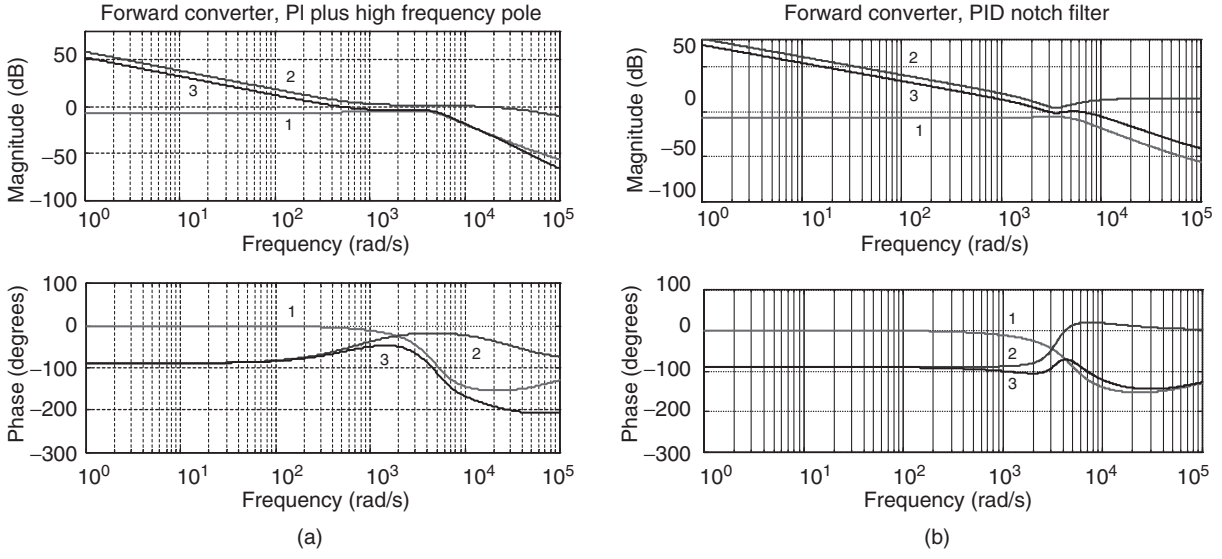


FIGURE 34.11 Bode plots for the forward converter. Trace 1 – switching converter magnitude and phase; trace 2 – compensator magnitude and phase; trace 3 – resulting magnitude and phase of the compensated converter: (a) PI plus high-frequency pole compensation with 115° phase margin, $\omega_{0dB} = 500$ rad/s and (b) PID notch filter compensation with 85° phase margin, $\omega_{0dB} = 6000$ rad/s.

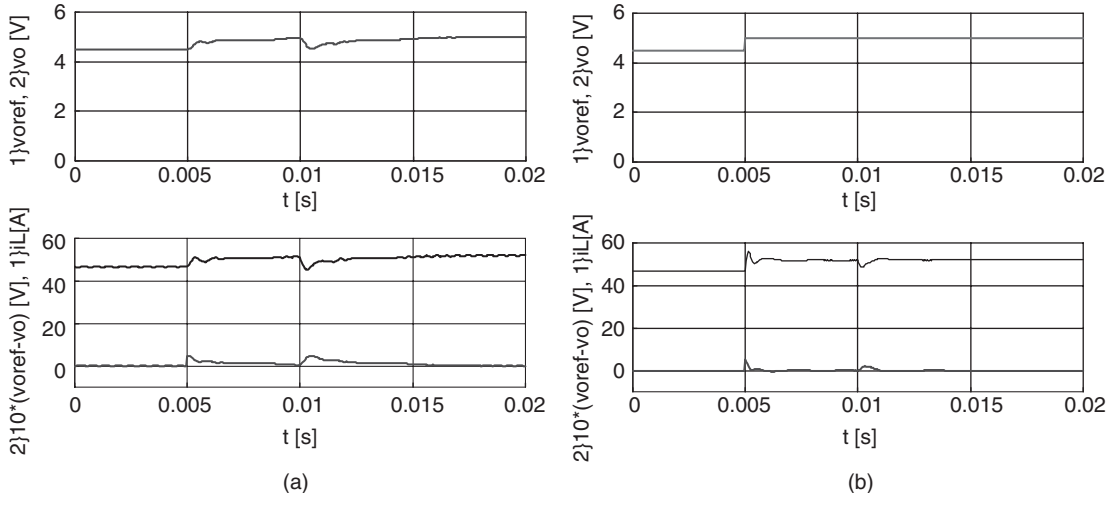


FIGURE 34.12 Transient responses of the compensated forward converter. At $t = 0.005$ s, v_{oref} step from 4.5 to 5 V. At $t = 0.01$ s, V_{DC} step from 300 to 260 V. Top graphs: step reference v_{oref} and output voltage v_o. Bottom graphs: top traces i_L current; bottom traces $10\times$ $(v_{oref} - v_o)$; (a) PI plus high-frequency pole compensation with 115° phase margin and $\omega_{0dB} = 500$ rad/s and (b) PID notch filter compensation with 85° phase margin and $\omega_{0dB} = 6000$ rad/s.

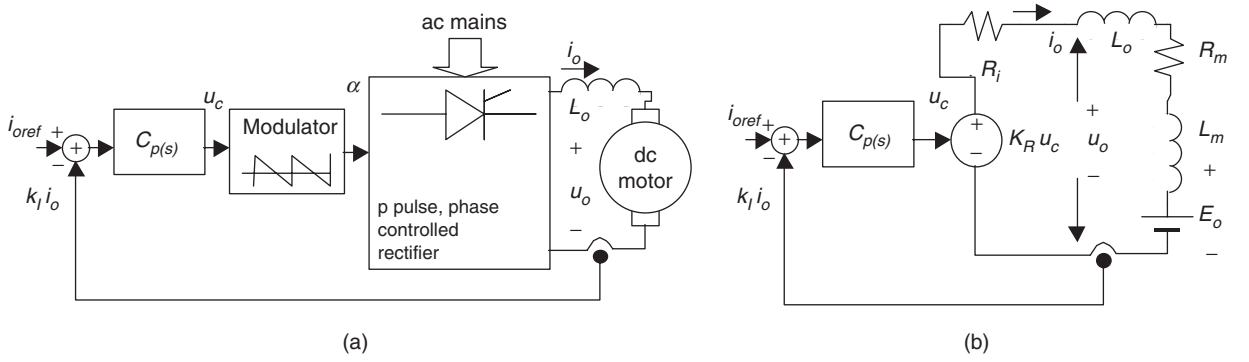


FIGURE 34.13 (a) Block diagram of a p pulse phase controlled rectifier feeding a separately excited dc motor and (b) equivalent averaged circuit.

points, the maximum value of K_R, denoted K_{RM}, can be used:

$$K_{RM} = U_p \frac{p}{2u_{cmax}} \sin\left(\frac{\pi}{p}\right) \tag{34.56}$$

The operation of the modulator, coupled to the rectifier thyristors, introduces a non-neglectable time delay, with mean value $T/2p$. Therefore, from Eq. (34.48) the modulator-rectifier transfer function $G_R(s)$ is

$$G_R(s) = \frac{U_{DC}(s)}{u_c(s)} = K_{RM}\, e^{-s(T/2p)} \approx \frac{K_{RM}}{1 + s\left(T/2p\right)} \tag{34.57}$$

Considering zero U_p perturbations, the rectifier equivalent averaged circuit (Fig. 34.13b) includes the loss-free rectifier output resistance R_i, due to the overlap in the commutation phenomenon caused by the mains inductance. Usually, $R_i \approx p\omega l/\pi$ where l is the equivalent inductance of the lines paralleled during the overlap, half of the line inductance for most rectifiers, except for single-phase bridge rectifiers where l is the line inductance. Here, L_o is the smoothing reactor and R_m, L_m, and E_o are respectively the armature internal resistance, inductance, and back electromotive force of a separately excited dc motor (typical load). Assuming the mean value of the output current as the controlled output, making $L_t = L_o + L_m$, $R_t = R_i + R_m$, $T_t = L_t/R_t$ and applying Laplace transforms to the differential equation obtained from the circuit of Fig. 34.13b, the output current transfer function is

$$\frac{i_o(s)}{U_{DC}(s) - E_o(s)} = \frac{1}{R_t(1 + sT_t)} \tag{34.58}$$

The rectifier and load are now represented by a perturbed (E_o) second-order system (Fig. 34.14). To achieve zero steady-state error, which ensures steady-state insensitivity to the perturbations, and to obtain closed-loop second-order dynamics, a PI controller (34.50) was selected for $C_p(s)$ (Fig. 34.14). Canceling the load pole $(-1/T_t)$ with the PI zero $(-1/T_z)$ yields:

$$T_z = L_t/R_t \tag{34.59}$$

The rectifier closed-loop transfer function $i_o(s)/i_{oref}(s)$, with zero E_o perturbations, is

$$\frac{i_o(s)}{i_{oref}(s)} = \frac{2pK_{RM}k_I/\left(R_t T_p T\right)}{s^2 + \left(2p/T\right)s + 2pK_{RM}k_I/\left(R_t T_p T\right)} \tag{34.60}$$

The final value theorem enables the verification of the zero steady-state error. Comparing the denominator of

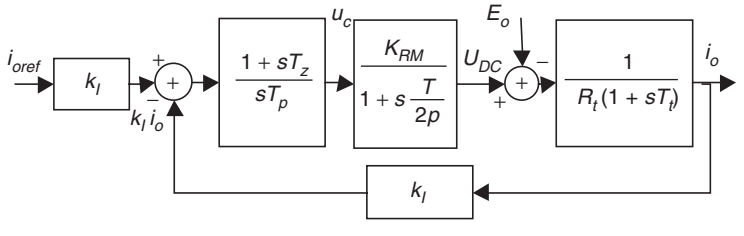


FIGURE 34.14 Block diagram of a PI controlled p pulse rectifier.

Eq. (34.60) to the second-order polynomial $s^2+2\zeta\omega_n s+\omega_n^2$ yields:

$$\omega_n^2 = 2pK_{RM}k_I/\left(R_t T_p T\right)$$
$$4\zeta^2\omega_n^2 = \left(2p/T\right)^2 \tag{34.61}$$

Since only one degree of freedom is available (T_p), the damping factor ζ is imposed. Usually $\zeta = \sqrt{2}/2$ is selected, since it often gives the best compromise between response speed and overshoot. Therefore, from Eq. (34.61), Eq. (34.62) arises:

$$Tp = 4\zeta^2 K_{RM}k_I T/\left(2pR_t\right) = K_{RM}k_I T/\left(pR_t\right) \tag{34.62}$$

Note that both T_z (34.59) and T_p (34.62) are dependent upon circuit parameters. They will have the correct values only for dc motors with parameters closed to the nominal load value. Using Eq. (34.62) in Eq. (34.60) yields Eq. (34.63), the second-order closed-loop transfer function of the rectifier, showing that, with loads close to the nominal value, the rectifier dynamics depend only on the mean delay time $T/2p$.

$$\frac{i_o(s)}{i_{oref}(s)} = \frac{1}{2\left(T/2p\right)^2 s^2 + sT/p + 1} \tag{34.63}$$

From Eq. (34.63) $\omega_n = \sqrt{2}p/T$ results, which is the maximum frequency allowed by $\omega T/2\mathrm{p} < \sqrt{2}/2$, the validity limit of Eq. (34.48). This implies that $\zeta \geq \sqrt{2}/2$, which confirms the preceding choice. For $U_p = 300\,\mathrm{V}$, $p = 6$, $T = 20\,\mathrm{ms}$, $l = 0.8\,\mathrm{mH}$, $R_m = 0.5\,\Omega$, $L_t = 50\,\mathrm{mH}$, $E_o = -150\,\mathrm{V}$, $u_{cmax} = 10\,\mathrm{V}$, $k_I = 0.1$, Fig. 34.15a shows the rectifier output voltage $u_{oN}(u_{oN} = u_o/U_p)$ and the step response of the output current $i_{oN}(i_{oN} = i_o/40)$ in accordance with Eq. (34.63). Notice that the rectifier is operating in the inverter mode. Fig. 34.15b shows the effect, in the i_o current, of a 50% reduction in the E_o value. The output current is initially disturbed but the error vanishes rapidly with time.

This modeling and compensator design are valid for small perturbations. For large perturbations either the rectifier will saturate or the firing angles will originate large current overshoots. For large signals, antiwindup schemes (Fig. 34.16a) or error ramp limiters (or soft starters) and limiters of the PI integral component (Fig. 34.16b) must be used. These solutions will also work with other switching converters.

To use this rectifier current controller as the inner control loop of a cascaded controller for the dc motor speed regulation, a useful first-order approximation of Eq. (34.63) is $i_o(s)/i_{oref}(s) \approx 1/(sT/p+1)$.

Although allowing a straightforward compensator selection and precise calculation of its parameters, the rectifier modeling presented here is not suited for stability studies. The rectifier root locus will contain two complex conjugate poles in branches parallel to the imaginary axis. To study the current controller stability, at least the second-order term of Eq. (34.48) in Eq. (34.57) is needed. Alternative ways include the first-order Padé approximation of $e^{-sT/2p}$, $e^{-sT/2p} \approx (1 - sT/4p)/(1 + sT/4p)$, or the second-order approximation, $e^{-sT/2p} \approx (1 - sT/4p + (sT/2p)^2/12)/(1 + sT/4p + (sT/2p)^2/12)$. These approaches introduce zeros in the right half-plane (nonminimum-phase systems), and/or extra poles, giving more realistic results. Taking a first-order approximation and root-locus techniques, it is found that the rectifier is stable for $T_p > K_{RM}k_I T/(4pR_t)$ ($\zeta > 0.25$). Another approach uses the conditions of magnitude and angle of the delay function $e^{-sT/2p}$ to obtain the

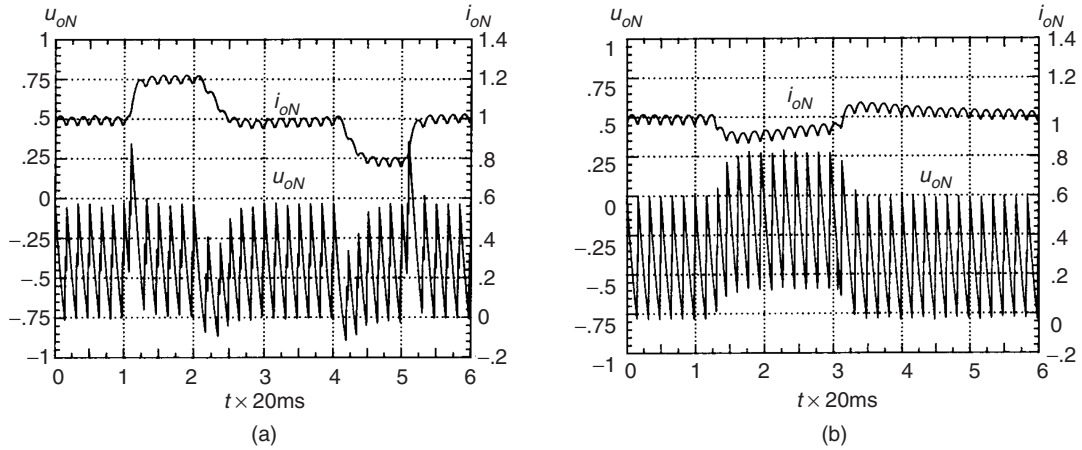


FIGURE 34.15 Transient response of the compensated rectifier: (a) step response of the controlled current i_o and (b) the current i_o response to a step chance to 50% of the E_o nominal value during 1.5 T.

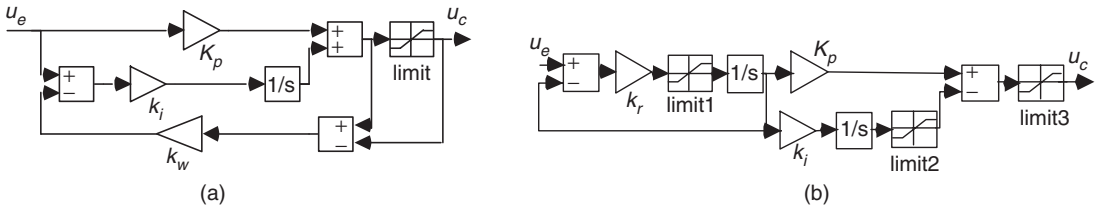


FIGURE 34.16 (a) PI implementation with antiwindup (usually $1/K_p \leq k_w \leq K_i/K_p$) to deal with rectifier saturation and (b) PI with ramp limiter/soft starter ($k_r \gg K_p$) and integral component limiter to deal with large perturbations.

system root locus. Also, the switching converter can be considered as a sampled data system, at frequency p/T, and Z transform can be used to determine the critical gain and first frequency of instability $p/(2T)$, usually half the switching frequency of the rectifier.

EXAMPLE 34.7 Buck–Boost dc/dc converter feedback design in the discontinuous mode

The methodologies just described do not apply to switching converters operating in the discontinuous mode. However, the derived equivalent averaged circuit approach can be used, calculating the mean value of the discontinuous current supplied to the load, to obtain the equivalent circuit. Consider the buck–boost converter of Example 34.1 (Fig. 34.1) with the new values $L_i = 40\,\mu\text{H}$, $C_o = 1000\,\mu\text{F}$, $R_o = 15\,\Omega$. The mean value of the current i_{Lo}, supplied to the output capacitor and resistor of the circuit operating in the discontinuous mode, can be calculated noting that, if the input V_{DC} and output v_o voltages are essentially constant (low ripple), the inductor current rises linearly from zero, peaking at $I_P = (V_{DC}/L_i)\delta_1 T$ (Fig. 34.17a). As the mean value of i_{Lo}, supposed linear, is $I_{Lo} = (I_P\delta_2 T)/(2T)$, using the steady-state input–output relation $V_{DC}\delta_1 = V_o\delta_2$ and the above I_P value, I_{Lo} can be written:

$$I_{Lo} = \frac{\delta_1^2 V_{DC}^2 T}{2L_i V_o} \tag{34.64}$$

This is a nonlinear relation that could be linearized around an operating point. However, switching converters in the discontinuous mode seldom operate just around an operating point. Therefore, using a quadratic modulator (Fig. 34.18), obtained integrating the ramp $r(t)$ (Fig. 34.6a) and comparing the quadratic curve to the term $u_{cPI}\,v_o/V_{DC}^2$ (which is easily implemented using the Unitrode UC3854 integrated circuit), the duty cycle δ_1 is $\delta_1 = \sqrt{u_{cPI}\,V_o/\left(u_{cmax}\,V_{DC}^2\right)}$, and a constant incremental factor K_{CV} can be obtained:

$$K_{CV} = \frac{\partial I_{Lo}}{\partial u_{cPI}} = \frac{T}{2u_{cmax}L_i} \tag{34.65}$$

Considering zero-voltage perturbations and neglecting the modulator delay, the equivalent averaged circuit (Fig. 34.17b) can be used to derive the output voltage to input current transfer function $v_o(s)/i_{Lo}(s) = R_o/(sC_oR_o + 1)$. Using a PI controller (34.50), the closed-loop transfer function is

$$\frac{v_o(s)}{v_{oref}(s)} = \frac{K_{CV}\,(1+sT_z)/C_oT_p}{s^2+s\left(T_p+T_zK_{CV}k_vR_o\right)\big/C_oR_oT_p+K_{CV}k_v/C_oT_p} \tag{34.66}$$

Since two degrees of freedom exist, the PI constants are derived imposing ζ and ω_n for the second-order denominator of Eq. (34.66), usually $\zeta \geq \sqrt{2}/2$ and $\omega_n \leq 2\pi f_s/10$. Therefore:

$$\begin{aligned} T_p &= K_{CV}k_v\big/\left(\omega_n^2 C_o\right) \\ T_z &= T_p\,(2\zeta\omega_n C_oR_o - 1)\big/\left(K_{CV}\,k_vR_o\right) \end{aligned} \tag{34.67}$$

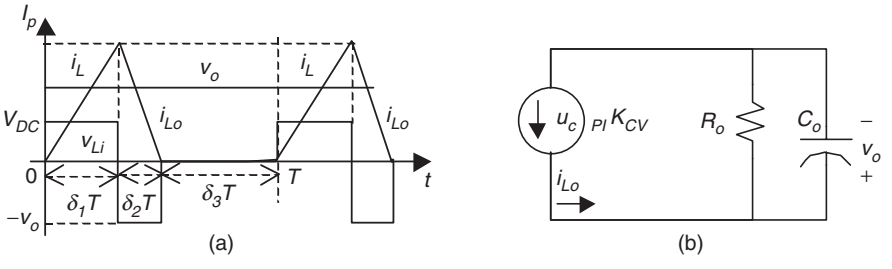


FIGURE 34.17 (a) Waveforms of the buck–boost converter in the discontinuous mode and (b) equivalent averaged circuit.

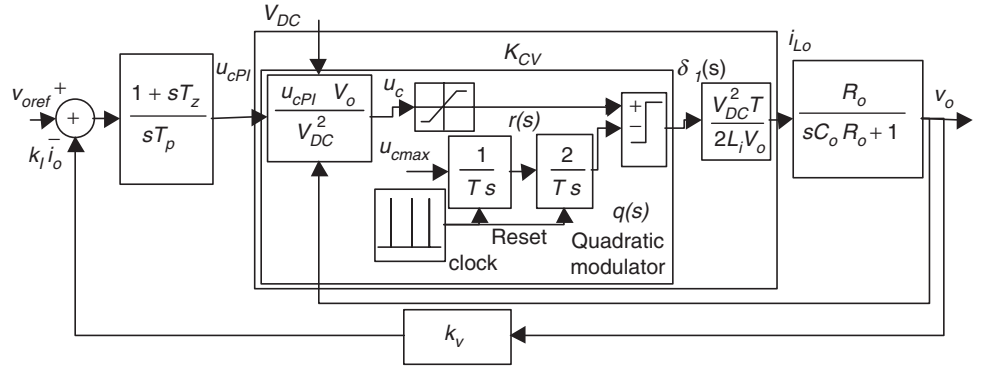


FIGURE 34.18 Block diagram of a PI controlled (feedforward linearized) buck–boost converter operating in the discontinuous mode.

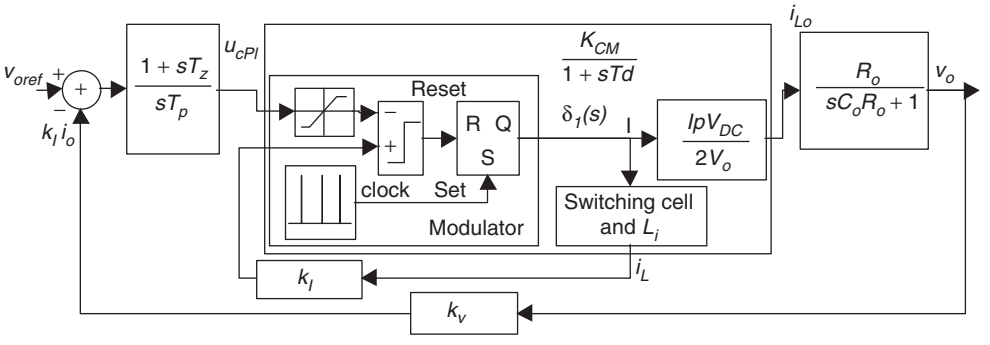


FIGURE 34.19 Block diagram of a current-mode controlled buck–boost converter operating in the discontinuous mode.

The transient behavior of this converter, with $\zeta = 1$ and $\omega_n \approx \pi f_s/10$, is shown in Fig. 34.20a. Compared to Example 34.2, the operation in the discontinuous conduction mode reduces, by 1, the order of the state-space averaged model and eliminates the zero in the right-half of the complex plane. The inductor current does not behave as a true state variable, since during the interval $\delta_3 T$ this current is zero, and this value is always the i_{Lo} current initial condition. Given the differences between these two examples, care should be taken to avoid the operation in the continuous mode of converters designed and compensated for the discontinuous mode. This can happen during turn-on or step load changes and, if not prevented, the feedback design should guarantee stability in both modes (Example 34.8, Fig. 34.19a).

EXAMPLE 34.8 Feedback design for the buck–boost dc/dc converter operating in the discontinuous mode and using current-mode control

The performances of the buck–boost converter operating in the discontinuous mode can be greatly enhanced if a *current-mode control* scheme is used, instead of the voltage mode controller designed in Example 34.7. Current-mode control in switching converters is the simplest form of state feedback. Current mode needs the measurement of the current i_L (Fig. 34.1) but greatly simplifies the modulator design (compare Fig. 34.18 to Fig. 34.19), since no modulator linearization is used. The measured value, proportional to the current i_L, is compared to the value u_{cPI} given by the output voltage controller (Fig. 34.19). The modulator switches off the power semiconductor when $k_I I_P = u_{cPI}$.

Expressed as a function of the peak i_L current I_P, I_{Lo} becomes (Example 34.7) $I_{Lo} = I_P \delta_1 V_{DC}/(2V_o)$, or considering the modulator task $I_{Lo} = u_{cPI}\delta_1 V_{DC}/(2k_I V_o)$. For small perturbations, the incremental gain is $K_{CM} = \partial I_{Lo}/\partial u_{cPI} = \delta_1 V_{DC}/(2k_I V_o)$. An I_{Lo} current delay $T_d = 1/(2f_s)$, related to the switching frequency f_s can be assumed. The current mode control transfer function $G_{CM}(s)$ is

$$G_{CM}(s) = \frac{I_{Lo}(s)}{u_{cPI}(s)} \approx \frac{K_{CM}}{1 + sT_d} \approx \frac{\delta_1 V_{DC}}{2k_I V_o (1 + sT_d)} \quad (34.68)$$

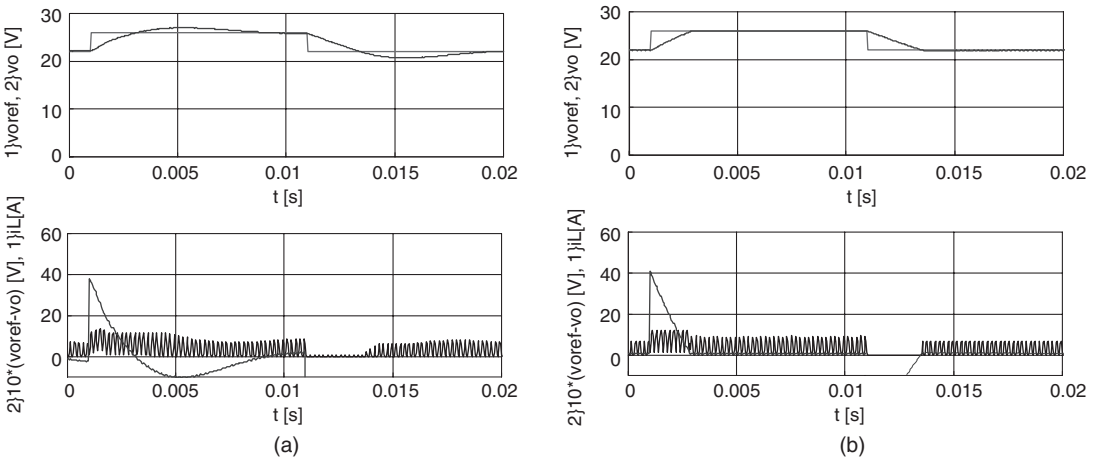


FIGURE 34.20 Transient response of the compensated buck–boost converter in the discontinuous mode. At $t = 0.001$ s v_{oref} step from 23 to 26 V. At $t = 0.011$ s, v_{oref} step from 26 to 23 V. Top graphs: step reference v_{oref} and output voltage v_o. Bottom graphs: pulses, i_L current; trace peaking at 40, $10\times$ $(v_{oref} - v_o)$: (a) PI controlled and feedforward linearized buck–boost converter with $\zeta = 1$ and $\omega_n \approx \pi f_s/10$ and (b) Current-mode controlled buck–boost with $\zeta = 1$ and maximum value $I_{pmax} = 15$ A.

Using the approach of Example 34.6, the values for T_z and T_p are given by Eq. (34.69).

$$\begin{aligned} T_z &= R_o C_o \\ T_p &= 4\zeta^2 K_{CM} k_v R_o T_d \end{aligned} \tag{34.69}$$

The transient behavior of this converter, with $\zeta = 1$ and maximum value for I_p, $I_{pmax} = 15$ A, is shown in Fig. 34.19b. The output voltage step response presents no overshoot, no steady-state error, and better dynamics, compared to the response (Fig. 34.19a) obtained using the quadratic modulator (Fig. 34.18). Notice that, with current mode control, the converter behaves like a reduced order system and the right half-plane zero is not present.

The current-mode control scheme can be advantageously applied to converters operating in the continuous mode, guarantying short-circuit protection, system order reduction, and better performances. However, for converters operating in the step-up (boost) regime, a stabilizing ramp with negative slope is required, to ensure stability, the stabilizing ramp will transform the signal u_{cPI} in a new signal $u_{cPI} - \text{rem}(k_{sr}t/T)$ where k_{sr} is the needed amplitude for the compensation ramp and the function rem is the remainder of the division of $k_{sr}t$ by T. In the next section, current control of switching converters will be detailed.

Closed-loop control of resonant converters can be achieved using the outlined approaches, if the resonant phases of operation last for small intervals compared to the fundamental period. Otherwise, the equivalent averaged circuit concept can often be used and linearized, now considering the resonant converter input–output relations, normally functions of the driving frequency and input or output voltages, to replace the δ_1 variable.

EXAMPLE 34.9 Output voltage control in three-phase voltage-source inverters using sinusoidal wave PWM (SWPWM) and space vector modulation (SVM)

Sinusoidal wave PWM

Voltage-source three-phase inverters (Fig. 34.21) are often used to drive squirrel cage induction motors (IM) in variable speed applications.

Considering almost ideal power semiconductors, the output voltage $u_{bk}(k \in \{1, 2, 3\})$ dynamics of the inverter is negligible as the output voltage can hardly be considered a state variable in the time scale describing the motor behavior. Therefore, the best known method to create sinusoidal output voltages uses an open-loop modulator with low-frequency sinusoidal waveforms $\sin(\omega t)$, with the amplitude defined by the modulation index m_i ($m_i \in [0, 1]$), modulating high-frequency triangular waveforms $r(t)$ (carriers), Fig. 34.22, a process similar to the one described in Section 34.2.4.

This sinusoidal wave PWM (SWPWM) modulator generates the variable γ_k, represented in Fig. 34.22 by the rectangular waveform, which describes the inverter k leg state:

$$\gamma_k = \begin{cases} 1 \rightarrow \text{when } m_i \sin(\omega t) > r(t) \\ 0 \rightarrow \text{when } m_i \sin(\omega t) < r(t) \end{cases} \tag{34.70}$$

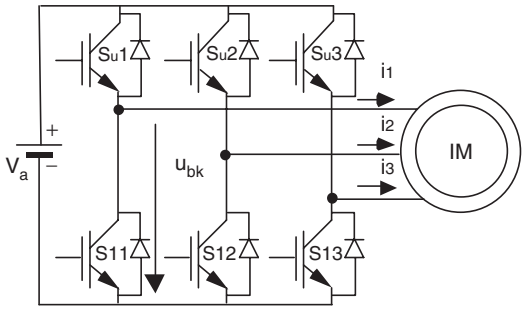


FIGURE 34.21 IGBT-based voltage-sourced three-phase inverter with induction motor.

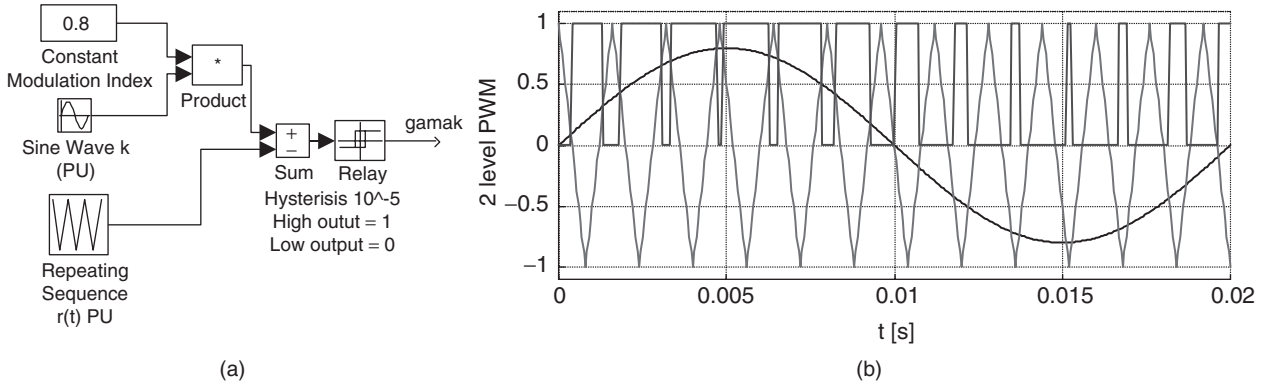


FIGURE 34.22 (a) SWPWM modulator schematic and (b) main SWPWM signals.

The turn-on and turn-off signals for the k leg inverter switches are related with the variable γ_k as follows:

$$\gamma_k = \begin{cases} 1 \rightarrow \text{then } Su_k \text{ is on and } sl_k \text{ is off} \\ 0 \rightarrow \text{then } Su_k \text{ is off and } sl_k \text{ is on} \end{cases} \tag{34.71}$$

This applies constant-frequency sinusoidally weighted PWM signals to the gates of each insulated gate bipolar transistor (IGBT). The PWM signals for all the upper IGBTs (Su_k, $k \in \{1, 2, 3\}$) must be 120° out of phase and the PWM signal for the lower IGBT Sl_k must be the complement of the Su_k signal. Since transistor turn-on times are usually shorter than turn-off times, some dead time must be included between the Su_k and Sl_k pulses to prevent internal short-circuits.

Sinusoidal PWM can be easily implemented using a microprocessor or two digital counters/timers generating the addresses for two lookup tables (one for the triangular function, another for supplying the per unit basis of the sine, whose frequency can vary). Tables can be stored in read only memories, ROM, or erasable programmable ROM, EPROM. One multiplier for the modulation index (perhaps into the digital-to-analog (D/A) converter for the sine ROM output) and one hysteresis comparator must also be included.

With SWPWM, the first harmonic maximum amplitude of the obtained line-to-line voltage is only about 86% of the inverter dc supply voltage V_a. Since it is expectable that this amplitude should be closer to V_a, different modulating voltages (for example, adding a third-order harmonic with one-fourth of the fundamental sine amplitude) can be used as long as the fundamental harmonic of the line-to-line voltage is kept sinusoidal. Another way is to leave SWPWM and consider the eight possible inverter output voltages trying to directly use then. This will lead to space vector modulation.

Space vector modulation

Space vector modulation (SVM) is based on the polar representation (Fig. 34.23) of the eight possible base output voltages of the three-phase inverter (Table 34.1, where v_α, v_β are the vector components of vector $\vec{V}_g, g \in \{0, 1, 2, 3, 4, 5, 6, 7\}$, obtained with Eq. (34.72). Therefore, as all the available voltages can be used, SVM does not present the voltage limitation of SWPWM.

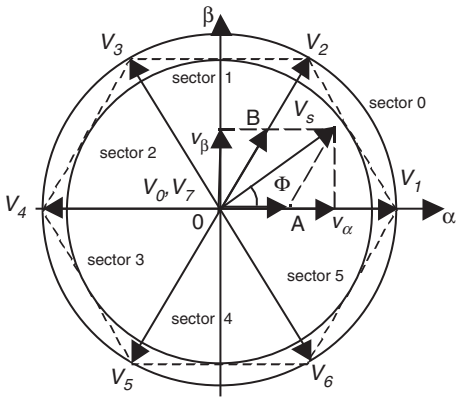


FIGURE 34.23 α, β space vector representation of the three-phase bridge inverter leg base vectors.

TABLE 34.1 The three-phase inverter with eight possible γ_k combinations, vector numbers, and respective α, β components

γ_1	γ_2	γ_3	u_{bk}	$u_{bk} - u_{bk+1}$	v_α	v_β	Vector
0	0	0	0	0	0	0	$\vec{V}_0$
1	0	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$\sqrt{2/3}V_a$	0	$\vec{V}_1$
1	1	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$V_a/\sqrt{6}$	$V_a/\sqrt{2}$	$\vec{V}_2$
0	1	0	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-V_a/\sqrt{6}$	$V_a/\sqrt{2}$	$\vec{V}_3$
0	1	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-\sqrt{2/3}V_a$	0	$\vec{V}_4$
1	1	1	V_a	0	0	0	$\vec{V}_7$
1	0	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$V_a/\sqrt{6}$	$-V_a/\sqrt{2}$	$\vec{V}_6$
0	0	1	$\gamma_k V_a$	$(\gamma_k - \gamma_{k+1})V_a$	$-V_a/\sqrt{6}$	$-V_a/\sqrt{2}$	$\vec{V}_5$

Furthermore, being a vector technique, SVM fits nicely with the vector control methods often used in IM drives.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \gamma_3 \end{bmatrix} V_a \quad (34.72)$$

Consider that the vector $\vec{V}_s$ (magnitude V_s, angle Φ) must be applied to the IM. Since there is no such vector available directly, SVM uses an averaging technique to apply the two vectors, $\vec{V}_1$ and $\vec{V}_2$, closest to $\vec{V}_s$. The vector $\vec{V}_1$ will be applied during $\delta_A T_s$ while vector $\vec{V}_2$ will last $\delta_B T_s$ (where $1/T_s$ is the inverter switching frequency, δ_A and δ_B are duty cycles, $\delta_A, \delta_B \in [0, 1]$). If there is any leftover time in the PWM period T_s, then the zero vector is applied during time $\delta_0 T_s = T_s - \delta_A T_s - \delta_B T_s$. Since there are two zero vectors ($\vec{V}_0$ and $\vec{V}_7$) a symmetric PWM can be devised, which uses both $\vec{V}_0$ and $\vec{V}_7$, as shown in Fig. 34.24. Such a PWM arrangement minimizes the power semiconductor switching frequency and IM torque ripples.

The input to the SVM algorithm is the space vector $\vec{V}_s$, into the sector s_n, with magnitude V_s and angle Φ_s. This vector can be rotated to fit into sector 0 (Fig. 34.23) reducing Φ_s to the first sector, $\Phi = \Phi_s - s_n\pi/3$. For any $\vec{V}_s$ that is not exactly along one of the six nonnull inverter base vectors (Fig. 34.23), SVM must generate an approximation by applying the two adjacent vectors during an appropriate amount of time. The algorithm can be devised considering that the projections of $\vec{V}_s$, onto the two closest base vectors, are values proportional to δ_A and δ_B duty cycles. Using simple trigonometric relations in sector 0 ($0 < \Phi < \pi/3$) Fig. 34.23, and considering K_T the proportional ratio, δ_A and δ_B are, respectively, $\delta_A = K_T\overline{OA}$ and $\delta_B = K_T\overline{OA}$, yielding:

$$\delta_A = K_T \frac{2V_s}{\sqrt{3}} \sin\left(\frac{\pi}{3} - \Phi\right)$$
$$\delta_B = K_T \frac{2V_s}{\sqrt{3}} \sin\Phi \quad (34.73)$$

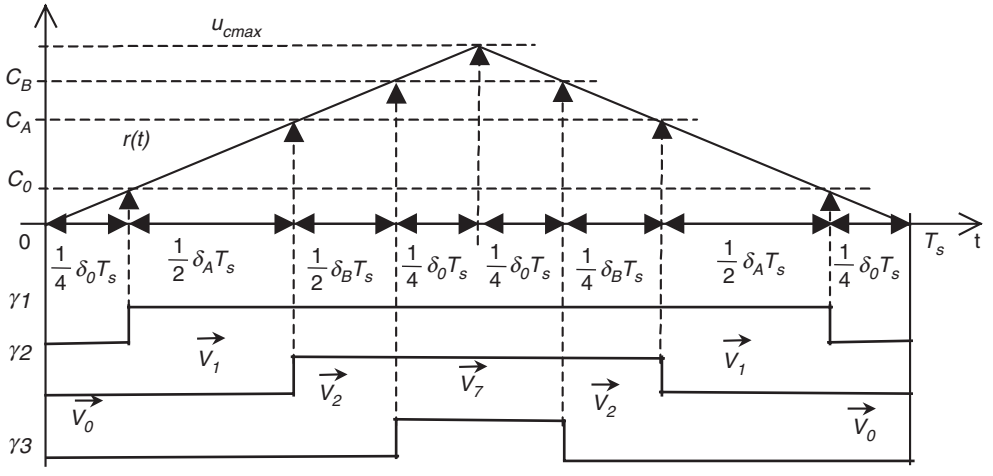


FIGURE 34.24 Symmetrical SVM.

The K_T value can be found if we notice that when $\vec{V}_s = \vec{V}_1$, $\delta_A = 1$, and $\delta_B = 0$ (or when $\vec{V}_s = \vec{V}_2$, $\delta_A = 0$, and $\delta_B = 1$). Therefore, since when $\vec{V}_s = \vec{V}_1$, $V_s = \sqrt{v_\alpha^2 + v_\beta^2} = \sqrt{2/3}V_a$, $\Phi = 0$, or when $\vec{V}_s = \vec{V}_2$, $V_s = \sqrt{2/3}V_a$, $\Phi = \pi/3$, the K_T constant is $K_T = \sqrt{3}/\left(\sqrt{2}V_a\right)$. Hence:

$$\begin{aligned}\delta_A &= \frac{\sqrt{2}\ V_s}{V_a}\sin\left(\frac{\pi}{3} - \Phi\right)\\ \delta_B &= \frac{\sqrt{2}\ V_s}{V_a}\sin\Phi\\ \delta_0 &= 1 - \delta_A - \delta_B\end{aligned} \tag{34.74}$$

The obtained resulting vector $\vec{V}_s$ cannot extend beyond the hexagon of Fig. 34.23. This can be understood if the maximum magnitude V_{sm} of a vector with $\Phi = \pi/6$ is calculated. Since, for $\Phi = \pi/6$, $\delta_A = 1/2$, and $\delta_B = 1/2$ are the maximum duty cycles, from Eq. (34.74) $V_{sm} = V_a/\sqrt{2}$ is obtained. This magnitude is lower than that of the vector $\vec{V}_1$ since the ratio between these magnitudes is $\sqrt{3}/2$. To generate sinusoidal voltages, the vector $\vec{V}_s$ must be inside the inner circle of Fig. 34.23, so that it can be rotated without crossing the hexagon boundary. Vectors with tips between this circle and the hexagon are reachable, but produce nonsinusoidal line-to-line voltages.

For sector 0, (Fig. 34.23) SVM symmetric PWM switching variables (γ_1, γ_2, γ_3) and intervals (Fig. 34.24) can be obtained by comparing a triangular wave with amplitude u_{cmax}, (Fig. 34.24, where $r(t) = 2u_{cmax}t/T_s$, $t \in [0, T_s/2]$) with the following values:

$$\begin{aligned}C_0 &= \frac{u_{c\max}}{2}\delta_0 = \frac{u_{c\max}}{2}(1 - \delta_A - \delta_B)\\ C_A &= \frac{u_{c\max}}{2}\left(\frac{\delta_0}{2} + \delta_A\right) = \frac{u_{c\max}}{2}(1 + \delta_A - \delta_B)\\ C_B &= \frac{u_{c\max}}{2}\left(\frac{\delta_0}{2} + \delta_A + \delta_B\right) = \frac{u_{c\max}}{2}(1 + \delta_A + \delta_B)\end{aligned} \tag{34.75}$$

Extension of Eq. (34.75) to all six sectors can be done if the sector number s_n is considered, together with the auxiliary matrix $\boldsymbol{\Xi}$:

$$\boldsymbol{\Xi}^T = \begin{bmatrix}-1 & -1 & 1 & 1 & 1 & -1\\ -1 & 1 & 1 & 1 & -1 & -1\end{bmatrix} \tag{34.76}$$

Generalization of the values C_0, C_A, and C_B, denoted C_{0sn}, C_{Asn}, and C_{Bsn} are written in Eq. (34.77), knowing that, for example, $\boldsymbol{\Xi}_{((sn+4)_{\text{mod }6}+1)}$ is the $\boldsymbol{\Xi}$ matrix row with number $(s_n + 4)_{\text{mod }6} + 1$.

$$\begin{aligned}C_{0sn} &= \frac{u_{c\max}}{2}\left(1 + \boldsymbol{\Xi}_{((Sn)\ \text{mod }6+1)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right)\\ C_{Asn} &= \frac{u_{c\max}}{2}\left(1 + \boldsymbol{\Xi}_{((Sn+4)\ \text{mod }6+1)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right)\\ C_{Bsn} &= \frac{u_{c\max}}{2}\left(1 + \boldsymbol{\Xi}_{((Sn+2)\ \text{mod }6+1)}\begin{bmatrix}\delta_A\\ \delta_B\end{bmatrix}\right)\end{aligned} \tag{34.77}$$

Therefore, γ_1, γ_2, γ_3 are:

$$\begin{aligned}\gamma_1 &= \begin{cases}0 \rightarrow \text{when } r(t) < C_{0sn}\\ 1 \rightarrow \text{when } r(t) > C_{0sn}\end{cases}\\ \gamma_2 &= \begin{cases}0 \rightarrow \text{when } r(t) < C_{Asn}\\ 1 \rightarrow \text{when } r(t) > C_{Asn}\end{cases}\\ \gamma_3 &= \begin{cases}0 \rightarrow \text{when } r(t) < C_{Bsn}\\ 1 \rightarrow \text{when } r(t) > C_{Bsn}\end{cases}\end{aligned} \tag{34.78}$$

Supposing that the space vector $\vec{V}_s$ is now specified in the orthogonal coordinates $\alpha, \beta(\vec{V}_\alpha, \vec{V}_\beta)$, instead of magnitude V_s and angle Φ_s, the duty cycles δ_A, δ_B can be easily calculated knowing that $v_\alpha = V_s\cos\Phi$, $v_\beta = V_s\sin\Phi$ and using Eq. (34.74):

$$\begin{aligned}\delta_A &= \frac{\sqrt{2}}{2V_a}\left(\sqrt{3}v_\alpha - v_\beta\right)\\ \delta_B &= \frac{\sqrt{2}}{V_a}v_\beta\end{aligned} \tag{34.79}$$

This equation enables the use of Eqs. (34.77) and (34.78) to obtain SVM in orthogonal coordinates.

Using SVM or SWPWM, the closed-loop control of the inverter output currents (induction motor stator currents) can be performed using an approach similar to that outlined in Example 34.6 and decoupling the currents expressed in a d, q rotating frame.

34.3 Sliding-mode Control of Switching Converters

34.3.1 Introduction

All the designed controllers for switching power converters are in fact variable structure controllers, in the sense that the control action changes rapidly from one to another of, usually, two possible $\delta(t)$ values, cyclically changing the converter topology. This is accomplished by the modulator (Fig. 34.6),

which creates the switching variable $\delta(t)$ imposing $\delta(t) = 1$ or $\delta(t) = 0$, to turn on or off the power semiconductors. As a consequence of this discontinuous control action, indispensable for efficiency reasons, state trajectories move back and forth around a certain average surface in the state-space, and variables present some ripple. To avoid the effects of this ripple in the modeling and to apply linear control methodologies to time-variant systems, average values of state variables and state-space averaged models or circuits were presented (Section 34.2). However, a nonlinear approach to the modeling and control problem, taking advantage of the inherent ripple and variable structure behavior of switching converters, instead of just trying to live with them, would be desirable, especially if enhanced performances could be attained.

In this approach switching converters topologies, as discrete nonlinear time-variant systems, are controlled to switch from one dynamics to another when just needed. If this switching occurs at a very high frequency (theoretically infinite), the state dynamics, described as in Eq. (34.4), can be enforced to slide along a certain prescribed state-space trajectory. The converter is said to be in sliding mode, the allowed deviations from the trajectory (the ripple) imposing the practical switching frequency.

Sliding mode control of variable structure systems, such as switching converters, is particularly interesting because of the inherent robustness [11, 12], capability of system order reduction, and appropriateness to the on/off switching of power semiconductors. The control action, being the control equivalent of the management paradigm "Just in Time" (JIT), provides timely and precise control actions, determined by the control law and the allowed ripple. Therefore, the switching frequency is not constant over all operating regions of the converter.

This section treats the derivation of the control (sliding surface) and switching laws, robustness, stability, constant-frequency operation, and steady-state error elimination necessary for sliding-mode control of switching converters, also giving some examples.

34.3.2 Principles of Sliding-mode Control

Consider the state-space switched model Eq. (34.4) of a switching converter subsystem, and input–output linearization or another technique, to obtain, from state-space equations, one Eq. (34.80), for each controllable subsystem output $\mathbf{y} = \mathbf{x}$. In the controllability canonical form [13] (also known as input–output decoupled or companion form), Eq. (34.80) is:

$$\frac{d}{dt}[x_h, \ldots, x_{j-1}, x_j]^T = [x_{h+1}, \ldots, x_j, -f_h(\mathbf{x}) - p_h(t) + b_h(\mathbf{x})u_h(t)]^T \tag{34.80}$$

where $\mathbf{x} = [x_h, \ldots, x_{j-1}, x_j]^T$ is the subsystem state vector, $f_h(\mathbf{x})$ and $b_h(\mathbf{x})$ are functions of $\mathbf{x}$, $p_h(t)$ represents the external disturbances, and $u_h(t)$ is the control input. In this special form of state-space modeling, the state variables are chosen so that the x_{i+1} variable ($i \in \{h, \ldots, j-1\}$) is the time derivative of x_i, that is $\mathbf{x} = \left[x_h, \dot{x}_h, \ddot{x}_h, \ldots, \overset{m}{x_h}\right]^T$, where $m = j - h$ [14].

34.3.2.1 Control Law (Sliding Surface)

The required closed-loop dynamics for the subsystem output vector $\mathbf{y} = \mathbf{x}$ can be chosen to verify Eq. (34.81) with selected k_i values. This is a model reference adaptive control approach to impose a state trajectory that advantageously reduces the system order $(j - h + 1)$.

$$\frac{dx_j}{dt} = -\sum_{i=h}^{j-1} \frac{k_i}{k_j} x_{i+1} \tag{34.81}$$

Effectively, in a single-input single-output (SISO) subsystem the order is reduced by unity, applying the restriction Eq. (34.81). In a multiple-input multiple-output (MIMO) system, in which ν independent restrictions could be imposed (usually with ν degrees of freedom), the order could often be reduced in ν units. Indeed, from Eq. (34.81), the dynamics of the jth term of $\mathbf{x}$ is linearly dependent from the $j - h$ first terms:

$$\frac{dx_j}{dt} = -\sum_{i=h}^{j-1} \frac{k_i}{k_j} x_{i+1} = -\sum_{i=h}^{j-1} \frac{k_i}{k_j} \frac{dx_i}{dt} \tag{34.82}$$

The controllability canonical model allows the direct calculation of the needed control input to achieve the desired dynamics Eq. (34.81). In fact, as the control action should enforce the state vector $\mathbf{x}$, to follow the reference vector $\mathbf{x}_r = \left[x_{h_r}, \dot{x}_{h_r}, \ddot{x}_{h_r}, \ldots, \overset{m}{x}_{h_r}\right]^T$, the tracking error vector will be $\mathbf{e} = [x_{h_r} - x_h, \ldots, x_{j-1r} - x_{j-1}, x_{jr} - x_j]^T$ or $\mathbf{e} = [e_{x_h}, \ldots, e_{xj-1}, e_{x_j}]^T$. Thus, equating the sub-expressions for $\mathrm{d}x_j/\mathrm{d}t$ of Eqs. (34.80) and (34.81), the necessary control input $u_h(t)$ is

$$u_h(t) = \frac{p_h(t) + f_h(x) + \frac{dx_j}{dt}}{b_h(x)} = \frac{p_h(t) + f_h(x) - \sum_{i=h}^{j-1} \frac{k_i}{k_j} x_{i+1_r} + \sum_{i=h}^{j-1} \frac{k_i}{k_j} e_{x_{i+1}}}{b_h(x)} \tag{34.83}$$

This expression is the required closed-loop control law, but unfortunately it depends on the system parameters, on external perturbations and is difficult to compute. Moreover, for some

output requirements, Eq. (34.83) would give extremely high values for the control input $u_h(t)$, which would be impractical or almost impossible.

In most switching converters $u_h(t)$ is discontinuous. Yet, if we assume one or more discontinuity borders dividing the state-space into subspaces, the existence and uniqueness of the solution is guaranteed out of the discontinuity borders, since in each subspace the input is continuous. The discontinuity borders are subspace switching hypersurfaces, whose order is the space order minus one, along which the subsystem state slides, since its intersections with the auxiliary equations defining the discontinuity surfaces can give the needed control input.

Within the sliding-mode control (SMC) theory, assuming a certain dynamic error tending to zero, one auxiliary equation (sliding surface) and the equivalent control input $u_h(t)$ can be obtained, integrating both sides of Eq. (34.82) with null initial conditions:

$$k_j x_j \sum_{i=h}^{j-1} k_i x_i = \sum_{i=h}^{j} k_i x_i = 0 \tag{34.84}$$

This equation represents the discontinuity surface (hyperplane) and just defines the necessary sliding surface $S(x_i, t)$ to obtain the prescribed dynamics of Eq. (34.81):

$$S(x_i, t) = \sum_{i=h}^{j} k_i x_i = 0 \tag{34.85}$$

In fact, by taking the first time derivative of $S(x_i, t)$, $\dot{S}(x_i, t) = 0$, solving it for $\mathrm{d}x_j/\mathrm{d}t$, and substituting the result in Eq. (34.83), the dynamics specified by Eq. (34.81) is obtained. This means that the control problem is reduced to a first-order problem, since it is only necessary to calculate the time derivative of Eq. (34.85) to obtain the dynamics (34.81) and the needed control input $u_h(t)$.

The sliding surface Eq. (34.85), as the dynamics of the converter subsystem, must be a Routh–Hurwitz polynomial and verify the sliding manifold invariance conditions, $S(x_i, t) = 0$ and $\dot{S}(x_i, t) = 0$. Consequently, the closed-loop controlled system behaves as a stable system of order $j - h$, whose dynamics is imposed by the coefficients k_i, which can be chosen by pole placement of the poles of the order $m = j - h$ polynomial. Alternatively, certain kinds of polynomials can be advantageously used [15]: Butterworth, Bessel, Chebyshev, elliptic (or Cauer), binomial, and minimum integral of time absolute error product (ITAE). Most useful are Bessel polynomials $B_E(s)$ Eq. (34.88), which minimize the system response time t_r, providing no overshoot, the polynomials $I_{TAE}(s)$ Eq. (34.87), that minimize the ITAE criterion for a system with desired natural oscillating frequency ω_o, and binomial polynomials $B_I(s)$ Eq. (34.86). For $m > 1$, ITAE polynomials give faster responses than binomial polynomials.

$$B_I(s)_m = (s+\omega_o)^m$$

$$= \begin{cases} m=0 \Rightarrow B_I(s)=1 \\ m=1 \Rightarrow B_I(s)=s+\omega_o \\ m=2 \Rightarrow B_I(s)=s^2+2\omega_o s+\omega_o^2 \\ m=3 \Rightarrow B_I(s)=s^3+3\omega_o s^2+3\omega_o^2 s+\omega_o^3 \\ m=4 \Rightarrow B_I(s)=s^4+4\omega_o s^3+6\omega_o^2 s^2+4\omega_o^3 s+\omega_o^4 \\ \ldots \end{cases} \tag{34.86}$$

$$I_{TAE}(s)_m = \begin{cases} m=0 \Rightarrow I_{TAE}(s)=1 \\ m=1 \Rightarrow I_{TAE}(s)=s+\omega_o \\ m=2 \Rightarrow I_{TAE}(s)=s^2+1.4\omega_o s+\omega_o^2 \\ m=3 \Rightarrow I_{TAE}(s)=s^3+1.75\omega_o s^2+2.15\omega_o^2 s+\omega_o^3 \\ m=4 \Rightarrow I_{TAE}(s)=s^4+2.1\omega_o s^3+3.4\omega_o^2 s^2 \\ \qquad\qquad +2.7\omega_o^3 s+\omega_o^4 \\ \ldots \end{cases} \tag{34.87}$$

$$B_E(s)_m = \begin{cases} m=0 \Rightarrow B_E(s)=1 \\ m=1 \Rightarrow B_E(s)=st_r+1 \\ m=2 \Rightarrow B_E(s)=\frac{(st_r)^2+3st_r+3}{3} \\ m=3 \Rightarrow B_E(s)=\frac{\left((st_r)^2+3.678st_r+6.459\right)(st_r+2.322)}{15} \\ \qquad\qquad =\frac{(st_r)^3+6(st_r)^2+15st_r+15}{15} \\ m=4 \Rightarrow B_E(s)=\frac{(st_r)^4+10(st_r)^3+45(st_r)^2+105(st_r)+105}{105} \\ \ldots \end{cases} \tag{34.88}$$

These polynomials can be the reference model for this model reference adaptive control method.

34.3.2.2 Closed-loop Control Input–Output Decoupled Form

For closed-loop control applications, instead of the state variables x_i, it is worthy to consider, as new state variables, the errors e_{x_i}, components of the error vector $\mathbf{e} = \left[e_{x_h}, \dot{e}_{x_h}, \ddot{e}_{x_h}, \ldots, \overset{m}{e}_{x_h}\right]^T$ of the state-space variables x_i, relative to a given reference x_{i_r} Eq. (34.90). The new controllability canonical model of the system is

$$\frac{d}{dt}[e_{x_h}, \ldots, e_{x_{j-1}}, e_{x_j}]^T = [e_{x_{h+1}}, \ldots, e_{x_j}, -f_e(\mathbf{e}) + p_e(t) - b_e(\mathbf{e})u_h(t)]^T \tag{34.89}$$

where $f_e(\mathbf{e})$, $p_e(t)$, and $b_e(\mathbf{e})$ are functions of the error vector $\mathbf{e}$.

As the transformation of variables

$$e_{x_i} = x_{i_r} - x_i \quad \text{with} \quad i = h, \ldots, j \tag{34.90}$$

is linear, the Routh–Hurwitz polynomial for the new sliding surface $S(e_{x_i}, t)$ is

$$S(e_{x_i}, t) = \sum_{i=h}^{j} k_i e_{x_i} = 0 \tag{34.91}$$

Since $e_{x_{i+1}}(s) = s e_{x_i}(s)$, this *control law*, from Eqs. (34.86–34.88) can be written as $S(\mathbf{e},s) = e_{x_i}(s+\omega_o)^m$, does not depend on circuit parameters, disturbances, or operating conditions, but only on the imposed k_i parameters and on the state variable errors e_{x_i}, which can usually be measured or estimated. The control law Eq. (34.91) enables the desired dynamics of the output variable(s), if the semiconductor switching strategy is designed to guarantee the system stability. In practice, the finite switching frequency of the semiconductors will impose a certain dynamic error ε tending to zero. The control law Eq. (34.91) is the required controller for the closed-loop SISO subsystem with output **y**.

34.3.2.3 Stability

Existence condition. The existence of the operation in sliding mode implies $S(e_{x_i}, t) = 0$. Also, to stay in this regime, the control system should guarantee $\dot{S}(e_{x_i}, t) = 0$. Therefore, the semiconductor switching law must ensure the stability condition for the system in sliding mode, written as

$$S(e_{x_i}, t)\dot{S}(e_{x_i}, t) < 0 \tag{34.92}$$

The fulfillment of this inequality ensures the convergence of the system state trajectories to the sliding surface $S(e_{x_i}, t) = 0$, since

– if $S(e_{x_i}, t) > 0$ and $\dot{S}(e_{x_i}, t) < 0$, then $S(e_{x_i}, t)$ will decrease to zero,
– if $S(e_{x_i}, t) < 0$ and $\dot{S}(e_{x_i}, t) > 0$, then $S(e_{x_i}, t)$ will increase toward zero.

Hence, if Eq. (34.92) is verified, then $S(e_{x_i}, t)$ will converge to zero. The condition (34.92) is the manifold $S(e_{x_i}, t)$ invariance condition, or the sliding-mode existence condition.

Given the statespace model Eq. (34.89) as a function of the error vector **e** and, from $\dot{S}(e_{x_i}, t) = 0$, the equivalent average control input $U_{eq}(t)$ that must be applied to the system in order that the system state slides along the surface Eq. (34.91), is given by

$$U_{eq}(t) = \frac{k_h \frac{de_{x_h}}{dt} + k_{h+1} \frac{de_{x_{h+1}}}{dt} + \cdots + k_{j-1} + \frac{de_{x_{j-1}}}{dt} + k_j\left(-f_e(\mathbf{e}) + p_e(t)\right)}{k_j b_e(\mathbf{e})} \tag{34.93}$$

This control input $U_{eq}(t)$ ensures the converter subsystem operation in the sliding mode.

Reaching condition. The fulfillment of $S(e_{x_i}, t)\dot{S}(e_{x_i}, t) < 0$, as $S(e_{x_i}, t)\dot{S}(e_{x_i}, t) = (1/2)\dot{S}^2(e_{x_i}, t)$, implies that the distance between the system state and the sliding surface will tend to zero, since $S^2(e_{x_i}, t)$ can be considered as a measure for this distance. This means that the system will reach sliding mode. Additionally, from Eq. (34.89) it can be written:

$$\frac{de_{x_j}}{dt} = -f_e(\mathbf{e}) + p_e(t) - b_e(\mathbf{e})u_h(t) \tag{34.94}$$

From Eq. (34.91), Eq. (34.95) is obtained.

$$S(e_{x_i}, t) = \sum_{i=h}^{j} k_i e_{x_i} = k_h e_{x_h} + k_{h+1}\frac{de_{x_h}}{dt} + k_{h+2}\frac{d^2 e_{x_h}}{dt^2} + \cdots + k_j \frac{d^m e_{x_h}}{dt^m} \tag{34.95}$$

If $S(e_{x_i}, t) > 0$, from the Routh–Hurwitz property of Eq. (34.91), then $e_{x_j} > 0$. In this case, to reach $S(e_{x_i}, t) = 0$ it is necessary to impose $-b_e(\mathbf{e})u_h(t) = -U$ in Eq. (34.94), with U chosen to guarantee $\mathrm{d}e_{x_j}/\mathrm{d}t < 0$. After a certain time, e_{x_j} will be $e_{x_j} = \mathrm{d}^m e_{x_h}/\mathrm{d}t^m < 0$, implying along with Eq. (34.95) that $\dot{S}(e_{x_i}, t) < 0$, thus verifying Eq. (34.92). Therefore, every term of $S(e_{x_i}, t)$ will be negative, which implies, after a certain time, an error $e_{x_h} < 0$ and $S(e_{x_i}, t) < 0$. Hence, the system will reach sliding mode, staying there if $U = U_{eq}(t)$. This same reasoning can be made for $S(e_{x_i}, t) < 0$, it is now being necessary to impose $-b_e(\mathbf{e})u_h(t) = +U$, with U high enough to guarantee $\mathrm{d}e_{x_j}/\mathrm{d}t > 0$.

To ensure that the system always reaches sliding-mode operation, it is necessary to calculate the maximum value of $U_{eq}(t)$, U_{eqmax}, and also impose the reaching condition:

$$U > U_{eqmax} \tag{34.96}$$

This means that the power supply voltage values U should be chosen high enough to additionally account for the maximum effects of the perturbations. With step inputs, even with $U > U_{eqmax}$, the converter usually loses sliding mode, but it will reach it again, even if the U_{eqmax} is calculated considering only the maximum steady-state values for the perturbations.

34.3.2.4 Switching Law

From the foregoing considerations, supposing a system with two possible structures, the semiconductor switching strategy must ensure $S(e_{x_i}, t)\dot{S}(e_{x_i}, t) < 0$. Therefore, if $S(e_{x_i}, t) > 0$, then $\dot{S}(e_{x_i}, t) < 0$, which implies, as seen, $-b_e(\mathbf{e})u_h(t) = -U$ (the sign of $b_e(\mathbf{e})$ must be known). Also, if $S(e_{x_i}, t) < 0$, then $\dot{S}(e_{x_i}, t) > 0$, which implies $-b_e(\mathbf{e})u_h(t) = +U$. This imposes the switching between two structures at infinite frequency. Since power semiconductors can switch only at finite frequency, in practice, a small enough error for $S(e_{x_i}, t)$ must

be allowed ($-\varepsilon < S(e_{x_i}, t) < +\varepsilon$). Hence, the switching law between the two possible system structures might be

$$u_h(t) = \begin{cases} U/be\,(\mathbf{e}) \text{ for } S(e_{x_i}, t) > +e \\ -U/be\,(\mathbf{e}) \text{ for } S(e_{x_i}, t) < -e \end{cases} \tag{34.97}$$

The condition Eq. (34.97) determines the control input to be applied and therefore represents the semiconductor switching strategy or switching function. This law determines a two-level pulse width modulator with JIT switching (variable frequency).

34.3.2.5 Robustness

The dynamics of a system, with closed-loop control using the control law Eq. (34.91) and the switching law Eq. (34.97), does not depend on the system operating point, load, circuit parameters, power supply, or bounded disturbances, as long as the control input $u_h(t)$ is large enough to maintain the converter subsystem in sliding mode. Therefore, it is said that the switching converter dynamics, operating in sliding mode, is robust against changing operating conditions, variations of circuit parameters, and external disturbances. The desired dynamics for the output variable(s) is determined only by the k_i coefficients of the control law Eq. (34.91), as long as the switching law (34.97) maintains the converter in sliding mode.

34.3.3 Constant-frequency Operation

Prefixed switching frequency can be achieved, even with the sliding-mode controllers, at the cost of losing the JIT action. As the sliding-mode controller changes the control input when needed, and not at a certain prefixed rhythm, applications needing constant switching frequency (such as thyristor rectifiers or resonant converters), must compare $S(e_{x_i}, t)$ (hysteresis width 2ι much narrower than 2ε) with auxiliary triangular waveforms (Fig. 34.25a), auxiliary sawtooth functions (Fig. 34.25b), three-level clocks (Fig. 34.25c), or phase locked loop control of the comparator hysteresis variable width 2ε[16]. However, as illustrated in Fig. 34.25d, steady-state errors do appear. Often, they should be eliminated as described in Section 34.3.4.

34.3.4 Steady-state Error Elimination in Converters with Continuous Control Inputs

In the ideal sliding mode, state trajectories are directed toward the sliding surface (34.91) and move exactly along the discontinuity surface, switching between the possible system structures, at infinite frequency. Practical sliding modes cannot switch at infinite frequency, and therefore exhibit phase plane trajectory oscillations inside a hysteresis band of width 2ε, centered in the discontinuity surface.

The switching law Eq. (34.91) permits no steady-state errors as long as $S(e_{x_i}, t)$ tends to zero, which implies no restrictions on the commutation frequency. Control circuits operating at constant frequency, or needed continuous inputs, or particular limitations of the power semiconductors, such as minimum on or off times, can originate $S(e_{x_i}, t) = \varepsilon_1 \neq 0$. The steady-state error (e_{x_h}) of the x_h variable, $x_{h_r} - x_h = \varepsilon_1/k_h$, can be eliminated, increasing the system order by 1. The new state-space controllability canonical form, considering the error e_{x_i}, between the variables and their references, as the state vector, is

$$\frac{d}{dt}\left[\int e_{x_h}dt, e_{x_h}, \ldots, e_{x_{j-1}}, e_{x_j}\right]^T = [e_{x_h}, e_{x_{h+1}}, \ldots, e_{x_j}, -f_e(\mathbf{e}) - p_e(t) - b_e(\mathbf{e})u_h(t)]^T \tag{34.98}$$

The new sliding surface $S(e_{x_i}, t)$, written from Eq. (34.91) considering the new system Eq. (34.98), is

$$S(e_{x_i}, t) = k_0 \int e_{x_h}dt + \sum_{i=h}^{j} k_i e_{x_i} = 0 \tag{34.99}$$

This sliding surface offers zero-state error, even if $S(e_{x_i}, t) = \varepsilon_1$ due to the hardware errors or fixed (or limited)

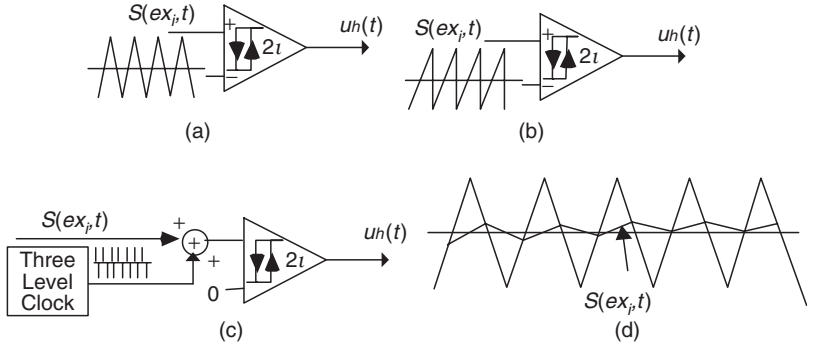


FIGURE 34.25 Auxiliary functions and methods to obtain constant switching frequency with sliding-mode controllers.

frequency switching. Indeed, at the steady state, the only nonnull term is $k_0 \int e_{x_h} dt = \varepsilon_1$. Also, like Eq. (34.91), this closed-loop control law does not depend on system parameters or perturbations to ensure a prescribed closed-loop dynamics similar to Eq. (34.81) with an error approaching zero.

The approach outlined herein precisely defines the control law (sliding surface (34.91) or (34.99)) needed to obtain the selected dynamics, and the switching law Eq. (34.97). As the control law allows the implementation of the system controller, and the switching law gives the PWM modulator, there is no need to design linear or nonlinear controllers, based on linear converter models, or devise offline PWM modulators. Therefore, sliding-mode control theory, applied to switching converters, provides a systematic method to generate both the controller(s) (usually nonlinear) and the modulator(s) that will ensure a model reference robust dynamics, solving the control problem of switching converters.

In the next examples, it is shown that the sliding-mode controllers use (nonlinear) state feedback, therefore, needing to measure the state variables and often other variables, since they use more system information. This is a disadvantage since more sensors are needed. However, the straightforward control design and obtained performances are much better than those obtained with the averaged models, the use of more sensors being really valued. Alternatively to the extra sensors, state observers can be used [13, 14].

34.3.5 Examples: Buck–Boost DC/DC Converter, Half-bridge Inverter, 12-pulse Parallel Rectifiers, Audio Power Amplifiers, Near Unity Power Factor Rectifiers, Multilevel Inverters, Matrix Converters

EXAMPLE 34.10 Sliding-mode control of the buck–boost dc/dc converter

Consider again the buck–boost converter of Fig. 34.1 and assume the converter output voltage v_o to be the controlled output. From Section 34.2, using the switched state-space model of Eq. (34.11), making $\mathrm{d}v_o/\mathrm{d}t = \theta$, and calculating the first time derivative of θ, the controllability canonical model (34.100), where $i_o = v_o/R_o$, is obtained:

$$\begin{aligned}\frac{\mathrm{d}v_o}{\mathrm{d}t} &= \theta = \frac{1-\delta(t)}{C_o} i_L - \frac{i_o}{C_o}\\ \frac{\mathrm{d}\theta}{\mathrm{d}t} &= -\frac{(1-\delta(t))^2}{L_i C_o} v_o - \frac{C_o\theta + i_o}{C_o(1-\delta(t))}\frac{\mathrm{d}\delta(t)}{\mathrm{d}t}\\ &\quad - \frac{1}{C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t} + \frac{\delta(t)(1-\delta(t))}{C_o L_i} V_{DC}\end{aligned} \tag{34.100}$$

This model, written in the form of Eq. (34.80), contains two state variables, v_o and θ. Therefore, from Eq. (34.91) and considering $e_{v_o} = v_{o_r} - v_o$, $e_\theta = \theta_r - \theta$, the control law (sliding surface) is

$$\begin{aligned}S(e_{x_i}, t) &= \sum_{i=h}^{2} k_i e_{x_i} = k_1(v_{o_r} - v_o) + k_2\frac{dv_{o_r}}{dt} - k_2\frac{dv_o}{dt}\\ &= k_1(v_{o_r} - v_o) + k_2\frac{dv_{o_r}}{dt} - \frac{k_2}{C_o}(1-\delta(t))i_L\\ &\quad + \frac{k_2}{C_o} i_o = 0\end{aligned} \tag{34.101}$$

This sliding surface depends on the variable $\delta(t)$, which should be precisely the result of the application, in Eq. (34.101), of a switching law similar to Eq. (34.97). Assuming an ideal up–down converter and slow variations, from Eq. (34.31) the variable $\delta(t)$ can be averaged to $\delta_1 = v_o/(v_o + V_{DC})$. Substituting this relation in Eq. (34.101), and rearranging, Eq. (34.102) is derived:

$$\begin{aligned}S(e_{x_i}, t) = \frac{C_o k_1}{k_2}\left(\frac{v_o + V_{DC}}{v_o}\right)\\ \times\left((v_{o_r} - v_o) + \frac{k_2}{k_1}\frac{dv_{o_r}}{dt} + \frac{k_2}{k_1}\frac{1}{C_o} i_o\right) - i_L = 0\end{aligned} \tag{34.102}$$

This control law shows that the power supply voltage V_{DC} must be measured, as well as the output voltage v_o and the currents i_o and i_L.

To obtain the switching law from stability considerations (34.92), the time derivative of $S(e_{x_i}, t)$, supposing $(v_o + V_{DC})/v_o$ almost constant, is

$$\begin{aligned}\dot{S}(e_{x_i}, t) = \frac{C_o k_1}{k_2}\left(\frac{v_o + V_{DC}}{v_o}\right)\\ \times\left(\frac{\mathrm{d}e_{v_o}}{\mathrm{d}t} + \frac{k_2}{k_1}\frac{\mathrm{d}^2 v_{o_r}}{\mathrm{d}t^2} + \frac{k_2}{k_1 C_o}\frac{\mathrm{d}i_o}{\mathrm{d}t}\right) - \frac{\mathrm{d}i_L}{\mathrm{d}t}\end{aligned} \tag{34.103}$$

If $S(e_{x_i}, t) > 0$ then, from Eq. (34.92), $\dot{S}(e_{x_i}, t) < 0$ must hold. Analyzing Eq. (34.103), we can conclude that, if $S(e_{x_i}, t) > 0$, $\dot{S}(e_{x_i}, t)$ is negative if, and only if, $\mathrm{d}i_L/\mathrm{d}t > 0$. Therefore, for positive errors $e_{v_o} > 0$ the current i_L must be increased, which implies $\delta(t) = 1$. Similarly, for $S(e_{x_i}, t) < 0$, $\mathrm{d}i_L/\mathrm{d}t < 0$ and $\delta(t) = 0$. Thus, a switching law similar to Eq. (34.97) is obtained:

$$\delta(t) = \begin{cases} 1 & \text{for } S(e_{x_i}, t) > +e \\ 0 & \text{for } S(e_{x_i}, t) < -e \end{cases} \tag{34.104}$$

The same switching law could be obtained from knowing the dynamic behavior of this nonminimum-phase up-down converter: to increase (decrease) the

output voltage, a previous increase (decrease) of the i_L current is mandatory.

Equation (34.101) shows that, if the buck–boost converter is into the sliding mode ($S(e_{x_i}, t) = 0$), the dynamics of the output voltage error tends exponentially to zero with time constant k_2/k_1. Since during step transients, the converter is in the reaching mode, the time constant k_2/k_1 cannot be designed to originate error variations larger than the one allowed by the self-dynamics of the converter excited by a certain maximum permissible i_L current. Given the polynomials (34.86–34.88) with $m = 1$, $k_1/k_2 = \omega_o$ should be much lower than the finite switching frequency ($1/T$) of the converter. Therefore, the time constant must obey $k_2/k_1 \gg T$. Then, knowing that k_2 and k_1 are both imposed, the control designer can tailor the time constant as needed, provided that the above restrictions are observed.

Short-circuit-proof operation for the sliding-mode controlled buck–boost converter can be derived from Eq. (34.102), noting that all the terms to the left of i_L represent the set point for this current. Therefore, limiting these terms (Fig. 34.26, saturation block, with $i_{Lmax} = 40\,\text{A}$), the switching law (34.104) ensures that the output current will not rise above the maximum imposed limit. Given the converter nonminimum-phase behavior, this i_L current limit is fundamental

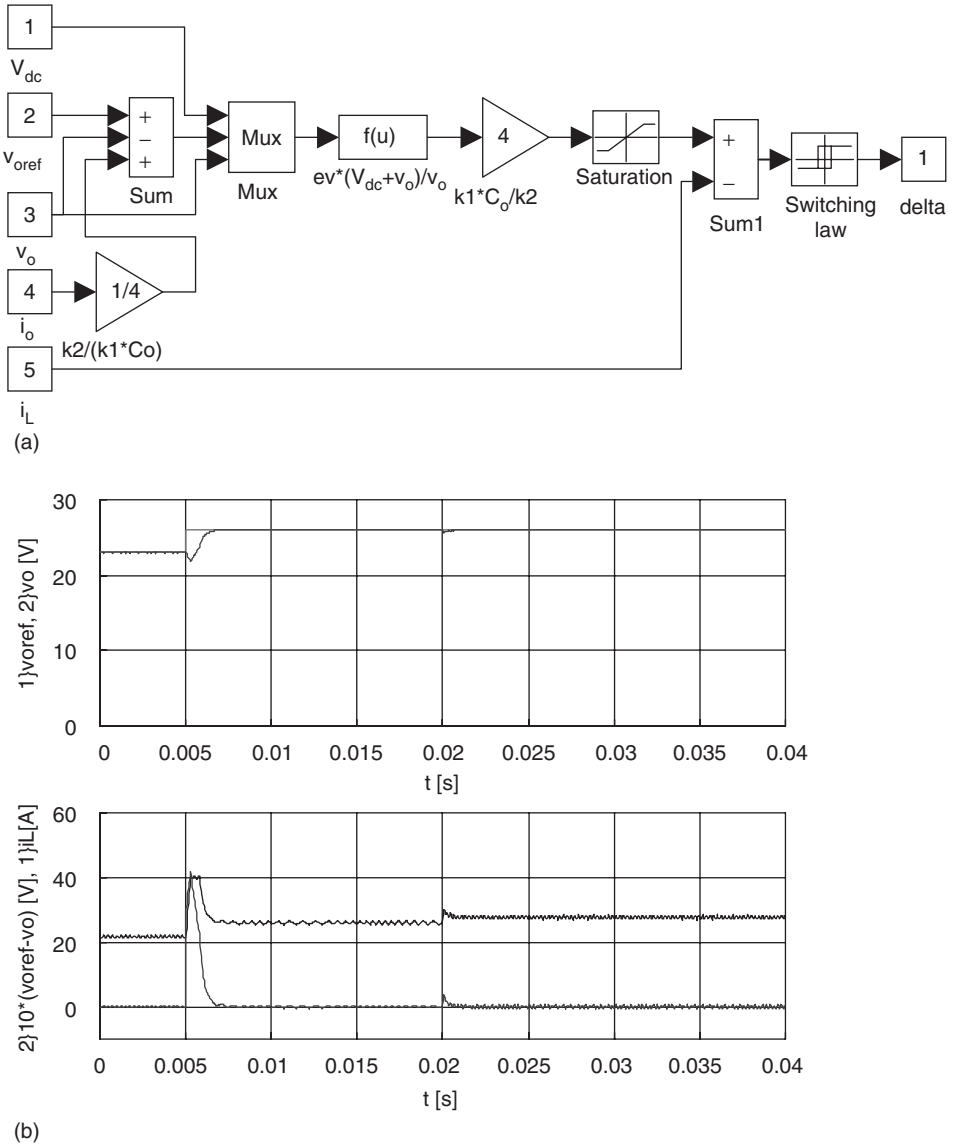


FIGURE 34.26 (a) Block diagram of the sliding-mode nonlinear controller for the buck–boost converter and (b) transient responses of the sliding-mode controlled buck–boost converter. At $t = 0.005\,\text{s}$, v_{oref} step from 23 to 26 V. At $t = 0.02\,\text{s}$, V_{DC} step from 26 to 23 V. Top graph: step reference v_{oref} and output voltage v_o. Bottom graph: trace starting at 20 is i_L current; trace starting at zero is $10\times(v_{oref} - v_o)$.

to reach the sliding mode of operation with step disturbances.

The block diagram (Fig. 34.26a) of the implemented control law Eq. (34.102) (with $C_o k_1/k_2 = 4$) and switching law (34.103) (with $\varepsilon = 0.3$) does not included the time derivative of the reference ($\mathrm{d}v_{o_r}/\mathrm{d}t$) since, in a dc/dc converter its value is considered zero. The controller hardware (or software), derived using just the sliding-mode approach, operates only in a closed-loop.

The resulting performance (Fig. 34.26b) is much better than that obtained with the PID notch filter (compare to Example 34.4, Fig. 34.9b), with a higher response speed and robustness against power-supply variations.

EXAMPLE 34.11 Sliding mode control of the single-phase half-bridge converter

Consider the half-bridge four quadrant converter of Fig. 34.27 with the output filter and the inductive load ($V_{DCmax} = 300\,\mathrm{V}$; $V_{DCmin} = 230\,\mathrm{V}$; $R_i = 0.1\,\Omega$; $L_o = 4\,\mathrm{mH}$; $C_o = 470\,\mu\mathrm{F}$; inductive load with nominal values $R_o = 7\,\Omega$, $L_o = 1\,\mathrm{mH}$).

Assuming that power switches, output filter capacitor, and power supply are all ideal, and a generic load with allowed slow variations, the switched state-space model of the converter, with state variables v_o and i_L, is

$$\frac{d}{dt}\begin{bmatrix} v_o \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & 1/C_o \\ -1/L_o & -R_i/L_o \end{bmatrix}\begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} -1/C_o & 0 \\ 0 & 1/L_o \end{bmatrix}\begin{bmatrix} i_o \\ \delta(t)V_{DC} \end{bmatrix} \tag{34.105}$$

where i_o is the generic load current and $v_{PWM} = \delta(t)V_{DC}$ is the extended PWM output voltage ($\delta(t) = +1$ when one of the upper main semiconductors of Fig. 34.27 is conducting and $\delta(t) = -1$ when one of the lower semiconductors is on).

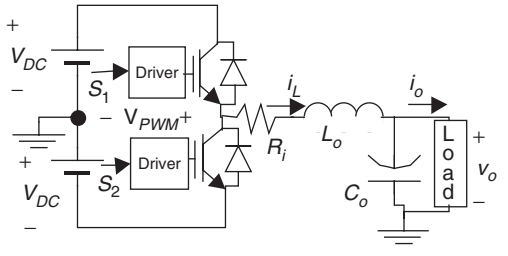


FIGURE 34.27 Half-bridge power inverter with insulated gate bipolar transistors, output filter, and load.

34.3.5.1 Output Current Control (Current-mode Control)

To perform as a v_{i_L} voltage controlled i_L current source (or sink) with transconductance g_m ($g_m = i_L/v_{i_L}$), this converter must supply a current i_L to the output inductor, obeying $i_L = g_m v_{i_L}$. Using a bounded v_{i_L} voltage to provide output short-circuit protection, the reference current for a sliding-mode controller must be $i_{L_r} = g_m v_{i_L}$. Therefore, the controlled output is the i_L current and the controllability canonical model (34.106) is obtained from the second equation of (34.105), since the dynamics of this subsystem, being governed by $\delta(t)V_{DC}$, is already in the controllability canonical form for this chosen output.

$$\frac{di_L}{dt} = -\frac{R_i}{L_o}i_L - \frac{1}{L_o}v_o + \frac{\delta(t)V_{DC}}{L_o} \tag{34.106}$$

A suitable sliding surface (34.107) is obtained from Eq. (34.91), making $e_{i_L} = i_{L_r} - i_L$.

$$S(e_{i_L}, t) = k_p e_{i_L} = k_p(i_{L_r} - i_L) = k_p(g_m v_{i_L} - i_L) = 0 \tag{34.107}$$

The switching law Eq. (34.108) can be devised calculating the time derivative of Eq. (34.107) $\dot{S}(e_{i_L}, t)$, and applying Eq. (34.92). If $S(e_{i_L}, t) > 0$, then $\mathrm{d}i_L/\mathrm{d}t > 0$ must hold to obtain $\dot{S}(e_{i_L}, t) < 0$, implying $\delta(t) = 1$.

$$\delta(t) = \begin{cases} 1 & \text{for } S(e_{i_L}, t) > +e \\ -1 & \text{for } S(e_{i_L}, t) < -e \end{cases} \tag{34.108}$$

The k_p value and the allowed the ripple ε define the instantaneous value of the variable switching frequency. The sliding-mode controller is represented in Fig. 34.28a. Step response (Fig. 34.29a) shows the variable-frequency operation, a very short rise time (limited only by the available power supply) and confirms the expected robustness against supply variations.

For systems where fixed-frequency operation is needed, a triangular wave, with frequency (10 kHz) slightly greater than the maximum variable frequency, can be added (Fig. 34.28b) to the sliding-mode controller, as explained in Section 34.3.3. Performances (Fig. 34.29b) are comparable to those of the variable-frequency sliding-mode controller (Fig. 34.29a). Fig. 34.29b shows the constant switching frequency, but also a steady-state error dependent on the operating point.

To eliminate this error, a new sliding surface Eq. (34.109), based on Eq. (34.99), should be used. The constants k_p and k_0 can be calculated, as discussed in Example 34.10.

$$S(e_{i_L}, t) = k_0 \int e_{i_L} dt + k_p e_{i_L} = 0 \tag{34.109}$$

The new constant-frequency sliding-mode current controller (Fig. 34.30a), with added antiwindup techniques (Example 34.6), since a saturation (errMax) is needed to keep the frequency constant, now presents no steady-state error (Fig. 34.30b). Performances are comparable to those of the

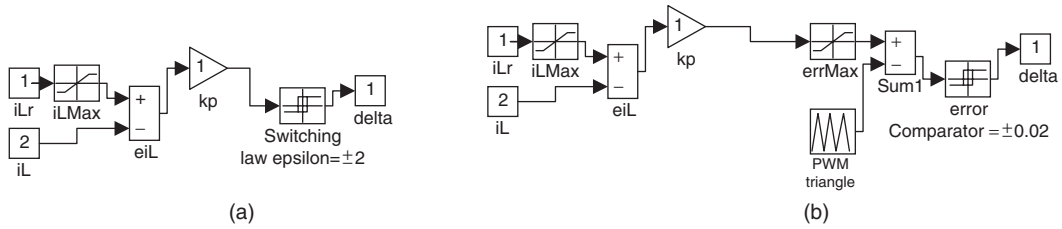


FIGURE 34.28 (a) Implementation of short-circuit-proof sliding-mode current controller (variable frequency) and (b) implementation of fixed frequency, short-circuit-proof sliding-mode current controller using a triangular waveform.

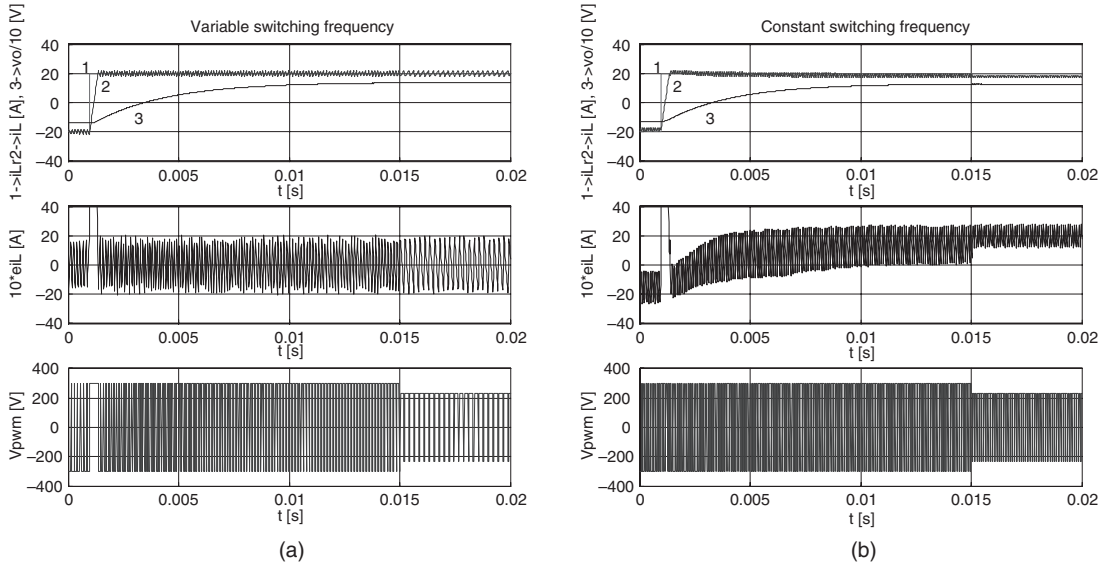


FIGURE 34.29 Performance of the transconductance amplifier; response to a i_{Lr} step from −20 to 20 A at $t = 0.001$ s and to a V_{DC} step from 300 to 230 V at $t = 0.015$ s: (a) variable-frequency sliding-mode controller and (b) fixed-frequency sliding-mide controller.

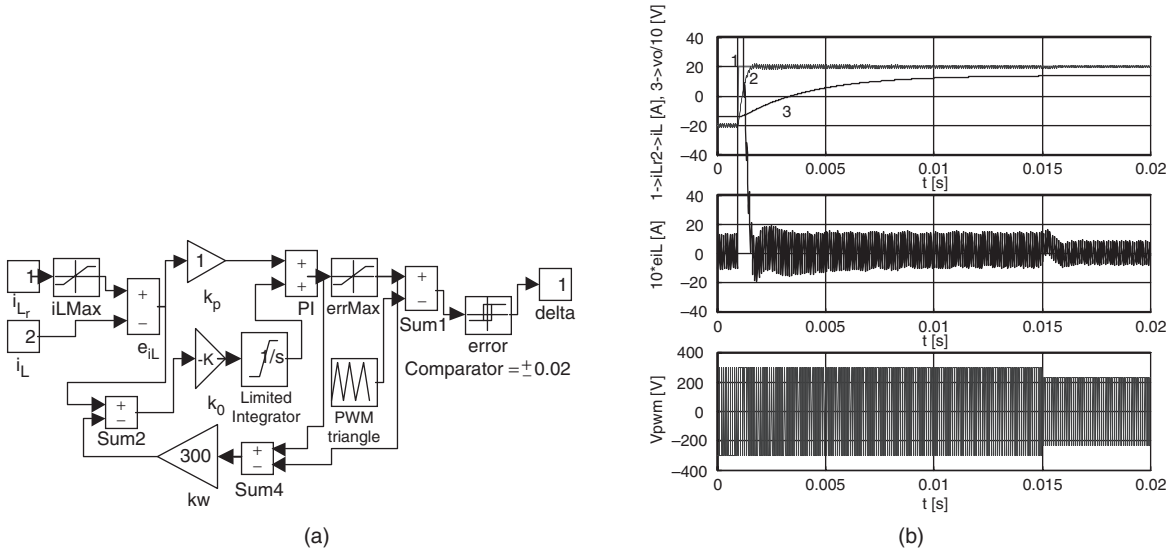


FIGURE 34.30 (a) Block diagram of the average current-mode controller (sliding mode) and (b) performance of the fixed-frequency sliding-mode controller with removed steady-state error: response to a i_{L_r} step from −20 to 20 A at $t = 0.001$ s and to a V_{DC} step from 300 to 230 V at $t = 0.015$ s.

variable-frequency controller, and no robustness loss is visible. The applied sliding-mode approach led to the derivation of the known average current-mode controller.

34.3.5.2 Output Voltage Control

To obtain a power operational amplifier suitable for building uninterruptible power supplies, power filters, power gyrators, inductance simulators, or power factor active compensators, v_o must be the controlled converter output. Therefore, using the input–output linearization technique, it is seen that the first time derivative of the output $(\mathrm{d}v_o/\mathrm{d}t) = (i_L - i_o)/C_o = \theta$, does not explicitly contain the control input $\delta(t)V_{DC}$. Then, the second derivative must be calculated. Taking into account Eq. (34.105), as $\theta = (i_L - i_o)/C_o$, Eq. (34.110) is derived.

$$\frac{d^2 v_o}{dt^2} = \frac{d}{dt}\theta = \frac{d}{dt}\left(\frac{i_L - i_o}{C_o}\right) = -\frac{R_i}{L_o}\theta - \frac{1}{L_o C_o}v_o - \frac{R_i}{L_o C_o}i_o - \frac{1}{C_o}\frac{di_o}{dt} + \frac{1}{L_o C_o}\delta(t)V_{DC} \tag{34.110}$$

This expression shows that the second derivative of the output depends on the control input $\delta(t)V_{DC}$. No further time derivative is needed, and the state-space equations of the equivalent circuit, written in the phase canonical form, are

$$\frac{d}{dt}\begin{bmatrix} v_o \\ \theta \end{bmatrix} = \begin{bmatrix} \theta \\ -\frac{R_i}{L_o}\theta - \frac{1}{L_o C_o}v_o - \frac{R_i}{L_o C_o}i_o - \frac{1}{C_o}\frac{di_o}{dt} + \frac{1}{L_o C_o}\delta(t)V_{DC} \end{bmatrix} \tag{34.111}$$

According to Eqs. (34.91), (34.111), and (34.105), considering that e_{v_o} is the feedback error $e_{v_o} = v_{o_r} - v_o$, a sliding surface $S(e_{v_o}, t)$, can be chosen:

$$S(e_{v_o}, t) = k_1 e_{v_o} + k_2 \frac{de_{v_o}}{dt} = e_{v_o} + \frac{k_2}{k_1}\frac{de_{v_o}}{dt} = e_{v_o} + \beta\frac{de_{v_o}}{dt} = \frac{C_o}{\beta}(v_{o_r} - v_o) + C_o\frac{dv_{o_r}}{dt} + i_o - i_L = 0 \tag{34.112}$$

where β is the time constant of the desired first-order response of output voltage ($\beta \gg T > 0$), as the strong relative degree [14] of this system is 2, and the sliding-mode operation reduces by one, the order of this system (the strong relative degree represents the number of times the output variable must be time differentiated until a control input explicitly appears).

Calculating $\dot{S}(e_{v_o}, t)$, the control strategy (switching law) Eq. (34.113) can be devised since, if $S(e_{v_o}, t) > 0$, then $\mathrm{d}i_L/\mathrm{d}t$ must be positive to obtain $\dot{S}(e_{i_L}, t) < 0$, implying $\delta(t) = 1$. Otherwise, $\delta(t) = -1$.

$$\delta(t) = \begin{cases} 1 & \text{for } S(e_{v_o}, t) > 0 (v_{PWM} = +V_{DC}) \\ -1 & \text{for } S(e_{v_o}, t) < 0 (v_{PWM} = -V_{DC}) \end{cases} \tag{34.113}$$

In the ideal sliding-mode dynamics, the filter input voltage v_{PWM} switches between V_{DC} and $-V_{DC}$ with the infinite frequency. This switching generates the equivalent control voltage V_{eq} that must satisfy the sliding manifold invariance conditions, $S(e_{v_o}, t) = 0$ and $\dot{S}(e_{v_o}, t) = 0$. Therefore, from $\dot{S}(e_{v_o}, t) = 0$, using Eqs. (34.112) and (34.105), (or from Eq. (34.110)), V_{eq} is

$$V_{eq} = L_o C_o \left[\frac{d^2 v_{o_r}}{dt^2} + \frac{1}{\beta}\frac{dv_{o_r}}{dt} + \frac{v_o}{L_o C_o} + \frac{(\beta R_i - L_o)i_L}{\beta L_o C_o}\frac{i_o}{\beta C_o} + \frac{1}{C_o}\frac{di_o}{dt}\right] \tag{34.114}$$

This equation shows that only smooth input v_{o_r} signals ("smooth" functions) can be accurately reproduced at the inverter output, as it contains derivatives of the v_{o_r} signal. This fact is a consequence of the stored electromagnetic energy. The existence of the sliding-mode operation implies the following necessary and sufficient condition:

$$-V_{DC} < V_{eq} < V_{DC} \tag{34.115}$$

Equation (34.115) enables the determination of the minimum input voltage V_{DC} needed to enforce the sliding-mode operation. Nevertheless, even in the case of $|V_{eq}| > |V_{DC}|$, the system experiences only a saturation transient and eventually reaches the region of sliding-mode operation, except if, in the steady state, operating point and disturbances enforce $|V_{eq}| > |V_{DC}|$.

In the ideal sliding mode, at infinite switching frequency, state trajectories are directed toward the sliding surface and move exactly along the discontinuity surface. Practical switching converters cannot switch at infinite frequency, so a typical implementation of Eq. (34.112) (Fig. 34.31a) with neglected $\dot{v}_{o_r}$ features a comparator with hysteresis 2ε, switching occurring at $|S(e_{v_o}, t)| > \varepsilon$ with frequency depending on the slopes of i_L. This hysteresis causes phase-plane trajectory oscillations of width 2ε around the discontinuity surface $S(e_{v_o}, t) = 0$, but the V_{eq} voltage is still correctly generated, since the resulting duty cycle is a continuous variable (except for error limitations in the hardware or software, which can be corrected using the approach pointed out by Eq. (34.98)).

The design of the compensator and the modulator is integrated with the same theoretical approach, since the signal $S(e_{v_o}, t)$ applied to a comparator generates the pulses for the power semiconductors drives. If the short-circuit-proof operation is built into the power semiconductor drives, there is the possibility to measure only the capacitor current $(i_L - i_o)$.

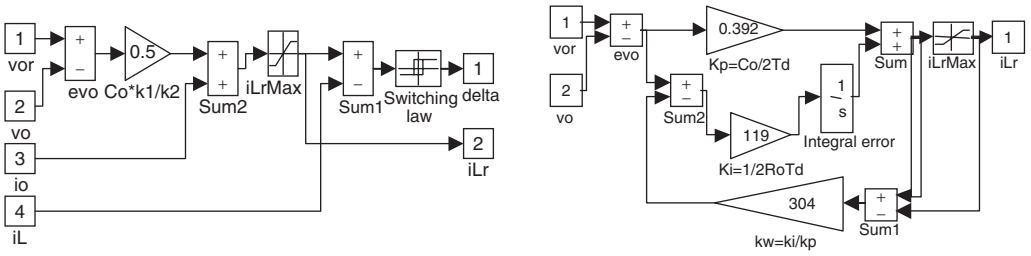


FIGURE 34.31 (a) Implementation of short-circuit-proof, sliding-mode output voltage controller (variable frequency) and (b) implementation of antiwindup PI current-mode (fixed frequency) controller.

34.3.5.3 Short-circuit Protection and Fixed-frequency Operation of the Power Operational Amplifier

If we note that all the terms to the left of i_L in Eq. (34.112) represent the value of i_{L_r}, a simple way to provide short-circuit protection is to bound the sum of all these terms (Fig. 34.31a with $i_{L_{rmax}} = 100\,\text{A}$). Alternatively, the output current controllers of Fig. 34.28 can be used, comparing Eq. (34.107) to Eq. (34.112), to obtain $i_{L_r} = S(e_{v_o}, t)/k_p + i_L$. Therefore, the block diagram of Fig. 34.31a provides the i_{L_r} output (for $k_p = 1$) to be the input of the current controllers (Fig. 34.28 and Fig. 34.31a). As seen, the controllers of Fig. 34.28b and Fig. 34.30a also ensure fixed-frequency operation.

For comparison purposes a proportional–integral (PI) controller, with antiwindup (Fig. 34.31b) for output voltage control, was designed, supposing the current-mode control of the half bridge ($i_{L_r} = g_m v_{i_L}/(1 + sT_d)$ considering a small delay T_d), a pure resistive load R_o, and using the approach outlined in Examples 34.6 and 34.8 ($k_v = 1$, $g_m = 1$, $\zeta^2 = 0.5$, $T_d = 600\,\mu\text{s}$). The obtained PI (34.50) parameters are

$$T_z = R_o C_o$$
$$T_p = 4\zeta^2 g_m k_v R_o T_d \tag{34.116}$$

Both variable frequency (Fig. 34.32) and constant frequency (Fig. 34.33) sliding-mode output voltage controllers present excellent performance and robustness with nominal loads. With loads much higher than the nominal value (Fig. 34.32b and Fig. 34.33b), the performance and robustness are also excellent. The sliding-mode constant-frequency PWM controller presents the additional advantage of injecting lower ripple in the load.

As expected, the PI regulator presents lower performance (Fig. 34.34). The response speed is lower and the insensitivity to power supply and load variations (Fig. 34.34b) is not as high as with the sliding mode. Nevertheless, the PI performances are acceptable, since its design was carried considering a slow

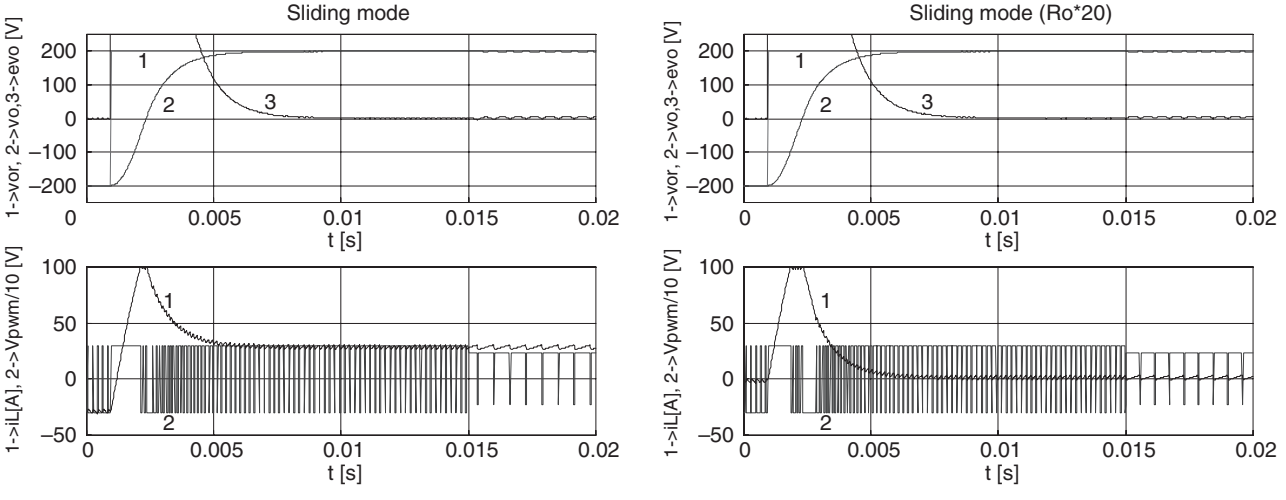


FIGURE 34.32 Performance of the power operational amplifier; response to a v_{o_r} step from −200 to 200 V at $t = 0.001$ s and to a V_{DC} step from 300 to 230 V at $t = 0.015$ s: (a) variable-frequency sliding mode (nominal load) and (b) variable-frequency sliding mode ($R_o \times 20$).

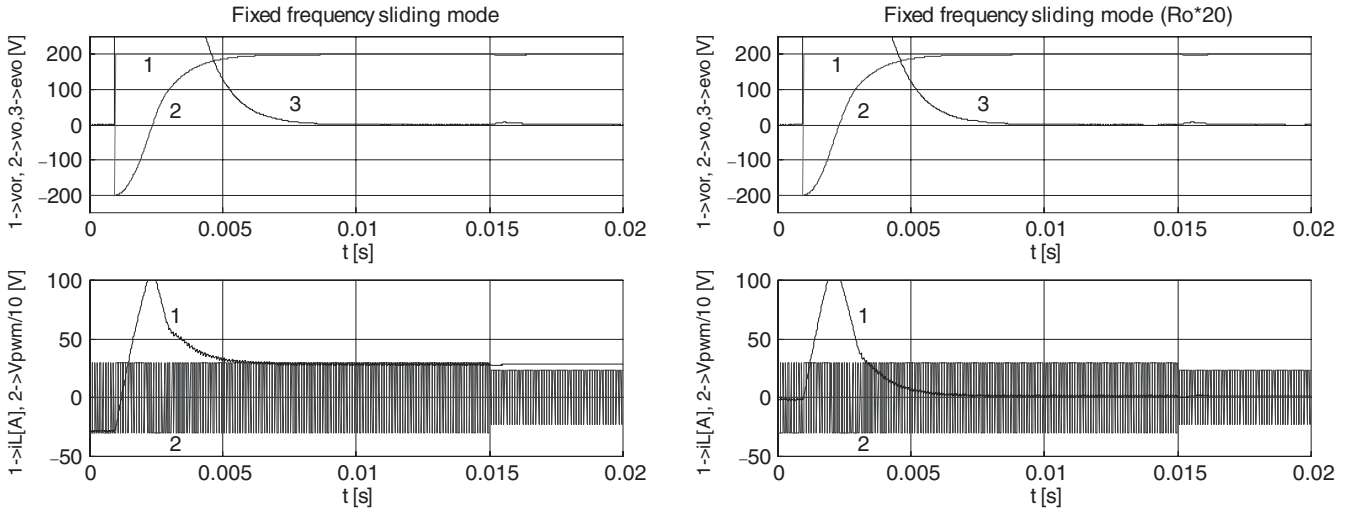


FIGURE 34.33 Performance of the power operational amplifier; response to a v_{o_r} step from −200 to 200 V at $t = 0.001$ s and to a V_{DC} step from 300 to 230 V at $t = 0.015$ s: (a) fixed-frequency sliding mode (nominal load) and (b) fixed-frequency sliding mode ($R_o \times 20$).

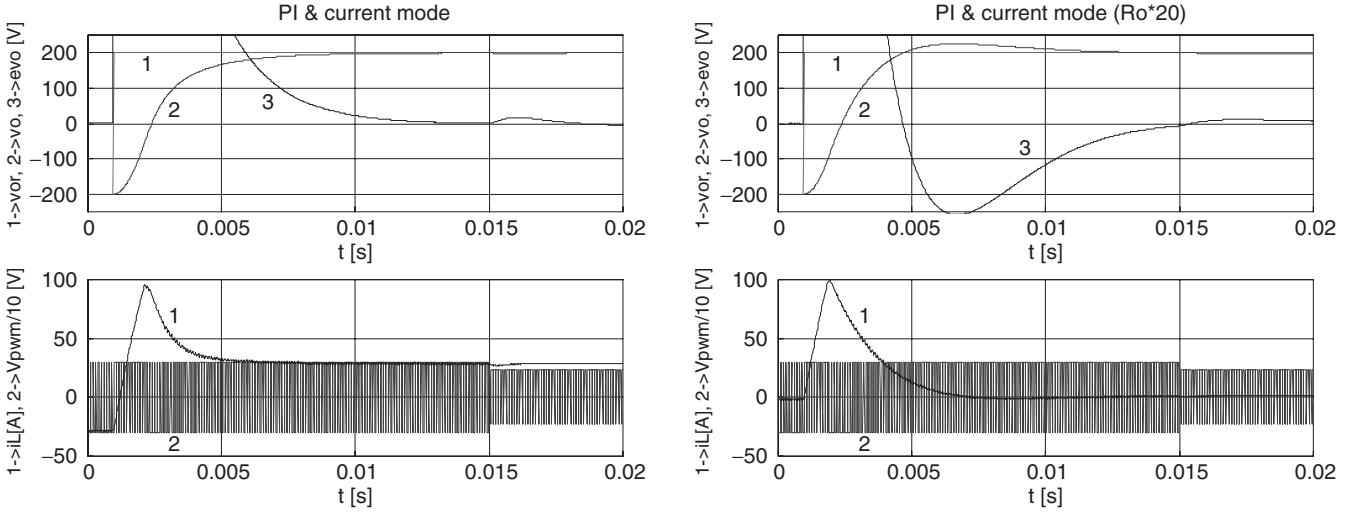


FIGURE 34.34 Performance of the PI controlled power operational amplifier; response to a v_{o_r} step from −200 to 200 V at $t = 0.001$ s and to a V_{DC} step from 300 to 230 V at $t = 0.015$ s: (a) PI current-mode controller (nominal load) and (b) PI current-mode controller ($R_o \times 20$).

and fast manifold sliding-mode approach: the fixed-frequency sliding-mode current controller (34.109) for the fast manifold (the i_L current dynamics) and the antiwindup PI for the slow manifold (the v_o voltage dynamics, usually much slower than the current dynamics).

EXAMPLE 34.12 Constant-frequency sliding-mode control of *p* pulse parallel rectifiers

This example presents a new paradigm to the control of thyristor rectifiers. Since p pulse rectifiers are variable-structure systems, sliding-mode control is applied here to 12-pulse rectifiers, still useful for very high-power applications [3]. The design determines the variables to be measured and the controlled rectifier presents robustness, and much shorter response times, even with the parameter uncertainty, perturbations, noise, and nonmodeled dynamics. These performances are not feasible using linear controllers, obtained here for comparison purposes.

34.3.5.4 Modeling the 12-pulse Parallel Rectifier

The 12-pulse rectifier (Fig. 34.35a) is built with four three-phase half-wave rectifiers, connected in parallel with current-sharing inductances l and l' merged with capacitors C', C_2, to

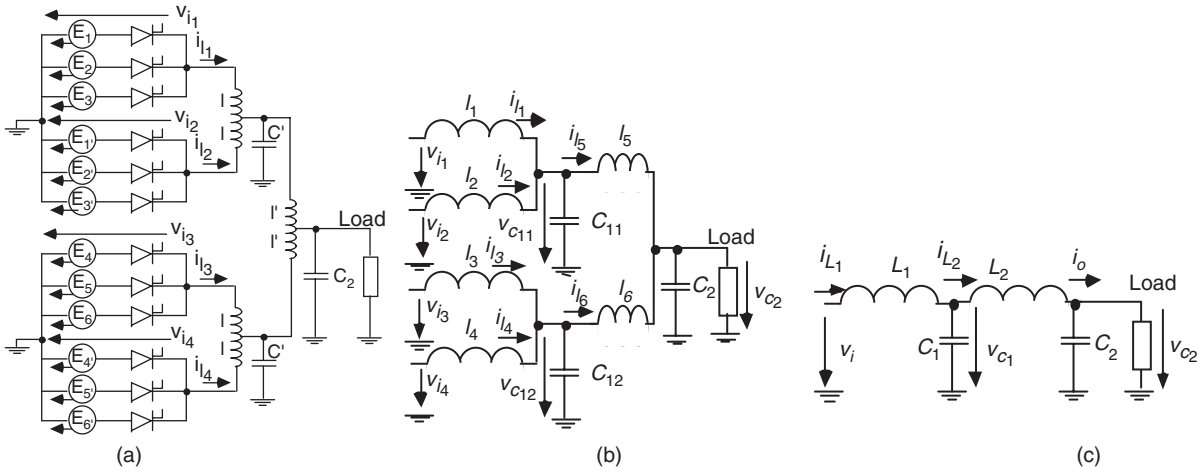


FIGURE 34.35 (a) 12-pulse rectifier with interphase reactors and intermediate capacitors; (b) rectifier model neglecting the half-wave rectifier dynamics; and (c) low-order averaged equivalent circuit for the 12-pulse rectifier with the resulting output double LC filter.

obtain a second-order LC filter. This allows low-ripple output voltage and continuous mode of operation (laboratory model with $l = 44\,\text{mH}$; $l' = 13\,\text{mH}$; $C' = C_2 = 10\,\text{mF}$; star-delta connected ac sources with $E_{RMS} \approx 65\,\text{V}$ and power rating 2.2 kW, load approximately resistive $R_o \approx 3$–$5\,\Omega$).

To control the output voltage v_{c_2}, given the complexity of the whole system, the best approach is to derive a low-order model. By averaging the four half-wave rectifiers, neglecting the rectifier dynamics and mutual couplings, the equivalent circuit of Fig. 34.35b is obtained ($l_1 = l_2 = l_3 = l_4 = l$; $l_5 = l_6 = l'$; $C_{11} = C_{12} = C'$). Since the rectifiers are identical, the equivalent 12-pulse rectifier model of Fig. 34.35c is derived, simplifying the resulting parallel associations ($L_1 = l/4$; $L_2 = l'/2$; $C_1 = 2C'$).

Considering the load current i_o as an external perturbation and v_i the control input, the state-space model of the equivalent circuit of Fig. 34.35c is

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 \\ 1/C_1 & -1/C_1 & 0 & 0 \\ 0 & 1/C_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix} + \begin{bmatrix} 1/L_1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1/C_2 \end{bmatrix} \begin{bmatrix} v_i \\ i_o \end{bmatrix} \tag{34.117}$$

34.3.5.5 Sliding-mode Control of the 12-pulse Parallel Rectifier

Since the output voltage v_{c_2} of the system must follow the reference $v_{c_{2r}}$, the system equations in the phase canonical (or controllability) form must be written, using the error $e_{v_{c_2}} = v_{c_{2r}} - v_{c_2}$ and its time derivatives as new state error variables, as done in Example 34.11.

$$\frac{d}{dt}\begin{bmatrix} e_{v_{c_2}} \\ e_\theta \\ e_\gamma \\ e_\beta \end{bmatrix} = \begin{bmatrix} e_\theta \\ e_\gamma \\ e_\beta \\ -\left(\frac{1}{C_1L_1}+\frac{1}{C_1L_2}+\frac{1}{C_2L_2}\right)e_\gamma - \frac{e_{v_{c_2}}}{C_1L_1C_2L_2} - \left(\frac{1}{C_1L_1C_2} + \frac{1}{C_1C_2L_2}\right)\frac{di_o}{dt} - \frac{1}{C_2}\frac{d^3i_o}{dt^3} - \frac{v_i}{C_1L_1C_2L_2} \end{bmatrix} \tag{34.118}$$

The sliding surface $S(e_{x_i}, t)$, designed to reduce the system order, is a linear combination of all the phase canonical state variables. Considering Eqs. (34.118) and (34.117), and the errors $e_{v_{c_2}}$, e_θ, e_γ, and e_β, the sliding surface can be expressed as a combination of the rectifier currents, voltages, and their time derivatives:

$$\begin{aligned} S(e_{x_i}, t) &= e_{v_{c_2}} + k_\theta e_\theta + k_\gamma e_\gamma + k_\beta e_\beta \\ &= v_{c_{2r}} + k_\theta\theta_r + k_\gamma\gamma_r + k_\beta\beta_r - \left(1 - \frac{k_\gamma}{C_2L_2}\right)v_{c_2} \\ &\quad - \frac{k_\gamma}{C_2L_2}v_{c_1} + \left(\frac{k_\theta}{C_2} - \frac{k_\beta}{C_2^2L_2}\right)i_o + \frac{k_\gamma}{C_2}\frac{di_o}{dt} + \frac{k_\beta}{C_2}\frac{d^2i_o}{dt^2} \\ &\quad - \frac{k_\beta}{C_1C_2L_2}i_{L_1} - \left(\frac{k_\theta}{C_2} - \frac{k_\beta}{C_1C_2L_2} - \frac{k_\beta}{C_2^2L_2}\right)i_{L_2} = 0 \end{aligned} \tag{34.119}$$

Equation (34.119) shows the variables to be measured (v_{c_2}, v_{c_1}, i_o, i_{L_1}, and i_{L_2}). Therefore, it can be concluded that the output current of each three-phase half-wave rectifier must be measured.

The existence of the sliding mode implies $S(e_{x_i}, t) = 0$ and $\dot{S}(e_{x_i}, t) = 0$. Given the state models (34.117, 34.118), and from $\dot{S}(e_{x_i}, t) = 0$, the available voltage of the power supply v_i must exceed the equivalent average dc input voltage V_{eq} (34.120), which should be applied at the filter input, in order that the system state slides along the sliding surface (34.119).

$$V_{eq} = \frac{C_1 L_1 C_2 L_2}{k_\beta}\left(\theta_r + k_\theta \gamma_r + k_\gamma \beta_r + k_\beta \dot{\beta}_r\right) + v_{c_2} - \frac{C_1 L_1 C_2 L_2}{k_\beta} \times \left(\theta + k_\gamma \beta\right) + \left(C_2 L_2 + C_2 L_1 + C_1 L_1 - C_1 L_1 C_2 L_2 \frac{k_\theta}{k_\beta}\right)\gamma + (L_1 + L_2)\frac{di_o}{dt} + C_1 L_1 L_2 \frac{d^3 i_o}{dt^3} \tag{34.120}$$

This means that the power supply root mean square (RMS) voltage values should be chosen high enough to account for the maximum effects of the perturbations. This is almost the same criterion adopted when calculating the RMS voltage values needed with linear controllers. However, as the V_{eq} voltage contains the derivatives of the reference voltage, the system will not be able to stay in sliding mode with a step as the reference.

The switching law would be derived, considering that, from Eq. (34.118) $b_e(\mathbf{e}) > 0$. Therefore, from Eq. (34.97), if $S(e_{x_i}, t) > +\varepsilon$, then $v_i(t) = V_{eq_{max}}$, else if $S(e_{x_i}, t) < -\varepsilon$, then $v_i(t) = -V_{eq_{max}}$. However, because of the lack of gate turn-off capability of the rectifier thyristors, power rectifiers cannot generate the high-frequency switching voltage $v_i(t)$, since the statistical mean delay time is $T/2p(T = 20\,\text{ms})$ and reaches $T/2$ when switching from $+V_{eq_{max}}$ to $-V_{eq_{max}}$. To control mains switched rectifiers, the described constant-frequency sliding-mode operation method is used, in which the sliding surface $S(e_{x_i}, t)$ instead of being compared to zero, is compared to an auxiliary constant-frequency function $r(t)$ (Fig. 34.6b) synchronized with the mains frequency. The new switching law is

$$\left.\begin{array}{l}\text{If } k_p S(e_{x_i}, t) > r(t) + \iota \Rightarrow \text{Trigger the next thyristor} \\ \text{If } k_p S(e_{x_i}, t) < r(t) - \iota \Rightarrow \text{Do not trigger any thyristor}\end{array}\right\} \Rightarrow v_i(t) \tag{34.121}$$

Since now $S(e_{x_i}, t)$ is not near zero, but around some value of $r(t)$, a steady-state error $e_{v_{c_{2av}}}$ appears $(\min[r(t)]/k_p < e_{v_{c_{2av}}} < \max[r(t)]/k_p)$, as seen in Example 34.11. Increasing the value of k_p (toward the ideal saturation control) does not overcome this drawback, since oscillations would appear even for moderate k_p gains, because of the rectifier dynamics. Instead, the sliding surface (34.122), based on Eq. (34.99), should be used. It contains an integral term, which, given the canonical controllability form and the Routh–Hurwitz property, is the only nonzero term at steady state, enabling the complete elimination of the steady-state error.

$$S_i(e_{x_i}, t) = \int e_{v_{c_2}}\, dt + k_{1v} e_{v_{c_2}} + k_{1\theta} e_\theta + k_{1\gamma} e_\gamma + k_{1\beta} e_\beta \tag{34.122}$$

To determine the k constants of Eq. (34.122) a pole-placement technique is selected, according to a fourth-order Bessel polynomial $B_E(s)_m$, $m = 4$, from Eq. (34.88), in order to obtain the smallest possible response time with almost no overshoot. For a delay characteristic as flat as possible, the delay t_r is taken inversely proportional to a frequency f_{ci} just below the lowest cutoff frequency ($f_{ci} < 8.44\,\text{Hz}$) of the double LC filter. For this fourth-order filter, the delay is $t_r = 2.8/(2\pi f_{ci})$. By choosing $f_{ci} = 7\,\text{Hz}$ ($t_r \approx 64\,\text{ms}$), and dividing all the Bessel polynomial terms by st_r, the characteristic polynomial (34.123) is obtained:

$$S_i(e_{x_i}, s) = \frac{1}{st_r} + 1 + \frac{45}{105} st_r + \frac{10}{105} s^2 t_r^2 + \frac{1}{105} s^3 t_r^3 \tag{34.123}$$

This polynomial must be applied to Eq. (34.122) to obtain the four sliding functions needed to derive the thyristor trigger pulses of the four three-phase half-wave rectifiers. These sliding functions will enable the control of the output current (i_{l_1}, i_{l_2}, i_{l_3}, and i_{l_4}) of each half-wave rectifier, improving the current sharing among them (Fig. 34.35b). Supposing equal current share, the relation between the i_{L_1} current and the output currents of each threephase rectifier is $i_{L_1} = 4i_{l_1} = 4i_{l_2} = 4i_{l_3} = 4i_{l_4}$. Therefore, for the nth half-wave three-phase rectifier, since for $n = 1$ and $n = 2$, $v_{c_1} = v_{c_{11}}$ and $i_{L_2} = 2i_{l_5}$ and for $n = 3$ and $n = 4$, $v_{c_1} = v_{c_{12}}$ and $i_{L_2} = 2i_{l_6}$, the four sliding surfaces are ($k_{1v} = 1$):

$$\begin{aligned} S_i(e_{x_i}, t)_n = \Bigg[& k_{1v} v_{c_{2r}} + \frac{45 t_r}{105}\theta_r + \frac{10 t_r^2}{105}\gamma_r + \frac{t_r^3}{105}\beta_r \\ & + \frac{1}{t_r}\int v_{c_{2r}} - v_{c_2}\, dt - \left(\frac{k_{1v}}{C_2 L_2} - \frac{10 t_r^2}{105 C_2 L_2}\right) v_{c_2} \\ & - \frac{10 t_r^2}{105 C_2 L_2} v_{c_{11_2}} + \left(\frac{45 t_r}{105 C_2} - \frac{t_r^3}{105 C_2^2 L_2}\right) i_o \\ & + \left(\frac{10 t_r^2}{105 C_2}\right)\frac{di_o}{dt} + \left(\frac{t_r^3}{105 C_2}\right)\frac{d^2 i_o}{dt^2}\Bigg] \Big/ 4 \\ & - \left[\left(\frac{45 t_r}{105 C_2} - \frac{t_r^3}{105 C_2^2 L_2} - \frac{t_r^3}{105 C_1 L_2 C_2}\right) i_{l_{5_6}}\right] \Big/ 2 \\ & - \left(\frac{t_r^3}{105 C_1 L_2 C_2}\right) i_{ln} \end{aligned} \tag{34.124}$$

If an inexpensive analog controller is desired, the successive time derivatives of the reference voltage and the output current of Eq. (34.124) can be neglected (furthermore, their calculation is noise prone). Nonzero errors on the first, second, and third-order derivatives of the controlled variable will appear, worsening the response speed. However, the steady-state error is not affected.

To implement the four equations (34.124), the variables v_{c_2}, $v_{c_{11}}$, $v_{c_{12}}$, i_o, i_{l_5}, i_{l_6}, i_{l_1}, i_{l_2}, i_{l_3}, and i_{l_4} must be measured. Although this could be done easily, it is very convenient to further simplify the practical controller, keeping its complexity and cost at the level of linear controllers, while maintaining the advantages of sliding mode. Therefore, the voltages $v_{c_{11}}$ and $v_{c_{12}}$ are assumed almost constant over one period of the filter input current, and $v_{c_{11}} = v_{c_{12}} = v_{c_2}$, meaning that $i_{l_5} = i_{l_6} = i_o/2$. With these assumptions, valid as the values of C' and C_2 are designed to provide an output voltage with very low ripple, the new sliding-mode functions are

$$S_i(e_{x_i}, t)_n \approx \frac{\frac{1}{t_r}\int vc_{2r} - vc_2 dt + k_{1v}(v_{c_{2r}} - v_{c_2}) + \frac{t_r^3}{105}\frac{1}{C_1C_2L_2}i_o}{4} - \left(\frac{t_r^3}{105C_1L_2C_2}\right) i_{ln} \tag{34.125}$$

These approximations disregard only the high-frequency content of $v_{c_{11}}$, $v_{c_{12}}$, i_{l_5}, and i_{l_6}, and do not affect the rectifier steady-state response, but the step response will be a little slower, although still much faster (150 ms, Fig. 34.39) than that obtained with linear controllers (280 ms, Fig. 34.38). Regardless of all the approximations, the low switching frequency of the rectifier would not allow the elimination of the dynamic errors. As a benefit of these approximations, the sliding-mode controller (Fig. 34.36a) will need only an extra current sensor (or a current observer) and an extra operational amplifier in comparison with linear controllers derived hereafter (which need four current sensors and six operational amplifiers). Compared to the total cost of the 12-pulse rectifier plus output filter, the control hardware cost is negligible in both the cases, even for medium-power applications.

34.3.5.6 Average Current-mode Control of the 12-pulse Rectifier

For comparison purposes a PI-based controller structure is designed (Fig. 34.36b), taking into account, that small mismatches of the line voltages or of the trigger angles can completely destroy the current share of the four paralleled rectifiers, inspite of the current equalizing inductances (l and l'). Output voltage control sensing only the output voltage is, therefore, not feasible. Instead, the slow and fast manifold approach is selected. For the fast manifold, four internal current control loops guarantee the same dc current level in each three-phase rectifier and limit the short-circuit currents. For the output slow dynamics, an external cascaded output voltage control loop (Fig. 34.36b), measuring the voltage applied to the load, is the minimum.

For a straightforward design, given the much slower dynamics of the capacitor voltages compared to the input current, the PI current controllers are calculated as shown in Example 34.6, considering the capacitor voltage constant during a switching period, and $r_t \approx 1\,\Omega$ the intrinsic resistance of the transformer windings, thyristor overlap, and inductor l. From Eq. (34.59), $T_z = l/r_t \approx 0.044$ s. From, Eq. (34.62), with the common assumptions, $T_p \approx 0.16k_I$ s ($p = 3$). These values guarantee a small overshoot (≈5%) and a current rise time of approximately $T/3$.

To design the external output voltage control loop, each current-controlled rectifier can be considered a voltage-controlled current source $i_{L_1}(s)/4$, since each half-wave rectifier current response will be much faster than the filter output voltage response. Therefore, in the equivalent circuit

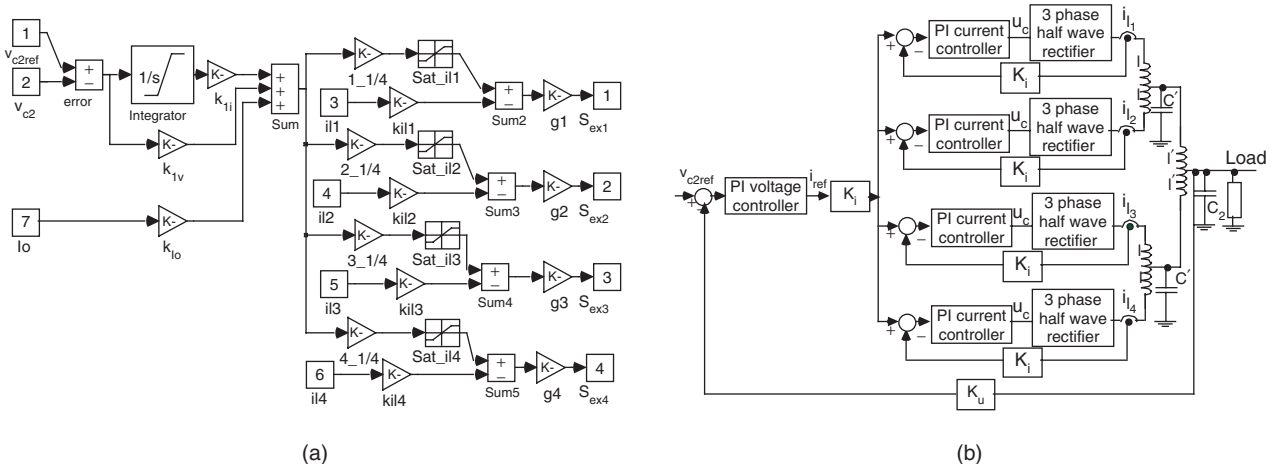


FIGURE 34.36 (a) Sliding-mode controller block diagram and (b) linear control hierarchy for the 12-pulse rectifier.

of Fig. 34.35b, the current source $i_{L_1}(s)$ substitutes the input inductor, yielding the transfer function $v_{c_2}(s)/i_{L_1}(s)$:

$$\frac{V_{c_2}(s)}{i_{L_1}(s)} = \frac{R_o}{C_2C_1L_2R_os^3 + C_1L_2s^2 + (C_2R_o + C_1R_o)s + 1} \tag{34.126}$$

Given the real pole ($p_1 = -6.7$) and two complex poles ($p_{2,3} = -6.65 \pm$ j140.9) of Eq. (34.126), the PI voltage controller zero ($1/T_{zv} = p_1$) can be chosen with a value equal to the transfer function real pole. The integral gain T_{pv} can be determined using a root-locus analysis to determine the maximum gain, that still guarantees the stability of the closed-loop controlled system. The critical gain for the PI was found to be $T_{zv}/T_{pv} \approx 0.4$, then $T_{pv} > 0.37$. The value $T_{pv} \approx 2$ was selected to obtain weak oscillations, together with almost no overshoot.

The dynamic and steady-state responses of the output currents of the four rectifiers (i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4}) and the output voltage v_{c_2} were analyzed using a step input from 2 to 2.5 A applied at $t = 1.1$ s, for the currents, and from 40 to 50 V for the v_{c_2} voltage. The PI current controllers (Fig. 34.37) show good sharing of the total current, a slight overshoot ($\zeta = 0.7$) and response time 6.6 ms (T/p).

The open-loop voltage v_{c_2} presents a rise time of 0.38 s. The PI voltage controller (Fig. 34.38) shows a response time of 0.4 s, no overshoot. The four three-phase half-wave rectifier output currents (i_{l_1}, i_{l_2}, i_{l_3}, and i_{l_4}) present nearly the same transient and steady-state values, with no very high current peaks. These results validate the assumptions made in the PI design.

The closed-loop performance of the fixed-frequency sliding-mode controller (Fig. 34.39) shows that all the i_{l_1}, i_{l_2}, i_{l_3}, and i_{l_4} currents are almost equal and have peak values only slightly higher than those obtained with the PI linear controllers. The output voltage presents a much faster response time (150 ms) than the PI linear controllers, negligible or no steady-state error, and no overshoot. From these waveforms

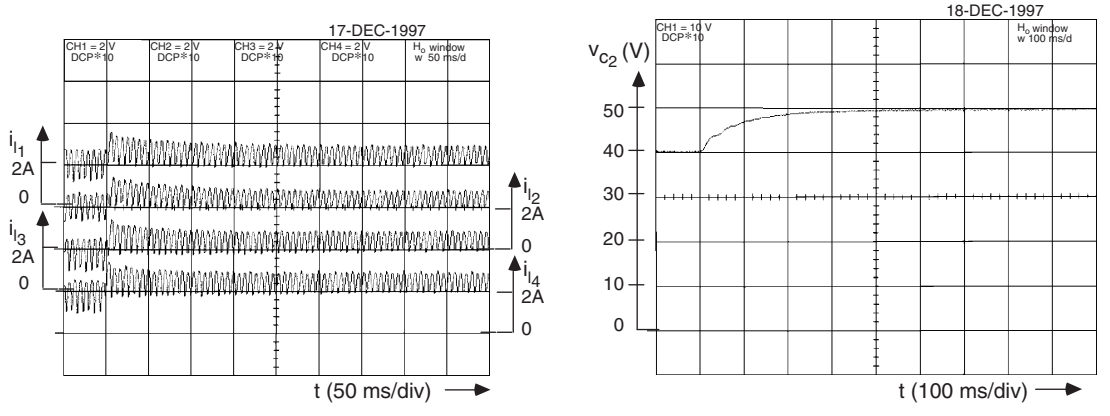


FIGURE 34.37 PI current controller performance: (a) i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4} closed-loop currents and (b) open-loop output voltage V_{c_2}.

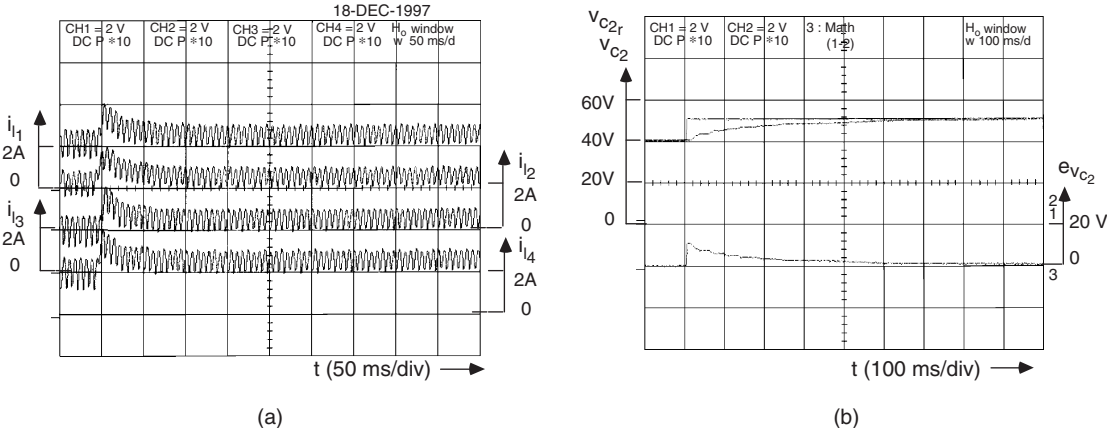


FIGURE 34.38 PI voltage controller performance: (a) i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4} closed-loop currents and (b) closed output voltage V_{c_2} and $l_{v_{c_2}}$ output voltage error.

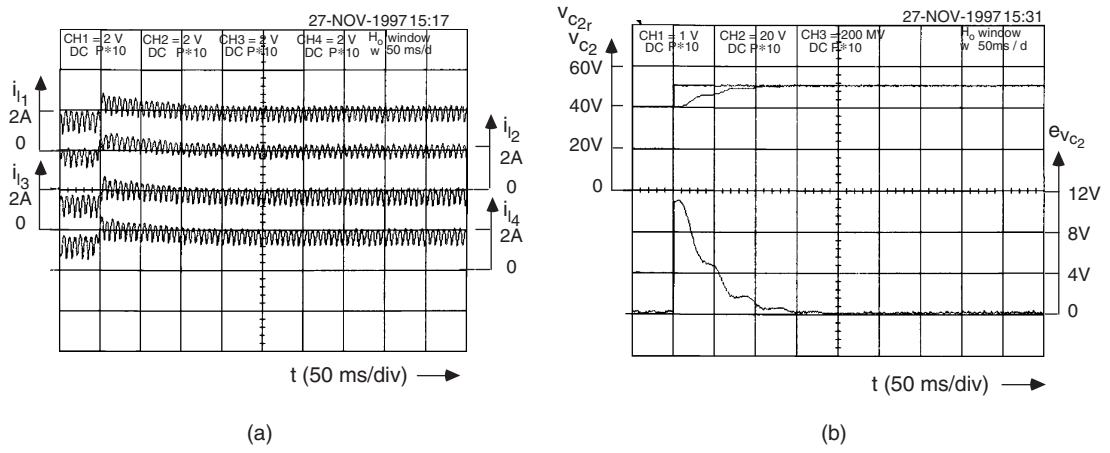


FIGURE 34.39 Closed-loop constant-frequency sliding-mode controller performance: (a) i_{l_1}, i_{l_2}, i_{l_3}, i_{l_4} closed-loop currents and (b) closed output voltage V_{c_2} and $e_{v_{c_2}}$ output voltage error.

it can be concluded that the sliding-mode controller provides a much more effective control of the rectifier, as the output voltage response time is much lower than the obtained with PI linear controllers, without significantly increasing the thyristor currents, overshoots, or costs. Furthermore, sliding mode is an elegant way to know the variables to be measured, and to design all the controller and the modulator electronics.

EXAMPLE 34.13 Sliding-mode control of pulse width modulation audio power amplifiers

Linear audio power amplifiers can be astonishing, but have efficiencies as low as 15–20% with speech or music signals. To improve the efficiency of audio systems while preserving the quality, PWM switching power amplifiers, enabling the reduction of the power-supply cost, volume, and weight and compensating the efficiency loss of modern loudspeakers, are needed. Moreover, PWM amplifiers can provide a complete digital solution for audio power processing.

For high-fidelity systems, PWM audio amplifiers must present flat passbands of at least 16–20 kHz (±0.5 dB), distortions less than 0.1% at the rated output power, fast dynamic response, and signal-to-noise ratios above 90 dB. This requires fast power semiconductors (usually metal-oxide semiconductor field effect transistor (MOSFET) transistors), capable of switching at frequencies near 500 kHz, and fast nonlinear controllers to provide the precise and timely control actions needed to accomplish the mentioned requirements and to eliminate the phase delays in the LC output filter and loudspeakers.

A low-cost PWM audio power amplifier, able to provide over 80 W to 8 Ω loads ($V_{dd} = 50$ V), can be obtained using a half-bridge power inverter (switching at $f_{PWM} \approx 450$ kHz), coupled to an output filter for high-frequency attenuation (Fig. 34.40). A low-sensitivity,

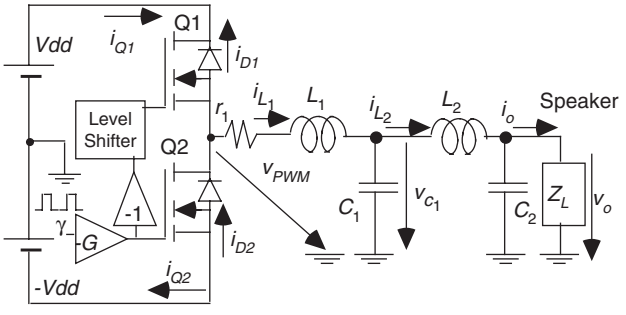


FIGURE 34.40 PWM audio amplifier with fourth-order Chebyshev low-pass output filter and loudspeaker load.

doubly terminated passive ladder (double LC), low-pass filter using fourth-order Chebyshev approximation polynomials is selected, given its ability to meet, while minimizing the number of inductors, the following requirements: passband edge frequency 21 kHz, passband ripple 0.5 dB, stopband edge frequency 300 kHz and 90 dB minimum attenuation in the stopband ($L_1 = 80\,\mu$H; $L_2 = 85\,\mu$H; $C_1 = 1.7\,\mu$F; $C_2 = 820$ nF; $R_2 = 8\,\Omega$; $r_1 = 0.47\,\Omega$).

34.3.5.7 Modeling the PWM Audio Amplifier

The two half-bridge switches must always be in complementary states, to avoid power supply internal short-circuits. Their state can be represented by the time-dependent variable γ, which is $\gamma = 1$ when Q1 is on and Q2 is off, and is $\gamma = -1$ when Q1 is off and Q2 is on.

Neglecting switch delays, on state semiconductor voltage drops, auxiliary networks, and supposing small dead times, the half-bridge output voltage (v_{PWM}) is $v_{PWM} = \gamma V_{dd}$. Considering the state variables and circuit components of

Fig. 34.40, and modeling the loudspeaker load as a disturbance represented by the current i_o (ensuring robustness to the frequency dependent impedance of the speaker), the switched state-space model of the PWM audio amplifier is

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ v_{c_1} \\ i_{L_2} \\ v_o \end{bmatrix} = \begin{bmatrix} -r_1/L_1 & -1/L_1 & 0 & 0 \\ 1/C_1 & 0 & -1/C_1 & 0 \\ 0 & 1/L_2 & 0 & -1/L_2 \\ 0 & 0 & 1/C_2 & 0 \end{bmatrix} \begin{bmatrix} i_{L_1} \\ v_{c_1} \\ i_{L_2} \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L_1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1/C_2 \end{bmatrix} \begin{bmatrix} \gamma V_{dd} \\ i_o \end{bmatrix} \tag{34.127}$$

This model will be used to define the output voltage v_o controller.

34.3.5.8 Sliding-mode Control of the PWM Audio Amplifier

The filter output voltage v_o, divided by the amplifier gain $(1/k_v)$, must follow a reference v_{o_r}. Defining the output error as $e_{v_o} = v_{o_r} - k_v v_o$, and also using its time derivatives $(e_\theta, e_\gamma, e_\beta)$ as a new state vector $\mathbf{e} = [e_{v_o}, e_\theta, e_\gamma, e_\beta]^T$, the system equations, in the phase canonical (or controllability) form, can be written in the form

$$\frac{d}{dt}[e_{v_o}, e_\theta, e_\gamma, e_\beta]^T = [e_\theta, e_\gamma, e_\beta, -f(e_{v_o}, e_\theta, e_\gamma, e_\beta) + p_e(t) - \gamma V_{dd}/C_1 L_1 C_2 L_2]^T \tag{34.128}$$

Sliding-mode control of the output voltage will enable a robust and reduced-order dynamics, independent of semiconductors, power supply, filter, and load parameters. According to Eqs. (34.91) and (34.128), the sliding surface is

$$\begin{aligned} S(e_{v_o}, e_\theta, e_\gamma, e_\beta, t) &= e_{v_o} + k_\theta e_\theta + k_\gamma e_\gamma + k_\beta e_\beta \\ &= v_{o_r} - k_v v_o + k_\theta \frac{d\left(v_{o_r} - k_v v_o\right)}{dt} \\ &\quad + k_\gamma \frac{d}{dt}\left(\frac{d\left(v_{o_r} - k_v v_o\right)}{dt}\right) \\ &\quad + k_\beta \frac{d}{dt}\left[\frac{d}{dt}\left(\frac{d\left(v_{o_r} - k_v v_o\right)}{dt}\right)\right] = 0 \end{aligned} \tag{34.129}$$

In sliding mode, Eq. (34.129) confirms the amplifier gain $(v_o/v_{o_r} = 1/k_v)$. To obtain a stable system and the smallest possible response time t_r, a pole placement according to a third-order Bessel polynomial is used. Taking t_r inversely proportional to a frequency just below the lowest cutoff frequency (ω_1) of the double LC filter $(t_r \approx 2.8/\omega_1 \approx 2.8/(2\pi \times 21\,\text{kHz}) \approx 20\,\mu\text{s})$ and using Eq. (34.88) with $m = 3$, the characteristic polynomial Eq. (34.130), verifying the Routh–Hurwitz criterion is obtained.

$$S(\mathbf{e}, s) = 1 + st_r + \frac{6}{15}(st_r)^2 + \frac{1}{15}(st_r)^3 \tag{34.130}$$

From Eq. (34.97) the switching law for the control input at time t_k, $\gamma(t_k)$, must be

$$\gamma(t_k) = \text{sgn}\left\{S(\mathbf{e}, t_k) + \varepsilon\, \text{sgn}\left[S(\mathbf{e}, t_{k-1})\right]\right\} \tag{34.131}$$

To ensure reaching and existence conditions, the power supply voltage V_{dd} must be greater than the maximum required mean value of the output voltage in a switching period $V_{dd} > (\overline{v_{PWMmax}})$. The sliding-mode controller (Fig. 34.41) is obtained from Eqs. (34.129–34.131) with $k_\theta = t_r$, $k_\gamma = 6t_r^2/15$, $k_\beta = t_r^3/15$. The derivatives can be approximated by the block diagram of Fig. 34.41b, were h is the oversampling period.

Fig. 34.42a shows the v_{PWM}, v_{o_r}, $v_o/10$, and the error $10 \times (v_{o_r} - v_o/10)$ waveforms for a 20 kHz sine input. The overall behavior is much better than the obtained with the sigma-delta controllers (Figs. 34.43 and 34.44) explained below for comparison purposes. There is no 0.5 dB loss or phase delay over the entire audio band; the Chebyshev filter behaves as a maximally flat filter, with higher stopband attenuation. Fig. 34.42b shows v_{PWM}, v_{o_r}, and $10 \times (v_{o_r} - v_o/10)$ with a 1 kHz square input. There is almost no steady-state error and almost no overshoot on the speaker voltage v_o, attesting to the speed of response ($t \approx 20\,\mu\text{s}$ as designed, since, in contrast to Example 34.12, no derivatives were neglected). The stability, the system order reduction, and the sliding-mode controller usefulness for the PWM audio amplifier are also shown.

34.3.5.9 Sigma Delta Controlled PWM Audio Amplifier

Assume now the fourth-order Chebyshev low-pass filter, as an ideal filter removing the high-frequency content of the v_{PWM} voltage. Then, the v_{PWM} voltage can be considered as the amplifier output. However, the discontinuous voltage $v_{PWM} = \gamma V_{dd}$ is not a state variable and cannot follow the almost continuous reference v_{PWM_r}. The new error variable $e_{vPWM} = v_{PWM_r} - k_v \gamma V_{dd}$ is always far from the zero value. Given this nonzero error, the approach outlined in Section 34.3.4 can be used. The switching law remains Eq. (34.131), but the new control law Eq. (34.132) is

$$S(e_{vPWM}, t) = \kappa \int (v_{PWM_r} - k_v \gamma V_{dd})dt = 0 \tag{34.132}$$

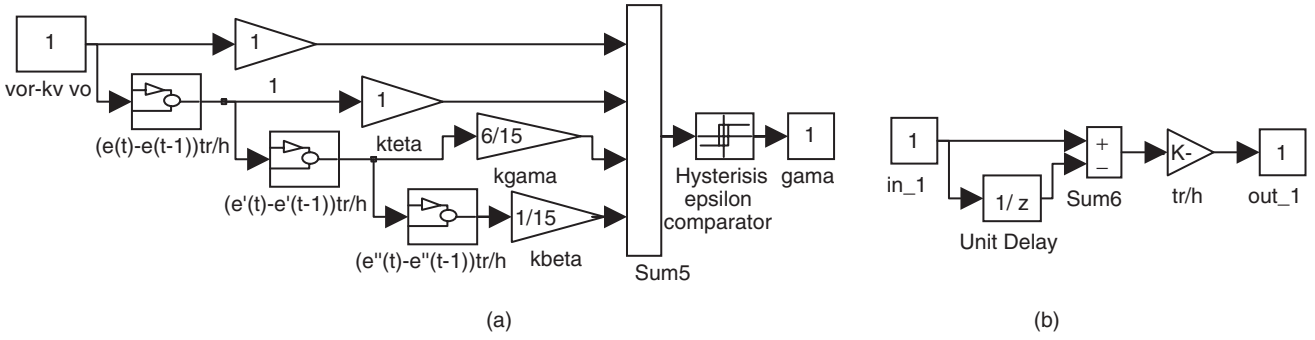


FIGURE 34.41 (a) Sliding-mode controller for the PWM audio amplifier and (b) implementation of the derivative blocks.

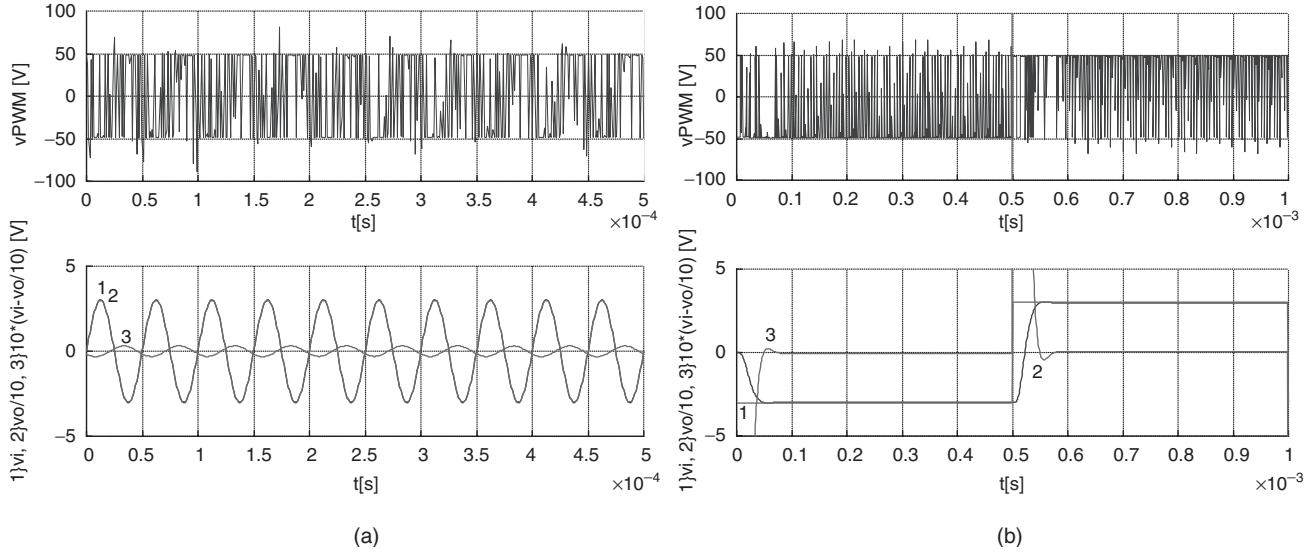


FIGURE 34.42 Sliding-mode controlled audio power amplifier performance (upper graphs show v_{PWM} , lower graph traces 1 show v_{o_r} ($v_{o_r} \equiv v_i$), lower graph traces 2 show $v_o/10$, and lower graph traces 3 show $10\times(v_{o_r} - v_o\ /10)$): (a) response to a 20 kHz sine input, at 55 W output power and (b) response to 1 kHz square wave input, at 100 W output power.

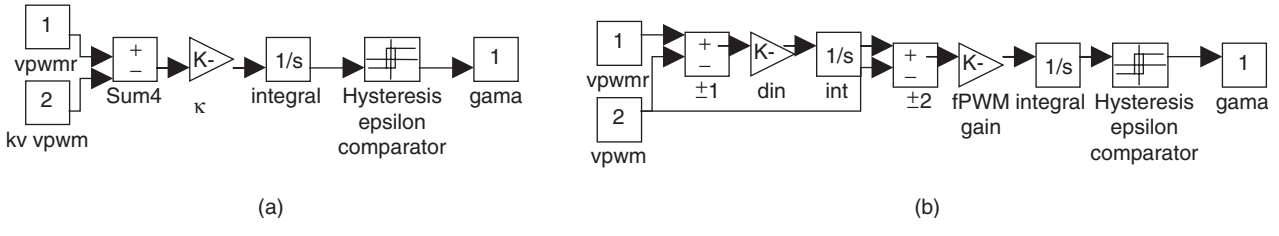


FIGURE 34.43 (a) First-order sigma delta modulator and (b) second-order sigma delta modulator.

The κ parameter is calculated to impose the maximum switching frequency f_{PWM}. Since $\kappa \int_0^{1/2f_{PWM}} (v_{PWM_{rmax}} + k_v V_{dd})dt = 2\varepsilon$, we obtain

$$f_{PWM} = \kappa(v_{PWM_{rmax}} + k_v V_{dd})/(4\varepsilon) \tag{34.133}$$

Assuming that v_{PWM_r} is nearly constant over the switching period $1/f_{PWM}$, Eq. (34.132) confirms the amplifier gain, since $\overline{v_{PWM}} = v_{PWM_r}/k_v$.

Practical implementation of this control strategy can be done using an integrator with gain κ ($\kappa \approx 1800$), and a comparator with hysteresis ε ($\varepsilon \approx 6$ mV), Fig. 34.43a. Such an arrangement is called a first-order sigma-delta ($\Sigma\Delta$) modulator.

Fig. 34.44a shows the v_{PWM}, v_{o_r}, and $v_o/10$ waveforms for a 20 kHz sine input. The overall behavior is as expected, because the practical filter and loudspeaker are not ideal, but notice the

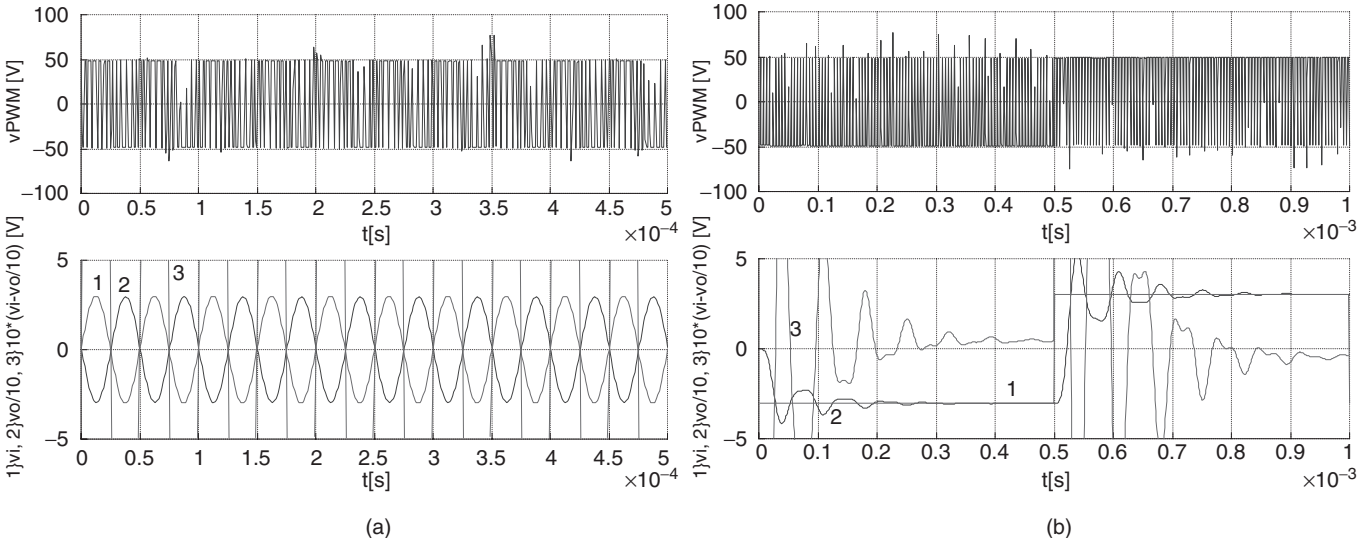


FIGURE 34.44 First-order sigma-delta audio amplifier performance (upper graphs show v_{PWM}, lower graphs trace 1 show $v_{o_r} \equiv v_i$, lower graphs trace 2 shows $v_o/10$, and lower graphs trace 3 show $10\times(v_{o_r} - v_o/10)$): (a) response to a 20 kHz sine input, at 55 W output power and (b) response to 1 kHz square wave input, at 100 W output power.

0.5 dB loss and phase delay of the speaker voltage v_o, mainly due to the output filter and speaker inductance. In Fig. 34.44b, the v_{PWM}, v_{o_r}, $v_o/10$, and error $10 \times (v_{o_r} - v_o/10)$ for a 1 kHz square input are shown. Note the oscillations and steady-state error of the speaker voltage v_o, due to the filter dynamics and double termination.

A second-order sigma-delta modulator is a better compromise between circuit complexity and signal-to-quantization noise ratio. As the switching frequency of the two power MOSFET (Fig. 34.40) cannot be further increased, the second-order structure named "cascaded integrators with feedback" (Fig. 34.43b) was selected, and designed to eliminate the step response overshoot found in Fig. 34.44b.

Fig. 34.45a, for 1 kHz square input, shows much less overshoot and oscillations than Fig. 34.44b. However, the v_{PWM}, v_{o_r}, and $v_o/10$ waveforms, for a 20 kHz sine input presented

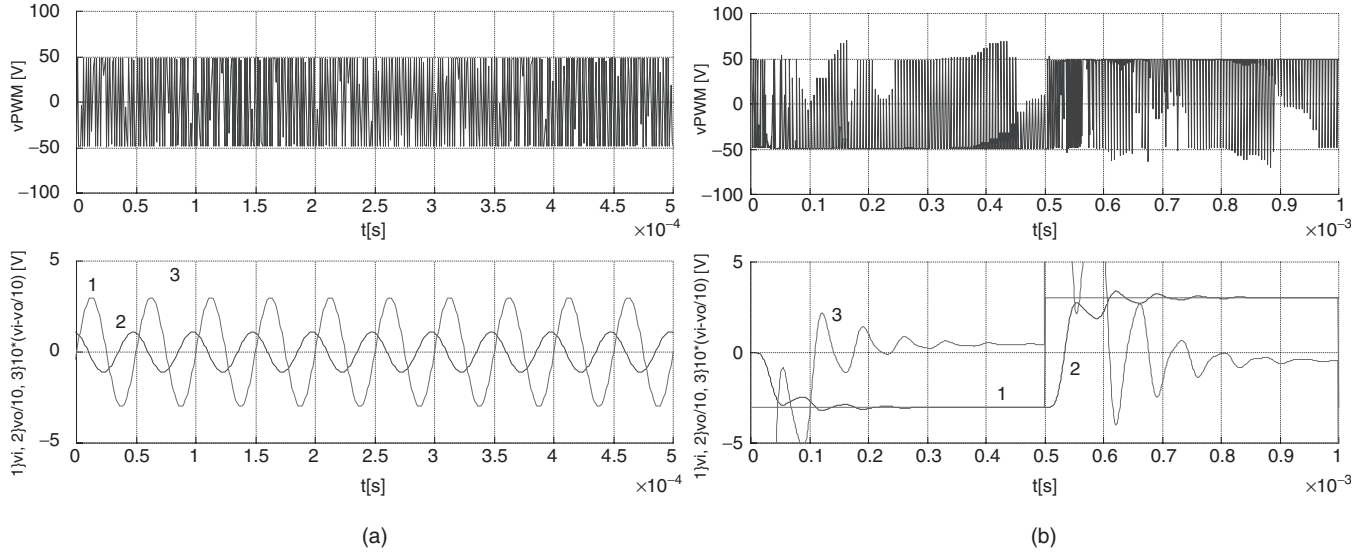


FIGURE 34.45 Second-order sigma-delta audio amplifier performance (upper graphs show v_{PWM}, lower graphs trace 1 show $v_{o_r} \equiv v_i$, lower graphs trace 2 show $v_o/10$, and lower graphs trace 3 show $10\times(v_{o_r} - v_o/10)$): (a) response to 1 kHz square wave input, at 100 W output power and (b) response to a 20 kHz sine input, at 55 W output power.

in Fig. 34.45b, show increased output voltage loss, compared to the first-order sigma-delta modulator, since the second-order modulator was designed to eliminate the v_o output voltage ringing (therefore reducing the amplifier bandwidth). The obtained performances with these and other sigma-delta structures are inferior to the sliding-mode performances (Fig. 34.42). Sliding mode brings definite advantages as the system order is reduced, flatter passbands are obtained, power supply rejection ratio is increased, and the nonlinear effects, together with the frequency-dependent phase delays, are cancelled out.

EXAMPLE 34.14 Sliding-mode control of near unity power factor PWM rectifiers

Boost-type voltage-sourced three-phase rectifiers (Fig. 34.46) are multiple-input multiple-output (MIMO) systems capable of bidirectional power flow, near unity power factor operation, and almost sinusoidal input currents, and can behave as ac/dc power supplies or power factor compensators.

The fast power semiconductors used (usually MOSFETs or IGBTs) can switch at frequencies much higher than the mains frequency, enabling the voltage controller to provide an output voltage with fast dynamic response.

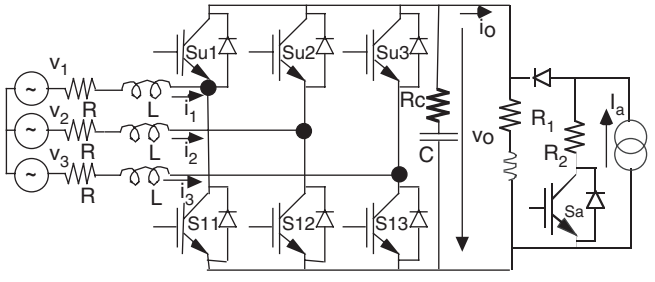


FIGURE 34.46 Voltage-sourced PWM rectifier with IGBTs and test load.

34.3.5.10 Modeling the PWM Boost Rectifier

Neglecting switch delays and dead times, the states of the switches of the kth inverter leg (Fig. 34.46) can be represented by the time-dependent nonlinear variables γ_k, defined as

$$\gamma_k = \begin{cases} 1> \text{ if } Su_k \text{ is on and } Sl_k \text{ is off} \\ 0> \text{ if } Su_k \text{ is off and } Sl_k \text{ is on} \end{cases} \tag{34.134}$$

Consider the displayed variables of the circuit (Fig. 34.46), where L is the value of the boost inductors, R their resistance, C the value of the output capacitor, and R_c its equivalent series resistance (ESR). Neglecting semiconductor voltage drops, leakage currents, and auxiliary networks, the application of Kirchhoff laws (taking the load current i_o as a time-dependent perturbation) yields the following switched state-space model of the boost rectifier:

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_o \end{bmatrix} = \begin{bmatrix} -R/L & 0 & 0 & -2\gamma_1+\gamma_2+\gamma_3/3L \\ 0 & -R/L & 0 & -2\gamma_2+\gamma_3+\gamma_1/3L \\ 0 & 0 & -R/L & -2\gamma_3+\gamma_1+\gamma_2/3L \\ A_{41} & A_{42} & A_{43} & A_{44} \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_o \end{bmatrix}$$
$$+\begin{bmatrix} 1/L & 0 & 0 & 0 & 0 \\ 0 & 1/L & 0 & 0 & 0 \\ 0 & 0 & 1/L & 0 & 0 \\ \gamma_1 R_c/L & \gamma_2 R_c/L & \gamma_3 R_c/L & -1/C & -R_c \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_o \\ di_o/dt \end{bmatrix} \tag{34.135}$$

where $A_{41} = \gamma_1\left(\frac{1}{C} - \frac{RR_c}{L}\right)$; $A_{42} = \gamma_2\left(\frac{1}{C} - \frac{RR_c}{L}\right)$; $A_{43} = \gamma_3\left(\frac{1}{C} - \frac{RR_c}{L}\right)$; $A_{44} = \frac{-2R_c(\gamma_1(\gamma_1-\gamma_2)+\gamma_2(\gamma_2-\gamma_3)+\gamma_3(\gamma_3-\gamma_1))}{3L}$.

Since the input voltage sources have no neutral connection, the preceding model can be simplified, eliminating one equation. Using the relationship (34.136) between the fixed frames $x_{1,2,3}$ and $x_{\alpha,\beta}$, in Eq. (34.135), the state-space model (34.137), in the α, β frame, is obtained.

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} \sqrt{2/3} & 0 \\ -\sqrt{1/6} & \sqrt{1/2} \end{bmatrix}\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{34.136}$$

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \\ v_o \end{bmatrix} = \begin{bmatrix} -R/L & \omega & -\gamma_\alpha/L \\ 0 & -R/L & -\gamma_\beta/L \\ A^\alpha_{31} & A^\alpha_{32} & A^\alpha_{33} \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \\ v_o \end{bmatrix}$$
$$+\begin{bmatrix} 1/L & 0 & 0 & 0 \\ 0 & 1/L & 0 & 0 \\ \gamma_\alpha R_c/L & \gamma_\beta R_c/L & -1/C & -R_c \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \\ i_o \\ di_o/dt \end{bmatrix} \tag{34.137}$$

where $A^\alpha_{31} = \gamma_\alpha\left(\frac{1}{C} - \frac{RR_c}{L}\right)$; $A^\alpha_{32} = \gamma_\beta\left(\frac{1}{C} - \frac{RR_c}{L}\right)$; $A^\alpha_{33} = \frac{-R_c\left(\gamma_\alpha^2+\gamma_\beta^2\right)}{L}$.

34.3.5.11 Sliding-mode Control of the PWM Rectifier

The model (34.137) is nonlinear and time-variant. Applying the Park transformation (34.138), using a frequency ω rotating

reference frame synchronized with the mains (with the q component of the supply voltages equal to zero), the nonlinear, time-invariant model (34.139) is written:

$$\begin{bmatrix} i_a \\ i_b \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{34.138}$$

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ v_o \end{bmatrix} = \begin{bmatrix} -R/L & \omega & -\gamma_d/L \\ -\omega & -R/L & -\gamma_q/L \\ A_{31}^d & A_{32}^d & A_{33}^d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L & 0 & 0 & 0 \\ 0 & 1/L & 0 & 0 \\ \gamma_d R_c/L & \gamma_q R_c/L & -1/C & -R_c \end{bmatrix} \begin{bmatrix} v_d \\ v_q \\ i_o \\ di_o dt \end{bmatrix} \tag{34.139}$$

where $A_{31}^d = \gamma_d\left(\frac{1}{C} - \frac{RR_c}{L}\right)$; $A_{32}^d = \gamma_q\left(\frac{1}{C} - \frac{RR_c}{L}\right)$; $A_{33}^d = \frac{-R_c\left(\gamma_d^2 + \gamma_q^2\right)}{L}$.

This state-space model can be used to obtain the feedback controllers for the PWM boost rectifier. Considering the output voltage v_o and the i_q current as the controlled outputs and γ_d, γ_q the control inputs (MIMO system), the input–output linearization of Eq. (34.72) gives the state-space equations in the controllability canonical form (34.140):

$$\frac{di_q}{dt} = -\omega i_d - \frac{R}{L} i_q - \frac{\gamma_q}{L} v_o + \frac{1}{L} v_q$$

$$\frac{dv_o}{dt} = \theta$$

$$\frac{d\theta}{dt} = \frac{R + R_c\left(\gamma_d^2 + \gamma_q^2\right)}{L}\theta - \frac{\gamma_d^2 + \gamma_q^2}{LC} v_o + \frac{\gamma_d v_d + \gamma_q v_q}{LC} - \frac{Ri_o}{LC} - \left(\frac{1}{C} + \frac{RR_c}{L}\right)\frac{di_o}{dt} + \omega\left(\frac{1}{C} - \frac{RR_c}{L}\right)\left(\gamma_d i_q - \gamma_q i_d\right) - R_c \frac{d^2 i_o}{dt^2} \tag{34.140}$$

where

$$\theta = \left(\frac{1}{C} - \frac{RR_c}{L}\right)\left(\gamma_d i_d + \gamma_q i_q\right) - \frac{R_c\left(\gamma_d^2 + \gamma_q^2\right)}{L} v_o + \frac{R_c}{L}\left(\gamma_d v_d + \gamma_q v_q\right) - \frac{i_o}{C} - R_c \frac{di_o}{dt}.$$

Using the rectifier overall power balance (from Tellegen's theorem, the converter is conservative, i.e. the power delivered to the load or dissipated in the converter intrinsic devices equals the input power), and neglecting the switching and output capacitor losses, $v_d i_d + v_q i_q = v_o i_o + R i_d^2$. Supposing unity power factor ($i_{qr} \approx 0$), and the output v_o at steady state, $\gamma_d i_d + \gamma_q i_q \approx i_o$, $v_d = \sqrt{3} V_{RMS}$, $v_q = 0$, $\gamma_q \approx v_q / v_o$, $\gamma_d \approx (v_d - R i_d)/v_o$. Then, from Eqs. (34.140) and (34.91), the following two sliding surfaces can be derived:

$$S_q(e_{i_q}, t) = k_{e_{iq}}(i_{qr} - i_q) = 0 \tag{34.141}$$

$$S_d(e_{v_o}, e_\theta, t) \approx \left[\beta^{-1}(v_{o_r} - v_o) + \frac{dv_{o_r}}{dt} + \frac{1}{C} i_o + R_c \frac{di_o}{dt}\right] \times \frac{LC}{L - CRR_c} \frac{v_o}{\sqrt{3} V_{RMS} - R i_d} - i_d = i_{d_r} - i_d = 0 \tag{34.142}$$

where β^{-1} is the time constant of the desired first-order response of output voltage v_o ($\beta \gg T > 0$). For the synthesis of the closed-loop control system, notice that the terms of Eq. (34.142) inside the square brackets can be assumed as the i_d reference current i_{d_r}. Furthermore, from Eqs. (34.141) and (34.142) it is seen that the current control loops for i_d and i_q are needed. Considering Eqs. (34.138) and (34.136), the two sliding surfaces can be written

$$S_\alpha(e_{i_\alpha}, t) = i_{\alpha_r} - i_\alpha = 0 \tag{34.143}$$

$$S_\beta(e_{i_\beta}, t) = i_{\beta_r} - i_\beta = 0 \tag{34.144}$$

The switching laws relating the sliding surfaces (34.143, 34.144) with the switching variables γ_k are

$$\begin{cases} \text{If } S_{\alpha\beta}(e_{i_{\alpha\beta}}, t) > \varepsilon \text{ then } i_{\alpha\beta_r} > i_{\alpha\beta} \text{ hence choose } \gamma_k \text{ to increase the } i_{\alpha\beta} \text{ current} \\ \text{If } S_{\alpha\beta}(e_{i_{\alpha\beta}}, t) < -\varepsilon \text{ then } i_{\alpha\beta_r} < i_{\alpha\beta} \text{ hence choose } \gamma_k \text{ to decrease the } i_{\alpha\beta} \text{ current} \end{cases} \tag{34.145}$$

The practical implementation of this switching strategy could be accomplished using three independent two-level hysteresis comparators. However, this might introduce limit cycles as only two line currents are independent. Therefore, the control laws (34.143, 34.144) can be implemented using the block diagram of Fig. 34.47a, with $d, q/\alpha, \beta$ (from Eq. (34.138)) and 1,2,3/α,β (from Eq. (34.136)) transformations and two three-level hysteretic comparators with equivalent hysteresis ε and ρ to limit the maximum switching frequency. A limiter is included to bound the i_d reference current to i_{dmax}, keeping the input line currents within a safe value. This helps to eliminate the nonminimum-phase behavior (outside sliding mode) when large transients are present, while providing short-circuit proof operation.

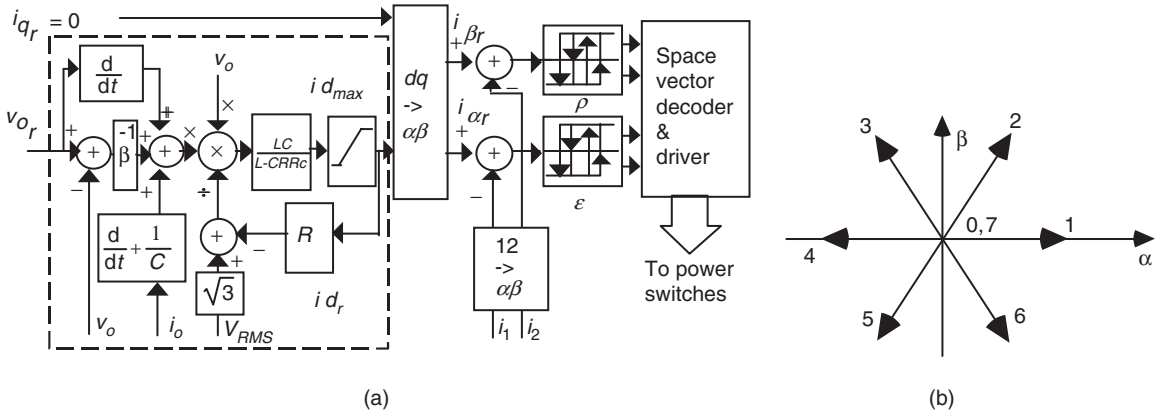


FIGURE 34.47 (a) Sliding-mode PWM controller modulator for the unity power factor three-phase PWM rectifier and (b) α, β space vector representation of the PWM bridge rectifier leg voltages.

34.3.5.12 α, β Space Vector Current Modulator

Depending on the values of γ_k, the bridge rectifier leg output voltages can assume only eight possible distinct states represented as voltage vectors in the α, β reference frame (Fig. 34.47b), for sources with isolated neutral.

With only two independent currents, two three-level hysteresis comparators, for the current errors, must be used in order to accurately select all eight available voltage vectors. Each three-level comparator can be obtained by summing the outputs of two comparators with two levels each. One of these two comparators ($\delta_{L\alpha}$, $\delta_{L\beta}$) has a wide hysteresis width and the other ($\delta_{N\alpha}$, $\delta_{N\beta}$) has a narrower hysteresis width. The hysteresis bands are represented by ε and ρ. Table 34.1 represents all possible output combinations of the resulting four two-level comparators, their sums giving the two three-level comparators (δ_α, δ_β), plus the voltage vector needed to accomplish the current tracking strategy $(i_{\alpha,\beta_r} - i_{\alpha,\beta}) = 0$ (ensuring $(i_{\alpha,\beta_r} - i_{\alpha,\beta}) \times d(i_{\alpha,\beta_r} - i_{\alpha,\beta})/dt < 0$), plus the γ_k variables and the α, β voltage components.

From the analysis of the PWM boost rectifier it is concluded that, if, for example, the voltage vector 2 is applied ($\gamma_1 = 1$, $\gamma_2 = 1$, $\gamma_3 = 0$), in boost operation, the currents i_α and i_β will both decrease. Oppositely, if the voltage vector 5 ($\gamma_1 = 0$, $\gamma_2 = 0$, $\gamma_3 = 1$) is applied, the currents i_α and i_β will both increase. Therefore, vector 2 should be selected when both i_α and i_β currents are above their respective references, that is for $\delta_\alpha = -1$, $\delta_\beta = -1$, whereas vector 5 must be chosen when both i_α and i_β currents are under their respective references, or for $\delta_\alpha = 1$, $\delta_\beta = 1$. Nearly all the outputs of Table 34.2 can be filled using this kind of reasoning.

TABLE 34.2 Two-level and three-level comparator results, showing corresponding vector choice, corresponding γ_k and vector α, β component voltages; vectors are mapped in Fig. 34.47b

$\delta_{L\alpha}$	$\delta_{N\alpha}$	$\delta_{L\beta}$	$\delta_{N\beta}$	δ_α	δ_β	**Vector**	γ_1	γ_2	γ_3	v_α	v_β
−0.5	−0.5	−0.5	−0.5	−1	−1	**2**	1	1	0	$v_o/\sqrt{6}$	$v_o/\sqrt{2}$
0.5	−0.5	−0.5	−0.5	0	−1	**2**	1	1	0	$v_o/\sqrt{6}$	$v_o/\sqrt{2}$
0.5	0.5	−0.5	−0.5	1	−1	**3**	0	1	0	$-v_o/\sqrt{6}$	$v_o/\sqrt{2}$
−0.5	0.5	−0.5	−0.5	0	−1	**3**	0	1	0	$-v_o/\sqrt{6}$	$v_o/\sqrt{2}$
−0.5	0.5	0.5	−0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
0.5	0.5	0.5	−0.5	1	0	**4**	0	1	1	$-\sqrt{2/3}v_o$	0
0.5	−0.5	0.5	−0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
−0.5	−0.5	0.5	−0.5	−1	0	**1**	1	0	0	$\sqrt{2/3}v_o$	0
−0.5	−0.5	0.5	0.5	−1	1	**6**	1	0	1	$v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
0.5	−0.5	0.5	0.5	0	1	**6**	1	0	1	$v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
0.5	0.5	0.5	0.5	1	1	**5**	0	0	1	$-v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
−0.5	0.5	0.5	0.5	0	1	**5**	0	0	1	$-v_o/\sqrt{6}$	$-v_o/\sqrt{2}$
−0.5	0.5	−0.5	0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
0.5	0.5	−0.5	0.5	1	0	**4**	0	1	1	$-\sqrt{2/3}v_o$	0
0.5	−0.5	−0.5	0.5	0	0	**0 or 7**	0 or 1	0 or 1	0 or 1	0	0
−0.5	−0.5	−0.5	0.5	−1	0	**1**	1	0	0	$\sqrt{2/3}v_o$	0

The cases where $\delta_\alpha = 0$, $\delta_\beta = -1$, the vector is selected upon the value of the i_α current error (if $\delta_{L\alpha} > 0$ and $\delta_{N\alpha} < 0$ then vector 2, if $\delta_{L\alpha} < 0$ and $\delta_{N\alpha} > 0$ then vector 3). When $\delta_\alpha = 0$, $\delta_\beta = 1$, if $\delta_{L\alpha} > 0$ and $\delta_{N\alpha} < 0$ then vector 6, else if $\delta_{L\alpha} < 0$ and $\delta_{N\alpha} > 0$ then vector 5. The vectors 0 and 7 are selected in order to minimize the switching frequency (if two of the three upper switches are on, then vector 7, otherwise vector 0). The space-vector decoder can be stored in a lookup table (or in an EPROM) whose inputs are the four two-level comparator outputs and the logic result of the operations needed to select between vectors 0 and 7.

34.3.5.13 PI Output Voltage Control of the Current-mode PWM Rectifier

Using the α, β current-mode hysteresis modulators to enforce the i_d and i_q currents to follow their reference values, i_{d_r}, i_{qr} (the values of L and C are such that the i_d and i_q currents usually exhibit a very fast dynamics compared to the slow dynamics of v_o), a first-order model (34.146) of the rectifier output voltage can be obtained from Eq. (34.73).

$$\frac{dv_o}{dt} = \left(\frac{1}{C} - \frac{RR_c}{L}\right)\left(\gamma_d i_{d_r} + \gamma_q i_{q_r}\right) - \frac{R_c\left(\gamma_d^2 + \gamma_q^2\right)}{L} v_o + \frac{R_c}{L}\left(\gamma_d v_d + \gamma_q v_q\right) - \frac{i_o}{C} - R_c\frac{di_o}{dt} \tag{34.146}$$

Assuming now a pure resistor load $R_1 = v_o/i_o$, and a mean delay T_d between the i_d current and the reference i_{d_r}, continuous transfer functions result for the i_d current ($i_d = i_{dr}(1+sT_d)^{-1}$) and for the v_o voltage ($v_o = k_A i_d/(1+sk_B)$ with k_A and k_B obtained from Eq. (34.146)). Therefore, using the same approach as Examples 34.6, 34.8, and 34.11, a linear PI regulator, with gains K_p and K_i (34.147), sampling the error between the output voltage reference v_{o_r} and the output v_o, can be designed to provide a voltage proportional (k_I) to the reference current $i_{d_r}(i_{d_r} = (K_p + K_i/s)k_I(v_{o_r} - v_o))$.

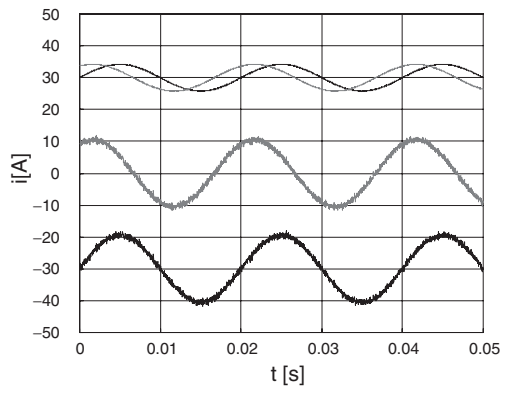
$$K_p = \frac{R_1 + R_c}{4\zeta^2 T_d R_1 K_1 \gamma_d (1/C - RR_c/L)}$$
$$K_i = \frac{\left(R_c(\gamma_d^2 + \gamma_q^2)/L\right) + (1/R_1 C)}{4\zeta^2 T_d K_1 \gamma_d (1/C - RR_c/L)} \tag{34.147}$$

These PI regulator parameters depend on the load resistance R_1, on the rectifier parameters (C, R_c, L, R), on the rectifier operating point γ_d, on the mean delay time T_d, and on the required damping factor ζ. Therefore, the expected response can only be obtained with the nominal load and input voltages, the line current dynamics depending on the K_p and K_i gains.

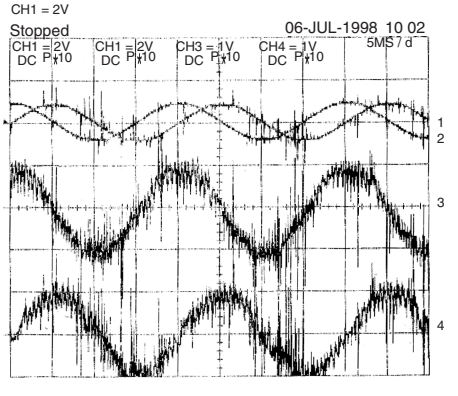
Results (Fig. 34.48) obtained with the values $V_{RMS} \approx 70\,\text{V}$, $L \approx 1.1\,\text{mH}$, $R \approx 0.1\,\Omega$, $C \approx 2000\,\mu\text{F}$ with equivalent series resistance ESR$\approx 0.1\,\Omega$ ($R_c \approx 0.1\,\Omega$), $R_1 \approx 25\,\Omega$, $R_2 \approx 12\,\Omega$, $\beta = 0.0012$, $K_p = 1.2$, $K_i = 100$, $k_I = 1$, show that the α, β space vector current modulator ensures the current tracking needed (Fig. 34.48) [17]. The v_o step response reveals a faster sliding-mode controller and the correct design of the current mode/PI controller parameters. The robustness property of the sliding-mode controlled output v_o, compared to the current mode/PI, is shown in Fig. 34.49.

EXAMPLE 34.15 Sliding-mode controllers for multilevel inverters

Diode clamped multilevel inverters (Fig. 34.50) are the converters of choice for high-voltage high-power dc/ac or ac/ac (with dc link) applications, as the active semiconductors (usually gate turn-off thyristors (GTO) or IGBT transistors) of n-level power conversion systems, must withstand only a fraction (normally $U_{cc}/(n-1)$) of the total supply voltage U_{cc}. Moreover, the output voltage of multilevel converters, being staircase-like



(a)



(b)

FIGURE 34.48 α, β space vector current modulator operation at near unity power factor: (a) simulation result ($i_{1r} + 30$; $i_{2_r} + 30$; $2\times i_1$; $2\times i_2 - 30$) and (b) experimental result ($1\rightarrow i_{1r}$, $2\rightarrow i_{2r}$ (10 A/div); $3\rightarrow i_1$, $4\rightarrow i_2$ (5 A/div)).

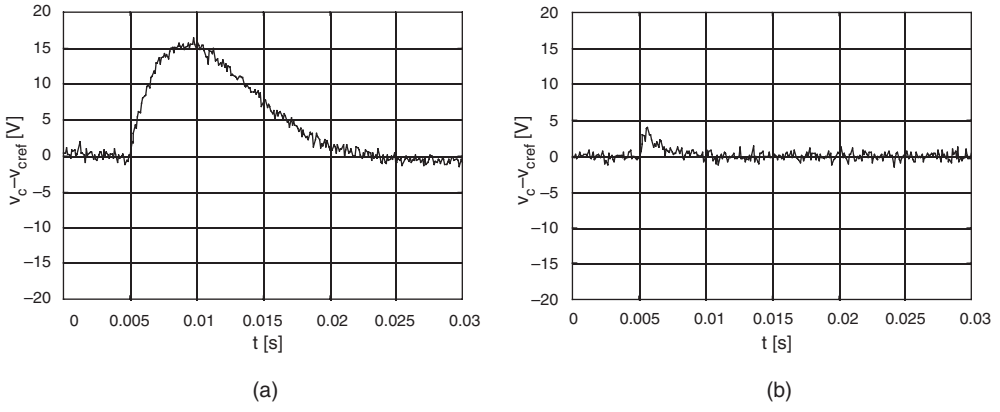


FIGURE 34.49 Transition from rectifier to inverter operation (i_o from 8 to -8 A) obtained by switching off IGBT S_a (Fig. 34.46) and using $I_a = 16$ A: (a) $v_o - v_{or}$ [v] with sliding-mode control and (b) $v_o - v_{or}$ [v] with current-mode /PI control.

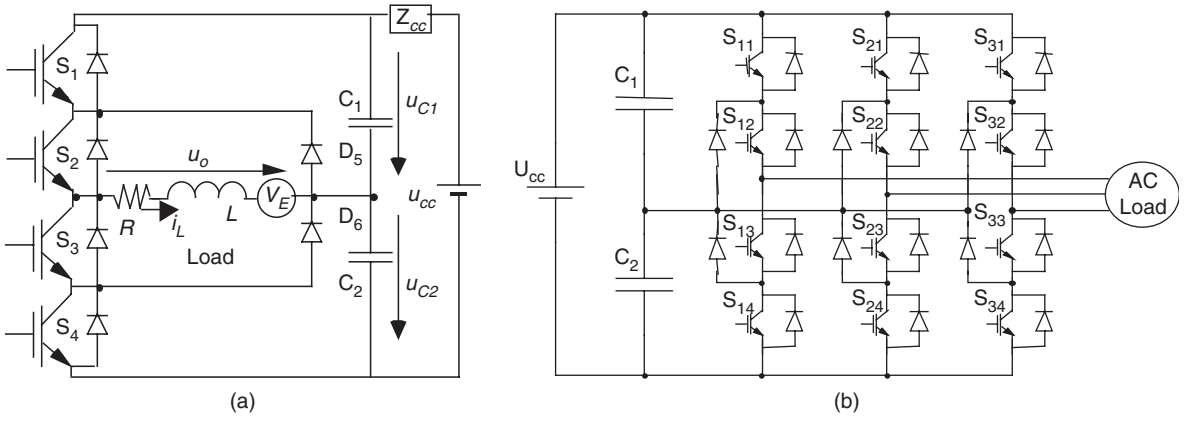


FIGURE 34.50 (a) Single-phase, neutral point clamped, three-level inverter with IGBTs and (b) three-phase, neutral-clamped, three-level inverter.

waveforms with n steps, features lower harmonic distortion compared to the two-level waveforms with the same switching frequency.

The advantages of multilevel converters are paid into the price of the capacitor supply voltage dividers (Fig. 34.51) and voltage equalization circuits, into the cost of extra power supply arrangements (Fig. 34.51c), and into increased control complexity. This example shows how to extend the two-level switching law (34.97) to n-level converters, and how to equalize the voltage of the capacitive dividers.

Considering single-phase three-level inverters (Fig. 34.50a), the open-loop control of the output voltage can be made using three-level SWPWM. The two-level modulator, seen in Example 34.9, can be easily extended (Fig. 34.52a) to generate the γ_{III} command (Fig. 34.52b) to three-level inverter legs, from the two-level γ_{II} signal, using the following relation:

$$\gamma_{III} = \gamma_{II}(m_i \sin(\omega t) - \text{sgn}(m_i \sin(\omega t))/2 - r(t)/2) - 1/2 + \text{sgn}(m_i \sin(\omega t))/2 \quad (34.148)$$

The required three-level SWPWM modulators for the output voltage synthesis seldom take into account the semiconductors and the capacitor voltage divider non-ideal characteristics. Consequently, the capacitor voltage divider tends to drift, one capacitor being overcharged, the other discharged, and an asymmetry appears in the currents of the power supply. A steady-state error in the output voltage can also be present. Sliding-mode control can provide the optimum switching timing between all the converter levels, together with robustness to supply voltage disturbances, semiconductor non-idealities, and load parameters.

A. Sliding-mode switching law For a variable-structure system where the control input $u_i(t)$ can present n levels, consider the n values of the integer variable γ, being $-(n-1)/2 \leq \gamma \leq (n-1)/2$ and $u_i(t) = \gamma U_{cc}/(n-1)$, dependent on the topology and on the conducting semiconductors. To ensure the sliding-mode manifold invariance condition (34.92) and the reaching mode behavior, the switching strategy $\gamma(t_{k+1})$

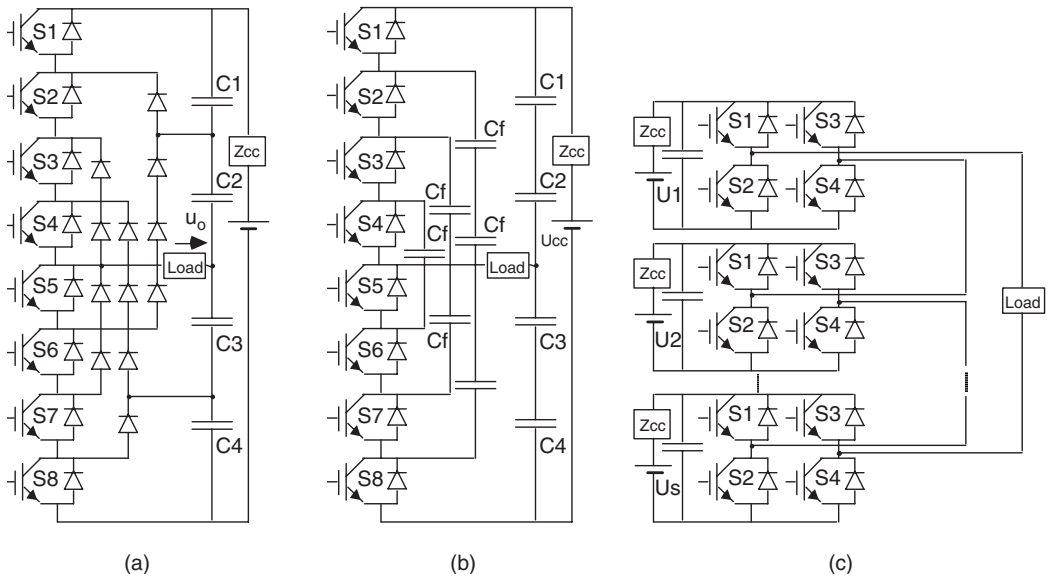


FIGURE 34.51 (a) Five-level ($n = 5$) diode clamped inverter with IGBTs; (b) five-level ($n = 5$) flying capacitor converter; and (c) multilevel converter based on cascaded full-bridge inverters.

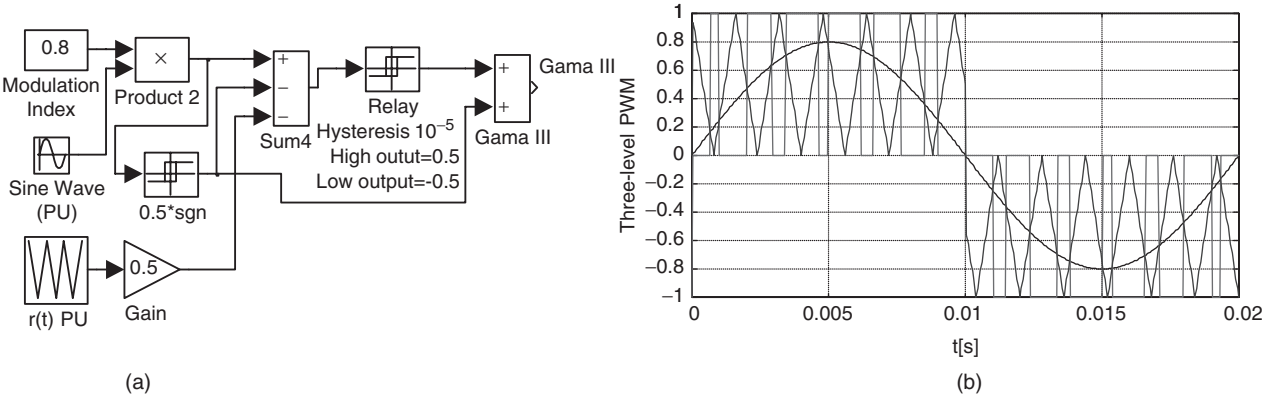


FIGURE 34.52 (a) Three-level SWPWM modulator schematic and (b) main three-level SWPWM signals.

for the time instant t_{k+1}, considering the value of $\gamma(t_k)$ must be

$$\gamma(t_{k+1}) = \begin{cases} \gamma(t_k) + 1 \text{ if } S(e_{x_i}, t) > \varepsilon \wedge \dot{S}(e_{x_i}, t) \\ \qquad\qquad > \varepsilon \wedge \gamma(t_k) < (n-1)/2 \\ \gamma(t_k) - 1 \text{ if } S(e_{x_i}, t) < -\varepsilon \wedge \dot{S}(e_{x_i}, t) \\ \qquad\qquad < -\varepsilon \wedge \gamma(t_k) > -(n-1)/2 \end{cases} \tag{34.149}$$

This switching law can be implemented as depicted in Fig. 34.53.

34.3.5.14 Control of the Output Voltage in Single-phase Multilevel Converters

To control the inverter output voltage, in closed-loop, in diode-clamped multilevel inverters with n levels and supply voltage U_{cc}, a control law similar to Eq. (34.132), $S(e_{uo}, t) = \kappa \int \left(u_{o_r} - k_v \gamma(t_k) U_{cc}/(n-1)\right) dt = 0$, is suitable.

Figure 34.54a shows the waveforms of a five-level sliding-mode controlled inverter, namely the input sinus voltage, the generated output staircase wave, and the sliding-surface instantaneous error. This error is always within a band centered around the zero value and presents zero mean value, which is not the case of sigma-delta modulators followed by n-level quantizers, where the error presents an offset mean value in each half period.

Experimental multilevel converters always show capacitor voltage unbalances (Fig. 34.54b) due to small differences between semiconductor voltage drops and circuitry offsets. To obtain capacitor voltage equalization, the voltage error $(v_{c_2} - U_{cc}/2)$ is fed back to the controller (Fig. 34.55a) to counteract the circuitry offsets. Experimental results (Fig. 34.54c)

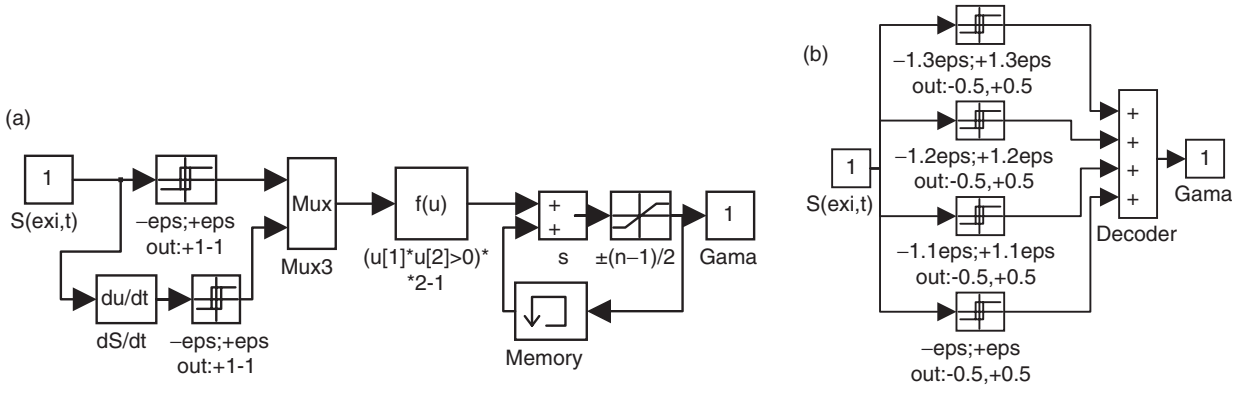


FIGURE 34.53 (a) Multilevel sliding-mode PWM modulator with n-level hysteresis comparator with quantization interval ε and (b) four hysteresis comparator implementation of a five-level switching law.

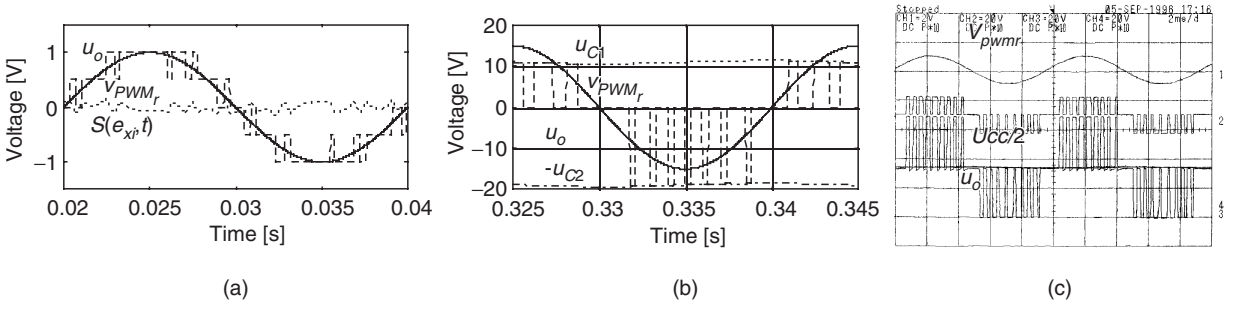


FIGURE 34.54 (a) Scaled waveforms of a five-level sliding-mode controlled single-phase converter, showing the input sinus voltage v_{PWM_r}, the generated output staircase wave u_o and the value of the sliding surface $S(e_{x_i},t)$; (b) scaled waveforms of a three-level neutral point clamped inverter showing the capacitor voltage unbalance (shown as two near flat lines touching the tips of the PWM pulses); and (c) experimental results from a laboratory prototype of a three-level single-phase power inverter with the capacitor voltage equalization described.

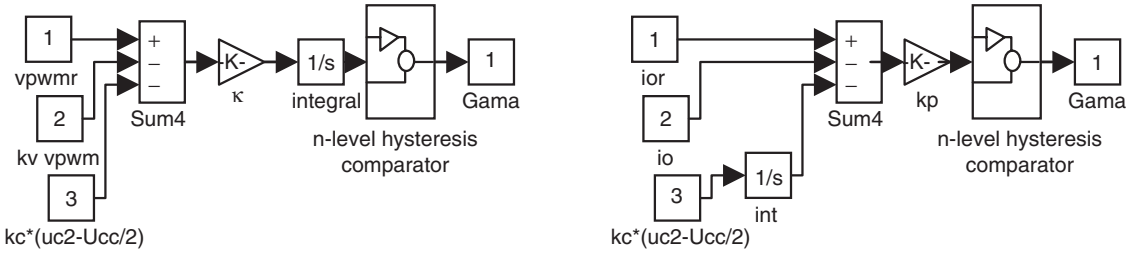


FIGURE 34.55 (a) Multilevel sliding-mode output voltage controller and PWM modulator with capacitor voltage equalization and (b) sliding-mode output current controller with capacitor voltage equalization.

clearly show the effectiveness of the correction made. The small steady-state error, between the voltages of the two capacitors, still present, could be eliminated using an integral regulator (Fig. 34.55b).

Figure 34.56 confirms the robustness of the sliding-mode controller to power supply disturbances.

34.3.5.15 Output Current Control in Single-phase Multilevel Converters

Considering an inductive load with current i_L, the control law (34.107) and the switching law of (34.159), should be used for single-phase multilevel inverters. Results obtained using the capacitor voltage equalization principle just described are shown in Fig. 34.57.

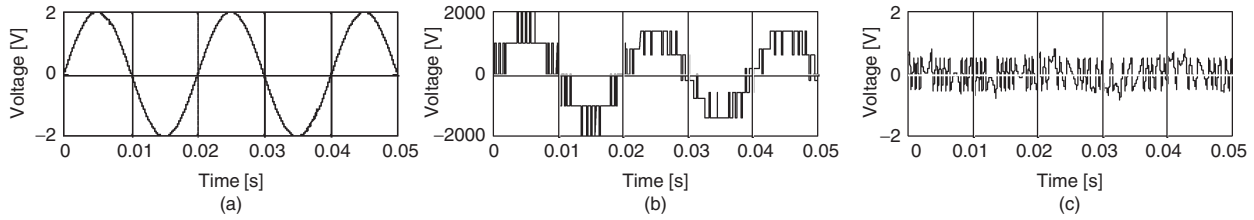


FIGURE 34.56 Simulated performance of a five-level power inverter, with a U_{cc} voltage dip (from 2 to 1.5 kV). Response to a sinusoidal wave of frequency 50 Hz: (a) v_{PWM_r} input; (b) PWM output voltage u_o; and (c) the integral of the error voltage, which is maintained close to zero.

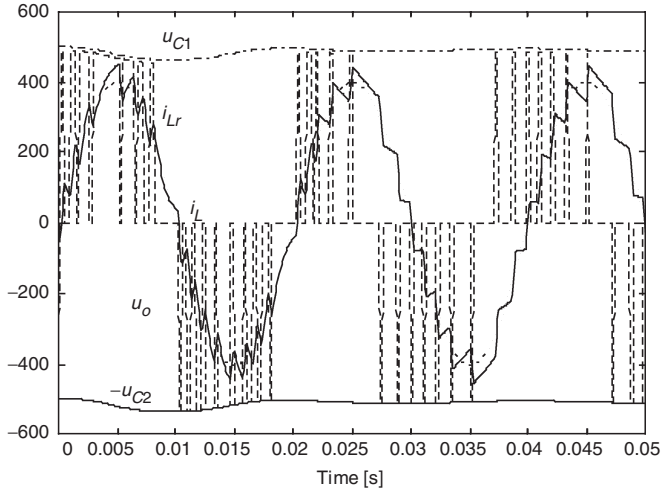


FIGURE 34.57 Operation of a three-level neutral point clamped inverter as a sinusoidal current source: Scaled waveforms of the output current sine wave reference i_{Lr}, the output current i_L, showing ripple, together with the PWM-generated voltage u_o, with nearly equal pulse heights, corresponding to the equalized dc capacitor voltages u_{C_1} and u_{C_2}.

EXAMPLE 34.16 Sliding-mode controllers for three-phase multilevel inverters

Three-phase n-level inverters (Fig. 34.58) are suitable for high-voltage, high-power dc/ac applications, such as modern high-speed railway traction drives, as the controlled turn-off semiconductors must block only a fraction (normally $U_{dc}/(n-1)$) of the total supply voltage U_{dc}.

This example presents a real-time modulator for the control of the three output voltages and capacitor voltage equalization, based on the use of sliding mode and space vectors represented in the α, β frame. Capacitor voltage equalization is done with the proper selection of redundant space vectors.

34.3.5.16 Output Voltage Control in Multilevel Converters

To guarantee the topological constraints of this converter and the correct sharing of the U_{dc} voltage by the semiconductors, the switching strategy for the k leg ($k \in \{1,2,3\}$) must ensure complementary states to switches S_{k1} and S_{k3}. The same restriction applies for S_{k2}, S_{k4}. Neglecting switching delays, dead times, on-state semiconductor voltage drops, snubber networks, and power supply variations, supposing small dead times and equal capacitor voltages $U_{C1} = U_{C2} = U_{dc}/2$, and using the time-dependent switching variable $\gamma_k(t)$, the leg output voltage U_k (Fig. 34.58) will be $U_k = \gamma_k(t)U_{dc}/2$, with

$$\gamma_k(t) = \begin{cases} 1 & \text{if } S_{k1} \wedge S_{k2} \text{ are ON } \wedge S_{k3} \wedge S_{k4} \text{ are OFF} \\ 0 & \text{if } S_{k2} \wedge S_{k3} \text{ are ON } \wedge S_{k1} \wedge S_{k4} \text{ are OFF} \\ -1 & \text{if } S_{k3} \wedge S_{k4} \text{ are ON } \wedge S_{k1} \wedge S_{k2} \text{ are OFF} \end{cases} \tag{34.150}$$

The converter output voltages U_{Sk} of vector $\mathbf{U}_S$ can be expressed

$$\mathbf{U}_S = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \gamma_3 \end{bmatrix} \frac{U_{dc}}{2} \tag{34.151}$$

The application of the Concordia transformation $U_{S1,2,3} = [\mathbf{C}]\ U_{S\alpha,\beta,o}$ (Eq. (34.152) to Eq. (34.151))

$$\begin{bmatrix} U_{S1} \\ U_{S2} \\ U_{S3} \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} U_{S\alpha} \\ U_{S\beta} \\ U_{So} \end{bmatrix} \tag{34.152}$$

gives the output voltage vector in the α, β coordinates $\mathbf{U}_{S_{\alpha,\beta}}$:

$$\mathbf{U}_{S_{\alpha,\beta}} = \begin{bmatrix} U_{S\alpha} \\ U_{S\beta} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \Gamma_1 \\ \Gamma_2 \\ \Gamma_3 \end{bmatrix}$$

$$\frac{U_{dc}}{2} = \begin{bmatrix} \Gamma_\alpha \\ \Gamma_\beta \end{bmatrix} \frac{U_{dc}}{2} \tag{34.153}$$

where

$$\Gamma_1 = \frac{2}{3}\gamma_1 - \frac{1}{3}\gamma_2 - \frac{1}{3}\gamma_3; \quad \Gamma_2 = \frac{2}{3}\gamma_2 - \frac{1}{3}\gamma_3 - \frac{1}{3}\gamma_1;$$

$$\Gamma_3 = \frac{2}{3}\gamma_3 - \frac{1}{3}\gamma_1 - \frac{1}{3}\gamma_2 \tag{34.154}$$

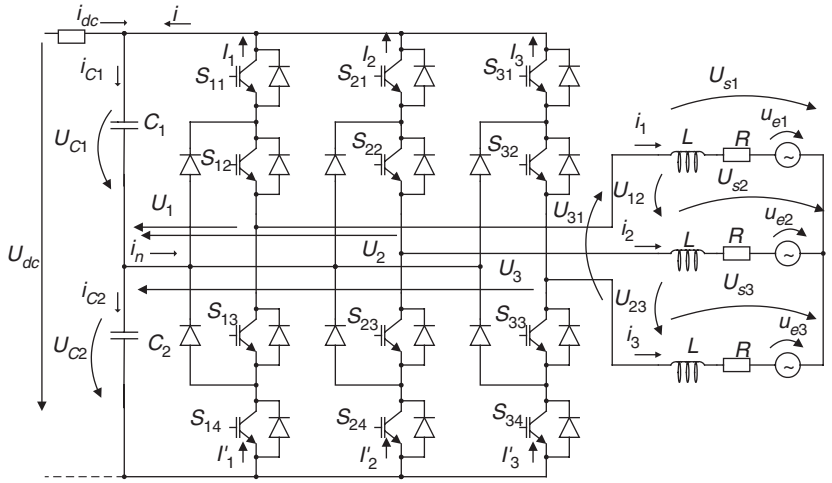


FIGURE 34.58 Three-phase, neutral point clamped, three-level inverter with IGBTs.

The output voltage vector in the α, β coordinates $\mathbf{U}_{S_{\alpha,\beta}}$ is discontinuous. A suitable state variable for this output can be its average value $\bar{\mathbf{U}}_{S_{\alpha,\beta}}$ during one switching period:

$$\bar{\mathbf{U}}_{S_{\alpha,\beta}} = \frac{1}{T}\int_0^T \mathbf{U}_{S_{\alpha,\beta}}dt = \frac{1}{T}\int_0^T \Gamma_{\alpha,\beta}\frac{U_{dc}}{2}dt \tag{34.155}$$

The controllable canonical form is

$$\frac{d}{dt}\bar{\mathbf{U}}_{S_{\alpha,\beta}} = \frac{\mathbf{U}_{S_{\alpha,\beta}}}{T} = \frac{\Gamma_{\alpha,\beta}}{T}\frac{U_{dc}}{2} \tag{34.156}$$

Considering the control goal $\bar{\mathbf{U}}_{S_{\alpha,\beta}} = \bar{\mathbf{U}}_{S_{\alpha,\beta_{ref}}}$ and Eq. (34.91), the sliding surface is

$$\mathbf{S}(\mathbf{e}_{\alpha,\beta},t) = \sum_{o=1}^{\varphi}\mathbf{k}_{\alpha\beta_o}\mathbf{e}_{\alpha,\beta_o} = \mathbf{k}_{\alpha,\beta_1}\mathbf{e}_{\alpha,\beta_1} = \mathbf{k}_{\alpha,\beta_1}\left(\bar{\mathbf{U}}_{S_{\alpha,\beta_{ref}}} - \bar{\mathbf{U}}_{S_{\alpha,\beta}}\right)$$

$$= \frac{\mathbf{k}_{\alpha,\beta}}{T}\int_0^T \left(\mathbf{U}_{S_{\alpha,\beta ref}} - \mathbf{U}_{S_{\alpha,\beta}}\right)dt = 0 \tag{34.157}$$

To ensure reaching mode behavior, and sliding-mode stability (34.92), as the first derivative of Eq. (34.157), $\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t)$, is

$$\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta}, t) = \frac{\mathbf{k}_{\alpha,\beta}}{T}\left(\mathbf{U}_{S_{\alpha,\beta ref}} - \mathbf{U}_{S_{\alpha,\beta}}\right) \tag{34.158}$$

The switching law is

$$\begin{aligned}&\mathbf{S}(\mathbf{e}_{\alpha,\beta},t) > 0 \Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t) < 0 \Rightarrow \mathbf{U}_{S_{\alpha,\beta}} > \mathbf{U}_{S_{\alpha,\beta ref}}\\ &\mathbf{S}(\mathbf{e}_{\alpha,\beta},t) < 0 \Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t) > 0 \Rightarrow \mathbf{U}_{S_{\alpha,\beta}} < \mathbf{U}_{S_{\alpha,\beta ref}}\end{aligned} \tag{34.159}$$

This switching strategy must select the proper values of $\mathbf{U}_{S_{\alpha,\beta}}$ from the available outputs. As each inverter leg (Fig. 34.58) can deliver one of the three possible output voltages ($U_{dc}/2$; 0; $-U_{dc}/2$), all the 27 possible output voltage vectors listed in Table 34.3 can be represented in the α, β frame of Fig. 34.59 (in per units, 1 p.u. = U_{dc}). There are nine different levels for the α space vector component and only five for the β component. However, considering any particular value of α (or β) component, there are at most five levels available in the remaining orthogonal component. From the load viewpoint, the 27 space vectors of Table 34.3 define only 19 distinct space positions (Fig. 34.59).

To select one of these 19 positions from the control law (34.157) and the switching law of Eq. (34.159), two five-level hysteretic comparators (Fig. 34.53b) must be used ($5^2 = 25$). Their outputs are the integer variables λ_α and λ_β, denoted $\lambda_{\alpha,\beta}$ ($\lambda_\alpha, \lambda_\beta \in \{-2; -1; 0; 1; 2\}$) corresponding to the five selectable levels of Γ_α and Γ_β. Considering the sliding-mode stability, $\lambda_{\alpha,\beta}$, at time step $j+1$, is given by Eq. (34.160), knowing their previous values at step j. This means that the output level is increased (decreased) if the error and its derivative are both positive (negative), provided the maximum (minimum) output level is not exceeded.

$$\begin{cases}(\lambda_{\alpha,\beta})_{j+1} = (\lambda_{\alpha,\beta})_j + 1 & \text{if } \mathbf{S}(\mathbf{e}_{\alpha,\beta},t) > \varepsilon \wedge \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t) > \varepsilon \wedge (\lambda_{\alpha,\beta})_j < 2\\ (\lambda_{\alpha,\beta})_{j+1} = (\lambda_{\alpha,\beta})_j - 1 & \text{if } \mathbf{S}(\mathbf{e}_{\alpha,\beta},t) < -\varepsilon \wedge \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t) < -\varepsilon \wedge (\lambda_{\alpha,\beta})_j > -2\end{cases} \tag{34.160}$$

The available space vectors must be chosen not only to reduce the mean output voltage errors, but also to guarantee transitions only between the adjacent levels, to minimize the capacitor voltage unbalance, to minimize the switching frequency, to observe minimum on or off times if applicable, and to equally stress all the semiconductors.

TABLE 34.3 Vectors of the three-phase three-level converter, switching variables γ_k, switch states s_{kj}, and the corresponding output voltages, line to neutral point, line-to-line, and α, β components in per units

Vector	γ_1	γ_2	γ_3	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	S_{31}	S_{32}	S_{33}	S_{34}	U_1	U_2	U_3	U_{12}	U_{23}	U_{31}	$U_{s\alpha}/U_{dc}$	$U_{s\beta}/U_{dc}$
1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	0	0	0	0.00	0.00
2	1	1	0	1	1	0	0	1	1	0	0	0	1	1	0	$U_{dc}/2$	$U_{dc}/2$	0	0	$U_{dc}/2$	$-U_{dc}/2$	0.20	0.35
3	1	1	−1	1	1	0	0	1	1	0	0	0	0	1	1	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	U_{dc}	$-U_{dc}$	0.41	0.71
4	1	0	−1	1	1	0	0	0	1	1	0	0	0	1	1	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	0.61	0.35
5	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	$U_{dc}/2$	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	0.41	0.00
6	1	0	1	1	1	0	0	0	1	1	0	1	1	0	0	$U_{dc}/2$	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	0.20	−0.35
7	1	−1	1	1	1	0	0	0	0	1	1	1	1	0	0	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	U_{dc}	$-U_{dc}$	0	0.41	−0.71
8	1	−1	0	1	1	0	0	0	0	1	1	0	1	1	0	$U_{dc}/2$	$-U_{dc}/2$	0	U_{dc}	$-U_{dc}/2$	$-U_{dc}/2$	0.61	−0.35
9	1	−1	−1	1	1	0	0	0	0	1	1	0	0	1	1	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	0	$-U_{dc}$	0.82	0.00
10	0	−1	−1	0	1	1	0	0	0	1	1	0	0	1	1	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}/2$	0.41	0.00
11	0	−1	0	0	1	1	0	0	0	1	1	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	0	0.20	−0.35
12	0	−1	1	0	1	1	0	0	0	1	1	1	1	0	0	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	$U_{dc}/2$	0.00	−0.71
13	0	0	1	0	1	1	0	0	1	1	0	1	1	0	0	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	−0.20	−0.35
14	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0.00	0.00
15	0	0	−1	0	1	1	0	0	1	1	0	0	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	0.20	0.35
16	0	1	−1	0	1	1	0	1	1	0	0	0	0	1	1	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	$-U_{dc}/2$	0.00	0.71
17	0	1	0	0	1	1	0	1	1	0	0	0	1	1	0	0	$U_{dc}/2$	0	$-U_{dc}/2$	$U_{dc}/2$	0	−0.20	0.35
18	0	1	1	0	1	1	0	1	1	0	0	1	1	0	0	0	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	0	$U_{dc}/2$	−0.41	0.00
19	−1	1	1	0	0	1	1	1	1	0	0	1	1	0	0	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}$	0	U_{dc}	−0.82	0.00
20	−1	1	0	0	0	1	1	1	1	0	0	0	1	1	0	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}$	U_{dc}	$U_{dc}/2$	−0.61	0.35
21	−1	1	−1	0	0	1	1	1	1	0	0	0	0	1	1	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}$	U_{dc}	0	−0.41	0.71
22	−1	0	−1	0	0	1	1	0	1	1	0	0	0	1	1	$-U_{dc}/2$	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	−0.20	0.35
23	−1	0	0	0	0	1	1	0	1	1	0	0	1	1	0	$-U_{dc}/2$	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	−0.41	0.00
24	−1	0	1	0	0	1	1	0	1	1	0	1	1	0	0	$-U_{dc}/2$	0	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	U_{dc}	−0.61	−0.35
25	−1	−1	1	0	0	1	1	0	0	1	1	1	1	0	0	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	0	$-U_{dc}/2$	U_{dc}	−0.41	−0.71
26	−1	−1	0	0	0	1	1	0	0	1	1	0	1	1	0	$-U_{dc}/2$	$-U_{dc}/2$	0	0	$-U_{dc}/2$	$U_{dc}/2$	−0.20	−0.35
27	−1	−1	−1	0	0	1	1	0	0	1	1	0	0	1	1	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	0	0	0	0.00	0.00

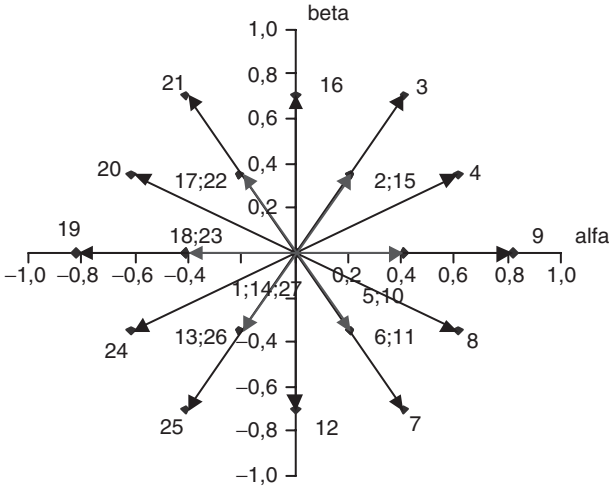


FIGURE 34.59 Output voltage vectors (1 to 27) of three-phase, neutral-clamped three-level inverters, in the α, β frame.

Using Eq. (34.160) and the control laws $S(\mathbf{e}_{\alpha,\beta,t})$ Eq. (34.157), Tables 34.4 and 34.5 can be used to choose the correct voltage vector in order to ensure stability, output voltage tracking, and DC capacitor voltage equalization. The vector with α, β components corresponding to the levels of the

TABLE 34.4 Switching table to be used if $(U_{C1} - U_{C2}) > \varepsilon_{eU}$ in the inverter mode, or $(U_{C1} - U_{C2}) < -\varepsilon_{eU}$ in the regenerative mode, showing vector selection upon the variables $\lambda_\alpha, \lambda_\beta$

$\lambda_\beta \backslash \lambda_\alpha$	**−2**	**−1**	**0**	**1**	**2**
−2	25	25	12	7	7
−1	24	13	13;6	6	8
0	19	18	1;14;27	5	9
1	20	17	17;2	2	4
2	21	21	16	3	3

TABLE 34.5 Switching table to be used if $(U_{C1} - U_{C2}) > \varepsilon_{eU}$ in the regenerative mode, or $(U_{C1} - U_{C2}) < -\varepsilon_{eU}$ in the inverter mode, showing vector selection upon the variables $\lambda_\alpha, \lambda_\beta$

$\lambda_\beta/\lambda_\alpha$	**−2**	**−1**	**0**	**1**	**2**
−2	25	25	12	7	7
−1	24	26	26;11	11	8
0	19	23	1;14;27	10	9
1	20	22	22;15	15	4
2	21	21	16	3	3

pair $\lambda_\beta, \lambda_\alpha$ is selected, provided that the adjacent transitions on inverter legs are obtained. If there is no directly corresponding vector, then the nearest vector guaranteeing adjacent transitions is selected. If a zero vector must be applied, then, one of the three zero vectors (1, 14, 27) is selected, to minimize the switching frequency. If more than one vector is the nearest, then, one of them is selected to equalize the capacitor voltages, as shown next.

34.3.5.17 DC Capacitor Voltage Equalization

The discrete values of $\lambda_{\alpha,\beta}$ allow 25 different combinations. As only 19 are distinct from the load viewpoint, the extra ones can be used to select vectors that are able to equalize the capacitor voltages ($U_{C1} = U_{C2} = U_{dc}/2$).

Considering the control goal $U_{C1} = U_{C2}$, since the first derivatives of U_{C1} and U_{C2} Eq. (34.161) directly depend on the $\gamma_k(t)$ control inputs, from Eq. (34.91) the sliding surface is given by Eq. (34.162), where k_U is a positive gain.

$$\frac{d}{dt}\begin{bmatrix} U_{C1} \\ U_{C2} \end{bmatrix} = \begin{bmatrix} -\frac{\gamma_1(1+\gamma_1)}{2C_1} & -\frac{\gamma_2(1+\gamma_2)}{2C_1} & -\frac{\gamma_3(1+\gamma_3)}{2C_1} & \frac{1}{C_1} \\ -\frac{\gamma_1(1-\gamma_1)}{2C_2} & -\frac{\gamma_2(1-\gamma_2)}{2C_2} & -\frac{\gamma_3(1-\gamma_3)}{2C_2} & \frac{1}{C_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_{dc} \end{bmatrix} \tag{34.161}$$

$$S(e_{Uc}, t) = k_U e_{Uc}(t) = k_U (U_{C1} - U_{C2}) = 0 \tag{34.162}$$

The first derivative of $U_{C1} - U_{C2}$ (the sliding surface) is (Fig. 34.58 with $C_1 = C_2 = C$):

$$\frac{d}{dt} e_{Uc} = \frac{i_{C1}}{C_1} - \frac{i_{C2}}{C_2} = \frac{i_n}{C} = \frac{(\gamma_3^2 - \gamma_1^2) i_1 + (\gamma_3^2 - \gamma_2^2) i_2}{C} \tag{34.163}$$

To ensure reaching mode behavior and sliding-mode stability, from Eq. (34.92), considering a small enough $e_{Uc}(t)$ error, ε_{eU}, the switching law is

$$\begin{aligned} S(e_{Uc}, t) > \varepsilon_{eU} &\Rightarrow \dot{S}(e_{Uc}, t) < 0 \Rightarrow i_n < 0 \\ S(e_{Uc}, t) < -\varepsilon_{eU} &\Rightarrow \dot{S}(e_{Uc}, t) > 0 \Rightarrow i_n > 0 \end{aligned} \tag{34.164}$$

From circuit analysis, it can be seen that vectors {2, 5, 6, 13, 17, 18} result in the discharge of capacitor C_1, if the converter operates in inverter mode, or in the charge of C_1, if the converter operates in boost-rectifier (regenerative) mode. Similar reasoning can be applied for vectors {10, 11, 15, 22, 23, 26} and capacitor C_2, since this vector set give i_n currents with opposite sign relatively to the set {2, 5, 6, 13, 17, 18}. Therefore, considering the vector $[\Upsilon_1, \Upsilon_2] = [(\gamma_1^2 - \gamma_3^2), (\gamma_2^2 - \gamma_3^2)]$ the switching law is:

IF $(U_{C1} - U_{C2}) > \varepsilon_{eU}$

THEN { IF the candidate vector from {2, 5, 6, 13, 17, 18} gives $(\Upsilon_1 i_1 + \Upsilon_2 i_2) > 0$, THEN choose the vector according to $\lambda_{\alpha,\beta}$ on Table 34.4; ELSE, the candidate vector of {10, 11, 15, 22, 23, 26} gives $(\Upsilon_1 i_1 + \Upsilon_2 i_2) > 0$, the vector being chosen according to $\lambda_{\alpha,\beta}$ from (table 34.5)

IF $(U_{C1} - U_{C2}) < -\varepsilon_{eU}$

THEN { IF the candidate vector from {2, 5, 6, 13, 17, 18} gives $(\Upsilon_1 i_1 + \Upsilon_2 i_2) < 0$, THEN choose the vector according to $\lambda_{\alpha,\beta}$ on Table 34.4; ELSE, the candidate vector of {10, 11, 15, 22, 23, 26} gives $(\Upsilon_1 i_1 + \Upsilon_2 i_2) < 0$, the vector being chosen according to $\lambda_{\alpha,\beta}$ from (table 34.5)

For example, consider the case where $U_{C1} > U_{C2} + \varepsilon_{eU}$. Then, the capacitor C_2 must be charged and Table 34.4 must be used if the multilevel inverter is operating in the inverter mode or Table 34.5 for the regenerative mode. Additionally, when using Table 34.4, if $\lambda_\alpha = -1$ and $\lambda_\beta = -1$, then vector 13 should be used.

Experimental results shown in Fig. 34.61 were obtained with a low-power, scaled down laboratory prototype (150 V, 3 kW) of a three-level inverter (Fig. 34.60), controlled by two four-level comparators, plus described capacitor voltage equalizing procedures and EPROM-based lookup Tables 34.3–34.5. Transistors IGBT (MG25Q2YS40) were switched at frequencies near 4 kHz, with neutral clamp diodes 40HFL, $C_1 \approx C_2 \approx$ 20 mF. The load was mainly inductive (3×10 mH, 2 Ω).

The inverter number of levels (three for the phase voltage and five for the line voltage), together with the adjacent transitions of inverter legs between levels, are shown in Fig. 34.61a and, in detail, in Fig. 34.62a.

The performance of the capacitor voltage equalizing strategy is shown in Fig. 34.62b, where the reference current of phase 1 and the output current of phase 3, together with the power supply voltage ($U_{dc} \approx 100$ V) and the voltage of capacitor $C_2(U_{C2})$, can be seen. It can be noted that the U_{C2} voltage is nearly half of the supply voltage. Therefore, the capacitor voltages are nearly equal. Furthermore, it can be stated that without this voltage equalization procedure, the three-level inverter operates only during a brief transient, during which one of the capacitor voltages vanishes to nearly zero volt and the other is overcharged to the supply voltage. Figure 34.61b shows the harmonic spectrum of the output voltages, where the harmonics due to the switching frequency (≈4.5 kHz) and the fundamental harmonic can be seen.

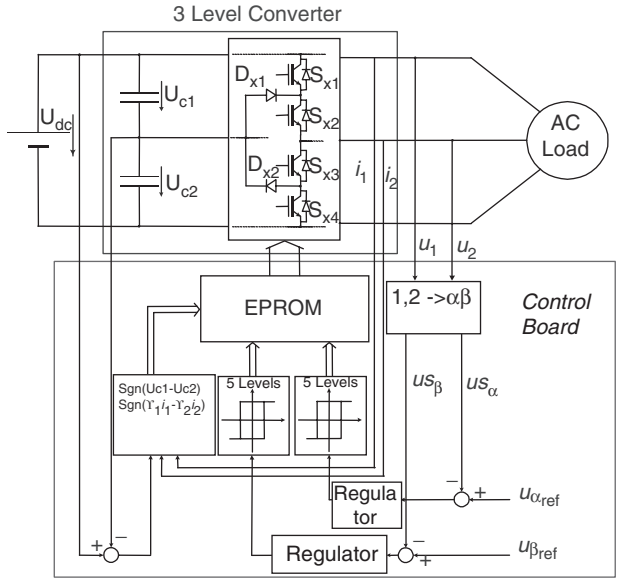


FIGURE 34.60 Block diagram of the multilevel converter and control board.

34.3.5.18 On-line Output Current Control in Multilevel Inverters

Considering a standard inductive balanced load (R, L) with electromotive force (u) and isolated neutral, the converter output currents i_k can be expressed

$$U_{Sk} = Ri_k + L\frac{di_k}{dt} + u_{ek} \tag{34.165}$$

Now analyzing the circuit of Fig. 34.58, the multilevel converter switched state-space model can be obtained:

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = -\begin{bmatrix} R/L & 0 & 0 \\ 0 & R/L & 0 \\ 0 & 0 & R/L \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} - \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/L \end{bmatrix}\begin{bmatrix} u_{e1} \\ u_{e2} \\ u_{e3} \end{bmatrix} + \begin{bmatrix} \Gamma_1/L \\ \Gamma_2/L \\ \Gamma_3/L \end{bmatrix}\frac{U_{dc}}{2} \tag{34.166}$$

The application of the Concordia matrix Eq. (34.152) to Eq. (34.166), reduces the number of the new model equations (Eq. (34.167)) to two, since an isolated neutral is assumed.

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = -\begin{bmatrix} R/L & 0 \\ 0 & R/L \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} - \begin{bmatrix} 1/L & 0 \\ 0 & 1/L \end{bmatrix}\begin{bmatrix} u_{e\alpha} \\ u_{e\beta} \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 1/L \end{bmatrix}\begin{bmatrix} U_{S\alpha} \\ U_{S\beta} \end{bmatrix} \tag{34.167}$$

The model Eq. (34.167) of this multiple-input multiple-output system (MIMO) with outputs i_α, i_β reveals the control inputs $U_{S\alpha}$, $U_{S\beta}$, dependent on the control variables $\gamma_k(t)$.

From Eqs. (34.167) and (34.91), the two sliding surfaces $\mathbf{S}(\mathbf{e}_{\alpha,\beta},t)$ are

$$\mathbf{S}(\mathbf{e}_{\alpha,\beta},t) = \mathbf{k}_{\alpha,\beta}(\mathbf{i}_{\alpha,\beta ref} - \mathbf{i}_{\alpha,\beta}) = \mathbf{k}_{\alpha,\beta}\mathbf{e}_{\alpha,\beta} = 0 \tag{34.168}$$

The first derivatives of Eq. (34.167), denoted $\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta,t})$, are

$$\begin{aligned}\dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t) &= \mathbf{k}_{\alpha,\beta}(\dot{\mathbf{i}}_{\alpha,\beta ref} - \dot{\mathbf{i}}_{\alpha,\beta}) \\ &= \mathbf{k}_{\alpha,\beta}\left[\dot{\mathbf{i}}_{\alpha,\beta ref} + \mathbf{R}\mathbf{L}^{-1}\mathbf{i}_{\alpha,\beta} + \mathbf{u}_{e\alpha,\beta}\mathbf{L}^{-1} - \mathbf{U}_{\mathbf{S}\alpha,\beta}\mathbf{L}^{-1}\right]\end{aligned} \tag{34.169}$$

Therefore, the switching law is

$$\begin{aligned}&\mathbf{S}(\mathbf{e}_{\alpha,\beta},t) > 0 \Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t) < 0 \Rightarrow \mathbf{U}_{S_{\alpha,\beta}} > \mathbf{L}\dot{\mathbf{i}}_{\alpha,\beta ref} + \mathbf{R}\mathbf{i}_{\alpha,\beta} + \mathbf{u}_{e\alpha,\beta} \\ &\mathbf{S}(\mathbf{e}_{\alpha,\beta},t) < 0 \Rightarrow \dot{\mathbf{S}}(\mathbf{e}_{\alpha,\beta},t) > 0 \Rightarrow \mathbf{U}_{S_{\alpha,\beta}} < \mathbf{L}\dot{\mathbf{i}}_{\alpha,\beta ref} + \mathbf{R}\mathbf{i}_{\alpha,\beta} + \mathbf{u}_{\mathbf{e}\alpha,\beta}\end{aligned} \tag{34.170}$$

These switching laws are implemented using the same α, β vector modulator described above in this example.

Figure 34.63a shows the experimental results. The multilevel converter and proposed control behavior are obtained for step inputs (4 to 2A) in the amplitude of the sinus references with frequency near 52 Hz ($U_{dc} \approx 150$ V). Observe the tracking ability, the fast transient response, and the balanced

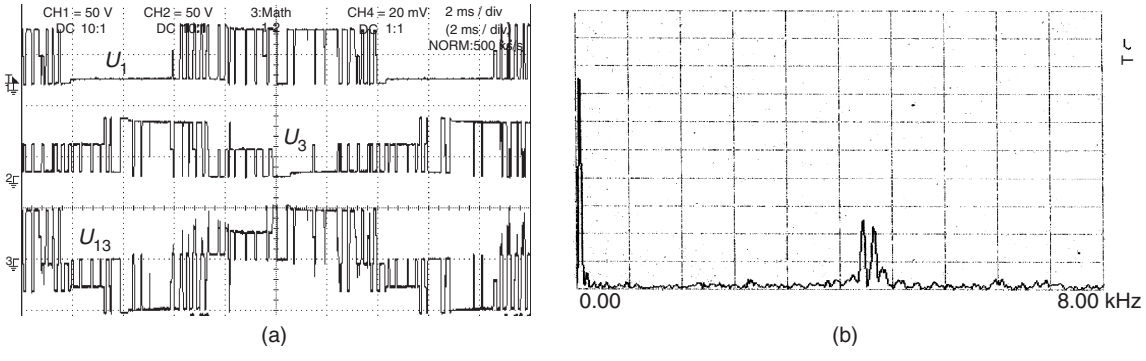


FIGURE 34.61 (a) Experimental results showing phase and line voltages and (b) harmonic spectrum of output voltages.

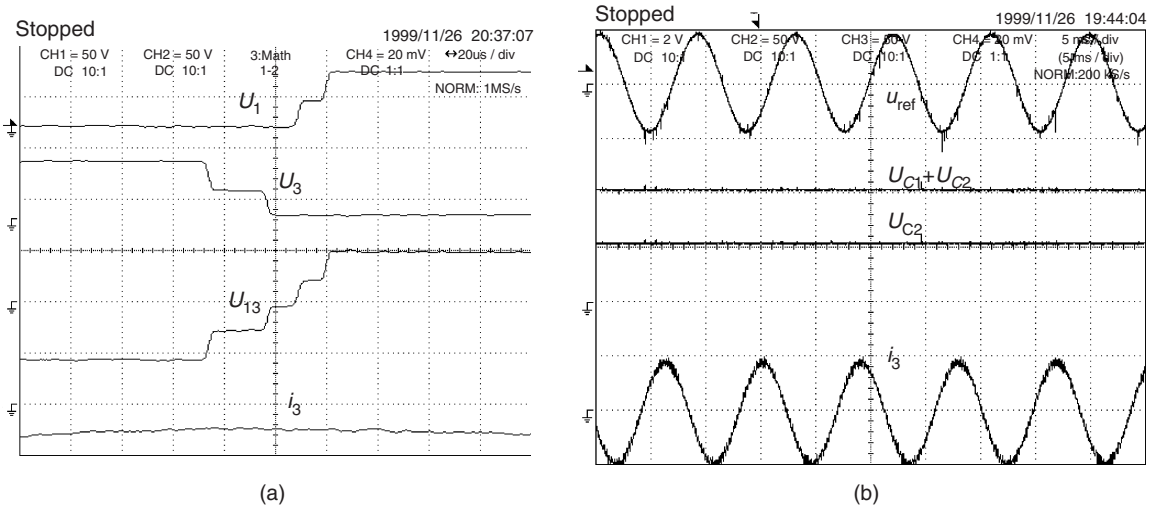


FIGURE 34.62 Experimental results showing (a) the transitions between adjacent voltage levels (50 V/div; time 20 μs/div) and (b) performance of the capacitor voltage equalizing strategy; from top trace to bottom: 1 is the voltage reference input; 2 is the power supply voltage; 3 is the mid-point capacitor voltage, which is maintained close to $U_{dc}/2$; 4 is the output current of phase 3(2 A/div; 50 V/div; 5 ms/div).

three-phase currents. Figure 34.63b shows almost the same test (step response from 2 to 4 A at the same frequency), but now the power supply is set at 50 V and the inductive load was unbalanced (±30% on resistor value). The response remains virtually the same, with tracking ability, almost no current distortions due to dead times or semiconductor voltage drops. These results confirm experimentally that the designed controllers are robust concerning these nonidealities.

EXAMPLE 34.17 Sliding-mode vector controllers for matrix converters

Matrix converters are all silicon ac/ac switching converters, able to provide variable amplitude almost sinusoidal output voltages, almost sinusoidal input currents, and controllable input power factor [18]. They seem to be very attractive to use in ac drives speed control as well as in applications related to power-quality enhancement. The lack of an intermediate energy storage link, their

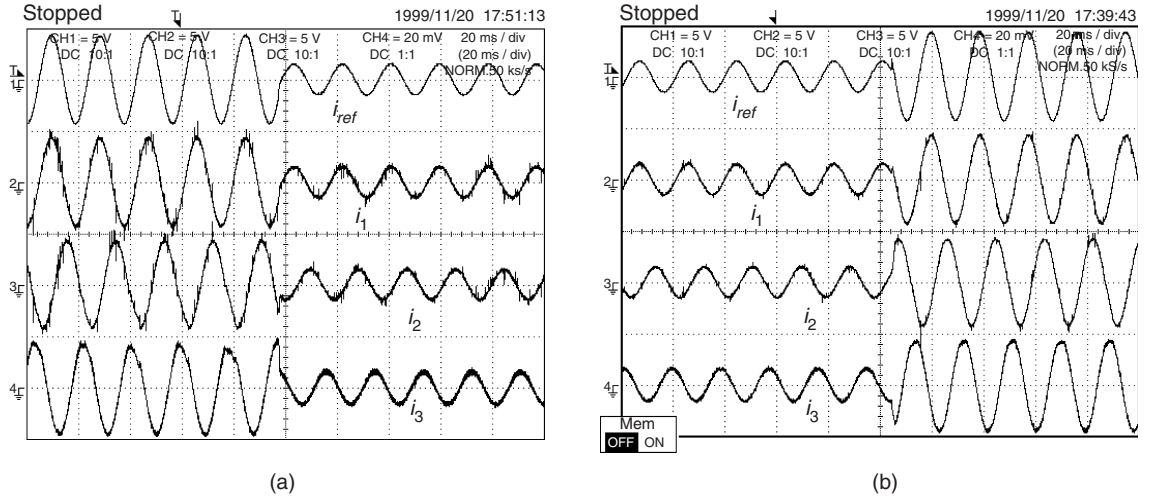


FIGURE 34.63 Step response of the current control method: (a) step from 4 to 2 A. Traces show the reference current for phase 1 and the three output currents with 150 V power supply (5 A/div; time scale 20 ms/div) and (b) step from 2 to 4 A in the reference amplitude at 52 Hz. Traces show the reference current for phase 1 and the three output currents with 50 V power supply.

main advantage, implies an input/output coupling which increases the control complexity.

This example presents the design of sliding-mode controllers considering the switched state-space model of the matrix converter (nine bidirectional power switches), including the three-phase input filter and the output load (Fig. 34.64).

34.3.5.19 Output Voltage Control

Ideal three-phase matrix converters are obtained by assembling nine bidirectional switches, with the turn-off capability, to allow the connection of each one of the input phases to any one of the output phases (Fig. 34.64). The states of these switches are usually represented as a nine-element matrix **S** (Eq. (34.171)), in which each matrix element, $S_{kj}\, k, j \in \{1, 2, 3\}$, has two possible states: $S_{kj} = 1$ if the switch is closed (ON) and $S_{kj} = 0$ if it is open (OFF). Only 27 switching combinations are possible (Table 34.6), as a result of the topological constraints (the input phases should never be short-circuited and the output inductive currents should never be interrupted), which implies that the sum of all the S_{kj} of each one of the matrix, k rows must always equal 1 (Eq. (34.171)).

$$S = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \quad \sum_{j=1}^{3} s_{kj} = 1 \quad k, j \in \{1, 2, 3\} \tag{34.171}$$

Based on the matrix **S**, the output phase v_A, v_B, v_C and line voltages v_{AB}, v_{BC}, v_{CA}, can be expressed in terms of the input phase voltages v_a, v_b, v_c. The input currents i_a, i_b, i_c can be expressed as a function of the output currents i_A, i_B, i_C:

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \mathbf{S} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix};$$

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = \begin{bmatrix} S_{11} - S_{21} & S_{12} - S_{22} & S_{13} - S_{23} \\ S_{21} - S_{31} & S_{22} - S_{32} & S_{23} - S_{33} \\ S_{31} - S_{11} & S_{32} - S_{12} & S_{33} - S_{13} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix};$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \mathbf{S}^T \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{34.172}$$

The application of the Concordia transformation $[X_{\alpha,\beta,0}]^T = \mathbf{C}^T [X_{a,b,c}]^T$ to Eq. (34.172) results in the output voltage vector:

$$v_{o_{\alpha\beta}} = \begin{bmatrix} v_{o_\alpha} \\ v_{o_\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \times \begin{bmatrix} S_{11} - S_{21} & S_{12} - S_{22} & S_{13} - S_{23} \\ S_{21} - S_{31} & S_{22} - S_{32} & S_{23} - S_{33} \\ S_{31} - S_{11} & S_{32} - S_{12} & S_{33} - S_{13} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \rho_{v_{\alpha\alpha}} & \rho_{v_{\alpha\beta}} \\ \rho_{v_{\beta\alpha}} & \rho_{v_{\beta\beta}} \end{bmatrix} \begin{bmatrix} v_{c_\alpha} \\ v_{c_\beta} \end{bmatrix} \tag{34.173}$$

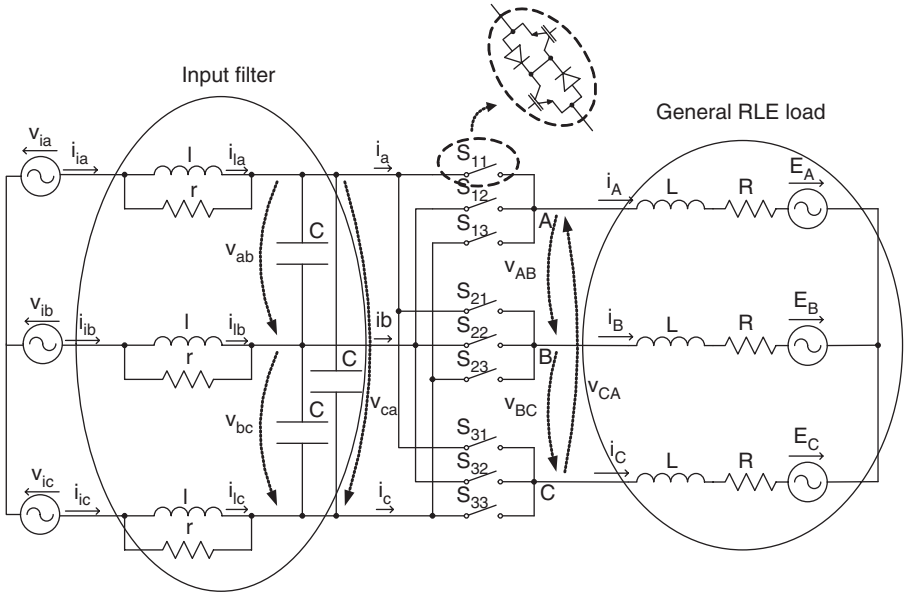


FIGURE 34.64 AC/AC matrix converter with input *lCr* filter.

TABLE 34.6 Switching combinations and output voltage/input current state-space vectors

Group	Name	A	B	C	v_{AB}	v_{BC}	v_{CA}	i_a	i_b	i_c	V_o	δ_o	I_i	μ_i
I	1g	a	b	c	v_{ab}	v_{bc}	v_{ca}	i_A	i_B	i_C	v_i	δ_i	i_o	μ_o
	2g	a	c	b	$-v_{ca}$	$-v_{bc}$	$-v_{ab}$	i_A	i_C	i_B	$-v_i$	$-\delta_i+4\pi/3$	i_o	$-\mu_o$
	3g	b	a	c	$-v_{ab}$	$-v_{ca}$	$-v_{bc}$	i_B	i_A	i_C	$-v_i$	$-\delta_i$	i_o	$-\mu_o+2\pi/3$
	4g	b	c	a	v_{bc}	v_{ca}	v_{ab}	i_C	i_A	i_B	v_i	$\delta_i+4\pi/3$	i_o	$\mu_o+2\pi/3$
	5g	c	a	b	v_{ca}	v_{ab}	v_{bc}	i_B	i_C	i_A	v_i	$\delta_i+2\pi/3$	i_o	$\mu_o+4\pi/3$
	6g	c	b	a	$-v_{bc}$	$-v_{ab}$	$-v_{ca}$	i_C	i_B	i_A	$-v_i$	$-\delta_i+2\pi/3$	i_o	$-\mu_o+4\pi/3$
II	+1	a	b	b	v_{ab}	0	$-v_{ab}$	i_A	$-i_A$	0	$2/\sqrt{3}v_{ab}$	$\pi/6$	$2/\sqrt{3}i_A$	$-\pi/6$
	−1	b	a	a	$-v_{ab}$	0	v_{ab}	$-i_A$	i_A	0	$-2/\sqrt{3}v_{ab}$	$\pi/6$	$-2/\sqrt{3}i_A$	$-\pi/6$
	+2	b	c	c	v_{bc}	0	$-v_{bc}$	0	i_A	$-i_A$	$2/\sqrt{3}v_{bc}$	$\pi/6$	$2/\sqrt{3}i_A$	$\pi/2$
	−2	c	b	b	$-v_{bc}$	0	v_{bc}	0	$-i_A$	i_A	$-2/\sqrt{3}v_{bc}$	$\pi/6$	$-2/\sqrt{3}i_A$	$\pi/2$
	+3	c	a	a	v_{ca}	0	$-v_{ca}$	$-i_A$	0	i_A	$2/\sqrt{3}v_{ca}$	$\pi/6$	$2/\sqrt{3}i_A$	$7\pi/6$
	−3	a	c	c	$-v_{ca}$	0	v_{ca}	i_A	0	$-i_A$	$-2/\sqrt{3}v_{ca}$	$\pi/6$	$-2/\sqrt{3}i_A$	$7\pi/6$
	+4	b	a	b	$-v_{ab}$	v_{ab}	0	i_B	$-i_B$	0	$2/\sqrt{3}v_{ab}$	$5\pi/6$	$2/\sqrt{3}i_B$	$-\pi/6$
	−4	a	b	a	v_{ab}	$-v_{ab}$	0	$-i_B$	i_B	0	$-2/\sqrt{3}v_{ab}$	$5\pi/6$	$-2/\sqrt{3}i_B$	$-\pi/6$
	+5	c	b	c	$-v_{bc}$	v_{bc}	0	0	i_B	$-i_B$	$2/\sqrt{3}v_{bc}$	$5\pi/6$	$2/\sqrt{3}i_B$	$\pi/2$
	−5	b	c	b	v_{bc}	$-v_{bc}$	0	0	$-i_B$	i_B	$-2/\sqrt{3}v_{bc}$	$5\pi/6$	$-2/\sqrt{3}i_B$	$\pi/2$
	+6	a	c	a	$-v_{ca}$	v_{ca}	0	$-i_B$	0	i_B	$2/\sqrt{3}v_{ca}$	$5\pi/6$	$2/\sqrt{3}i_B$	$7\pi/6$
	−6	c	a	c	v_{ca}	$-v_{ca}$	0	i_B	0	$-i_B$	$-2/\sqrt{3}v_{ca}$	$5\pi/6$	$-2/\sqrt{3}i_B$	$7\pi/6$
	+7	b	b	a	0	v_{ab}	v_{ab}	i_C	$-i_C$	0	$2/\sqrt{3}v_{ab}$	$3\pi/2$	$2/\sqrt{3}i_C$	$-\pi/6$
	−7	a	a	b	0	v_{ab}	v_{ab}	$-i_C$	i_C	0	$-2/\sqrt{3}v_{ab}$	$3\pi/2$	$-2/\sqrt{3}i_C$	$-\pi/6$
	+8	c	c	b	0	$-v_{bc}$	v_{bc}	0	i_C	$-i_C$	$2/\sqrt{3}v_{bc}$	$3\pi/2$	$2/\sqrt{3}i_C$	$\pi/2$
	−8	b	b	c	0	v_{bc}	$-v_{bc}$	0	$-i_C$	i_C	$-2/\sqrt{3}v_{bc}$	$3\pi/2$	$-2/\sqrt{3}i_C$	$\pi/2$
	+9	a	a	c	0	$-v_{ca}$	v_{ca}	$-i_C$	0	i_C	$2/\sqrt{3}v_{ca}$	$3\pi/2$	$2/\sqrt{3}i_C$	$7\pi/6$
	−9	c	c	a	0	v_{ca}	$-v_{ca}$	i_C	0	$-i_C$	$-2/\sqrt{3}v_{ca}$	$3\pi/2$	$-2/\sqrt{3}i_C$	$7\pi/6$
III	z_a	a	a	a	0	0	0	0	0	0	0	-	0	-
	z_b	b	b	b	0	0	0	0	0	0	0	-	0	-
	z_c	c	c	c	0	0	0	0	0	0	0	-	0	-

where $v_{c\alpha\beta}$ is the input filter capacitor voltage and $\rho_{v_{\alpha\alpha}}, \rho_{v_{\alpha\beta}}, \rho_{v_{\beta\alpha}}, \rho_{v_{\beta\beta}}$ are functions of the ON/OFF state of the nine S_{kj} switches:

$$\begin{bmatrix} \rho_{v_{\alpha\alpha}} & \rho_{v_{\alpha\beta}} \\ \rho_{v_{\beta\alpha}} & \rho_{v_{\beta\beta}} \end{bmatrix} = \begin{bmatrix} 1/2(S_{11}-S_{21}-S_{12}+S_{22}) & \sqrt{3}/2(S_{11}-S_{21}+S_{12}-S_{22}) \\ 1/2\sqrt{3}(S_{11}+S_{21}-2S_{31}-S_{12}-S_{22}+2S_{32}) & 1/2(S_{11}+S_{21}-2S_{31}+S_{12}+S_{22}-2S_{32}) \end{bmatrix} \tag{34.174}$$

The average value $\overline{v_{o_{\alpha,\beta}}}$ of the output voltage vector, in $\alpha\beta$ coordinates, during one switching period is the output variable to be controlled (since $v_{o_{\alpha,\beta}}$ is discontinuous).

$$\overline{v_{o_{\alpha\beta}}} = \frac{1}{T_s}\int_{nT_s}^{(n+1)T_s} v_{o_{\alpha\beta}}\,dt \tag{34.175}$$

Considering the control goal $\overline{v_{o_{\alpha\beta}}} = \overline{v_{o_{\alpha\beta_{ref}}}}$, the sliding surface $S(e_{\alpha\beta}, t)$ ($k_{\alpha\beta} > 0$) is:

$$S(e_{\alpha\beta}, t) = \frac{k_{\alpha\beta}}{T}\int_0^T (v_{o_{\alpha\beta_{ref}}} - v_{o_{\alpha\beta}})dt = 0 \tag{34.176}$$

The first derivative of Eq. (34.176) is:

$$\dot{S}(e_{\alpha\beta}, t) = k_\alpha(v_{o_{\alpha\beta_{ref}}} - v_{o_{\alpha\beta}}) \tag{34.177}$$

As the sliding-mode stability is guaranteed if $S_{\alpha\beta}(e_{\alpha\beta}, t)\,\dot{S}_{\alpha\beta}(e_{\alpha\beta}, t) < 0$, the criterion to choose the state-space vectors is:

$$\begin{aligned} &S_{\alpha\beta}(e_{\alpha\beta}, t) < 0 \Rightarrow \dot{S}_{\alpha\beta}(e_{\alpha\beta}, t) > 0 \Rightarrow v_{o_{\alpha\beta}} < v_{o_{\alpha\beta_{ref}}} \\ &S_{\alpha\beta}(e_{\alpha\beta}, t) > 0 \Rightarrow \dot{S}_{\alpha\beta}(e_{\alpha\beta}, t) < 0 \Rightarrow v_{o_{\alpha\beta}} > v_{o_{\alpha\beta_{ref}}} \end{aligned} \tag{34.178}$$

This implies that the sliding mode is reached only when the vector applied to the converter has the desired amplitude and angle.

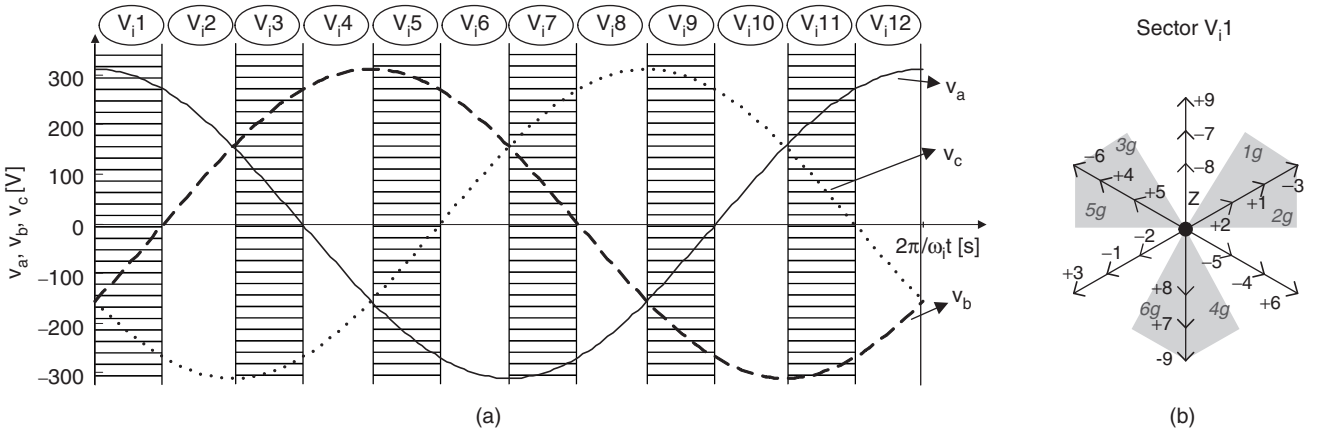


FIGURE 34.65 (a) Input voltages and their corresponding sector and (b) representation of the output voltage state-space vectors when the input voltages are located at sector V_i1.

According to Table 34.6, the 6 vectors of group I have fixed amplitude but time varying phase, the 18 vectors of group II have variable amplitude and vectors of group III are null. Therefore, from the load viewpoint, the 18 highest amplitude vectors (6 vectors from group I and 12 vectors from group II) and one null vector are suitable to guarantee the sliding-mode stability.

Therefore, if two three-level comparators ($C_{\alpha\beta} \in \{-1, 0, 1\}$) are used to quantize the deviations of Eq. (34.178) from zero, the nine output voltage error combinations (3^3) are not enough to guarantee the choice of all the 19 available vectors. The extra vectors may be used to control the input power factor. As an example, if the output voltage error is quantized as $C_\alpha = 1$, $C_\beta = 1$, at sector V_i1 (Fig. 34.65), the vectors -3, $+1$, or 1g might be used to control the output voltage. The final choice would depend on the input current error.

34.3.5.20 Input Power Factor Control

Assuming that the source is a balanced sinusoidal three-phase voltage supply with frequency ω_i, the switched state-space model equations of the converter input filter is obtained in abc coordinates.

$$\begin{cases} \frac{di_{l_a}}{dt} = \frac{1}{3l} v_{bc} + \frac{2}{3l} v_{ca} + \frac{1}{l} v_{i_a} \\ \frac{di_{l_b}}{dt} = -\frac{2}{3l} v_{bc} - \frac{1}{3l} v_{ca} + \frac{1}{l} v_{i_b} \\ \frac{dv_{bc}}{dt} = \frac{1}{3C} i_{l_a} + \frac{2}{3C} i_{l_b} - \frac{1}{3Cr} v_{bc} + \frac{1}{3Cr} v_{i_a} + \frac{2}{3Cr} v_{i_b} \\ \qquad -\frac{1}{3C}(S_{11} - S_{31} + 2S_{12} - S_{32})\, i_A \\ \qquad -\frac{1}{3C}(S_{21} - S_{31} + 2S_{22} - S_{32})\, i_B \\ \frac{dv_{ca}}{dt} = -\frac{2}{3C} i_{l_a} - \frac{1}{3C} i_{l_b} - \frac{1}{3Cr} v_{ca} - \frac{2}{3Cr} v_{i_a} - \frac{1}{3Cr} v_{i_b} \\ \qquad +\frac{1}{3C}(2S_{11} - 2S_{31} + S_{12} - S_{32})\, i_A \\ \qquad +\frac{1}{3C}(2S_{21} - 2S_{31} + S_{22} - S_{32})\, i_B \end{cases} \tag{34.179}$$

To control the input power factor, a reference frame synchronous with one of the input voltages v_{i_a}, may be used applying the Blondel–Park transformation to the matrix converter switched state-space model (Eq. (34.179)), where ($\rho_{i_{dd}}, \rho_{i_{dq}}, \rho_{i_{qd}}, \rho_{i_{qq}}$ are functions of the ON/OFF states of the nine S_{kj} switches):

$$\begin{cases} \frac{di_{l_d}}{dt} = \omega_i i_{l_q} - \frac{1}{2l} v_{c_d} - \frac{1}{2\sqrt{3}l} v_{c_q} + \frac{1}{l} v_{i_q} \\ \frac{di_{l_q}}{dt} = -\omega_i i_{l_d} + \frac{1}{2\sqrt{3}l} v_{c_d} - \frac{1}{2l} v_{c_q} + \frac{1}{l} v_{i_q} \\ \frac{dv_{c_d}}{dt} = \frac{1}{2C} i_{l_d} - \frac{1}{2\sqrt{3}C} i_{l_q} - \frac{1}{3Cr} v_{c_d} + \omega_i v_{cq} + \frac{-\rho_{i_{dd}} + \left(\rho_{i_{qd}}/\sqrt{3}\right)}{2C} i_{o_d} \\ \qquad + \frac{-\rho_{i_{dq}} + \left(\rho_{i_{qq}}/\sqrt{3}\right)}{2C} i_{o_q} + \frac{1}{2Cr} v_{i_d} - \frac{1}{2\sqrt{3}Cr} v_{i_q} \\ \frac{dv_{c_q}}{dt} = \frac{1}{2\sqrt{3}C} i_{l_d} + \frac{1}{2C} i_{l_q} - \omega_i v_{cd} - \frac{1}{3Cr} v_{c_q} + \frac{-\left(\rho_{i_{dd}}/\sqrt{3}\right) - \rho_{i_{qd}}}{2C} i_{o_d} \\ \qquad + \frac{-\left(\rho_{i_{dq}}/\sqrt{3}\right) - \rho_{i_{qq}}}{2C} i_{o_q} + \frac{1}{2\sqrt{3}Cr} v_{i_d} + \frac{1}{2Cr} v_{i_q} \end{cases} \tag{34.180}$$

As a consequence, neglecting ripples, all the input variables become time-invariant, allowing a better understanding of the sliding-mode controller design, as well as the choice of the most adequate state-space vector. Using this state-space model, the input i_{i_d} and i_{i_q} currents are:

$$\begin{cases} i_{i_d} = i_{l_d} + \frac{l}{r}\left(\frac{di_{l_d}}{dt} - \omega i_{l_q}\right) \\ i_{i_q} = i_{l_q} + \frac{l}{r}\left(\frac{di_{l_q}}{dt} + \omega i_{l_d}\right) \end{cases} \Leftrightarrow \begin{cases} i_{i_d} = i_{l_d} - \frac{1}{2r} v_{c_d} - \frac{1}{2\sqrt{3}r} v_{c_q} + \frac{1}{r} v_{i_d} \\ i_{i_q} = i_{l_q} + \frac{1}{2\sqrt{3}r} v_{c_d} - \frac{1}{2r} v_{c_q} + \frac{1}{r} v_{i_q} \end{cases} \tag{34.181}$$

The input power factor controller should consider the input–output power constraint (Eq. (34.182)) (the converter losses and ripples are neglected), obtained as a function of the input and output voltages and currents (the input

voltage v_{iq} is equal to zero in the chosen dq rotating frame). The choice of one output voltage vector automatically defines the instantaneous value of the input $i_{i_d}(t)$ current.

$$v_{i_d} i_{i_d} \approx \frac{1}{3}\left(\frac{\sqrt{3}}{2} v_{o_d} + \frac{1}{2} v_{o_q}\right) i_{o_d} + \frac{1}{3}\left(-\frac{1}{2} v_{o_d} + \frac{\sqrt{3}}{2} v_{o_q}\right) i_{o_q} \tag{34.182}$$

Therefore, only the sliding surface associated to the $i_{i_q}(t)$ current is needed, expressed as a function of the system state variables and based on the state-space model determined in Eq. (34.180):

$$\begin{cases} \frac{di_{i_q}}{dt} = -\omega i_{l_d} + \frac{1}{3Cr} i_{l_q} + \left(-\frac{1}{6\sqrt{3}Cr^2} + \frac{\omega}{2r}\right) v_{c_d} \\ \quad + \left(\frac{1}{6Cr^2} + \frac{\omega}{2\sqrt{3}r}\right) v_{c_q} + \frac{1}{2\sqrt{3}l} v_{c_d} - \frac{1}{2l} v_{c_q} \\ \quad + \frac{1}{3Cr}\left(\rho_{i_{qd}} i_{o_d} + \rho_{i_{qq}} i_{o_q}\right) \frac{1}{r}\frac{dv_{i_q}}{dt} - \frac{1}{3Cr^2} v_{i_q} + \frac{1}{l} v_{i_q} \end{cases} \tag{34.183}$$

As the derivative of the input i_{i_q} current depends directly on the control variables $\rho_{i_{qd}}$, $\rho_{i_{qq}}$, the sliding function $S_{i_q}(e_{i_q}, t)$ will depend only on the input current error $e_{i_q} = i_{i_{qref}} - i_{i_q}$.

$$S_{i_q}(e_{i_q}, t) = k_{i_q}\left(i_{i_{qref}} - i_{i_q}\right) \tag{34.184}$$

As the sliding-mode stability is guaranteed if $S_{\alpha\beta}(e_{\alpha\beta}, t)\, \dot{S}_{\alpha\beta}(e_{\alpha\beta}, t) < 0$, the criterion to choose the state-space vectors is:

$$\begin{aligned} &S_{i_q}(e_{i_q},\ t) > 0 \Rightarrow \dot{S}_{i_q}(e_{i_q},\ t) < 0 \Rightarrow \frac{di_q}{dt} > \frac{di_{q_{ref}}}{dt} \Rightarrow i_{i_q} \uparrow \\ &S_{i_q}(e_{i_q},\ t) < 0 \Rightarrow \dot{S}_{i_q}(e_{i_q},\ t) > 0 \Rightarrow \frac{di_q}{dt} < \frac{di_{q_{ref}}}{dt} \Rightarrow i_{i_q} \downarrow \end{aligned} \tag{34.185}$$

Also, to choose the adequate input current vector it is necessary: (a) to know the location of the output currents, as the input currents depend on the output currents location (Table 34.6); (b) to know the dq frame location. As in the chosen frame (synchronous with the v_{i_a} input voltage), the dq-axis location depends on the v_{i_a} input voltage location, the sign of the input current vector i_{i_q} component can be determined knowing the location of the input voltages and the location of the output currents (Fig. 34.66).

Considering the previous example, at sector V_i1 (Fig. 34.65), for an error of $C_\alpha = 1$ and $C_\beta = 1$, vectors -3, $+1$ or 1g might be used to control the output voltage. When compared, at sector I_o1 (Fig. 34.66b), these three vectors have positive i_d components and, as a result, will have a similar effect on the input i_d current. However, they have a different effect on the i_q current: vector -3 has a positive i_q component, vector $+1$ has a negative i_q component and vector 1g has a nearly zero i_q component. As a result, if the output voltage errors are $C_\alpha = 1$ and $C_\beta = 1$, at sectors V_i1 and I_o1, vector -3 should be chosen if the input current error is quantized as $C_{iq} = 1$ (Fig. 34.66b), vector $+1$ should be chosen if the input current error is quantized as $C_{iq} = -1$ and if the input current error is $C_{iq} = 0$, vector 1g or -3 might be used.

When the output voltage errors are quantized as zero $C_{\alpha\beta} = 0$, the null vectors of group III should be used only if the input current error is $C_{iq} = 0$. Otherwise (being $C_{i_q} \neq 0$), the lowest amplitude voltage vectors ($\{+2, -8, +5, -2, +8, -5\}$ at sector V_i1 at Fig. 34.65b), that were not used to control the output voltages, might be chosen to control the input i_q current as these vectors may have a strong influence on the input i_q current component (Fig. 34.66b).

To choose one of these six vectors, only the vectors located as near as possible to the output voltages sector (Fig. 34.67) are chosen (to minimize the output voltage ripple), and a five level comparator is enough. As a result, there will be $9 \times 5 = 45$ error combinations to select 27 space vectors. Therefore, the same vector may have to be used for more than one error combination.

With this reasoning, it is possible to obtain Table 34.7 for sector V_i1, I_o1, and V_o1 and generalize it for all the other sectors.

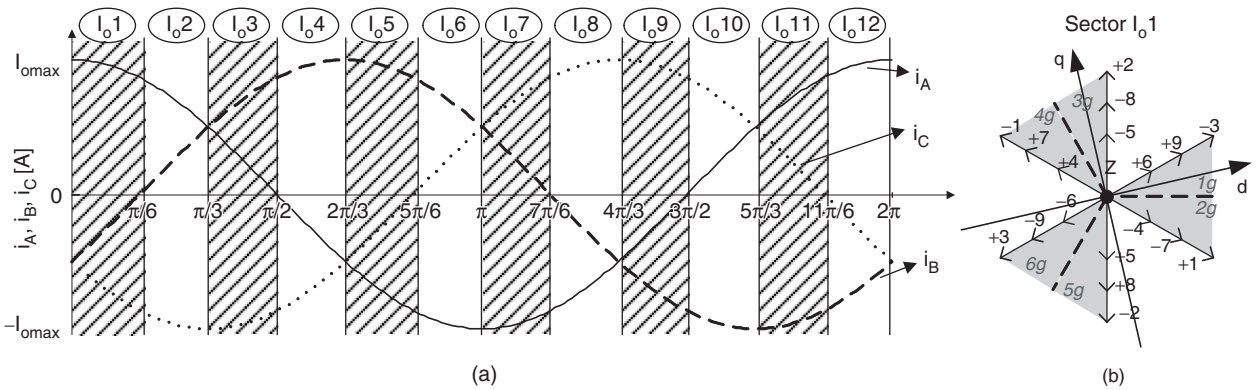


FIGURE 34.66 (a) Output currents and their corresponding sector and (b) representation of input current state-space vectors, when the output currents are located at sector I_o1. The dq-axis is represented considering that the input voltages are located in zone $\mathbf{V_i}1$.

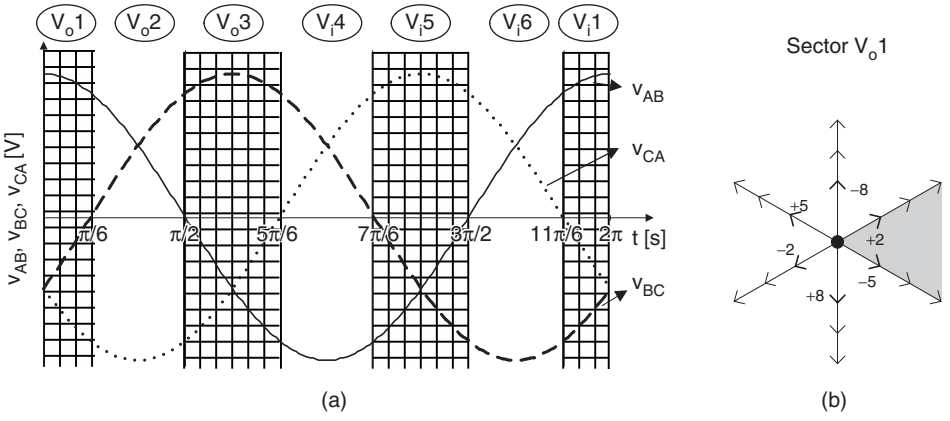


FIGURE 34.67 (a) Output voltages and their corresponding sector and (b) representation of the lowest amplitude output voltage vectors, when the input voltages are located at sector V_o1.

TABLE 34.7 State-space vectors choice at sector V_i1, I_o1, and V_o1

		C_{iq}				
C_α	C_β	**−2**	**−1**	**0**	**1**	**2**
−1	**−1**	+3	+3	+3	−1	−1
−1	**0**	5g	+3	−6	−1	−1
−1	**1**	−6	−6	−6	+4	3g
0	**−1**	6g	−9	−9	+7	4g
0	**0**	+8	+8	0	−5	2
0	**1**	−7	−7	+9	+9	+9
1	**−1**	−4	−4	+6	+6	+6
1	**0**	+1	+1	+6	−3	−3
1	**1**	+1	+1	1g	−3	−3

The experimental results shown in (Fig. 34.68) were obtained with a low-power prototype (1 kW), with two three-level comparators and one five-level comparator, associated to an EPROM lookup table. The transistors IGBT were switched at frequencies near 10 kHz.

The results show the response to a step on the output voltage reference (Fig. 34.68a) and on the input reference current (Fig. 34.68b), for a three-phase output load (R = 7 Ω, L = 15 mH), with $k_{\alpha\beta}$ = 100 and k_{iq} = 2. These results show that the matrix converter may operate with a near unity input power factor (Fig. 34.68a – f_o = 20 Hz), or with lead/lag power factor (Fig. 34.68b), guaranteeing very low ripple on the output currents, a good tracking capability and fast transient response times.

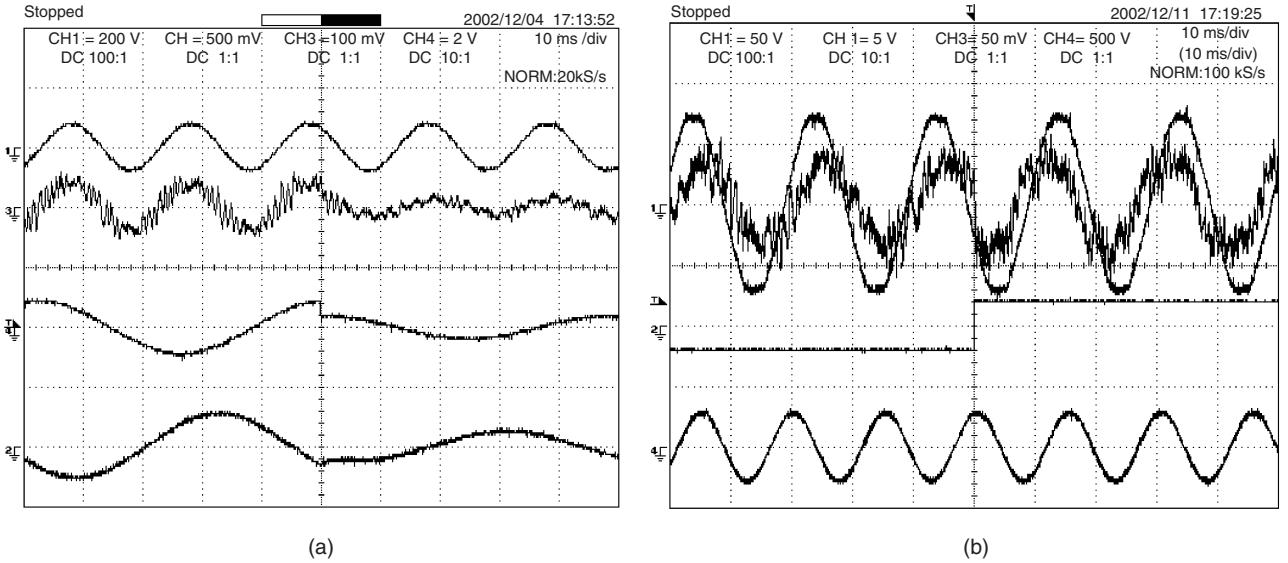


FIGURE 34.68 Dynamic responses obtained with a three-phase load: (a) output reference voltage step (R = 7 Ω, L = 15 mH, f_o = 20 Hz): input voltage $v_{i_a}(t)$ (CH1), input current $i_{i_a}(t)$ (CH3), output reference voltage $v_{BC_{ref}}(t)$ (CH4), and output current $i_A(t)$ (CH2) and (b) input reference current $i_{i_{qref}}(t)$ step: input voltage $v_{i_a}(t)$ (CH1), input current $i_{i_a}(t)$ (CH3), input reference current $i_{i_{qref}}(t)$ (CH2), and output current $i_A(t)$ (CH4).

34.4 Fuzzy Logic Control of Switching Converters

34.4.1 Introduction

Fuzzy logic control is a heuristic approach that easily embeds the knowledge and key elements of human thinking in the design of nonlinear controllers [19–21]. Qualitative and heuristic considerations, which cannot be handled by conventional control theory, can be used for control purposes in a systematic form, and applying fuzzy control concepts [22]. Fuzzy logic control does not need an accurate mathematical model, can work with imprecise inputs, can handle nonlinearity, and can present disturbance insensitivity greater than the most nonlinear controllers. Fuzzy logic controllers usually outperform other controllers in complex, nonlinear, or undefined systems for which a good practical knowledge exists.

Fuzzy logic controllers are based on fuzzy sets, i.e. classes of objects in which the transition from membership to nonmembership is smooth rather than abrupt. Therefore, boundaries of fuzzy sets can be vague and ambiguous, making them useful for approximation models.

The first step in the fuzzy controller synthesis procedure is to define the input and output variables of the fuzzy controller. This is done accordingly with the expected function of the controller. There are no general rules to select those variables, although typically the variables chosen are the states of the controlled system, their errors, error variation and/or error accumulation. In switching power converters, the fuzzy controller input variables are commonly the output voltage or current error, and/or the variation or accumulation of this error. The output variables $u(k)$ of the fuzzy controller can define the converter duty cycle (Fig. 34.60), or a reference current to be applied in an inner current-mode PI or a sliding-mode controller.

The fuzzy controller rules are usually formulated in linguistic terms. Thus, the use of linguistic variables and fuzzy sets implies the fuzzification procedure, i.e. the mapping of the input variables into suitable linguistics values.

Rule evaluation or decision-making infers, using an inference engine, the fuzzy control action from the knowledge of the fuzzy rules and the linguistic variable definition.

The output of a fuzzy controller is a fuzzy set, and thus it is necessary to perform a defuzzification procedure, i.e. the conversion of the inferred fuzzy result to a nonfuzzy (crisp) control action, that better represents the fuzzy one. This last step obtains the crisp value for the controller output $u(k)$ (Fig. 34.69).

These steps can be implemented on-line or off-line. On-line implementation, useful if an adaptive controller is intended, performs real-time inference to obtain the controller output and needs a fast enough processor. Off-line implementation employs a lookup table built according to the set of all possible combinations of input variables. To obtain this lookup table, the input values in a quantified range are converted (fuzzification) into fuzzy variables (linguistic). The fuzzy set output, obtained by the inference or decision-making engine according to linguistic control rules (designed by the knowledge expert), is then, converted into numeric controller output values (defuzzification). The table contains the output for all the combinations of quantified input entries. Off-line process can actually reduce the controller actuation time since the only effort is limited to consulting the table at each iteration.

This section presents the main steps for the implementation of a fuzzy controller suitable for switching converter control. A meaningful example is provided.

34.4.2 Fuzzy Logic Controller Synthesis

Fuzzy logic controllers consider neither the parameters of the switching converter or their fluctuations, nor the operating conditions, but only the experimental knowledge of the switching converter dynamics. In this way, such a controller can be used with a wide diversity of switching converters implying only small modifications. The necessary fuzzy rules are simply obtained considering roughly the knowledge of the switching converter dynamic behavior.

34.4.2.1 Fuzzification

Assume, as fuzzy controller input variables, an output voltage (or current) error, and the variation of this error. For the output, assume a signal $u(k)$, the control input of the converter.

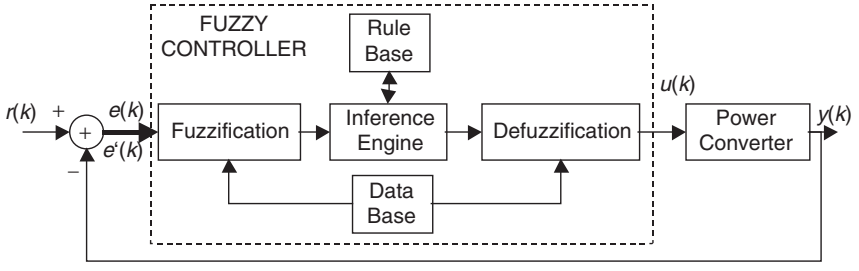


FIGURE 34.69 Structure of a fuzzy logic controller.

A. Quantization Levels Consider the reference $r(k)$ of the converter output kth sample, $y(k)$. The tracking error $e(k)$ is $e(k) = r(k) - y(k)$ and the output error change $\Delta_e(k)$, between the samples k and $k-1$, is determined by $\Delta_e(k) = e(k) - e(k-1)$.

These variables and the fuzzy controller output $u(k)$, usually ranging from -10 to 10 V, can be quantified in m levels $\{-(m-1)/2, +(m-1)/2\}$. For off-line implementation, m sets a compromise between the finite length of a lookup table and the required precision.

B. Linguistic Variables and Fuzzy Sets The fuzzy sets for x_e, the linguistic variable corresponding to the error $e(k)$, for $x_{\Delta e}$, the linguistic variable corresponding to the error variation $\Delta_e(k)$, and for x_u the linguistic variable of the fuzzy controller output $u(k)$, are usually defined as positive big (*PB*), positive medium (*PM*), positive small (*PS*), zero (*ZE*), negative small (*NS*), negative medium (*NM*), and negative big (*NB*), instead of having numerical values.

In most cases, the use of these seven fuzzy sets is the best compromise between accuracy and computational task.

C. Membership Functions A fuzzy subset, for example $\mathbf{S}_i$ ($\mathbf{S}_i$ = (NB, NM, NS, ZE, PS, PM, or PB)) of a universe E, collection of $e(k)$ values denoted generically by $\{e\}$, is characterized by a membership function μ_{Si}: $E \rightarrow [0,1]$, associating with each element e of universe E, a number $\mu_{Si}(e)$ in the interval [0,1], which represents the grade of membership of e to E. Therefore, each variable is assigned a membership grade to each fuzzy set, based on a corresponding membership function (Fig. 34.70). Considering the m quantization levels, the membership function $\mu_{Si}(e)$ of the element e in the universe of discourse E, may take one of the discrete values included in $\mu_{Si}(e) \in \{0; 0.2; 0.4; 0.6; 0.8; 1; 0.8; 0.6; 0.4; 0.2; 0\}$. Membership functions are stored in the database (Fig. 34.69).

Considering $e(k) = 2$ and $\Delta_e(k) = -3$, taking into account the staircase-like membership functions shown in Fig. 34.70, it can be said that x_e is *PS* and also *ZE*, being equally *PS* and *ZE*. Also, $x_{\Delta e}$ is *NS* and *ZE*, being less *ZE* than *NS*.

D. Linguistic Control Rules The generic linguistic control rule has the following form: "IF $x_e(k)$ is membership of the set $\mathbf{S}_i$ = (NB, NM, NS, ZE, PS, PM, or PB) AND $x_{\Delta e}(k)$ is membership of the set $\mathbf{S}_j$ = (NB, NM, NS, ZE, PS, PM, or PB), THEN the output control variable is membership of the set $\mathbf{S}_u$ = (NB, NM, NS, ZE, PS, PM, or PB)."

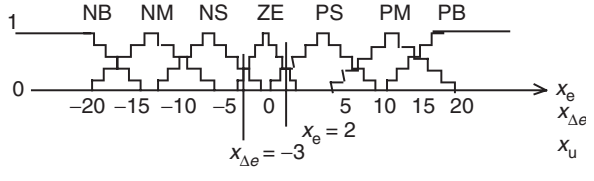


FIGURE 34.70 Membership functions in the universe of discourse.

Usually, the rules are obtained considering the most common dynamic behavior of switching converters, the second-order system with damped oscillating response (Fig. 34.71). Analyzing the error and its variation, together with the rough linguistic knowledge of the needed control input, an expert can obtain linguistic control rules such as the ones displayed in Table 34.8. For example, at point 6 of Fig. 34.71 the rule is "if $x_e(k)$ is NM AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ should be NM."

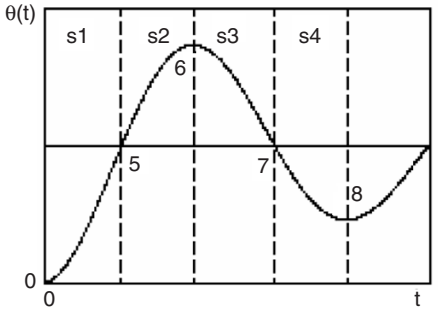


FIGURE 34.71 Reference dynamic model of switching converters: second-order damped oscillating error response.

TABLE 34.8 Linguistic control rules

$x_e(k)x_{\Delta e}(k)$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NM	NM	PS	PM
NM	NB	NB	NM	NS	NM	PM	PB
NS	NB	NB	NM	NS	NS	PM	PB
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NB	NM	PS	PS	PM	PB	PB
PM	NB	NM	PM	PS	PM	PB	PB
PB	NM	NS	PM	PM	PB	PB	PB

Table 34.8, for example, states that:

IF $x_e(k)$ is NB AND $x_{\Delta e}(k)$ is NB, THEN $x_u(k+1)$ must be NB, or
IF $x_e(k)$ is PS AND $x_{\Delta e}(k)$ is NS, THEN $x_u(k+1)$ must be NS, or
IF $x_e(k)$is PS AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ must be PS, or
IF $x_e(k)$ is ZE AND $x_{\Delta e}(k)$ is NS, THEN $x_u(k+1)$ must be NS, or
IF $x_e(k)$ is ZE AND $x_{\Delta e}(k)$ is ZE, THEN $x_u(k+1)$ must be ZE, or
IF…

These rules (rule base) alone do not allow the definition of the control output, as several of them may apply at the same time.

34.4.2.2 Inference Engine

The result of a fuzzy control algorithm can be obtained using the control rules of Table 34.8, the membership functions, and an inference engine. In fact, any quantified value for $e(k)$ and $\Delta_e(k)$ is often included into two linguistic variables. With the membership functions used, and knowing that the controller considers $e(k)$ and $\Delta_e(k)$, the control decision generically must be taken according to four linguistic control rules.

To obtain the corresponding fuzzy set, the min–max inference method can be used. The minimum operator describes the "AND" present in each of the four rules, that is, it calculates the minimum between the discrete value of the membership function $\mu_{Si}(x_e(k))$ and the discrete value of the membership function $\mu_{Sj}(x_{\Delta e}(k))$. The "THEN" statement links this minimum to the membership function of the output variable. The membership function of the output variable will therefore include trapezoids limited by the segment $\min(\mu_{Si}(x_e(k)), \mu_{Sj}(x_{\Delta e}(k)))$.

The OR operator linking the different rules is implemented by calculating the maximum of all the (usually four) rules. This mechanism to obtain the resulting membership function of the output variable is represented in Fig. 34.72.

34.4.2.3 Defuzzification

As shown, the inference method provides a resulting membership function $\mu_{Sr}(x_u(k))$, for the output fuzzy variable x_u (Fig. 34.72). Using a defuzzification process, this final membership function, obtained by combining all the membership functions, as a consequence of each rule, is then converted into a numerical value, called $u(k)$. The defuzzification strategy can be the center of area (COA) method. This method generates one output value $u(k)$, which is the abscissa of the gravity center of the resulting membership function area, given by the following relation:

$$u(k) = \left(\sum_{i=1}^{m} \mu_{Sr}(x_u(k)) x_u(k) \right) \Big/ \sum_{i=1}^{m} \mu_{Sr}(x_u(k)) \quad (34.186)$$

This method provides good results for output control. Indeed, for a weak variation of $e(k)$ and $\Delta_e(k)$, the center of the area will move just a little, and so does the controller output value. By comparison, the alternative defuzzification method, mean of maximum strategy (MOM) is advantageous for fast response, but it causes a greater steady-state error and overshoot (considering no perturbations).

34.4.2.4 Lookup Table Construction

Using the rules given in Table 34.8, the min–max inference procedure and COA defuzzification, all the controller output values for all quantified $e(k)$ and $\Delta_e(k)$, can be stored in an array to serve as the decision-lookup table. This lookup table usually has a three-dimensional representation similar to Fig. 34.73. A microprocessor-based control algorithm just picks up output values from the lookup table.

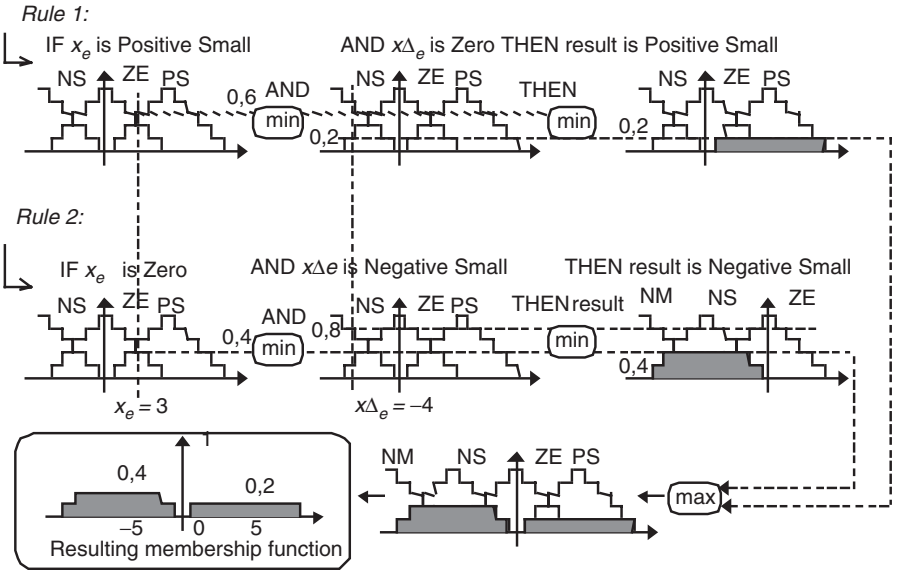


FIGURE 34.72 Application of the min–max operator to obtain the output membership function.

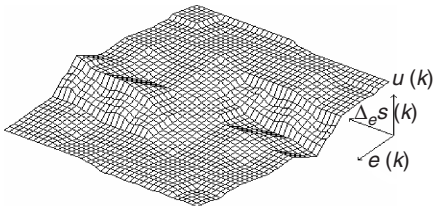


FIGURE 34.73 Three-dimensional view of the lookup table.

34.4.3 Example: Near Unity Power Factor Buck–Boost Rectifier

EXAMPLE 34.18 Fuzzy logic control of unity power factor buck–boost rectifiers

Consider the near unity power factor buck–boost rectifier of Fig. 34.74.

The switched state-space model of this converter can be written:

$$\begin{cases} \frac{di_s}{dt} = -\frac{R_f}{L_f} i_s - \frac{1}{L_f} v_{C_f} + \frac{1}{L_f} v_s \\ \frac{dv_{C_f}}{dt} = \frac{1}{C_f} i_s - \frac{\gamma_p}{C_f} i_{L_o} \\ \frac{di_{L_o}}{dt} = \frac{\gamma_p}{L_o} v_{C_f} - \frac{\gamma(1-|\gamma_p|)}{L_o} V_{C_o} \\ \frac{dV_{C_o}}{dt} = \frac{1-|\gamma_p|}{C_o} i_{L_o} - \frac{1}{R_o C_o} V_o \end{cases} \tag{34.187}$$

$$\text{where} \quad \gamma_p = \begin{cases} 1\,, & (\textit{switch } 1 \textit{ and } 4 \textit{ are ON}) \textit{ and} \\ & (\textit{switch } 2 \textit{ and } 3 \textit{ are OFF}) \\ 0\,, & \textit{all switches are OFF} \\ -1, & (\textit{switch } 2 \textit{ and } 3 \textit{ are ON}) \textit{ and} \\ & (\textit{switch } 1 \textit{ and } 4 \textit{ are OFF}) \end{cases}$$

$$\text{and} \quad \gamma = \begin{cases} 1\,, & i_{L_o} > 0 \\ 0\,, & i_{L_o} \le 0 \end{cases}$$

For comparison purposes, a PI output voltage controller is designed considering that a current-mode PWM modulator enforces the reference value for the i_s current (which usually exhibits a fast dynamics compared with the dynamics of V_{C_o}). A first-order model, similar to Eq. (34.146) is obtained. The PI gains are similar to Eq. (34.116) and load-dependent ($K_p = C_o/(2T_d)$, $K_i = 1/(2T_d R_o)$).

A fuzzy controller is obtained considering the approach outlined, with seven membership functions for the output voltage error, five for its change, and three membership functions for the output. The linguistic control rules are obtained as the ones depicted in Table 34.8 and the lookup table gives a mapping similar to Fig. 34.73. Performances obtained for the step response show a fuzzy controlled rectifier behavior close to the PI behavior. The advantages of the fuzzy controller emerge for perturbed loads or power supplies, where the low sensitivity of the fuzzy controller to system parameters is clearly seen (Fig. 34.75). Therefore, the fuzzy controllers can be advantageous for switching converters with changing loads, power supply voltages, and other external disturbances.

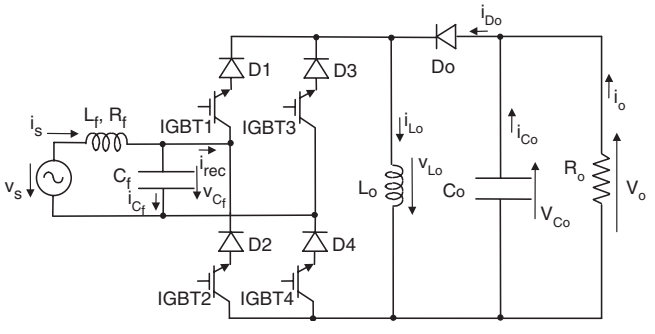


FIGURE 34.74 Unity power factor buck–boost rectifier with four IGBTs.

34.5 Conclusions

Control techniques for switching converters were reviewed. Linear controllers based on state-space averaged models or circuits are well established and suitable for the application of linear systems control theory. Obtained linear controllers are useful, if the converter operating point is almost constant and the disturbances are not relevant. For changing operating points and strong disturbances, linear controllers can be enhanced with nonlinear, antiwindup, soft-start, or saturation techniques. Current-mode control will also help to overcome the main drawbacks of linear controllers.

Sliding mode is a nonlinear approach well adapted for the variable structure of the switching converters. The critical problem of obtaining the correct sliding surface was highlighted, and examples were given. The sliding-mode control law allows the implementation of the switching converter controller, and the switching law gives the PWM modulator. The system variables to be measured and fed back are identified. The obtained reduced-order dynamics is not dependent on system parameters or power supply (as long as it is high enough), presents no steady-state errors, and has a faster response speed (compared with linear controllers), as the system order is reduced and non-idealities are eliminated. Should the measure of the state variables be difficult, state observers may be used, with steady-state errors easily corrected. Sliding-mode controllers provide robustness against bounded disturbances and an elegant way to obtain the controller and modulator, using just the same theoretical approach. Fixed-frequency operation was addressed and solved, together with the short-circuit-proof operation.

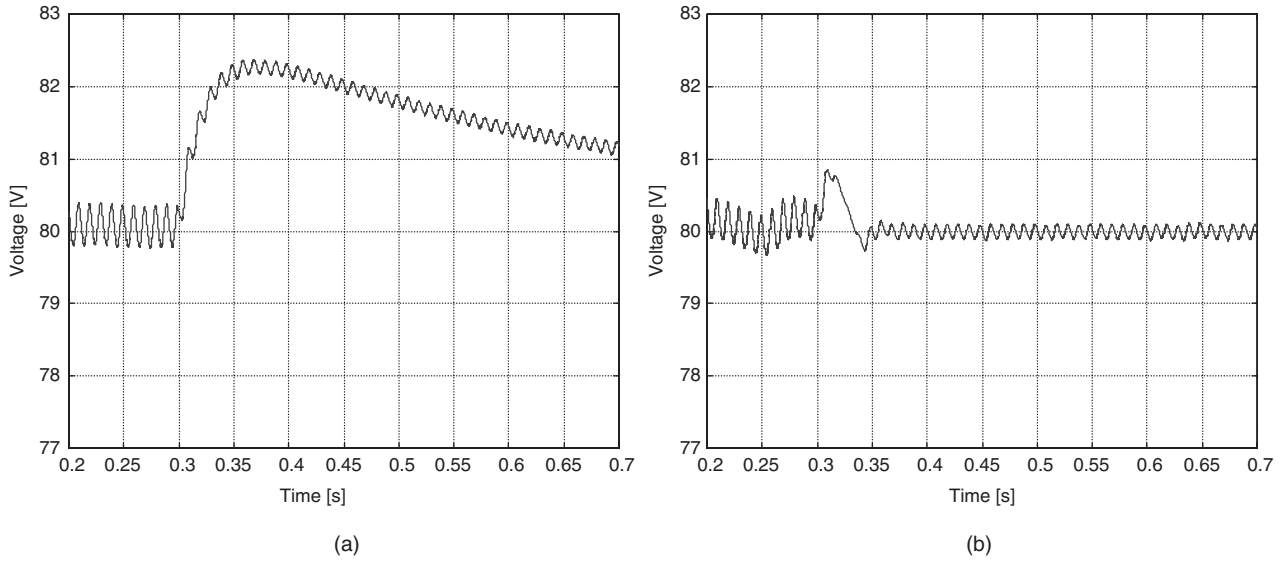


FIGURE 34.75 Simulated result of the output voltage response to load disturbances ($R_o = 50$–$150\ \Omega$ at time 0.3 s): (a) PI control and (b) fuzzy logic control.

Presently, fixed-frequency techniques were applied to converters that can only operate with fixed frequency. Sliding-mode techniques were successfully applied to MIMO switching power converters and to multilevel converters, solving the capacitor voltage divider equalization. Sliding-mode control needs more information from the controlled system than do the linear controllers, but is probably the most adequate tool to solve the control problem of switching power converters.

Fuzzy logic controller synthesis was briefly presented. Fuzzy logic controllers are based on human experience and intuition and do not depend on system parameters or operating points. Fuzzy logic controllers can be easily applied to various types of power converters having the same qualitative dynamics. Fuzzy logic controllers, like sliding-mode controllers, show robustness to load and power supply perturbations, semiconductor non-idealities (such as switch delays or uneven conduction voltage drops), and dead times. The controller implementation is simple, if based on the off-line concept. On-line implementation requires a fast microprocessor but can include adaptive techniques to optimize the rule base and/or the database.

Acknowledgments

J. Fernando Silva thanks all the researchers whose works contributed to this chapter, namely Professors S. Pinto, V. Pires, J. Quadrado, T. Amaral, M. Crisóstomo, Engineers J. Costa, N. Rodrigues, and the suggestions of Professor M. P. Kazmierkowski. The authors also thank FCT, POSI, POCTI, FEDER for funding the projects enabling the presented results.

References

1. Bose, B. K. *Power Electronics and AC Drives*, Prentice-Hall, New Jersey, 1986.
2. Kassakian, J. Schlecht, M. and Verghese, G. *Principles of Power Electronics*, Addison Wesley, 1992.
3. Rashid, M. *Power Electronics: Circuits, Devices and Applications*, 2nd ed., Prentice-Hall International, 1993.
4. Thorborg, K. *Power Electronics*, Prentice-Hall, 1988.
5. Mohan, N. Undeland, T. and Robins, W. *Power Electronics: Converters, Applications and Design*, 2nd ed., John Wiley & Sons, 1995.
6. Sum, K. K. *Switched Mode Power Conversion*, Marcel Dekker Inc., 1984.
7. Bühler, H. *Electronique de Réglage et de Commande*, Traité D'électricité, vol. XV, éditions Georgi, 1979.
8. Irwin, J. D. ed. *The Industrial Electronics Handbook*, CRC/IEEE Press, 1996.
9. Chryssis, G. *High Frequency Switching Power Supplies*, McGraw-Hill, 1984.
10. Labrique, F. and Santana, J. *Electrónica de Potência*, Fundação Calouste Gulbenkian, Lisboa, 1991.
11. Utkin, V. I. *Sliding Modes and Their Application on Variable Structure Systems*, MIR Publishers Moscow, 1978.
12. Utkin, V. I. *Sliding Modes in Control Optimization*, Springer-Verlag, 1981.
13. Ogata, K. *Modern Control Engineering*, 3rd ed., Prentice-Hall International, 1997.
14. Levine, W. S. ed. *The Control Handbook*, CRC/IEEE Press, 1996.
15. Fernando Silva, J. *Electrónica Industrial*, Fundação Calouste Gulbenkian, Lisboa, 1998.
16. Fernando Silva, J. *Sliding Mode Control Design of Control and Modulator Electronics for Power Converters*, Special Issue on Power Electronics of Journal on Circuits, Systems and Computers, vol. 5, no. 3, pp. 355–371, 1995.
17. Fernando Silva, J. *Sliding Mode Control of Boost Type Unity Power Factor PWM Rectifiers*, IEEE Trans. on Industrial Electronics,

Special Section on High-Power-Factor Rectifiers I, vol. 46, no. 3, pp. 594–603, June 1999. ISSN 0278-0046.
18. José Rodriguez, Special Section on Matrix Converters, *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, April 2002.
19. Zadeh, L. A. "Fuzzy Sets", *Information and Control*, vol. 8, pp. 338–353, 1965.
20. Zadeh, L. A. "Outline of a New Approach to the Analysis of Complex Systems and Decision Process," *IEEE Trans. Syst. Man Cybern.*, vol. SMC-3, pp. 28–44, 1973.
21. Zimmermann, H. J. *Fuzzy Sets: Theory and its Applications*, Kluwer-Nijhoff, 1995.
22. Candel, A. and Langholz, G. *Fuzzy Control Systems*, CRC Press, 1994.