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Three-phase Controlled Rectifiers

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12.1 Introduction

Three-phase controlled rectifiers have a wide range of applications, from small rectifiers to large high voltage direct current (HVDC) transmission systems. They are used for electrochemical processes, many kinds of motor drives, traction equipment, controlled power supplies and many other applications. From the point of view of the commutation process, they can be classified into two important categories: *line-commutated controlled rectifiers (thyristor rectifiers) and force-commutated pulse width modulated (PWM) rectifiers.*

12.2 Line-commutated Controlled Rectifiers

12.2.1 Three-phase Half-wave Rectifier

Figure 12.1 shows the three-phase half-wave rectifier topology. To control the load voltage, the half-wave rectifier uses three common-cathode thyristor arrangement. In this figure, the power supply and the transformer are assumed ideal. The thyristor will conduct (*ON* state), when the anode-to-cathode voltage v_{AK} is positive and a firing current pulse i_G is applied to the gate terminal. Delaying the firing pulse by an angle α controls the load voltage. As shown in Fig. 12.2, the firing angle α

is measured from the crossing point between the phase supply voltages. At that point, the anode-to-cathode thyristor voltage v_{AK} begins to be positive. Figure 12.3 shows that the possible range for gating delay is between $\alpha = 0°$ and $\alpha = 180°$, but because of commutation problems in actual situations, the maximum firing angle is limited to around 160°. As shown in Fig. 12.4, when the load is resistive, current i_d has the same waveform of the load voltage. As the load becomes more and more inductive, the current flattens and finally becomes constant. The thyristor goes to the non-conducting condition (*OFF* state) when the following thyristor is switched *ON*, or the current, tries to reach a negative value.

With the help of Fig. 12.2, the load average voltage can be evaluated, and is given by:

$$V_D = \frac{V_{MAX}}{\frac{2}{3}\pi} \int\limits_{-\pi/3+\alpha}^{\pi/3+\alpha} \cos \omega t \cdot d(\omega t)$$

$$= V_{MAX} \frac{\sin \frac{\pi}{3}}{\frac{\pi}{3}} \cdot \cos \alpha \approx 1.17 \cdot V_{f-N}^{rms} \cdot \cos \alpha \qquad (12.1)$$

where V_{MAX} is the secondary phase-to-neutral peak voltage, V_{f-N}^{rms} its root mean square (*rms*) value and ω is the angular frequency of the main power supply. It can be seen from Eq. (12.1) that the load average voltage V_D is modified by
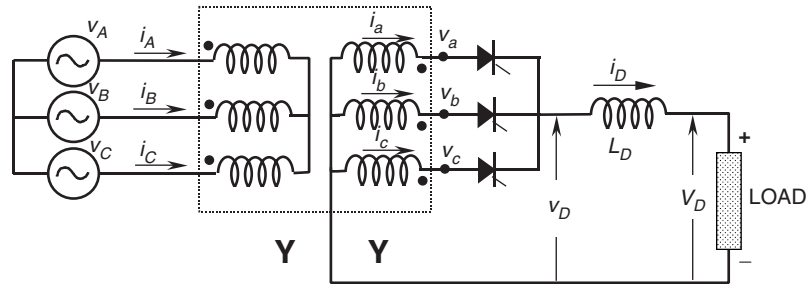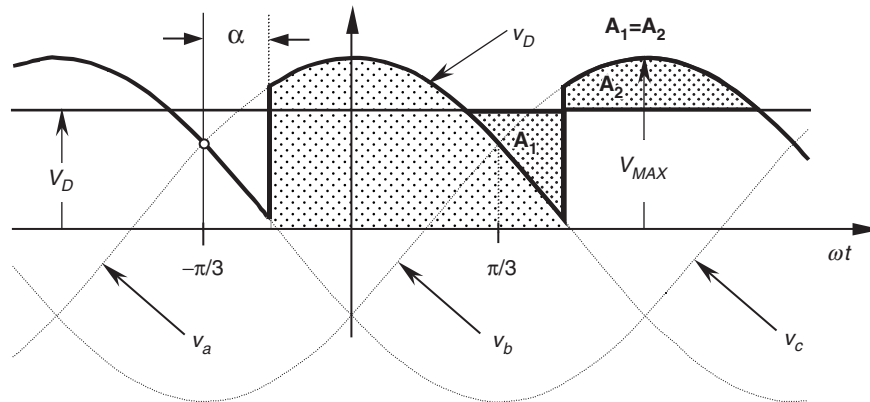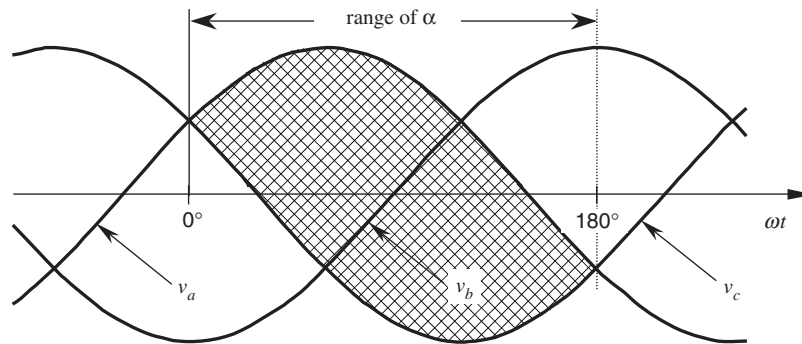
FIGURE 12.1   Three-phase half-wave rectifier.

FIGURE 12.2   Instantaneous *dc* voltage v_D, average *dc* voltage V_D, and firing angle α.

FIGURE 12.3   Possible range for gating delay in angle α.

changing firing angle α. When $\alpha < 90°$, V_D is positive and when $\alpha > 90°$, the average *dc* voltage becomes negative. In such a case, the rectifier begins to work as an inverter and the load needs to be able to generate power reversal by reversing its *dc* voltage.

The *ac* currents of the half-wave rectifier are shown in Fig. 12.5. This drawing assumes that the *dc* current is constant (very large L_D). Disregarding commutation overlap, each valve conducts during 120° per period. The secondary currents (and thyristor currents) present a *dc* component that is undesirable, and makes this rectifier not useful for high power applications.

The primary currents show the same waveform, but with the *dc* component removed. This very distorted waveform requires an input filter to reduce harmonics contamination.

The current waveforms shown in Fig. 12.5 are useful for designing the power transformer. Starting from:

$$VA_{prim} = 3 \cdot V^{rms}_{(prim)f-N} \cdot I^{rms}_{prim}$$

$$VA_{sec} = 3 \cdot V^{rms}_{(sec)f-N} \cdot I^{rms}_{sec} \qquad (12.2)$$
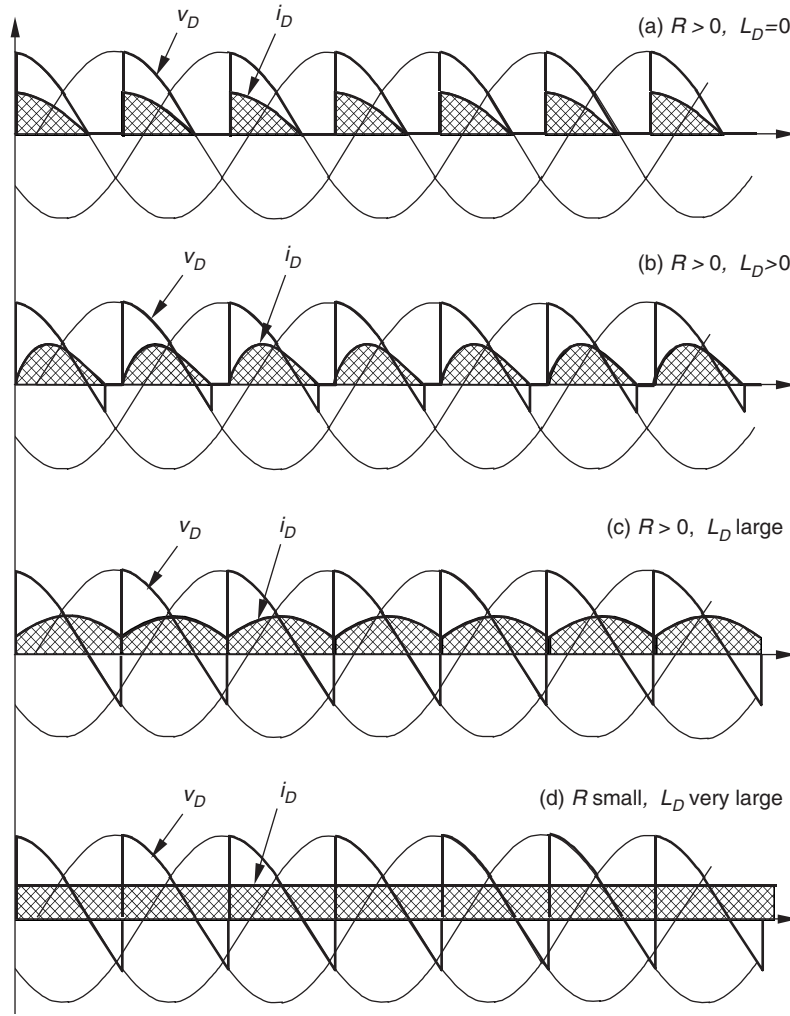
$$P_D = V_D \cdot I_D$$

FIGURE 12.4   *DC* current waveforms.

where VA_{prim} and VA_{sec} are the ratings of the transformer for the primary and secondary side respectively. Here P_D is the power transferred to the *dc* side. The maximum power transfer is with $\alpha = 0°$ (or $\alpha = 180°$). Then, to establish a relation between *ac* and *dc* voltages, Eq. (12.1) for $\alpha = 0°$ is required:

$$V_D = 1.17 \cdot V^{rms}_{(sec)f-N} \qquad (12.3)$$

and:

$$V_D = 1.17 \cdot a \cdot V^{rms}_{(prim)f-N} \qquad (12.4)$$

where *a* is the secondary to primary turn relation of the transformer. On the other hand, a relation between the currents is also possible to obtain. With the help of Fig. 12.5:

$$I^{rms}_{sec} = \frac{I_D}{\sqrt{3}} \qquad (12.5)$$

$$I^{rms}_{prim} = a \cdot \frac{I_D \sqrt{2}}{3} \qquad (12.6)$$

Combining Eqs. (12.2) to (12.6), it yields:

$$VA_{prim} = 1.21 \cdot P_D$$
$$VA_{sec} = 1.48 \cdot P_D \qquad (12.7)$$

Equation (12.7) shows that the power transformer has to be oversized 21% at the primary side, and 48% at the secondary side. Then, a special transformer has to be built for this rectifier. In terms of average *VA*, the transformer needs to be 35% larger that the rating of the *dc* load. The larger rating of the secondary with respect to primary is because the secondary carries a *dc* component inside the windings. Furthermore, the transformer is oversized because the circulation of current harmonics does not generate active power. Core saturation, due to
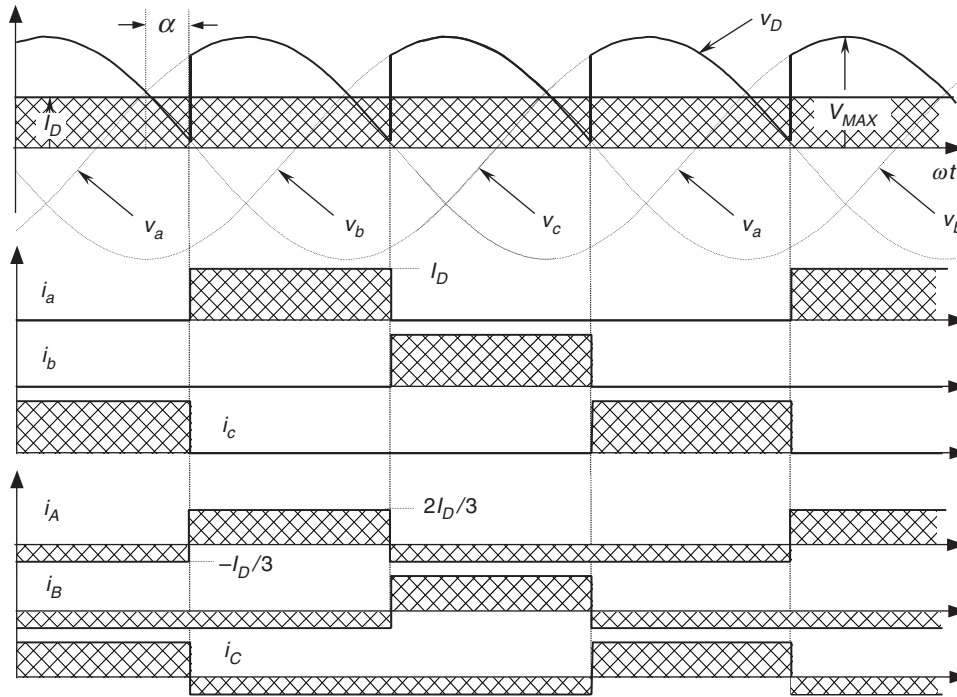
FIGURE 12.5 *AC* current waveforms for the half-wave rectifier.
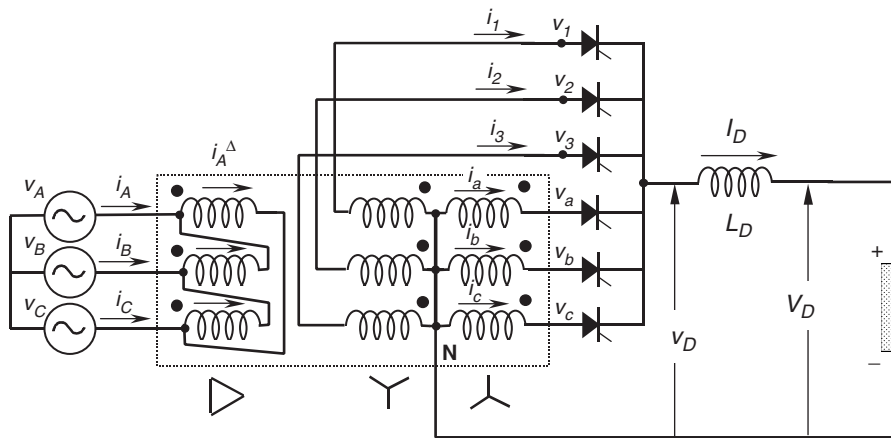
FIGURE 12.6 Six-pulse rectifier.

the *dc* components inside the secondary windings, also needs to be taken in account for iron oversizing.

12.2.2 Six-pulse or Double Star Rectifier

The thyristor side windings of the transformer shown in Fig. 12.6 form a six-phase system, resulting in a six-pulse starpoint (midpoint connection). Disregarding commutation overlap, each valve conducts only during 60° per period. The direct voltage is higher than that from the half-wave rectifier

and its average value is given by:

$$V_D = \frac{V_{MAX}}{\frac{\pi}{3}} \int\limits_{-\pi/6+\alpha}^{\pi/6+\alpha} \cos\omega t \cdot d\left(\omega t\right)$$

$$= V_{MAX} \frac{\sin\frac{\pi}{6}}{\frac{\pi}{6}} \cdot \cos\alpha \approx 1.35 \cdot V_{f-N}^{rms} \cdot \cos\alpha \qquad (12.8)$$

The *dc* voltage ripple is also smaller than the one generated by the half-wave rectifier, due to the absence of the third harmonic with its inherently high amplitude. The smoothing

FIGURE 12.7 *AC* current waveforms for the six-pulse rectifier.

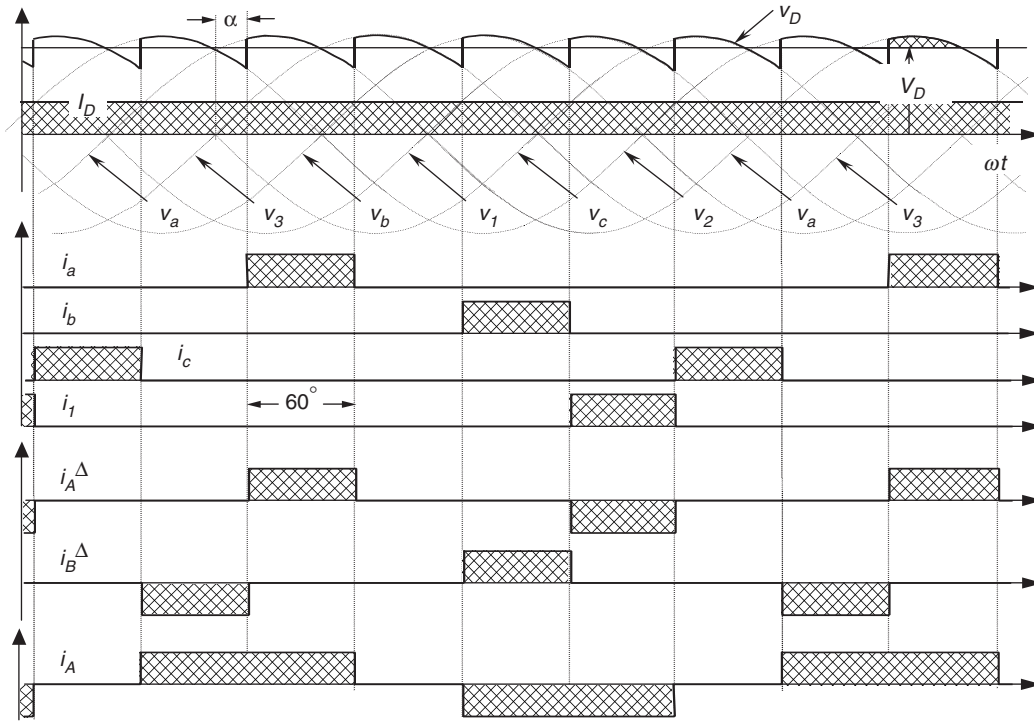reactor L_D is also considerably smaller than the one needed for a three-pulse (half-wave) rectifier.

The *ac* currents of the six-pulse rectifier are shown in Fig. 12.7. The currents in the secondary windings present a *dc* component, but the magnetic flux is compensated by the double star. As can be observed, only one valve is fired at a time and then this connection in no way corresponds to a parallel connection. The currents inside the delta show a symmetrical waveform with 60° conduction. Finally, due to the particular transformer connection shown in Fig. 12.6, the source currents also show a symmetrical waveform, but with 120° conduction.

Evaluation of the the rating of the transformer is done in similar fashion to the way the half-wave rectifier is evaluated:

$$VA_{prim} = 1.28 \cdot P_D$$
$$VA_{sec} = 1.81 \cdot P_D \tag{12.9}$$

Thus the transformer must be oversized 28% at the primary side and 81% at the secondary side. In terms of size it has an average apparent power of 1.55 times the power P_D(55% oversized). Because of the short conducting period of the valves, the transformer is not particularly well utilized.

12.2.3 Double Star Rectifier with Interphase Connection

This topology works as two half-wave rectifiers in parallel, and is very useful when high *dc* current is required. An optimal way to reach both good balance and elimination of harmonics is through the connection shown in Fig. 12.8. The two rectifiers are shifted by 180°, and their secondary neutrals are connected through a middle-point autotransformer called "interphase transformer." The interphase transformer is connected between the two secondary neutrals and the middle point at the load return. In this way, both groups operate in parallel. Half the direct current flows in each half of the interphase transformer, and then its iron core does not become saturated. The potential of each neutral can oscillate independently, generating an almost triangular voltage waveform (v_T) in the interphase transformer, as shown in Fig. 12.9. As this converter work like two half-wave rectifiers connected in parallel, the load average voltage is the same as in Eq. (12.1):

$$V_D \approx 1.17 \cdot V_{f-N}^{rms} \cdot \cos \alpha \tag{12.10}$$

where V_{f-N}^{rms} is the phase-to-neutral *rms* voltage at the valve side of the transformer (secondary).

The Fig. 12.9 also shows the two half-wave rectifier voltages, related to their respective neutrals. Voltage v_{D1} represents the potential between the common cathode connection and the neutral N1. The voltage v_{D2} is between the common cathode connection and N2. It can be seen that the two instantaneous voltages are shifted, which gives as a result, a voltage v_D that is smoother than v_{D1} and v_{D2}.

Figure 12.10 shows how v_D, v_{D1}, v_{D2}, and v_T change when the firing angle changes from $\alpha = 0°$ to 180°.

FIGURE 12.8   Double star rectifier with interphase transformer.

FIGURE 12.9   Operation of the interphase connection for $\alpha = 0°$.

The transformer rating in this case is:

$$VA_{prim} = 1.05 \cdot P_D$$
$$VA_{sec} = 1.48 \cdot P_D \tag{12.11}$$

And the average rating power will be 1.26 P_D, which is better than the previous rectifiers (1.35 for the half-wave rectifier and 1.55 for the six-pulse rectifier). Thus the transformer is well utilized. Figure 12.11 shows *ac* current waveforms for a rectifier with interphase transformer.

12.2.4   Three-phase Full-wave Rectifier or Graetz Bridge

Parallel connection via interphase transformers permits the implementation of rectifiers for high current applications. Series connection for high voltage is also possible, as shown in the full-wave rectifier of Fig. 12.12. With this arrangement, it can be seen that the three common cathode valves generate a positive voltage with respect to the neutral, and the three common anode valves produce a negative voltage. The result is a *dc* voltage, twice the value of the half-wave rectifier. Each half of the bridge is a three-pulse converter group. This bridge connection is a two-way connection and alternating currents flow in the valve-side transformer windings during both half periods, avoiding *dc* components into the windings, and saturation in the transformer magnetic core. These characteristics make the so-called Graetz bridge the most widely used line-commutated thyristor rectifier. The configuration does not need any special transformer and works as a six-pulse rectifier. The series characteristic of this rectifier produces a *dc* voltage twice the value of the half-wave rectifier. The load average voltage is given by:

$$V_D = \frac{2 \cdot V_{MAX}}{\frac{2}{3}\pi} \int_{-\pi/3+\alpha}^{\pi/3+\alpha} \cos\omega t \cdot d\,(\omega t)$$

$$= 2 \cdot V_{MAX} \frac{\sin\frac{\pi}{3}}{\frac{\pi}{3}} \cdot \cos\alpha \approx 2.34 \cdot V_{f-N}^{rms} \cdot \cos\alpha \tag{12.12}$$
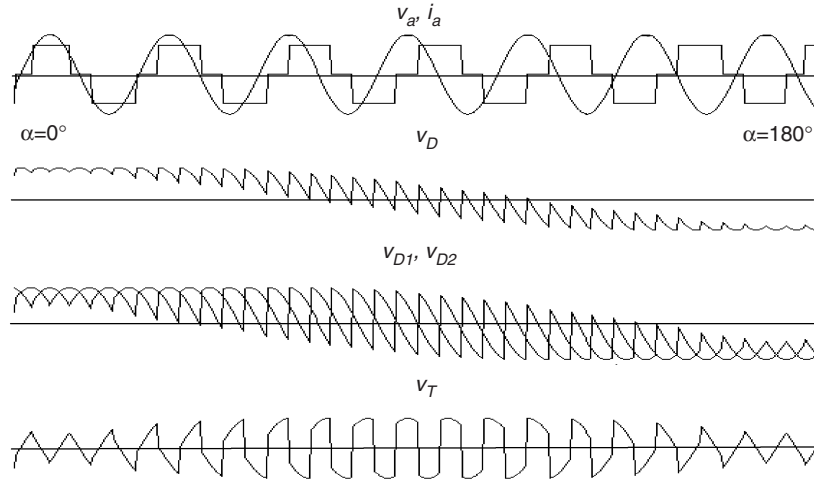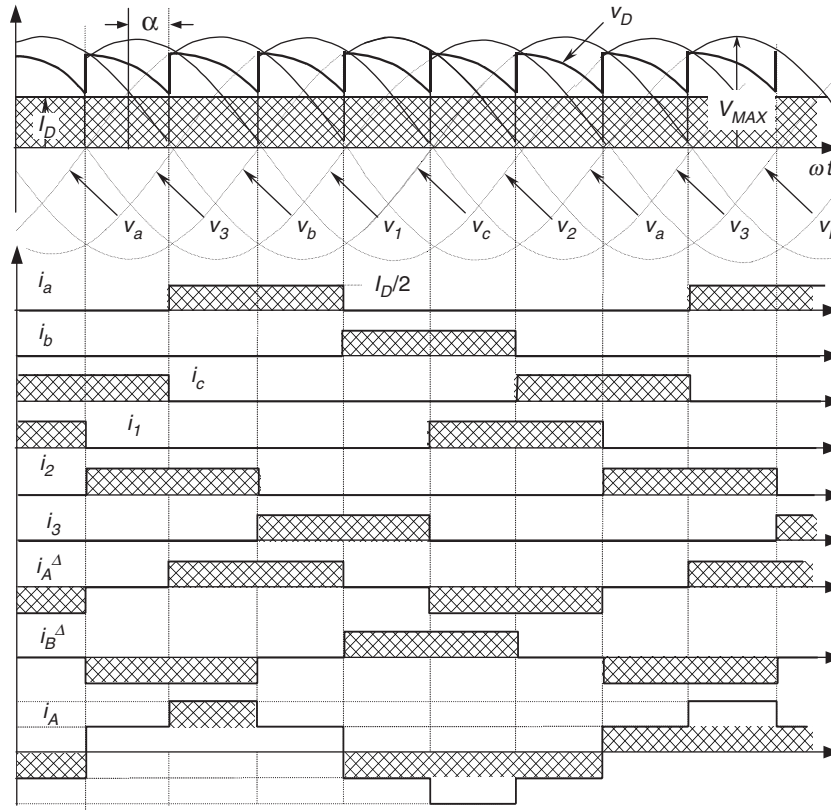
FIGURE 12.10 Firing angle variation from $\alpha = 0°$ to $180°$.

FIGURE 12.11 *AC* current waveforms for the rectifier with interphase transformer.

or

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{sec}}{\pi} \cos\alpha \approx 1.35 \cdot V_{f-f}^{sec} \cdot \cos\alpha \quad (12.13)$$

where V_{MAX} is the peak phase-to-neutral voltage at the secondary transformer terminals, V_{f-N}^{rms} its *rms* value,

and V_{f-f}^{sec} the *rms* phase-to-phase secondary voltage, at the valve terminals of the rectifier.

Figure 12.13 shows the voltages of each half-wave bridge of this topology, v_D^{pos} and v_D^{neg}, the total instantaneous *dc* voltage v_D, and the anode-to-cathode voltage v_{AK} in one of the bridge thyristors. The maximum value of v_{AK} is $\sqrt{3} \cdot V_{MAX}$,
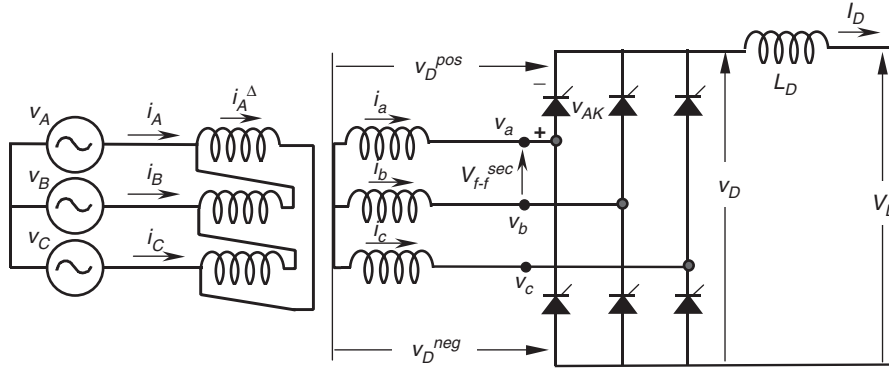
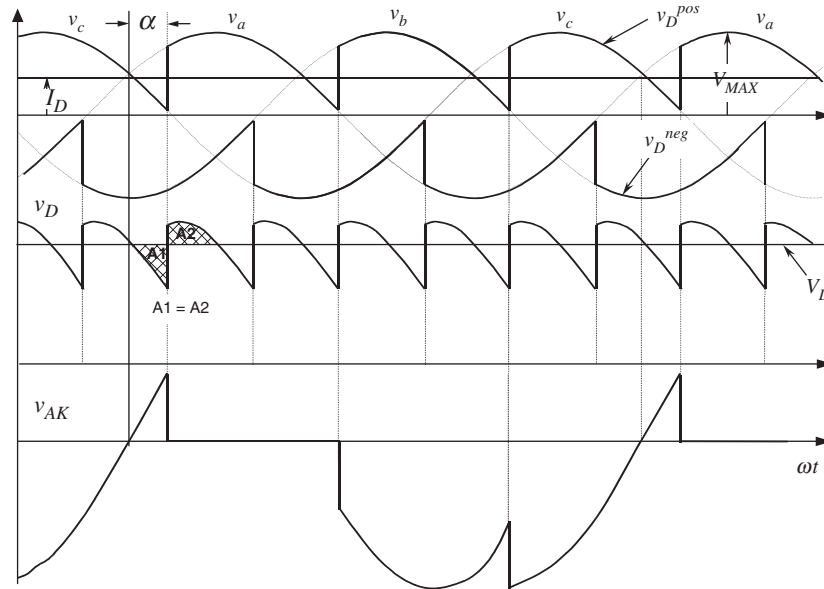**FIGURE 12.12** Three-phase full-wave rectifier or Graetz bridge.

FIGURE 12.13 Voltage waveforms for the Graetz bridge.

which is the same as that of the half-wave converter and the interphase transformer rectifier. The double star rectifier presents a maximum anode-to-cathode voltage of two times V_{MAX}. Figure 12.14 shows the currents of the rectifier, which assumes that L_D is large enough to keep the *dc* current smooth. The example is for the same ΔY transformer connection shown in the topology of Fig. 12.12. It can be noted that the secondary currents do not carry any *dc* component, thereby avoiding overdesign of the windings and transformer saturation. These two figures have been drawn for a firing angle, α of approximately 30°. The perfect symmetry of the currents in all windings and lines is one of the reasons why this rectifier is the most popular of its type. The transformer rating in this case is

$$VA_{prim} = 1.05 \cdot P_D$$

$$VA_{sec} = 1.05 \cdot P_D$$

(12.14)

As can be noted, the transformer needs to be oversized only 5%, and both primary and secondary windings have the same rating. Again, this value can be compared with the previous rectifier transformers: $1.35P_D$ for the half-wave rectifier, $1.55P_D$ for the six-pulse rectifier, and $1.26P_D$ for the interphase transformer rectifier. The Graetz bridge makes excellent use of the power transformer.

12.2.5 Half Controlled Bridge Converter

The fully controlled three-phase bridge converter shown in Fig. 12.12 has six thyristors. As already explained here, this circuit operates as a rectifier when each thyristor has a firing angle $\alpha < 90°$ and functions as an inverter for $\alpha > 90°$. If inverter operation is not required, the circuit may be simplified by replacing three controlled rectifiers with power diodes, as in Fig. 12.15a. This simplification is economically attractive
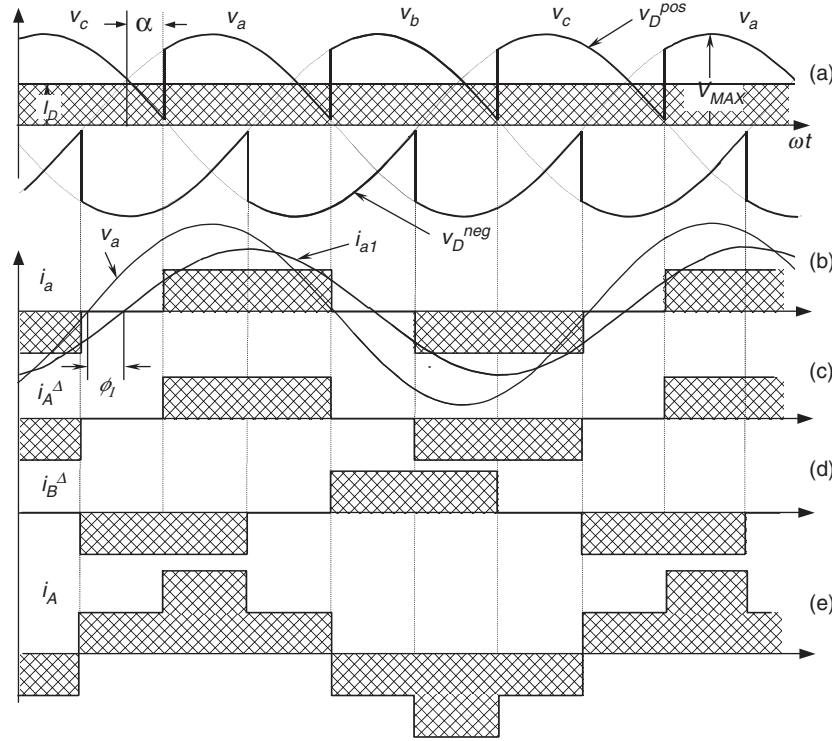
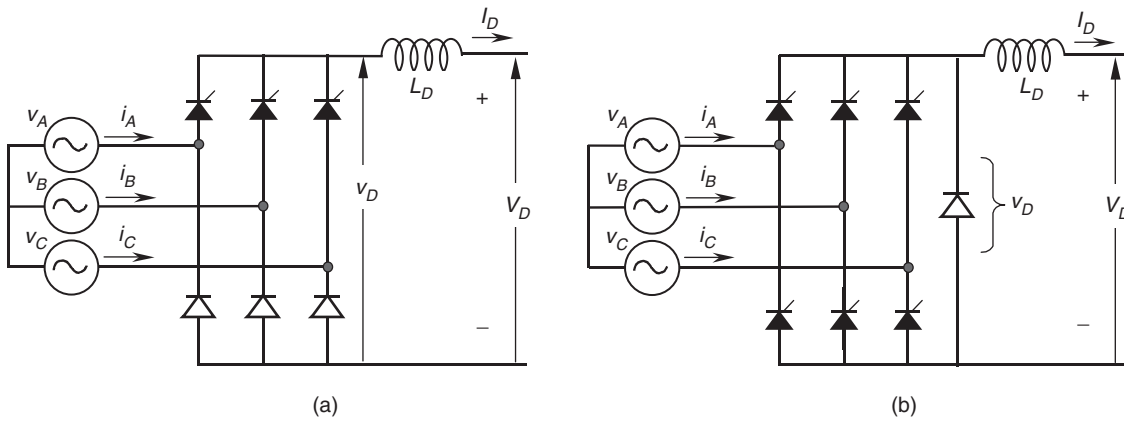**FIGURE 12.14**   Current waveforms for the Graetz bridge.

FIGURE 12.15   One-quadrant bridge converter circuits: (a) half-controlled bridge and (b) free-wheeling diode bridge.

because diodes are considerably less expensive than thyristors and they do not require firing angle control electronics.

The half controlled bridge, or "semiconverter," is analyzed by considering it as a phase-controlled half-wave circuit in series with an uncontrolled half-wave rectifier. The average *dc* voltage is given by the following equation

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{sec}}{2\pi}(1 + \cos\alpha) \qquad (12.15)$$

Then, the average voltage V_D never reaches negative values. The output voltage waveforms of half-controlled bridge are similar to those of a fully controlled bridge with a free-wheeling diode. The advantage of the free-wheeling diode connection, shown in Fig. 12.15b is that there is always a path for the *dc* current, independent of the status of the *ac* line and of the converter. This can be important if the load is inductive–resistive with a large time constant, and there is an interruption in one or more of the line phases. In such a case, the load current could commutate to the free-wheeling diode.
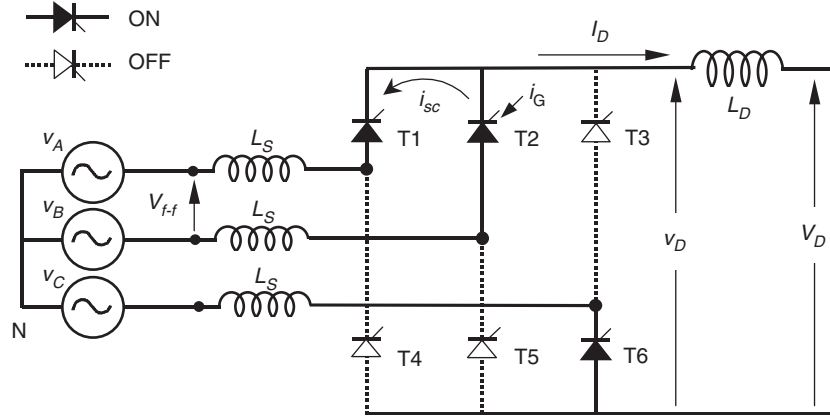
FIGURE 12.16   Commutation process.

12.2.6 Commutation

The description of the converters in the previous sections was based upon assumption that the commutation was instantaneous. In practice this is not possible, because the transfer of current between two consecutive valves in a commutation group takes a finite time. This time, called *overlap time*, depends on the phase-to-phase voltage between the valves participating in the commutation process, and the line inductance L_S between the converter and power supply. During the overlap time, two valves conduct, and the phase-to-phase voltage drops entirely on the inductances L_S. Assuming the *dc* current I_D to be smooth and with the help of Fig. 12.16, the following relation is deduced

$$2L_S \cdot \frac{di_{sc}}{dt} = \sqrt{2} \cdot V_{f-f} \sin \omega t = v_A - v_B \qquad (12.16)$$

where i_{sc} is the current in the valve being fired during the commutation process (thyristor T2 in Fig. 12.16). This current can be evaluated, and it yields

$$i_{sc} = -\frac{\sqrt{2}}{2L_S} \cdot V_{f-f} \frac{\cos \omega t}{\omega} + C \qquad (12.17)$$

The constant "C" is evaluated through initial conditions at the instant when T2 is ignited. In terms of angle, when $\omega t = \alpha$.

$$\text{when } \omega t = \alpha, \quad i_{sc} = 0$$

$$\therefore C = \frac{V_{f-f}^{sec}}{\sqrt{2} \cdot \omega L_S} \cos \alpha \qquad (12.18)$$

Replacing Eq. (12.18) in (12.17):

$$i_{sc} = \frac{V_{f-f}}{\sqrt{2} \cdot \omega L_S} \cdot (\cos \alpha - \cos \omega t) \qquad (12.19)$$

Before commutation, the current I_D was carried by thyristor T1 (see Fig. 12.16). During the commutation time, the load current I_D remains constant, i_{sc} returns through T1, and T1 is automatically switched off when the current i_{sc} reaches the value of I_D. This happens because thyristors cannot conduct in reverse direction. At this moment, the overlap time lasts and the current I_D is then conducted by T2. In terms of angle, when $\omega t = \alpha + \mu$, $i_{sc} = I_D$, where μ is defined as the "*overlap angle*." Replacing this final condition in Eq. (12.19) yields

$$I_D = \frac{V_{f-f}^{sec}}{\sqrt{2} \cdot \omega L_S} \cdot [\cos \alpha - \cos (\alpha + \mu)] \qquad (12.20)$$

To avoid confusion in a real analysis, it has to be remembered that V_{f-f} corresponds to the secondary voltage in case of transformer utilization. For this reason, the abbreviation "sec" has been added to the phase-to-phase voltage in Eq. (12.20).

During commutation, two valves conduct at a time, which means that there is an instantaneous short circuit between the two voltages participating in the process. As the inductances of each phase are the same, the current i_{sc} produces the same voltage drop in each L_S, but with opposite sign because this current flows in reverse direction and with opposite slope in each inductance. The phase with the higher instantaneous voltage suffers a voltage drop $-\Delta v$ and the phase with the lower voltage suffers a voltage increase $+\Delta v$. This situation affects the *dc* voltage V_C, reducing its value an amount ΔV_{med}. Figure 12.17 shows the meanings of Δv, ΔV_{med}, μ, and i_{sc}.

The area ΔV_{med} showed in Fig. 12.17, represents the loss of voltage that affects the average voltage V_C, and can be evaluated through the integration of Δv during the overlap angle μ. The voltage drop Δv can be expressed as

$$\Delta v = \left(\frac{v_A - v_B}{2} \right) = \frac{\sqrt{2} \cdot V_{f-f}^{sec} \sin \omega t}{2} \qquad (12.21)$$
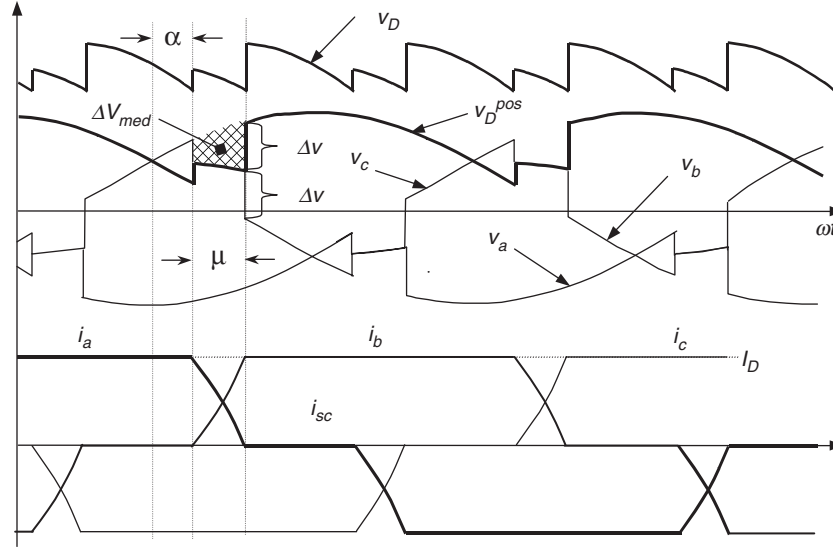
FIGURE 12.17   Effect of the overlap angle on the voltages and currents.

Integrating Eq. (12.21) into the corresponding period (60°) and interval (μ) and starting at the instant when the commutation begins (α)

$$\Delta V_{med} = \frac{3}{\pi} \cdot \frac{1}{2} \int\limits_{\alpha}^{\alpha+\mu} \sqrt{2} \cdot V_{f-f}^{sec} \sin \omega t \cdot d\omega t \qquad (12.22)$$

$$\Delta V_{med} = \frac{3 \cdot V_{f-f}^{sec}}{\pi \cdot \sqrt{2}} \left[\cos \alpha - \cos (\alpha + \mu)\right] \qquad (12.23)$$

Subtracting ΔV_{med} in Eq. (12.13)

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{sec}}{\pi} \cos \alpha - \Delta V_{med} \qquad (12.24)$$

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{sec}}{2\pi} \left[\cos \alpha + \cos (\alpha + \mu)\right] \qquad (12.25)$$

or

$$V_D = \frac{3 \cdot \sqrt{2} \cdot V_{f-f}^{sec}}{\pi} \left[\cos \left(\alpha + \frac{\mu}{2}\right) \cos \frac{\mu}{2}\right] \qquad (12.26)$$

Equations (12.20) and (12.25) can be written as a function of the primary winding of the transformer, if there is any transformer.

$$I_D = \frac{a \cdot V_{f-f}^{prim}}{\sqrt{2} \cdot \omega L_S} \cdot \left[\cos \alpha - \cos (\alpha + \mu)\right] \qquad (12.27)$$

$$V_D = \frac{3 \cdot \sqrt{2} \cdot a \cdot V_{f-f}^{prim}}{2\pi} \left[\cos \alpha + \cos (\alpha + \mu)\right] \qquad (12.28)$$

where $a = V_{f-f}^{sec}/V_{f-f}^{prim}$. With Eqs. (12.27) and (12.28) one gets

$$V_D = \frac{3 \cdot \sqrt{2}}{\pi} \cdot a \cdot V_{f-f}^{prim} \cos \alpha - \frac{3I_D\omega L_S}{\pi} \qquad (12.29)$$

Equation (12.29) allows a very simple equivalent circuit of the converter to be made, as shown in Fig. 12.18. It is important to note that the equivalent resistance of this circuit is not real, because it does not dissipate power.

From the equivalent circuit, regulation curves for the rectifier under different firing angles are shown in Fig. 12.19. It should be noted that these curves correspond only to an ideal situation, but helps in understanding the effect of voltage drop Δv on dc voltage. The commutation process and the overlap angle also affects the voltage v_a and anode-to-cathode thyristor voltage, as shown in Fig. 12.20.
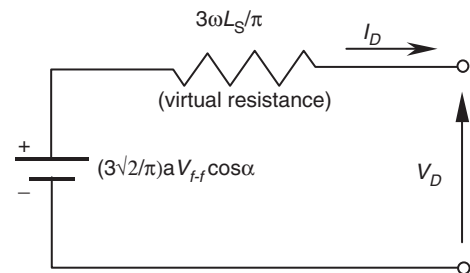

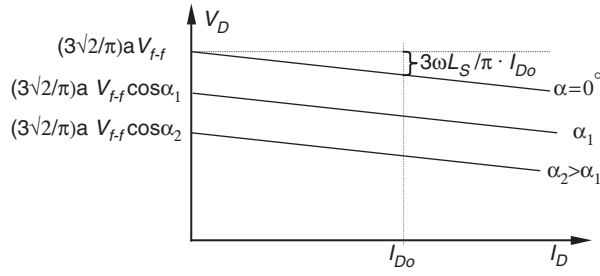**FIGURE 12.18**   Equivalent circuit for the converter.

FIGURE 12.19 *DC* voltage regulation curves for rectifier operation.

12.2.7 Power Factor

The displacement factor of the fundamental current, obtained from Fig. 12.14 is

$$\cos\phi_1 = \cos\alpha \qquad (12.30)$$

In the case of non-sinusoidal current, the active power delivered per phase by the sinusoidal supply is

$$P = \frac{1}{T}\int_0^T v_a(t)i_a(t)dt = V_a^{rms}I_{a1}^{rms}\cos\phi_1 \qquad (12.31)$$

where V_a^{rms} is the *rms* value of the voltage v_a and I_{a1}^{rms} the *rms* value of i_{a1} (fundamental component of i_a). Analog relations can be obtained for v_b and v_c.

The apparent power per phase is given by

$$S = V_a^{rms}I_a^{rms} \qquad (12.32)$$

The power factor is defined by

$$PF = \frac{P}{S} \qquad (12.33)$$

By substituting Eqs. (12.30), (12.31), and (12.32) into Eq. (12.33), the power factor can be expressed as follows

$$PF = \frac{I_{a1}^{rms}}{I_a^{rms}}\cos\alpha \qquad (12.34)$$

This equation shows clearly that due to the non-sinusoidal waveform of the currents, the power factor of the rectifier is negatively affected by both the firing angle α and the distortion of the input current. In effect, an increase in the distortion of the current produces an increase in the value of I_a^{rms} in Eq. (12.34), which deteriorates the power factor.

12.2.8 Harmonic Distortion

The currents of the line-commutated rectifiers are far from being sinusoidal. For example, the currents generated from the Graetz rectifier (see Fig. 12.14b) have the following harmonic content

$$i_A = \frac{2\sqrt{3}}{\pi}I_D(\cos\omega t - \frac{1}{5}\cos 5\omega t + \frac{1}{7}\cos 7\omega t$$

$$- \frac{1}{11}\cos 11\omega t + \ldots) \qquad (12.35)$$

Some of the characteristics of the currents, obtained from Eq. (12.35) include: (i) the absence of triple harmonics; (ii) the presence of harmonics of order $6k \pm 1$ for integer values of k; (iii) those harmonics of orders $6k + 1$ are of positive sequence; (iv) those of orders $6k - 1$ are of negative sequence; (v) the *rms* magnitude of the fundamental frequency is
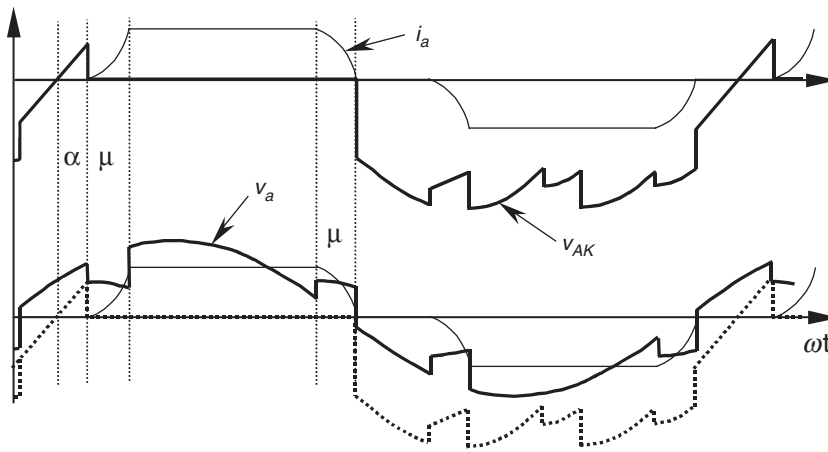
$$I_1 = \frac{\sqrt{6}}{\pi}I_D \qquad (12.36)$$

FIGURE 12.20 Effect of the overlap angle on v_a and on thyristor voltage v_{AK}.

and (vi) the *rms* magnitude of the *n*th harmonic is

$$I_n = \frac{I_1}{n} \qquad (12.37)$$

If either, the primary or the secondary three-phase windings of the rectifier transformer are connected in delta, the *ac* side current waveforms consist of the instantaneous differences between two rectangular secondary currents 120° apart as shown in Fig. 12.14e. The resulting Fourier series for the current in phase "a" on the primary side is

$$i_A = \frac{2\sqrt{3}}{\pi} I_D (\cos\omega t + \frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega t$$

$$- \frac{1}{11}\cos 11\omega t + \ldots) \qquad (12.38)$$

This series differs from that of a star connected transformer only by the sequence of rotation of harmonic orders $6k \pm 1$ for odd values of *k*, i.e. the 5th, 7th, 17th, 19th, etc.

12.2.9 Special Configurations for Harmonic Reduction

A common solution for harmonic reduction is through the connection of passive filters, which are tuned to trap a particular harmonic frequency. A typical configuration is shown in Fig. 12.21.

However, harmonics also can be eliminated using special configurations of converters. For example, 12-pulse configuration consists of two sets of converters connected as shown
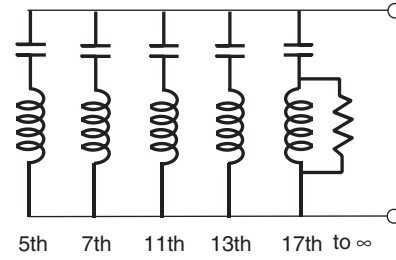

FIGURE 12.21 Typical passive filter for one phase.

in Fig. 12.22. The resultant *ac* current is given by the sum of the two Fourier series of the star connection (Eq. (12.35)) and delta connection transformers (Eq. (12.38))

$$i_A = 2\left(\frac{2\sqrt{3}}{\pi}\right) I_D (\cos\omega t - \frac{1}{11}\cos 11\omega t + \frac{1}{13}\cos 13\omega t$$

$$- \frac{1}{23}\cos 23\omega t + \ldots) \qquad (12.39)$$

The series only contains harmonics of order $12k \pm 1$. The harmonic currents of orders $6k \pm 1$ (with *k* odd), i.e. 5th, 7th, 17th, 19th, etc. circulate between the two converter transformers but do not penetrate the *ac* network.

The resulting line current for the 12-pulse rectifier, shown in Fig. 12.23, is closer to a sinusoidal waveform than previous line currents. The instantaneous *dc* voltage is also smoother with this connection.
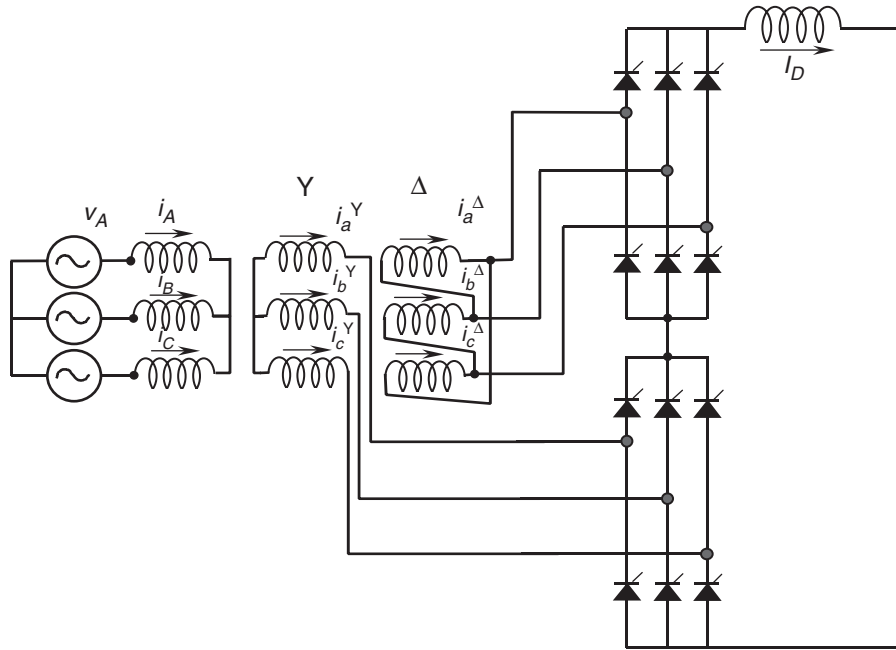

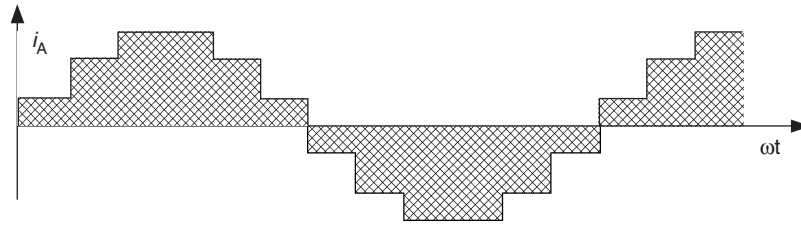**FIGURE 12.22** 12-pulse rectifier configuration.

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FIGURE 12.23 Line current for the 12-pulse rectifier.
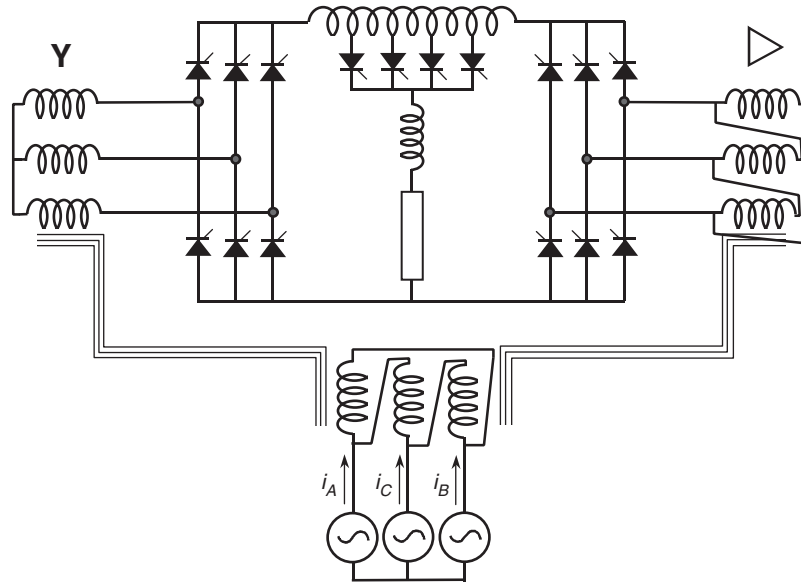

FIGURE 12.24 *DC* ripple reinjection technique for 48-pulse operation.

Higher pulse configuration using the same principle is also possible. The 12-pulse rectifier was obtained with a 30° phase shift between the two secondary transformers. The addition of further, appropriately shifted, transformers in parallel provides the basis for increasing pulse configurations. For instance, 24-pulse operation is achieved by means of four transformers with 15° phase shift, and 48-pulse operation requires eight transformers with 7.5° phase shift (transformer connections in zig-zag configuration).

Although theoretically possible, pulse numbers above 48 are rarely justified due to the practical levels of distortion found in the supply voltage waveforms. Further, the converter topology becomes more and more complicated.

An ingenious and very simple way to reach high pulse operation is shown in Fig. 12.24. This configuration is called *dc* ripple reinjection. It consists of two parallel converters connected to the load through a multistep reactor. The reactor uses a chain of thyristor-controlled taps, which are connected to symmetrical points of the reactor. By firing the thyristors located at the reactor at the right time, high-pulse operation is reached. The level of pulse operation depends on the number of thyristors connected to the reactor. They multiply the

basic level of operation of the two converters. The example, is Fig. 12.24, shows a 48-pulse configuration, obtained by the multiplication of basic 12-pulse operation by four reactor thyristors. This technique also can be applied to series connected bridges.

Another solution for harmonic reduction is the utilization of active power filters. Active power filters are special pulse width modulated (PWM) converters, able to generate the harmonics the converter requires. Figure 12.25 shows a current controlled shunt active power filter.

12.2.10 Applications of Line-commutated Rectifiers in Machine Drives

Important applications for line-commutated three-phase controlled rectifiers, are found in machine drives. Figure 12.26 shows a *dc* machine control implemented with a six-pulse rectifier. Torque and speed are controlled through the armature current I_D, and excitation current I_{exc}. Current I_D is adjusted with V_D, which is controlled by the firing angle α through Eq. (12.12). This *dc* drive can operate in two quadrants: positive and negative *dc* voltage. This two-quadrant
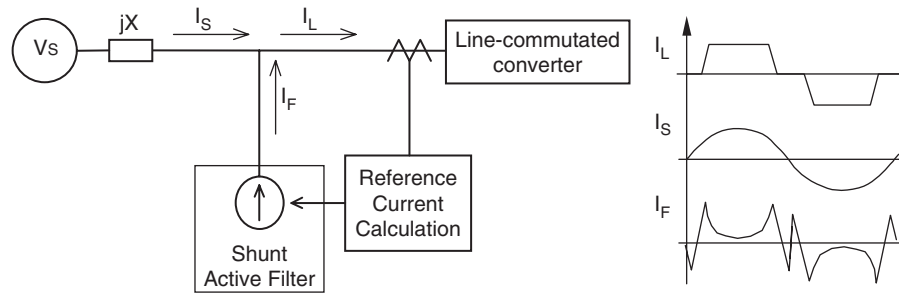
FIGURE 12.25 Current controlled shunt active power filter.

operation allows regenerative braking when $\alpha > 90°$ and $I_{exc} < 0$.

The converter of Fig. 12.26 can also be used to control synchronous machines, as shown in Fig. 12.27. In this case, a second converter working in the inverting mode operates the machine as self-controlled synchronous motor. With this second converter, the synchronous motor behaves like a *dc* motor but has none of the disadvantages of mechanical commutation. This converter is not line commutated, but machine commutated.

The nominal synchronous speed of the motor on a 50 or 60 Hz *ac* supply is now meaningless and the upper speed limit is determined by the mechanical limitations of the rotor construction. There is disadvantage that the rotational *emfs* required for load commutation of the machine side converter are not available at standstill and low speeds. In such a case, auxiliary force commutated circuits must be used.

The line-commutated rectifier controls the torque of the machine through firing angle α. This approach gives direct torque control of the commutatorless motor and is analogous to the use of armature current control shown in Fig. 12.26 for the converter-fed *dc* motor drive.

Line-commutated rectifiers are also used for speed control of wound rotor induction motors. Subsynchronous and supersynchronous static converter cascades using a naturally commutated *dc* link converter, can be implemented. Figure 12.28 shows a supersynchronous cascade for a wound rotor induction motor, using a naturally commutated *dc* link converter.

In the supersynchronous cascade shown in Fig. 12.28, the right hand bridge operates at slip frequency as a rectifier or inverter, while the other operates at network frequency as an inverter or rectifier. Control is difficult near synchronism when slip frequency *emfs* are insufficient for natural commutation and special circuit configuration employing forced commutation or devices with a self-turn-off capability are necessary for the passage through synchronism. This kind of supersynchronous cascade works better with cycloconverters.

12.2.11 Applications in HVDC Power Transmission

High voltage direct current (HVDC) power transmission is the most powerful application for line-commutated converters that exist today. There are power converters with ratings in excess of 1000 MW. Series operation of hundreds of valves can be found in some HVDC systems. In high power and long distance applications, these systems become more economical than conventional *ac* systems. They also have some other advantages compared with *ac* systems:

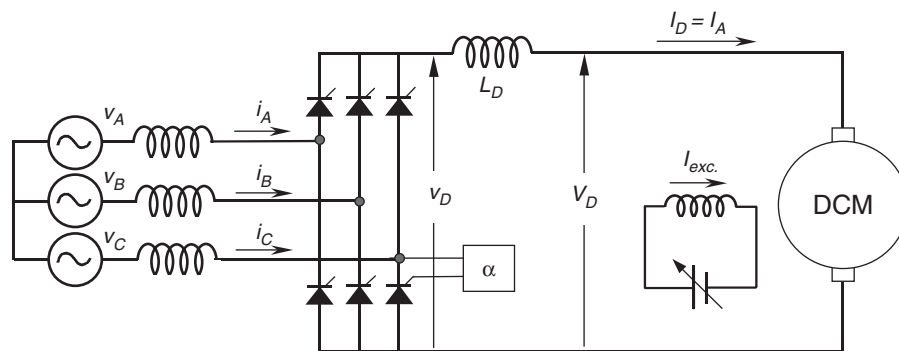1. they can link two *ac* systems operating unsynchronized or with different nominal frequencies, that is 50 ↔ 60 Hz;

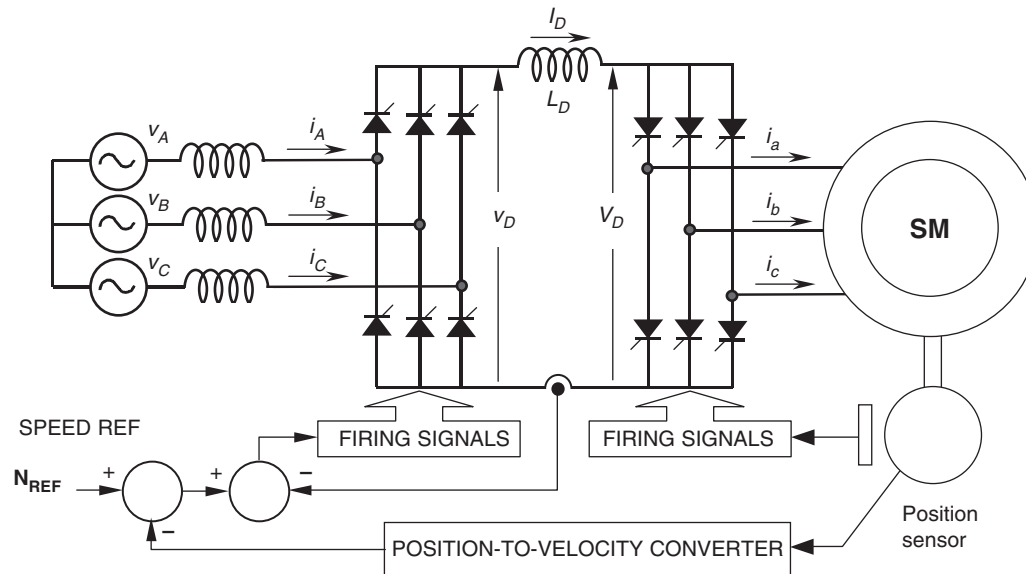**FIGURE 12.26** *DC* machine drive with a six-pulse rectifier.

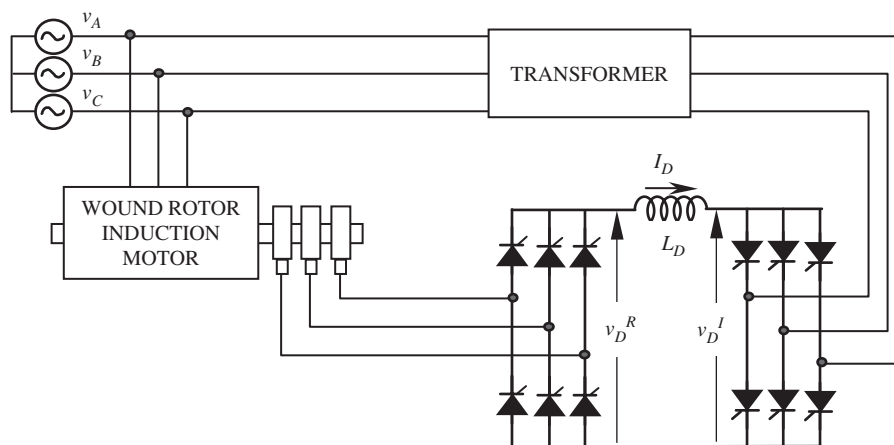**FIGURE 12.27**　Self-controlled synchronous motor drive.

FIGURE 12.28　Supersynchronous cascade for a wound rotor induction motor.

2. they can help in stability problems related with sub-synchronous resonance in long *ac* lines;
3. they have very good dynamic behavior and can interrupt short-circuit problems very quickly;
4. if transmission is by submarine or underground cable, it is not practical to consider *ac* cable systems exceeding 50 km, but *dc* cable transmission systems are in service whose length is in hundreds of kilometers and even distances of 600 km or greater have been considered feasible;
5. reversal of power can be controlled electronically by means of the delay firing angles α; and
6. some existing overhead *ac* transmission lines cannot be increased. If overbuilt with or upgraded to

dc transmission can substantially increase the power transfer capability on the existing right-of-way.

The use of HVDC systems for interconnections of asynchronous systems is an interesting application. Some continental electric power systems consist of asynchronous networks such as those for the East, West, Texas, and Quebec networks in North America, and islands loads such as that for the Island of Gotland in the Baltic Sea make good use of the HVDC interconnections.

Nearly all HVDC power converters with thyristor valves are assembled in a converter bridge of 12-pulse configuration, as shown in Fig. 12.29. Consequently, the *ac* voltages applied to each six-pulse valve group which makes up the 12-pulse
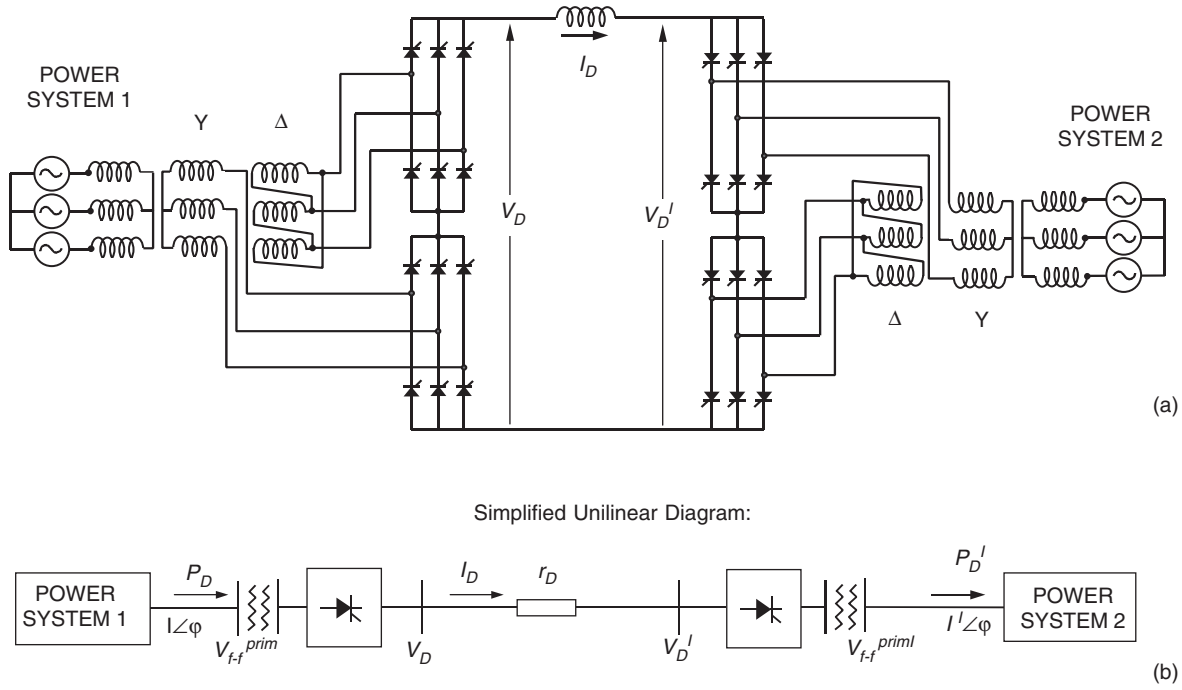
FIGURE 12.29 Typical HVDC power system: (a) detailed circuit and (b) unilinear diagram.

valve group have a phase difference of 30° which is utilized to cancel the *ac* side, 5th and 7th harmonic currents and *dc* side, 6th harmonic voltage, thus resulting in a significant saving in harmonic filters.

Some useful relations for HVDC systems include:

a) Rectifier Side:

$$P_D = V_D \cdot I_D = \sqrt{3} \cdot V_{f-f}^{prim} \cdot I_{line}^{rms} \cos \varphi \qquad (12.40)$$
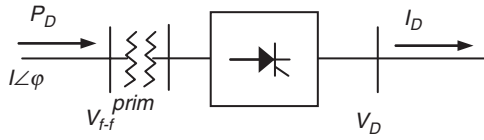
$$I_P = I \cos \varphi$$

$$I_Q = I \sin \varphi$$

$$\therefore P_D = V_D \cdot I_D = \sqrt{3} \cdot V_{f-f}^{prim} \cdot I_P \qquad (12.41)$$

$$I_P = \frac{V_D \cdot I_D}{\sqrt{3} \cdot V_{f-f}^{prim}} \qquad (12.42)$$

$$I_P = \frac{a^2\sqrt{3} \cdot V_{f-f}^{prim}}{4\pi \cdot \omega L_S} [\cos 2\alpha - \cos 2(\alpha + \mu)] \qquad (12.43)$$

$$I_Q = \frac{a^2\sqrt{3} \cdot V_{f-f}^{prim}}{4\pi \cdot \omega L_S} [\sin 2(\alpha + \mu) - \sin 2\alpha - 2\mu] \qquad (12.44)$$

$$I_P = I_D \frac{a\sqrt{6}}{\pi} \left[\frac{\cos \alpha + \cos (\alpha + \mu)}{2} \right] \qquad (12.45)$$

Fundamental secondary component of I

$$I = \frac{a\sqrt{6}}{\pi} I_D \qquad (12.46)$$

Replacing Eq. (12.46) in (12.45)

$$I_P = I \cdot \left[\frac{\cos \alpha + \cos (\alpha + \mu)}{2} \right] \qquad (12.47)$$

as $I_P = I \cos \varphi$, it yields Fig. 12.30a

$$\cos \varphi = \left[\frac{\cos \alpha + \cos (\alpha + \mu)}{2} \right] \qquad (12.48)$$

b) Inverter Side:
The same equations are applied for the inverter side, but the firing angle α is replaced by γ, where γ is

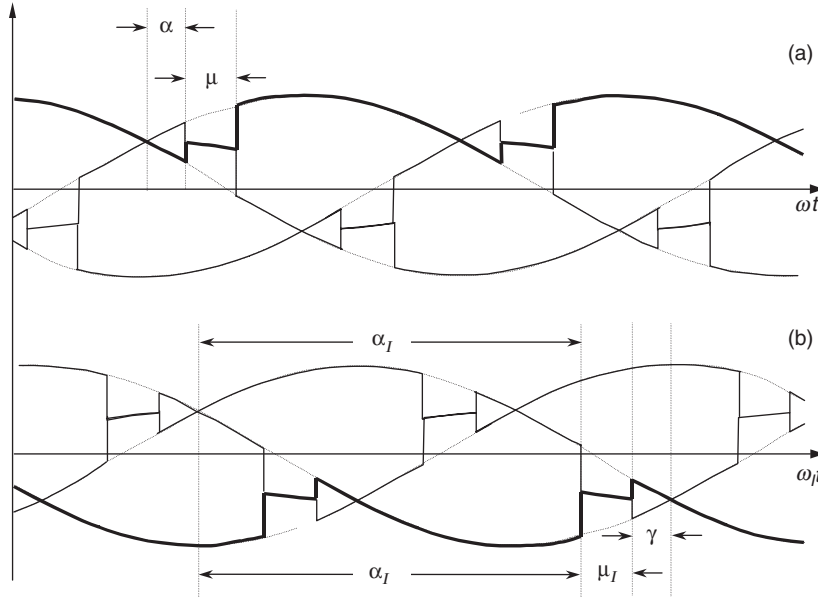$$\gamma = 180° - (\alpha + \mu) \qquad (12.49)$$

FIGURE 12.30   Definition of angle γ for inverter side: (a) rectifier side and (b) inverter side.
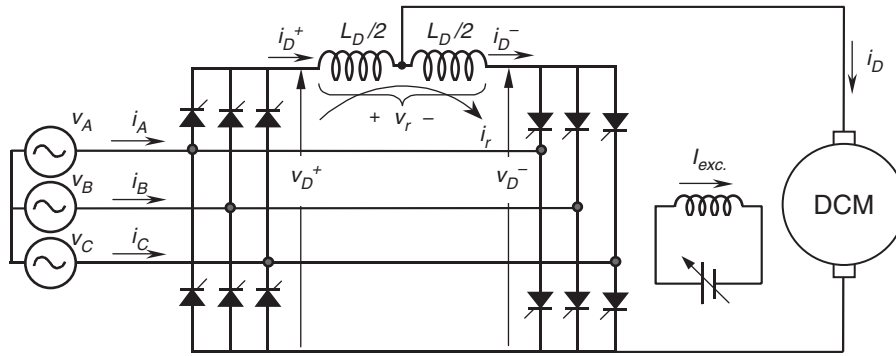

FIGURE 12.31   Dual converter in a four-quadrant *dc* drive.

As reactive power always goes in the converter direction, Eq. (12.44) for inverter side becomes (Fig. 12.30b)

$$I_{QI} = -\frac{a_I^2 \sqrt{3} \cdot V_{f-f_I}^{prim}}{4\pi \cdot \omega_I L_I} \left[\sin 2(\gamma + \mu_I) - \sin 2\gamma - 2\mu_I \right]$$

$$(12.50)$$

12.2.12 Dual Converters

In many variable-speed drives, four-quadrant operation is required, and three-phase dual converters are extensively used in applications up to 2 MW level. Figure 12.31 shows a three-phase dual converter, where two converters are connected back-to-back.

In the dual converter, one rectifier provides the positive current to the load and the other the negative current. Due to the instantaneous voltage differences between the output

voltages of the converters, a circulating current flows through the bridges. The circulating current is normally limited by circulating reactor, L_D, as shown in Fig. 12.31. The two converters are controlled in such a way that if α^+ is the delay angle of the positive current converter, the delay angle of the negative current converter is $\alpha^- = 180° - \alpha^+$.

Figure 12.32 shows the instantaneous *dc* voltages of each converter, v_D^+ and v_D^-. Despite the average voltage V_D is the same in both the converters, their instantaneous voltage differences shown as voltage v_r, are producing the circulating current i_r, which is superimposed with the load currents i_D^+ and i_D^-.

To avoid the circulating current i_r, it is possible to implement a "circulating current free" converter if a dead time of a few milliseconds is acceptable. The converter section, not required to supply current, remains fully blocked. When a current reversal is required, a logic switch-over system determines
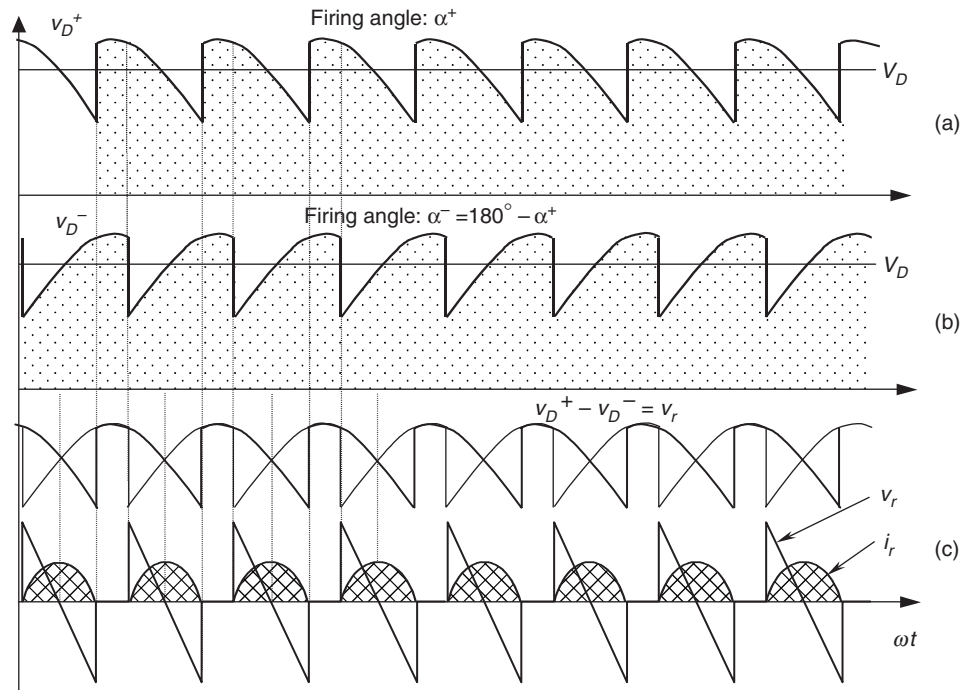
FIGURE 12.32 Waveform of circulating current: (a) instantaneous *dc* voltage from positive converter: (b) instantaneous *dc* voltage from negative converter; and (c) voltage difference between v_D^+ and v_D^-, v_r, and circulating current i_r.

at first the instant at which the conducting converter's current becomes zero. This converter section is then blocked and the further supply of gating pulses to it is prevented. After a short safety interval (dead time), the gating pulses for the other converter section are released.

12.2.13 Cycloconverters

A different principle of frequency conversion is derived from the fact that a dual converter is able to supply an *ac* load with a lower frequency than the system frequency. If the control signal of the dual converter is a function of time, the output voltage will follow this signal. If this control signal value alters sinusoidally with the desired frequency, then the waveform depicted in Fig. 12.33a consists of a single-phase voltage with a large harmonic current. As shown in Fig. 12.33b, if the load is inductive, the current will present less distortion than voltage.

The cycloconverter operates in all four quadrants during a period. A pause (dead time) at least as small as the time required by the switch-over logic occurs after the current reaches zero, that is, between the transfer to operation in the quadrant corresponding to the other direction of current flow.

Three single-phase cycloconverters may be combined to build a three-phase cycloconverter. The three-phase cyclo-converters find an application in low-frequency, high-power requirements. Control speed of large synchronous motors in the low-speed range is one of the most common applications

of three-phase cycloconverters. Figure 12.34 is a diagram for this application. They are also used to control slip frequency in wound rotor induction machines, for supersynchronous cascade (Scherbius system).

12.2.14 Harmonic Standards and Recommended Practices

In view of the proliferation of the power converter equipment connected to the utility system, various national and international agencies have been considering limits on harmonic current injection to maintain good power quality. As a consequence, various standards and guidelines have been established that specify limits on the magnitudes of harmonic currents and harmonic voltages.

The Comité Européen de Normalisation Electrotechnique (CENELEC), International Electrical Commission (IEC), and West German Standards (VDE) specify the limits on the voltages (as a percentage of the nominal voltage) at various harmonics frequencies of the utility frequency, when the equipment-generated harmonic currents are injected into a network whose impedances are specified.

According with Institute of Electrical and Electronic Engineers-519 standards (IEEE), Table 12.1 lists the limits on the harmonic currents that a user of power electronics equipment and other non-linear loads is allowed to inject into the
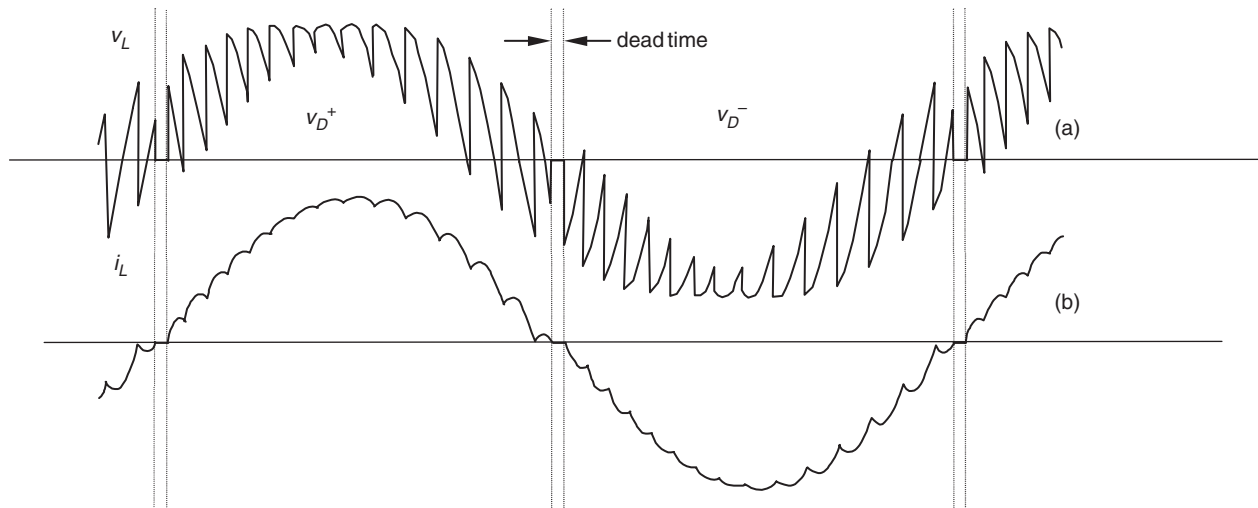
FIGURE 12.33 Cycloconverter operation: (a) voltage waveform and (b) current waveform for inductive load.
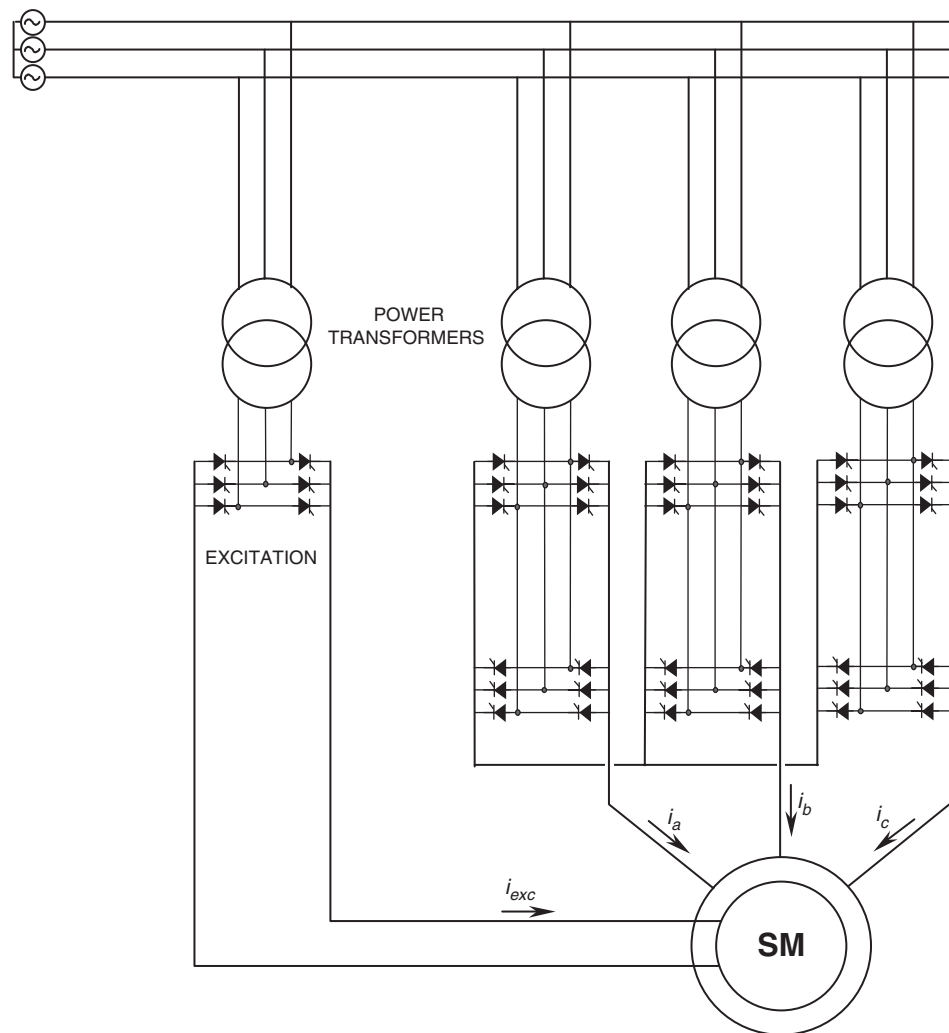

FIGURE 12.34 Synchronous machine drive with a cycloconverter.

TABLE 12.1 Harmonic current limits in percent of fundamental

Short circuit current (pu)	$h < 11$	$11 < h < 17$	$17 < h < 23$	$23 < h < 35$	$35 < h$	*THD*
<20	4.0	2.0	1.5	0.6	0.3	5.0
20–50	7.0	3.5	2.5	1.0	0.5	8.0
50–100	10.0	4.5	4.0	1.5	0.7	12.0
100–1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

TABLE 12.2 Harmonic voltage limits in percent of fundamental

Voltage level	2.3–69 kV	69–138 kV	>138 kV
Maximum for individual harmonic	3.0	1.5	1.0
Total harmonic distortion (*THD*)	5.0	2.5	1.5

utility system. Table 12.2 lists the quality of voltage that the utility can furnish the user.

In Table 12.1, the values are given at the point of connection of non-linear loads. The *THD* is the total harmonic distortion given by Eq. (12.51) and *h* is the number of the harmonic.

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \qquad (12.51)$$

The total current harmonic distortion allowed in Table 12.1 increases with the value of short circuit current.

The total harmonic distortion in the voltage can be calculated in a manner similar to that given by Eq. (12.51). Table 12.2 specifies the individual harmonics and the *THD* limits on the voltage that the utility supplies to the user at the connection point.

12.3 Force-commutated Three-phase Controlled Rectifiers

12.3.1 Basic Topologies and Characteristics

Force-commutated rectifiers are built with semiconductors with gate-turn-off capability. The gate-turn-off capability allows full control of the converter, because valves can be switched *ON* and *OFF* whenever is required. This allows the commutation of the valves, hundreds of times in one period which is not possible with line-commutated rectifiers, where thyristors are switched *ON* and *OFF* only once a cycle. This feature has the following advantages: (a) the current or voltage can be modulated (PWM), generating less harmonic contamination; (b) power factor can be controlled and even it can be made leading; and (c) they can be built as voltage source or current source rectifiers; (d) the reversal of power in thyristor rectifiers is by reversal of voltage at the *dc* link. Instead, force-commutated rectifiers can be implemented for both, reversal of voltage or reversal of current.

There are two ways to implement force-commutated three-phase rectifiers: (a) as a current source rectifier, where power reversal is by *dc* voltage reversal; and (b) as a voltage source rectifier, where power reversal is by current reversal at the *dc* link. Figure 12.35 shows the basic circuits for these two topologies.

12.3.2 Operation of the Voltage Source Rectifier

The voltage source rectifier is by far the most widely used, and because of the duality of the two topologies showed in Fig. 12.35, only this type of force-commutated rectifier will be explained in detail.

The voltage source rectifier operates by keeping the *dc* link voltage at a desired reference value, using a feedback control loop as shown in Fig. 12.36. To accomplish this task, the *dc* link voltage is measured and compared with a reference V_{REF}. The error signal generated from this comparison is used to switch the six valves of the rectifier *ON* and *OFF*. In this way, power can come or return to the *ac* source according with the *dc* link voltage requirements. The voltage V_D is measured at the capacitor C_D.

When the current I_D is positive (rectifier operation), the capacitor C_D is discharged, and the error signal ask the control block for more power from the *ac* supply. The control block takes the power from the supply by generating the appropriate PWM signals for the six valves. In this way, more current flows from the *ac* to the *dc* side and the capacitor voltage is recovered. Inversely, when I_D becomes negative (inverter operation), the capacitor C_D is overcharged and the error signal ask the control to discharge the capacitor and return power to the *ac* mains.

The PWM control can manage not only the active power, but also the reactive power, allowing this type of rectifier to correct power factor. In addition, the *ac* current waveforms can be maintained as almost sinusoidal, which reduces harmonic contamination to the mains supply.
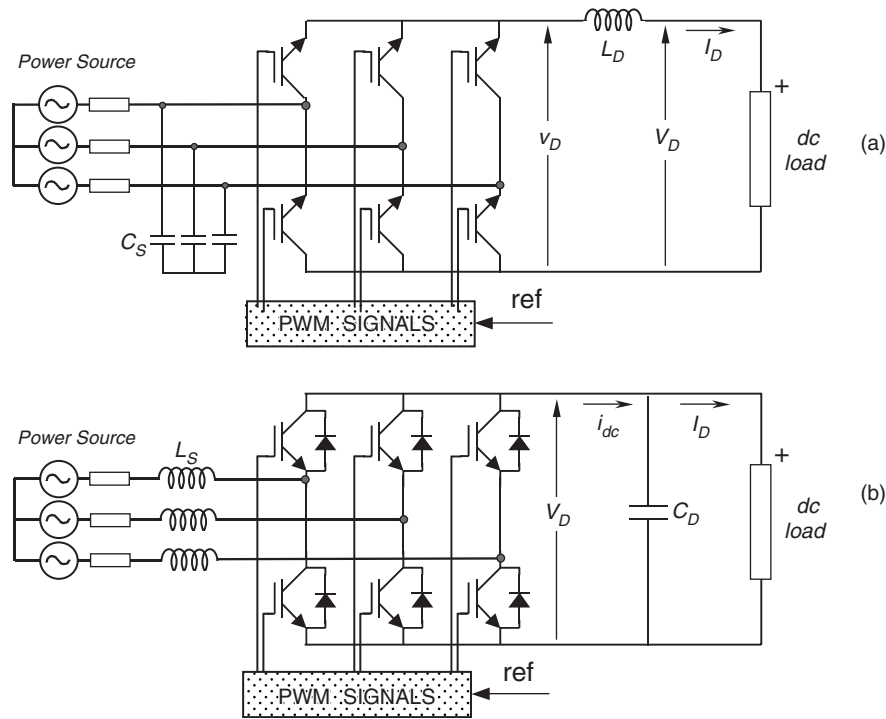
FIGURE 12.35   Basic topologies for force-commutated PWM rectifiers: (a) current source rectifier and (b) voltage source rectifier.
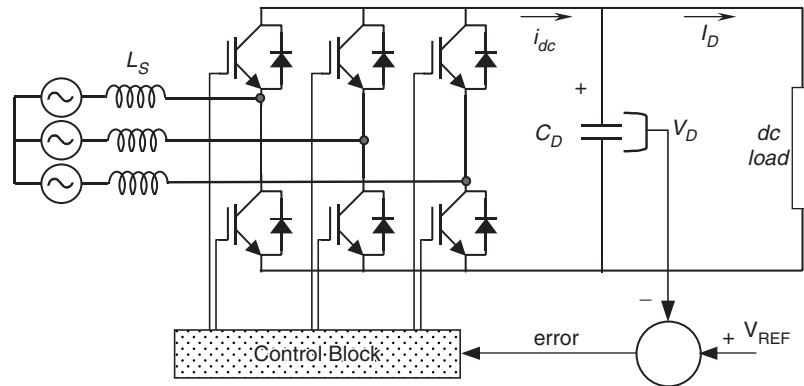

FIGURE 12.36   Operation principle of the voltage source rectifier.

The PWM consists of switching the valves *ON* and *OFF*, following a pre-established template. This template could be a sinusoidal waveform of voltage or current. For example, the modulation of one phase could be as the one shown in Fig. 12.37. This PWM pattern is a periodical waveform whose fundamental is a voltage with the same frequency of the template. The amplitude of this fundamental, called V_{MOD} in Fig. 12.37, is also proportional to the amplitude of the template.

To make the rectifier work properly, the PWM pattern must generate a fundamental V_{MOD} with the same frequency as the power source. Changing the amplitude of this fundamental and its phase shift with respect to the mains, the rectifier can be controlled to operate in the four quadrants: leading power factor rectifier, lagging power factor rectifier, leading power factor inverter, and lagging power factor inverter. Changing the pattern of modulation, as shown in Fig. 12.38, modifies the magnitude of V_{MOD}. Displacing the PWM pattern changes the phase shift.

The interaction between V_{MOD} and V (source voltage) can be seen through a phasor diagram. This interaction permits understanding of the four-quadrant capability of this rectifier. In Fig. 12.39, the following operations are displayed: (a) rectifier at unity power factor; (b) inverter at unity power factor; (c) capacitor (zero power factor); and (d) inductor (zero power factor).
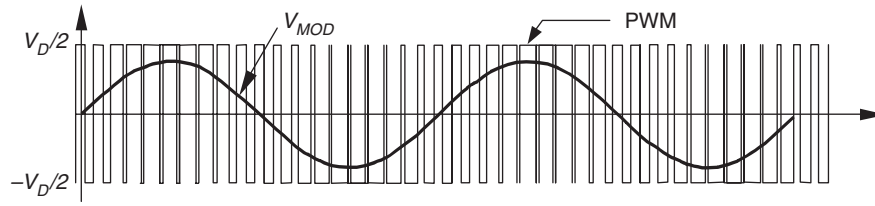
FIGURE 12.37   A PWM pattern and its fundamental V_{MOD}.
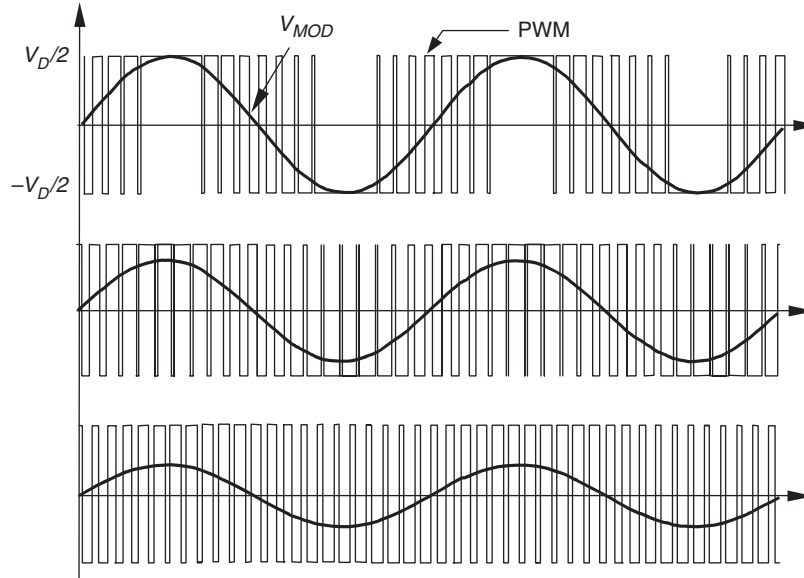
FIGURE 12.38   Changing V_{MOD} through the PWM pattern.

In Fig. 12.39, I_S is the *rms* value of the source current i_s. This current flows through the semiconductors in the way shown in Fig. 12.40. During the positive half cycle, the transistor T_N, connected at the negative side of the *dc* link is switched *ON*, and the current i_s begins to flow through T_N (i_{Tn}). The current returns to the mains and comes back to the valves, closing a loop with another phase, and passing through a diode connected at the same negative terminal of the *dc* link. The current can also go to the *dc* load (inversion) and return through another transistor located at the positive terminal of the *dc* link. When the transistor T_N is switched *OFF*, the current path is interrupted and the current begins to flow through the diode D_P, connected at the positive terminal of the *dc* link. This current, called i_{Dp} in Fig. 12.39, goes directly to the *dc* link, helping in the generation of the current i_{dc}. The current i_{dc} charges the capacitor C_D and permits the rectifier to produce *dc* power. The inductances L_S are very important in this process, because they generate an induced voltage which allows the conduction of the diode D_P. Similar operation occurs during the negative half cycle, but with T_P and D_N (see Fig. 12.40).

Under inverter operation, the current paths are different because the currents flowing through the transistors come mainly from the *dc* capacitor, C_D. Under rectifier operation,

the circuit works like a boost converter and under inverter, it works as a buck converter.

To have full control of the operation of the rectifier, their six diodes must be polarized negatively at all values of instantaneous *ac* voltage supply. Otherwise diodes will conduct, and the PWM rectifier will behave like a common diode rectifier bridge. The way to keep the diodes blocked is to ensure a *dc* link voltage higher than the peak *dc* voltage generated by the diodes alone, as shown in Fig. 12.41. In this way, the diodes remain polarized negatively, and they will conduct only when at least one transistor is switched *ON*, and favorable instantaneous *ac* voltage conditions are given. In the Fig. 12.41, V_D represents the capacitor *dc* voltage, which is kept higher than the normal diode-bridge rectification value v_{BRIDGE}. To maintain this condition, the rectifier must have a control loop like the one displayed in Fig. 12.36.

12.3.3 PWM Phase-to-phase and Phase-to-neutral Voltages

The PWM waveforms shown in the preceding figures are voltages measured between the middle point of the *dc* voltage and the corresponding phase. The phase-to-phase PWM voltages
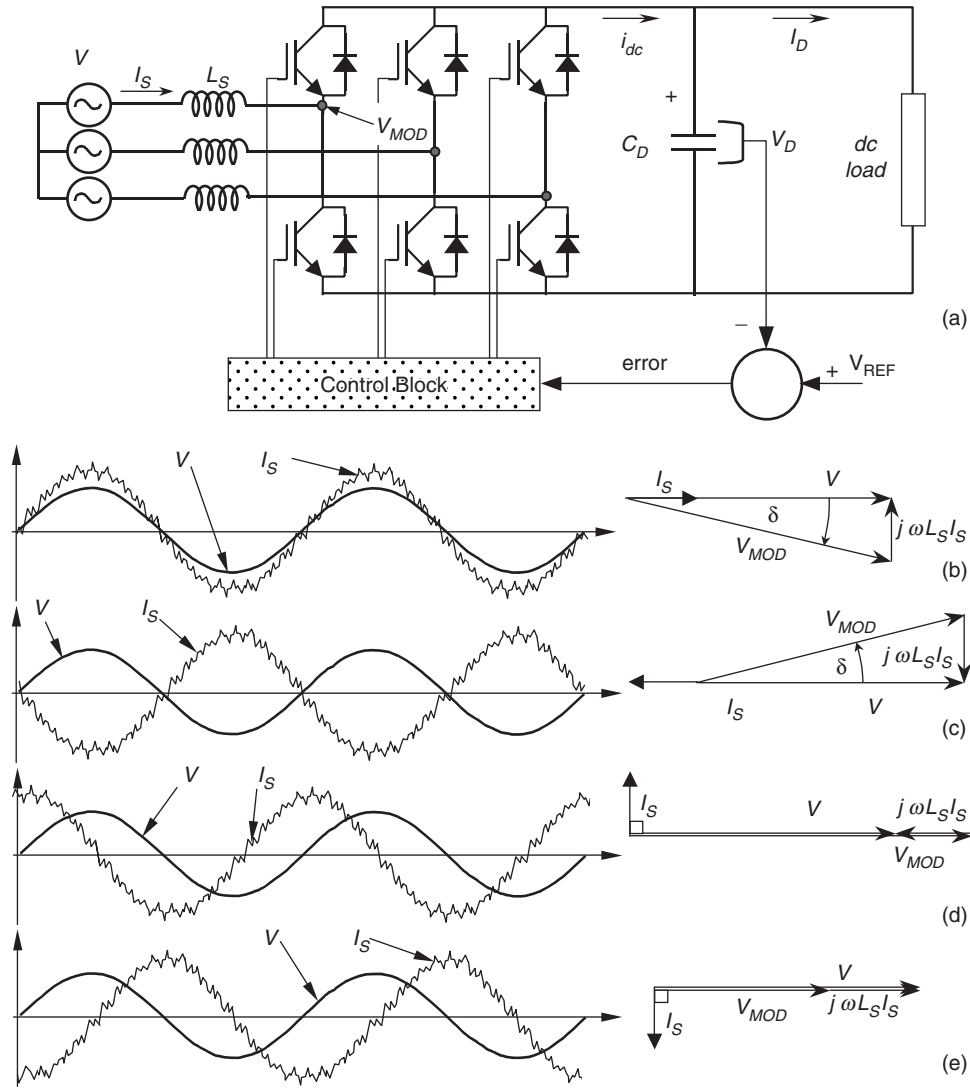
FIGURE 12.39 Four-quadrant operation of the force-commutated rectifier: (a) the PWM force-commutated rectifier; (b) rectifier operation at unity power factor; (c) inverter operation at unity power factor; (d) capacitor operation at zero power factor; and (e) inductor operation at zero power factor.

can be obtained with the help of Eq. (12.52), where the voltage V_{PWM}^{AB} is evaluated.

$$V_{PWM}^{AB} = V_{PWM}^{A} - V_{PWM}^{B} \qquad (12.52)$$

where V_{PWM}^{A} and V_{PWM}^{B} are the voltages measured between the middle point of the *dc* voltage, and the phases *a* and *b* respectively. In a less straightforward fashion, the phase-to-neutral voltage can be evaluated with the help of Eq. (12.53).

$$V_{PWM}^{AN} = \frac{1}{3}(V_{PWM}^{AB} - V_{PWM}^{CA}) \qquad (12.53)$$

where V_{PWM}^{AN} is the phase-to-neutral voltage for phase *a,* and V_{PWM}^{jk} is the phase-to-phase voltage between phase *j* and phase *k.* Figure 12.42 shows the PWM patterns for the phase-to-phase and phase-to-neutral voltages.

12.3.4 Control of the *DC* Link Voltage

Control of the *dc* link voltage requires a feedback control loop. As already explained in Section 12.3.2, the *dc* voltage V_D is compared with a reference V_{REF}, and the error signal "e" obtained from this comparison is used to generate a template waveform. The template should be a sinusoidal waveform with the same frequency of the mains supply. This template is used to produce the PWM pattern and allows controlling
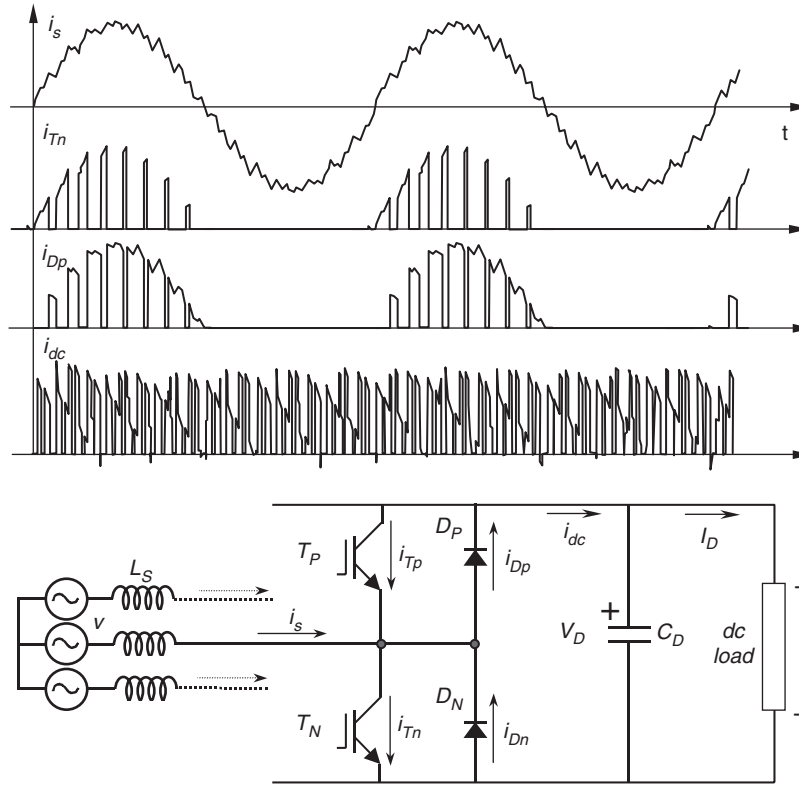
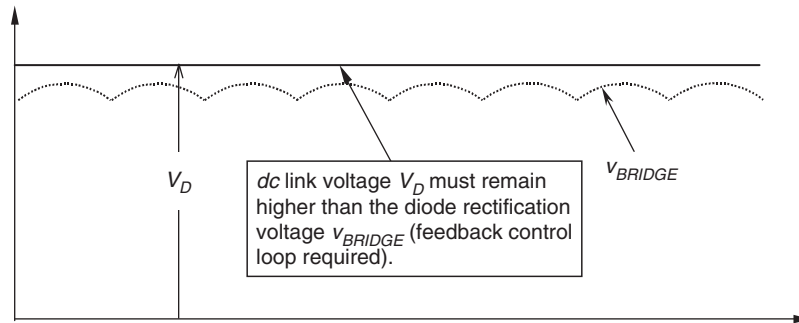**FIGURE 12.40** Current waveforms through the mains, the valves, and the *dc* link.

FIGURE 12.41 The *DC* link voltage condition for the operation of the PWM rectifier.

the rectifier in two different ways: (1) as a voltage-source current-controlled PWM rectifier or (2) as a voltage-source voltage-controlled PWM rectifier. The first method controls the input current, and the second controls the magnitude and phase of the voltage V_{MOD}. The current-controlled method is simpler and more stable than the voltage-controlled method, and for these reasons it will be explained first.

12.3.4.1 Voltage-source Current-controlled PWM Rectifier

This method of control is shown in the rectifier in Fig. 12.43. Control is achieved by measuring the instantaneous phase currents and forcing them to follow a sinusoidal current reference template, I_ref. The amplitude of the current reference template, I_{MAX} is evaluated using the following equation

$$I_{MAX} = G_C \cdot e = G_C \cdot (V_{REF} - v_D) \qquad (12.54)$$

where G_C is shown in Fig. 12.43 and represents a controller such as PI, P, Fuzzy, or other. The sinusoidal waveform of the template is obtained by multiplying I_{MAX} with a sine function, with the same frequency of the mains, and with the desired phase-shift angle φ, as shown in Fig. 12.43. Further, the template must be synchronized with the power supply. After that,
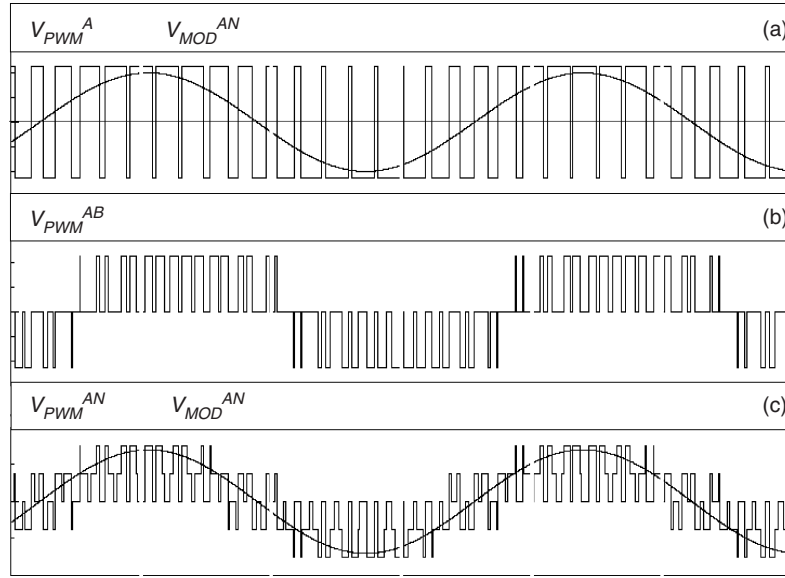
FIGURE 12.42 PWM phase voltages: (a) PWM phase modulation; (b) PWM phase-to-phase voltage; and (c) PWM phase-to-neutral voltage.
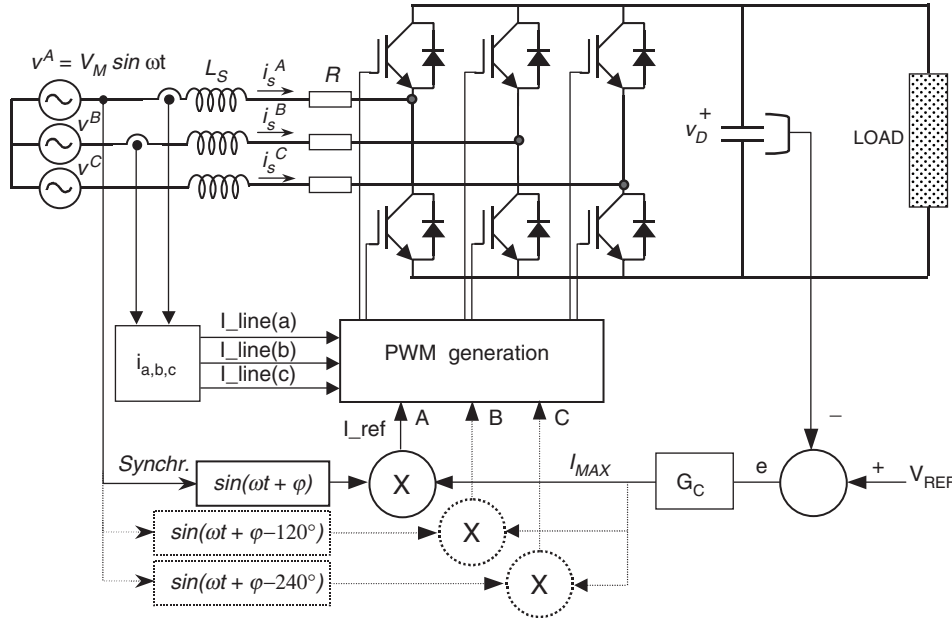

FIGURE 12.43 Voltage-source current-controlled PWM rectifier.

the template has been created and is ready to produce the PWM pattern.

However, one problem arises with the rectifier because the feedback control loop on the voltage V_C can produce instability. Then it becomes necessary to analyze this problem during rectifier design. Upon introducing the voltage feedback and the G_C controller, the control of the rectifier can be represented in a block diagram in Laplace dominion, as shown in Fig. 12.44. This block diagram represents a linearization of the system around an operating point, given by the *rms* value of the input current, I_S.

The blocks $G_1(s)$ and $G_2(s)$ in Fig. 12.44 represent the transfer function of the rectifier (around the operating point) and the transfer function of the *dc* link capacitor C_D respectively.

$$G_1(s) = \frac{\Delta P_1(s)}{\Delta I_S(s)} = 3 \cdot (V \cos \varphi - 2RI_S - L_S I_S s) \quad (12.55)$$

$$G_2(s) = \frac{\Delta V_D(s)}{\Delta P_1(s) - \Delta P_2(s)} = \frac{1}{V_D \cdot C_D \cdot s} \quad (12.56)$$

where $\Delta P_1(s)$ and $\Delta P_2(s)$ represent the input and output power of the rectifier in Laplace dominion, V the *rms* value of
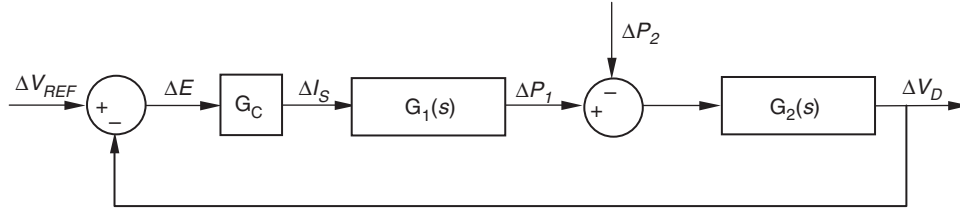
FIGURE 12.44 Closed-loop rectifier transfer function.

the mains voltage supply (phase-to-neutral), I_S the input current being controlled by the template, L_S the input inductance, and R the resistance between the converter and power supply. According to stability criteria, and assuming a *PI* controller, the following relations are obtained

$$I_S \leq \frac{C_D \cdot V_D}{3K_P \cdot L_S} \qquad (12.57)$$

$$I_S \leq \frac{K_P \cdot V \cdot \cos\varphi}{2R \cdot K_P + L_S \cdot K_I} \qquad (12.58)$$

These two relations are useful for the design of the current-controlled rectifier. They relate the values of *dc* link capacitor, *dc* link voltage, *rms* voltage supply, input resistance and inductance, and input power factor, with the *rms* value of the input current, I_S. With these relations the proportional and integral gains K_P and K_I can be calculated to ensure the stability of the rectifier. These relations only establish limitations for rectifier operation, because negative currents always satisfy the inequalities.

With these two stability limits satisfied, the rectifier will keep the *dc* capacitor voltage at the value of V_{REF} (*PI* controller), for all load conditions, by moving power from the *ac* to the *dc* side. Under inverter operation, the power will move in the opposite direction.

Once the stability problems have been solved and the sinusoidal current template has been generated, a modulation method will be required to produce the PWM pattern for the power valves. The PWM pattern will switch the power valves to force the input currents I_line to follow the desired current template I_ref. There are many modulation methods in the literature, but three methods for voltage-source current-controlled rectifiers are the most widely used ones: *periodical sampling* (PS), *hysteresis band* (HB), and *triangular carrier* (TC).

The PS method switches the power transistors of the rectifier during the transitions of a square wave clock of fixed frequency: the *periodical sampling* frequency. In each transition, a comparison between I_ref and I_line is made, and corrections take place. As shown in Fig. 12.45a, this type of control is very simple to implement: only a comparator and a D-type flip-flop are needed per phase. The main advantage of this method is that the minimum time between switching
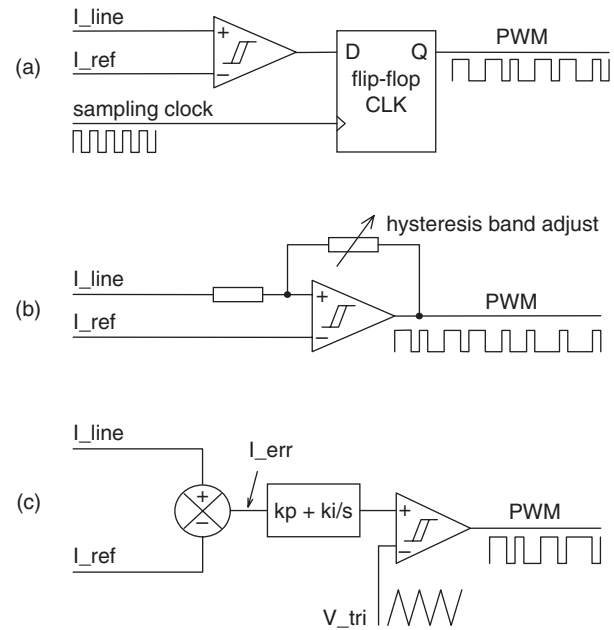

FIGURE 12.45 Modulation control methods: (a) periodical sampling; (b) hysteresis band; and (c) triangular carrier.

transitions is limited to the period of the sampling clock. This characteristic determines the maximum switching frequency of the converter. However, the average switching frequency is not clearly defined.

The HB method switches the transistors when the error between I_ref and I_line exceeds a fixed magnitude: the *hysteresis band*. As it can be seen in Fig. 12.45b, this type of control needs a single comparator with hysteresis per phase. In this case the switching frequency is not determined, but its maximum value can be evaluated through the following equation

$$f_S^{max} = \frac{V_D}{4h \cdot L_S} \qquad (12.59)$$

where h is the magnitude of the hysteresis band.

The TC method, shown in Fig. 12.45c, compares the error between I_ref and I_line with a triangular wave. This triangular wave has fixed amplitude and frequency and is called the *triangular carrier*. The error is processed through a

proportional-integral (PI) gain stage before comparison with the TC takes place. As can be seen, this control scheme is more complex than PS and HB. The values for k_p and k_i determine the transient response and steady-state error of the TC method. It has been found empirically that the values for k_p and k_i shown in Eqs. (12.60) and (12.61) give a good dynamic performance under several operating conditions.

$$k_p = \frac{L_s \cdot \omega_c}{2 \cdot V_D} \qquad (12.60)$$

$$k_i = \omega_c \cdot K_P \qquad (12.61)$$

where L_S is the total series inductance seen by the rectifier, ω_c is the TC frequency, and V_D is the *dc* link voltage of the rectifier.

In order to measure the level of distortion (or undesired harmonic generation) introduced by these three control methods, Eq. (12.62) is defined

$$\%Distortion = \frac{100}{I_{rms}} \sqrt{\frac{1}{T} \int_T (I\_line - I\_ref)^2 \, dt} \qquad (12.62)$$

In Eq. (12.62), the term I_{rms} is the effective value of the desired current. The term inside the square root gives the rms value of the error current, which is undesired. This formula measures the percentage of error (or distortion) of the generated waveform. This definition considers the ripple, amplitude, and phase errors of the measured waveform, as opposed to the *THD*, which does not take into account offsets, scalings, and phase shifts.

Figure 12.46 shows the current waveforms generated by the three aforementioned methods. The example uses an average switching frequency of 1.5 kHz. The PS is the worst, but its digital implementation is simpler. The HB method and TC
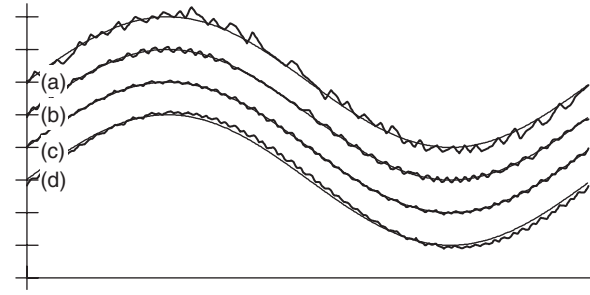

FIGURE 12.46   Waveforms obtained using 1.5 kHz switching frequency and $L_S = 13$ mH: (a) PS method; (b) HB method; (c) TC method ($K_P + K_I$); and (d) TC method (K_P only).

with PI control are quite similar, and the TC with only proportional control gives a current with a small phase shift. However, Fig. 12.47 shows that the higher the switching frequency, the closer the results obtained with the different modulation methods. Over 6 kHz of switching frequency, the distortion is very small for all methods.

12.3.4.2 Voltage-source Voltage-controlled PWM Rectifier

Figure 12.48 shows a one-phase diagram from which the control system for a voltage-source voltage-controlled rectifier is derived. This diagram represents an equivalent circuit of the fundamentals, that is, pure sinusoidal at the mains side and pure *dc* at the *dc* link side. The control is achieved by creating a sinusoidal voltage template V_{MOD}, which is modified in amplitude and angle to interact with the mains voltage *V*. In this way the input currents are controlled without measuring them. The template V_{MOD} is generated using the differential equations that govern the rectifier.
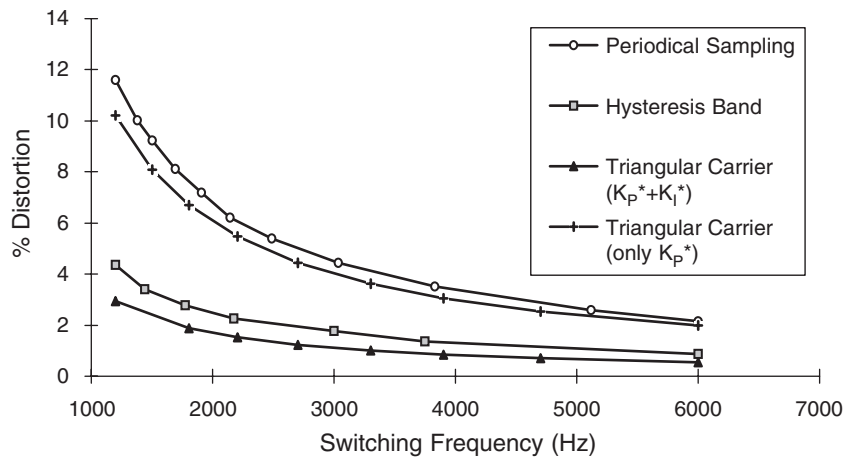

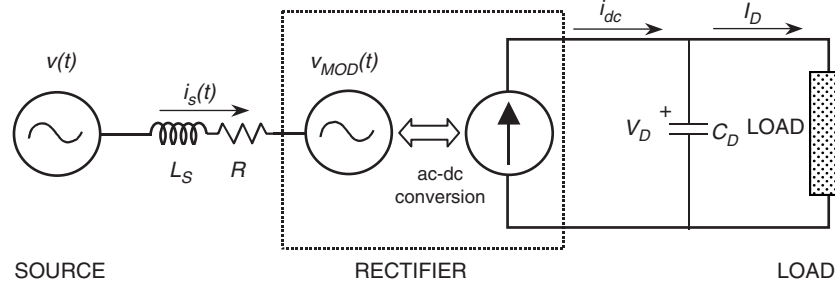**FIGURE 12.47**   Distortion comparison for a sinusoidal current reference.

FIGURE 12.48 One-phase fundamental diagram of the voltage source rectifier.

The following differential equation can be derived from Fig. 12.48

$$v(t) = L_S \frac{di_s}{dt} + Ri_s + v_{MOD}(t) \qquad (12.63)$$

Assuming that $v(t) = V\sqrt{2} \sin \omega t$, then the solution for $i_s(t)$, to acquire a template V_{MOD} able to make the rectifier work at constant power factor, should be of the form

$$i_s(t) = I_{max}(t) \sin(\omega t + \varphi) \qquad (12.64)$$

Equations (12.63), (12.64), and $v(t)$ allows a function of time able to modify V_{MOD} in amplitude and phase that will make the rectifier work at a fixed power factor. Combining these equations with $v(t)$ yields

$$v_{MOD}(t) = \left[V\sqrt{2} + X_S I_{max} \sin \varphi - \left(RI_{max} + L_S \frac{dI_{max}}{dt} \right) \cos \varphi \right] \sin \omega t$$
$$- \left[X_S I_{max} \cos \varphi + \left(RI_{max} + L_S \frac{dI_{max}}{dt} \right) \sin \varphi \right] \cos \omega t$$
$$(12.65)$$

Equation (12.65) provides a template for V_{MOD}, which is controlled through variations of the input current amplitude I_{max}. Substituting the derivatives of I_{max} into Eq. (12.65) make sense, because I_{max} changes every time the *dc* load is modified. The term X_S in Eq. (12.65) is ωL_S. This equation can also be written for unity power factor operation. In such a case, $\cos \varphi = 1$ and $\sin \varphi = 0$.

$$v_{MOD}(t) = \left(V\sqrt{2} - RI_{max} - L_S \frac{dI_{max}}{dt} \right) \sin \omega t$$
$$- X_S I_{max} \cos \omega t \qquad (12.66)$$

With this last equation, a unity power factor, voltage source, voltage-controlled PWM rectifier can be implemented as shown in Fig. 12.49. It can be observed that Eqs. (12.65) and (12.66) have an *in-phase* term with the mains supply ($\sin \omega t$) and an *in-quadrature* term ($\cos \omega t$). These two terms allow

the template V_{MOD} to change in magnitude and phase so as to have full unity power factor control of the rectifier.

Compared with the control block of Fig. 12.43, in the voltage-source voltage-controlled rectifier of Fig. 12.49, there is no need to sense the input currents. However, to ensure stability limits as good as the limits of the current-controlled rectifier, the blocks "$-R-sL_S$" and "$-X_S$" in Fig. 12.49, have to emulate and reproduce exactly the real values of R, X_S, and L_S of the power circuit. However, these parameters do not remain constant, and this fact affects the stability of this system, making it less stable than the system showed in Fig. 12.43. In theory, if the impedance parameters are reproduced exactly, the stability limits of this rectifier are given by the same equations as used for the current-controlled rectifier seen in Fig. 12.43 (Eqs. (12.57) and (12.58)).

Under steady-state, I_{max} is constant, and Eq. (12.66) can be written in terms of phasor diagram, resulting in Eq. (12.67). As shown in Fig. 12.50, different operating conditions for the unity power factor rectifier can be displayed with this equation

$$\vec{V}_{MOD} = \vec{V} - R\vec{I}_S - jX_S\vec{I}_S \qquad (12.67)$$

With the sinusoidal template V_{MOD} already created, a modulation method to commutate the transistors will be required. As in the case of current-controlled rectifier, there are many methods to modulate the template, with the most well known the so-called *sinusoidal pulse width modulation* (SPWM), which uses a TC to generate the PWM as shown in Fig. 12.51. Only this method will be described in this chapter.

In this method, there are two important parameters to define: the amplitude modulation ratio or modulation index *m*, and the frequency modulation ratio *p*. Definitions are given by

$$m = \frac{V_{MOD}^{max}}{V_{TRIANG}^{max}} \qquad (12.68)$$

$$p = \frac{f_T}{f_S} \qquad (12.69)$$

where V_{MOD}^{max} and V_{TRIANG}^{max} are the amplitudes of V_{MOD} and V_{TRIANG} respectively. On the other hand, f_S is the frequency of
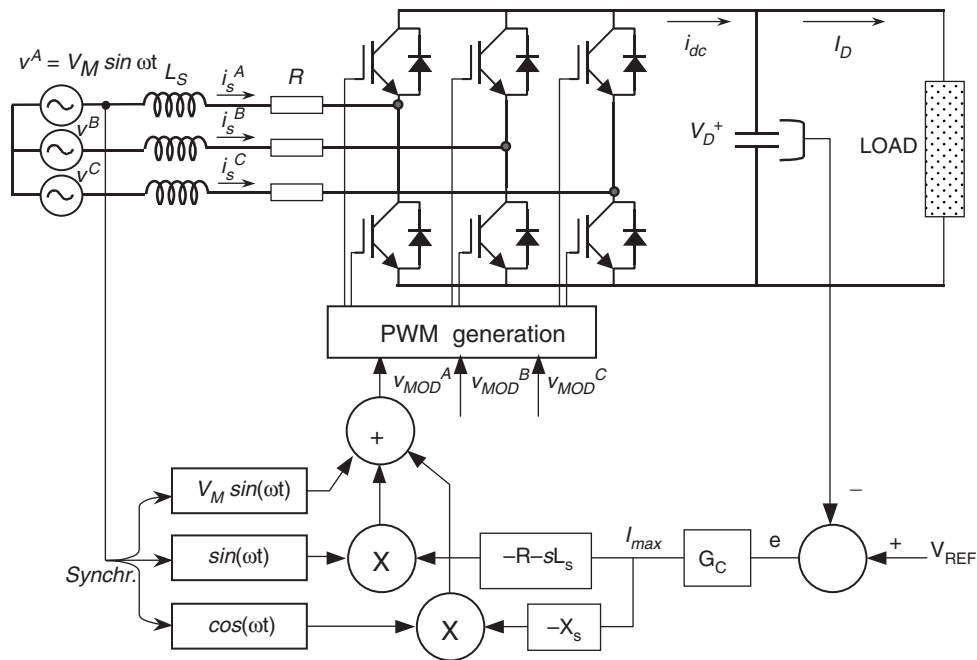
FIGURE 12.49 Implementation of the voltage-controlled rectifier for unity power factor operation.
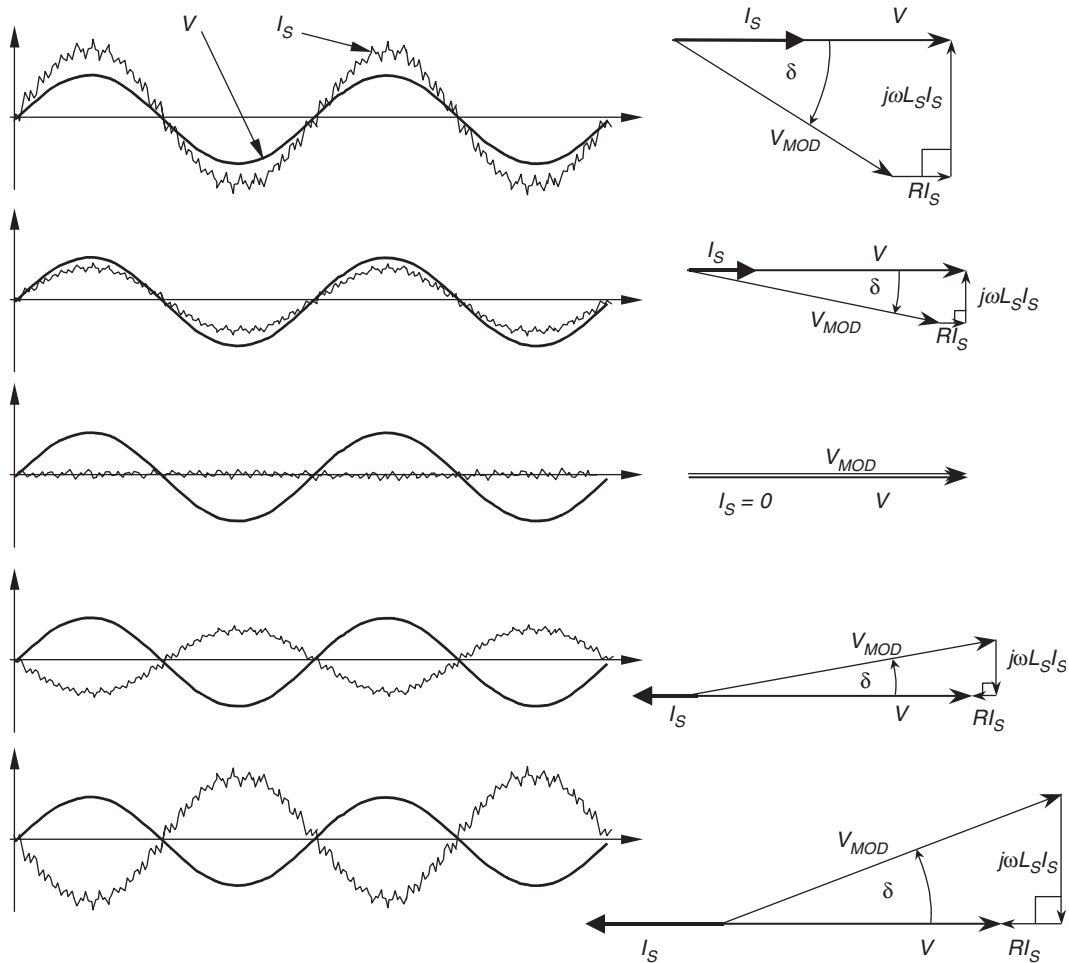

FIGURE 12.50 Steady-state operation of the unity power factor rectifier under different load conditions.
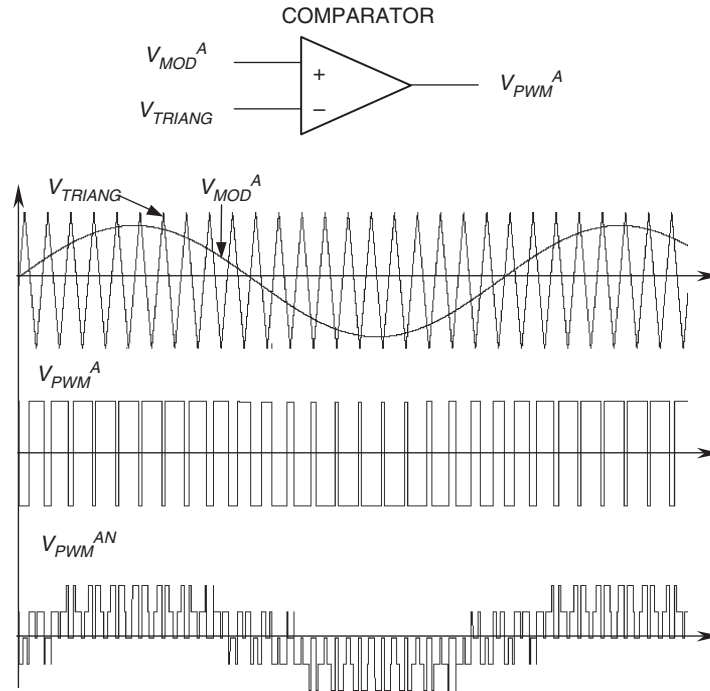
COMPARATOR

$V_{MOD}{}^A$

V_{TRIANG}

$V_{PWM}{}^A$

V_{TRIANG} $V_{MOD}{}^A$

$V_{PWM}{}^A$

$V_{PWM}{}^{AN}$

FIGURE 12.51 Sinusoidal modulation method based on TC.

the mains supply and f_T the frequency of the TC. In Fig. 12.51, $m = 0.8$ and $p = 21$. When $m > 1$ overmodulation is defined.

The modulation method described in Fig. 12.51 has a harmonic content that changes with p and m. When $p < 21$, it is recommended that synchronous PWM be used, which means that the TC and the template should be synchronized. Furthermore, to avoid subharmonics, it is also desired that p be an integer. If p is an odd number, even harmonics will be eliminated. If p is a multiple of 3, then the PWM modulation of the three phases will be identical. When m increases, the amplitude of the fundamental voltage increases proportionally, but some harmonics decrease. Under overmodulation ($m > 1$), the fundamental voltage does not increase linearly, and more harmonics appear. Figure 12.52 shows the harmonic spectrum
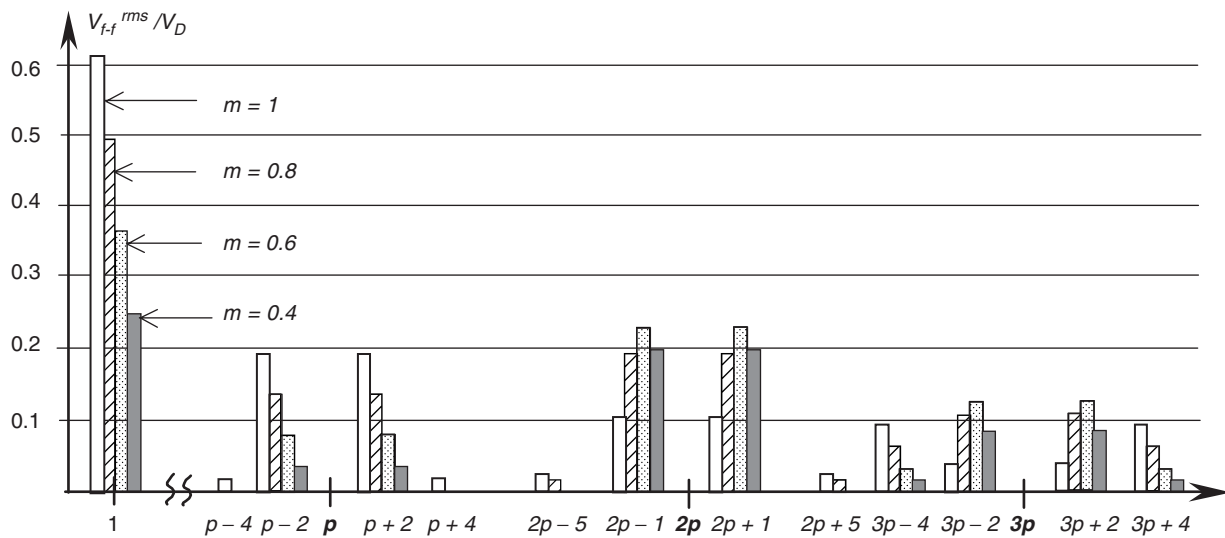
$V_{f\text{-}f}{}^{rms} / V_D$

0.6

0.5

0.4

0.3

0.2

0.1

$m = 1$

$m = 0.8$

$m = 0.6$

$m = 0.4$

1   $p-4$ $p-2$ **p** $p+2$ $p+4$ $2p-5$ $2p-1$ **2p** $2p+1$ $2p+5$ $3p-4$ $3p-2$ **3p** $3p+2$ $3p+4$

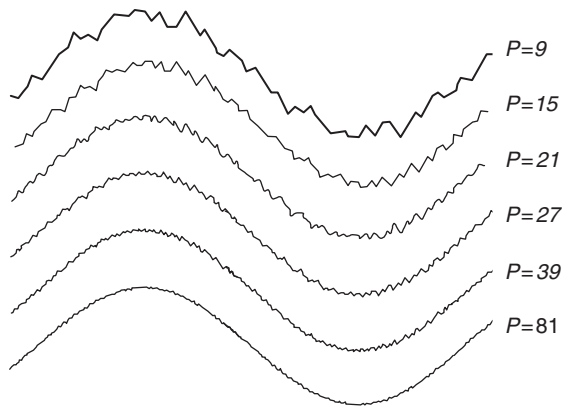**FIGURE 12.52** Harmonic spectrum for SPWM modulation.

FIGURE 12.53   Current waveforms for different values of *p*.

of the three-phase PWM voltage waveforms for different values of *m*, and *p* = 3*k* where *k* is an odd number.

Due to the presence of the input inductance L_S, the harmonic currents that result are proportionally attenuated with the harmonic number. This characteristic is shown in the current waveforms of Fig. 12.53, where larger *p* numbers generate cleaner currents. The rectifier that originated the currents of Fig. 12.53 has the following characteristics: $V_D = 450 \, V_{dc}$, $V_{f-f}^{rms} = 220 \, V_{ac}$, $L_S = 2 \, \text{mH}$, and input current $I_S = 80 \, A_{rms}$. It can be observed that with $p > 21$ the current distortion is quite small. The value of $p = 81$ in Fig. 12.53 produces an almost pure sinusoidal waveform, and it means 4860 Hz

of switching frequency at 60 Hz or only 4.050 Hz in a rectifier operating in a 50 Hz supply. This switching frequency can be managed by MOSFETs, IGBTs, and even Power Darlingtons. Then a number $p = 81$, is feasible for today's low and medium power rectifiers.

12.3.4.3 Voltage-source Load-controlled PWM Rectifier

A simple method of control for small PWM rectifiers (up to 10–20 kW) is based on direct control of the *dc* current. Figure 12.54 shows the schematic of this control system. The fundamental voltage V_{MOD} modulated by the rectifier is produced by a fixed and unique PWM pattern, which can be carefully selected to eliminate most undesirable harmonics. As the PWM does not change, it can be stored in a permanent digital memory (ROM).

The control is based on changing the power angle δ between the mains voltage *V* and fundamental PWM voltage V_{MOD}. When δ changes, the amount of power flow transferred from the *ac* to the *dc* side also changes. When the power angle is negative (V_{MOD} lags *V*), the power flow goes from the *ac* to the *dc* side. When the power angle is positive, the power flows in the opposite direction. Then, the power angle can be controlled through the current I_D. The voltage V_D does not need to be sensed, because this control establishes a stable *dc* voltage operation for each *dc* current and power angle. With these characteristics, it is possible to find a relation between I_D and δ so as to obtain constant *dc* voltage for all load conditions.
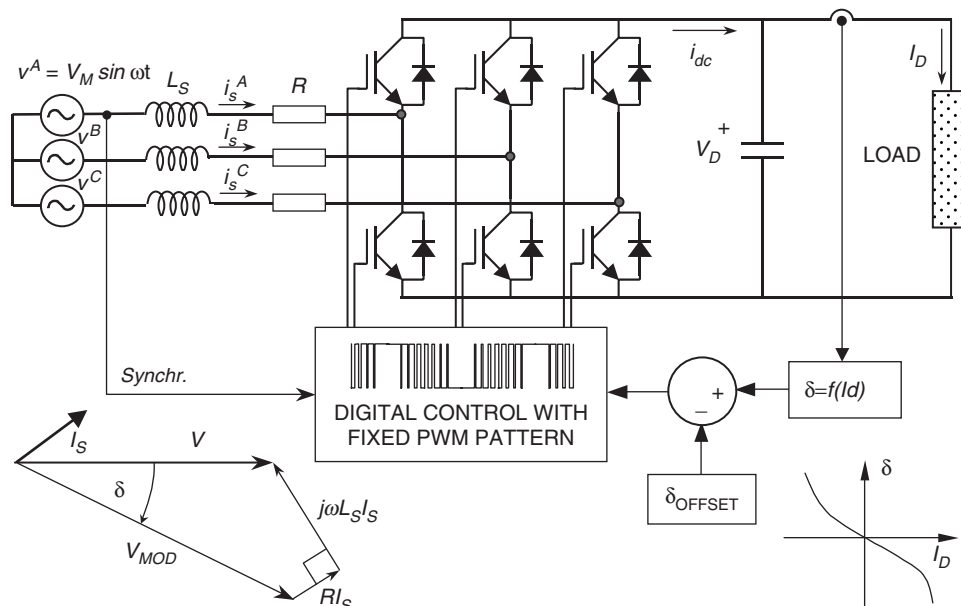

FIGURE 12.54   Voltage-source load-controlled PWM rectifier.

This relation is given by

$$I_D = f(\delta) = \frac{V\left(\cos\delta - \frac{\omega L_S}{R}\sin\delta - 1\right)}{R\left[1 + \left(\frac{\omega L_S}{R}\right)^2\right]} \qquad (12.70)$$

From Eq. (12.70) a plot and a reciprocal function $\delta = f(I_D)$ is obtained to control the rectifier. The relation between I_D and δ allows for leading power factor operation and null regulation. The leading power factor operation is shown in the phasor diagram of Fig. 12.54.

The control scheme of the voltage-source load-controlled rectifier is characterized by the following: (i) there are neither input current sensors nor *dc* voltage sensor; (ii) it works with a fixed and predefined PWM pattern; (iii) it presents very good stability; (iv) its stability does not depend on the size of the *dc* capacitor; (v) it can work at leading power factor for all load conditions; and (vi) it can be adjusted with Eq. (12.70) to work at zero regulation. The drawback appears when *R* in Eq. (12.70) becomes negligible, because in such a case the control system is unable to find an equilibrium point for the *dc* link voltage. That is why this control method is not applicable to large systems.

12.3.5 New Technologies and Applications of Force-commutated Rectifiers

The additional advantages of force-commutated rectifiers with respect to line-commutated rectifiers, make them better candidates for industrial requirements. They permit new applications such as rectifiers with harmonic elimination capability (active filters), power factor compensators, machine drives with four-quadrant operation, frequency links to connect 50 Hz with 60 Hz systems, and regenerative converters for traction power supplies. Modulation with very fast valves such as IGBTs permit almost sinusoidal currents to be obtained. The dynamics of these rectifiers is so fast that they can reverse power almost instantaneously. In machine drives, current source PWM rectifiers, like the one shown in Fig. 12.35a, can be used to drive *dc* machines from the three-phase supply. Four-quadrant applications using voltage-source PWM rectifiers, are extended for induction machines, synchronous machines with starting control, and special machines such as brushless-*dc* motors. Back-to-back systems are being used in Japan to link power systems with different frequencies.

12.3.5.1 Active Power Filter

Force-commutated PWM rectifiers can work as active power filters. The voltage-source current-controlled rectifier has the capability to eliminate harmonics produced by other polluting loads. It only needs to be connected as shown in Fig. 12.55.

The current sensors are located at the input terminals of the power source and these currents (instead of the rectifier currents) are forced to be sinusoidal. As there are polluting loads in the system, the rectifier is forced to deliver the harmonics that loads need, because the current sensors do not allow the harmonics going to the mains. As a result, the rectifier currents become distorted, but an adequate *dc* capacitor C_D can keep the *dc* link voltage in good shape. In this way the rectifier can do its duty, and also eliminate harmonics to the source. In addition, it also can compensate power factor and unbalanced load problems.

12.3.5.2 Frequency Link Systems

Frequency link systems permit power to be transferred form one frequency to another one. They are also useful for linking unsynchronized networks. Line-commutated converters are widely used for this application, but they have some drawbacks that force-commutated converters can eliminate. For example, the harmonic filters requirement, the poor power factor, and the necessity to count with a synchronous compensator when generating machines at the load side are absent. Figure 12.56 shows a typical line-commutated system in which a 60 Hz load is fed by a 50 Hz supply. As the 60 Hz side needs excitation to commutate the valves, a synchronous compensator has been required.

In contrast, an equivalent system with force-commutated converters is simpler, cleaner, and more reliable. It is implemented with a *dc* voltage-controlled rectifier, and another identical converter working in the inversion mode. The power factor can be adjusted independently at the two *ac* terminals, and filters or synchronous compensators are not required. Figure 12.57 shows a frequency link system with force-commutated converters.

12.3.5.3 Special Topologies for High Power Applications

High power applications require series- and/or parallel-connected rectifiers. Series and parallel operation with force-commutated rectifiers allow improving the power quality because harmonic cancellation can be applied to these topologies. Figure 12.58 shows a series connection of force-commutated rectifiers, where the modulating carriers of the valves in each bridge are shifted to cancel harmonics. The example uses sinusoidal PWM that are with TC shifted.

The waveforms of the input currents for the series connection system are shown in Fig. 12.59. The frequency modulation ratio shown in this figure is for $p = 9$. The carriers are shifted by 90° each, to obtain harmonics cancellation. Shifting of the carriers δ_T depends on the number of converters in series (or in parallel), and is given by

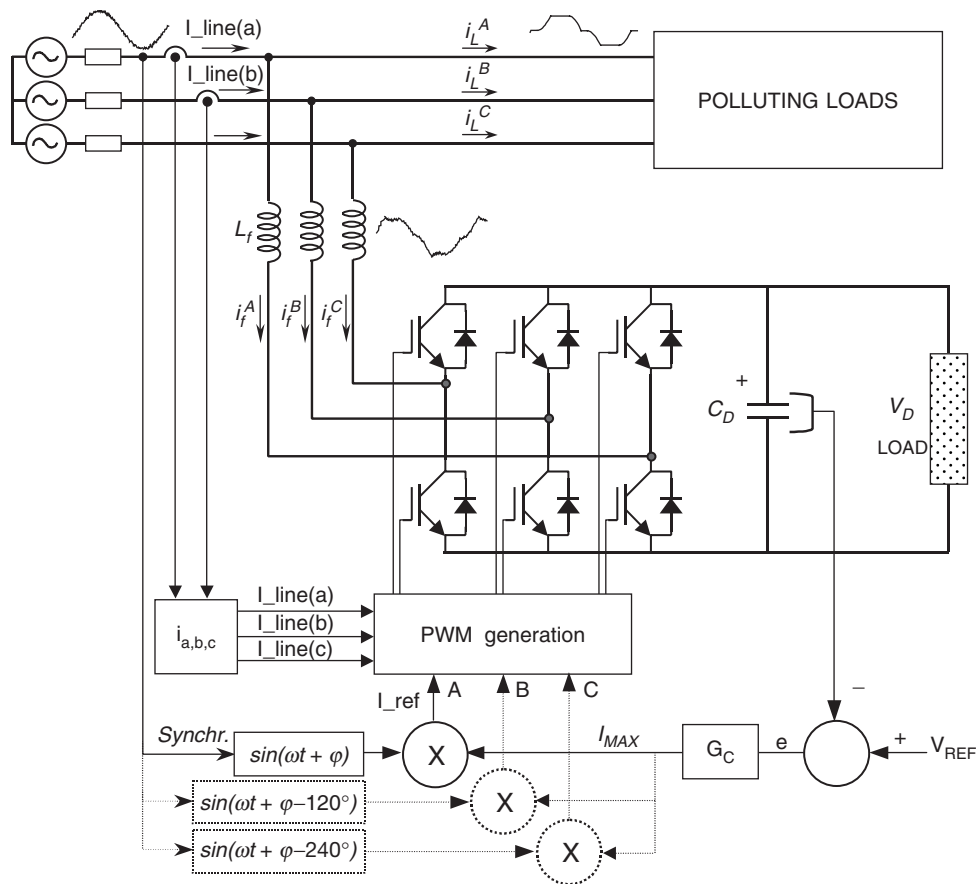$$\delta_T = \frac{2\pi}{n} \qquad (12.71)$$

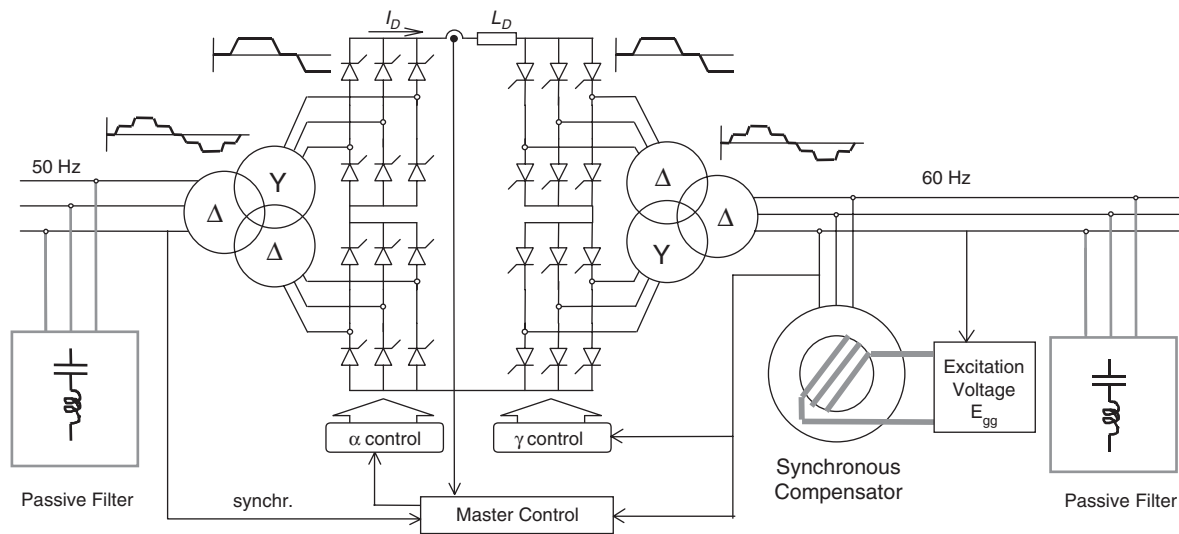**FIGURE 12.55**   Voltage-source rectifier with harmonic elimination capability.

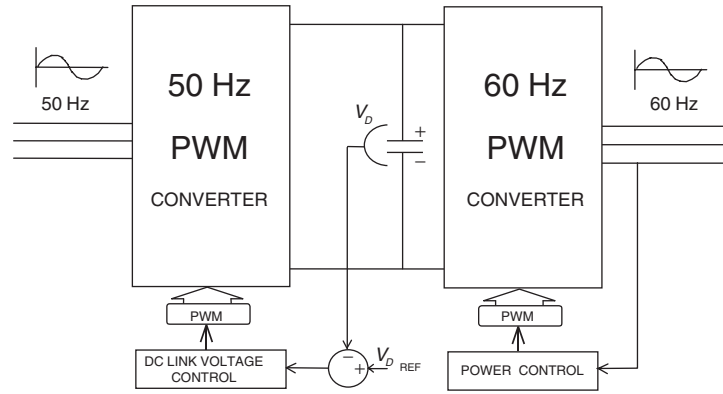**FIGURE 12.56**   Frequency link systems with line-commutated converters.

FIGURE 12.57 Frequency link systems with force-commutated converters.
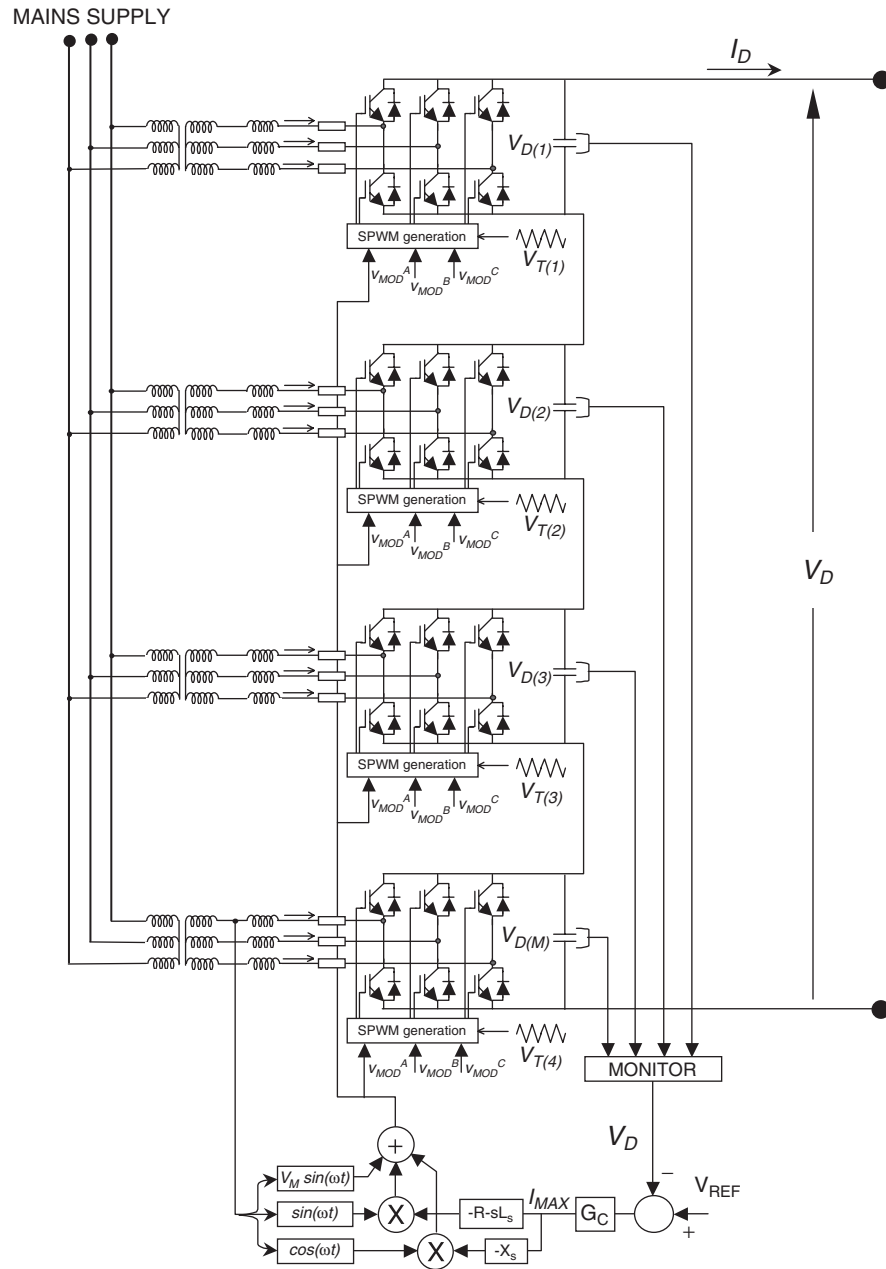

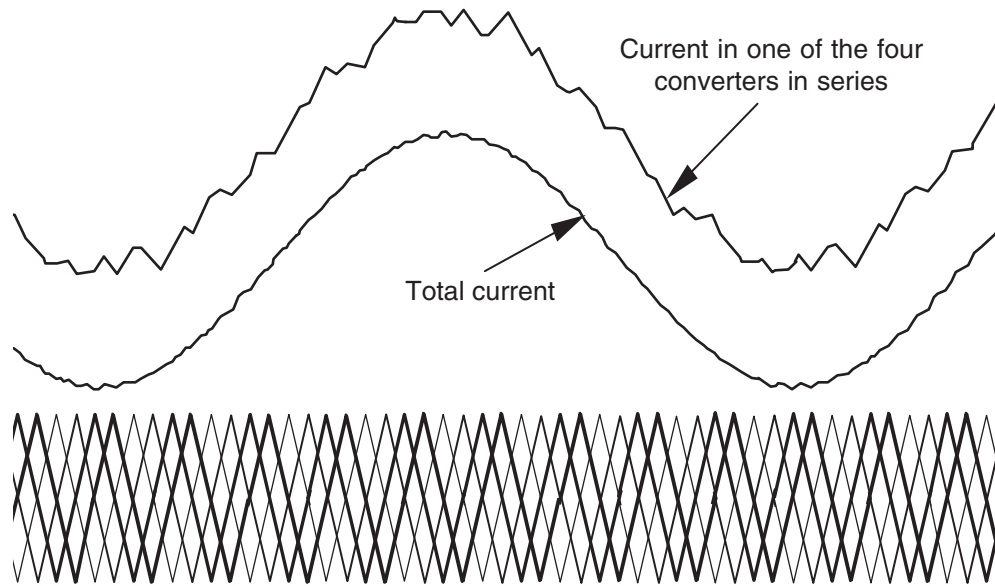**FIGURE 12.58** Series connection system with force-commutated rectifiers.

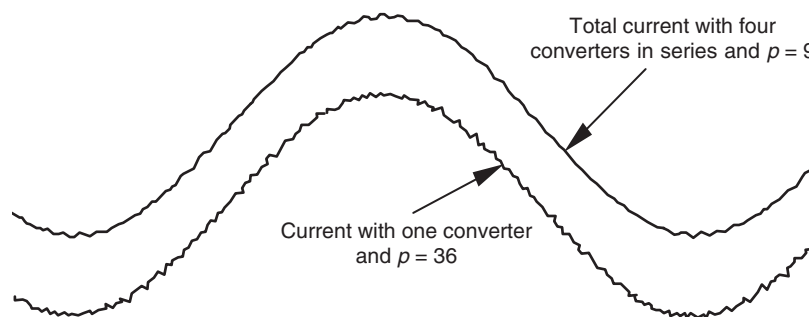**FIGURE 12.59** Input currents and carriers of the series connection system of Fig. 12.58.

FIGURE 12.60 Four converters in series and $p = 9$ compared with one converter and $p = 36$.

where n is the number of converters in series or in parallel. It can be observed that despite the low value of p, the total current becomes quite clean and clear, better than the current of one of the converters in the chain.

The harmonic cancellation with series- or parallel-connected rectifiers, using the same modulation but the carriers shifted, is quite effective. The resultant current is better with n converters and frequency modulation $p = p_1$ than with one converter and $p = n \cdot p_1$. This attribute is verified in Fig. 12.60, where the total current of four converters in series with $p = 9$ and carriers shifted, is compared with the current of only one converter and $p = 36$. This technique also allows for the use of valves with slow commutation times, such as high power GTOs. Generally, high power valves have low commutation times and hence the parallel and/or series options remain very attractive.

Another special topology for high power was implemented for Asea Brown Boveri (ABB) in Bremen. A 100 MW power converter supplies energy to the railways at $16^{2/3}$ Hz. It uses basic "H" bridges like the one shown in Fig. 12.61, connected to the load through power transformers. These transformers are connected in parallel at the converter side, and in series at the load side.

The system uses SPWM with TCs shifted, and depending on the number of converters connected in the chain of bridges, the voltage waveform becomes more and more sinusoidal. Figure 12.62 shows a back-to-back system using a chain of 12 "H" converters connected as showed in Fig. 12.61b.

The *ac* voltage waveform obtained with the topology of Fig. 12.62 is displayed in Fig. 12.63. It can be observed that the voltage is formed by small steps that depend on the number of converters in the chain (12 in this case). The current is almost perfectly sinusoidal.

Figure 12.64 shows the voltage waveforms for different number of converters connected in the bridge. It is clear that the larger the number of converters, the better the voltage.

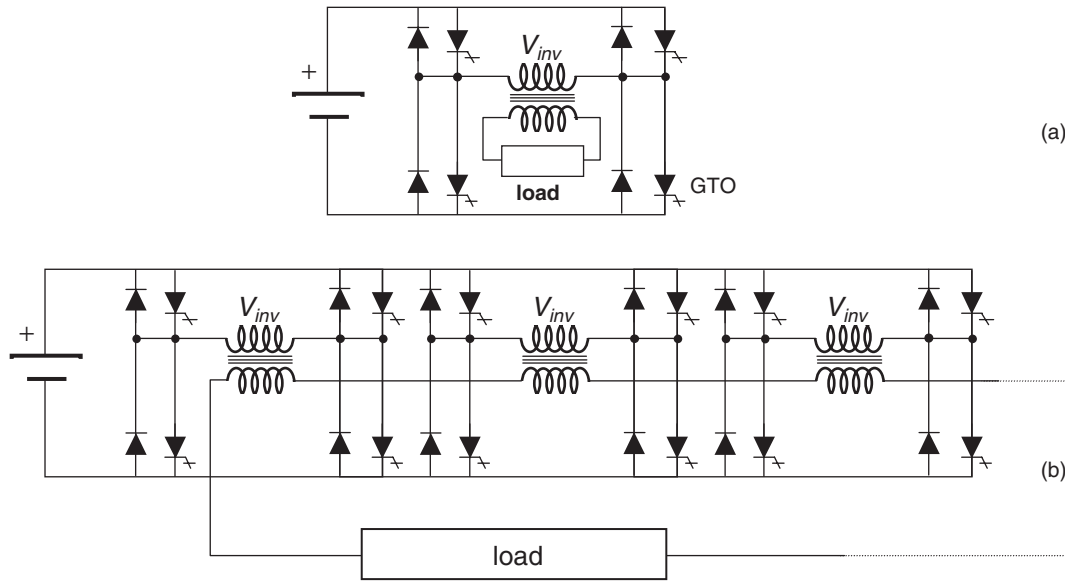Another interesting result with this converter is that the *ac* voltages become modulated by both PWM and amplitude

FIGURE 12.61   The "H" modulator: (a) one bridge and (b) bridges connected in series at load side through isolation transformers.
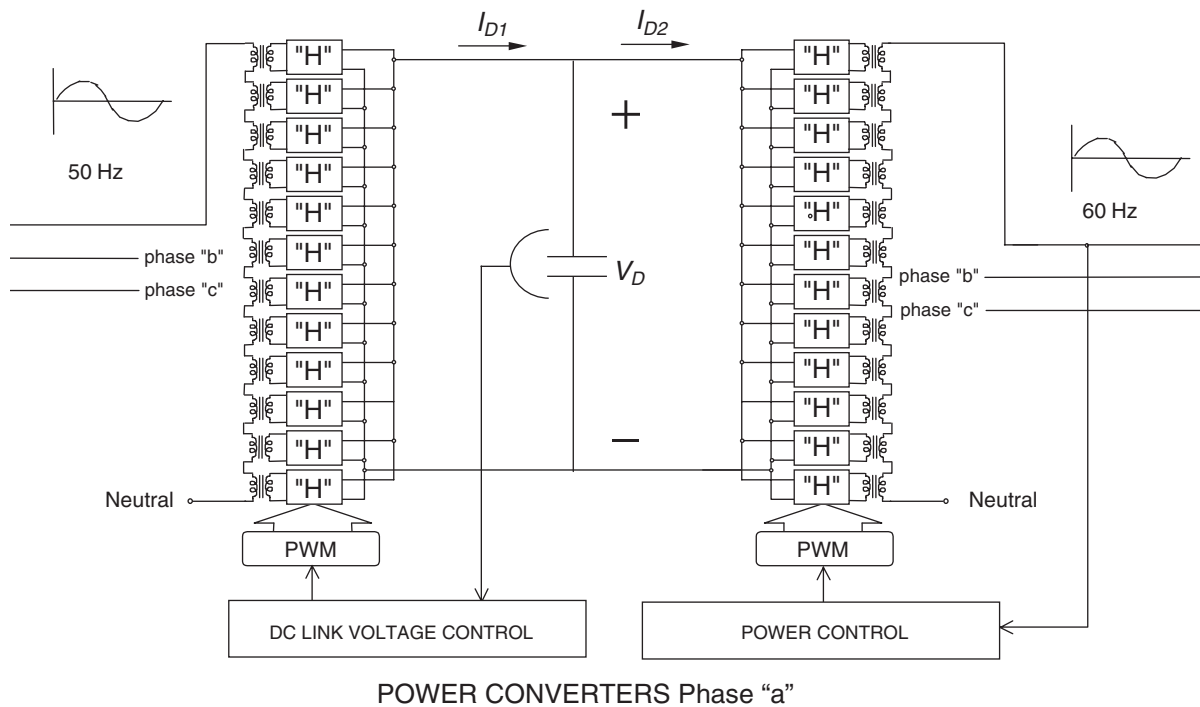

FIGURE 12.62   Frequency link with force-commutated converters and sinusoidal voltage modulation.

modulation (AM). This is because when the pulse modulation changes, the steps of the amplitude change. The maximum number of steps of the resultant voltage is equal to the number of converters. When the voltage decreases, some steps disappear, and then the AM becomes a discrete function. Figure 12.65 shows the AM of the voltage.

12.3.5.4 Machine Drives Applications

One of the most important applications of force-commutated rectifiers is in machine drives. Line-commutated thyristor converters have limited applications because they need excitation to extinguish the valves. This limitation do not allow the use of line-commutated converters in induction machine drives.
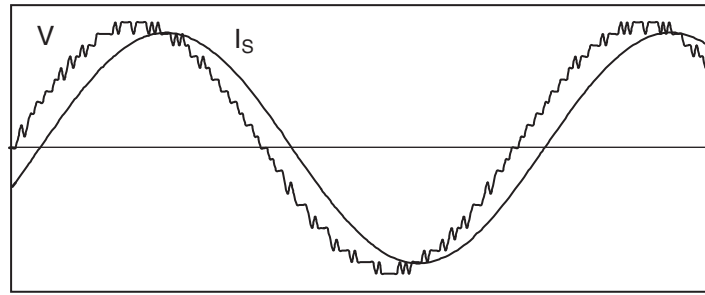
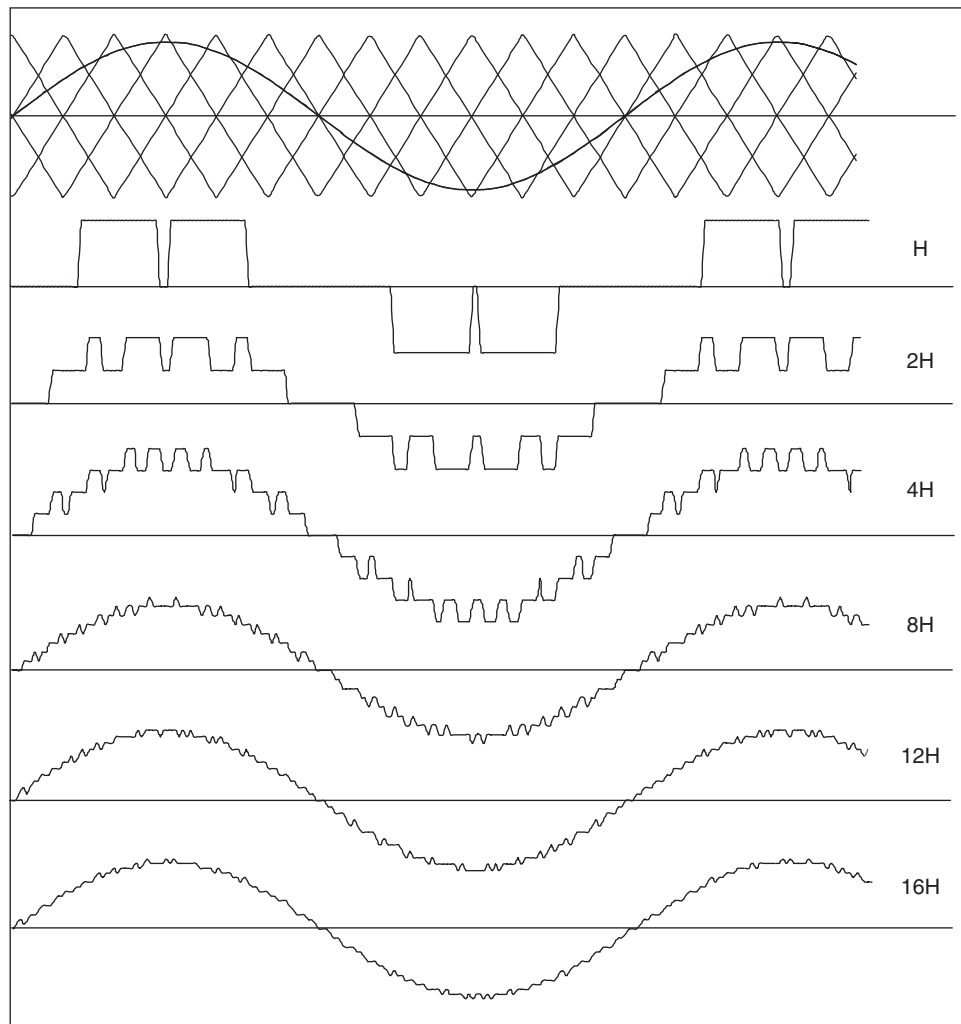**FIGURE 12.63**   Voltage and current waveforms with 12 converters.

FIGURE 12.64   Voltage waveforms with different numbers of "H" bridges in series.

On the other hand, with force-commutated converters four-quadrant operation is achievable. Figure 12.66 shows a typical frequency converter with a force-commutated rectifier–inverter link. The rectifier side controls the *dc* link, and the inverter side controls the machine. The machine can be a synchronous, brushless *dc*, or induction machine. The reversal of both speed and power are possible with this topology. At the rectifier side, the power factor can be controlled, and even with an inductive load such as an induction machine, the source can "see" the load as capacitive or resistive. Changing the frequency of the inverter controls the machine speed, and the torque is controlled through the stator currents and
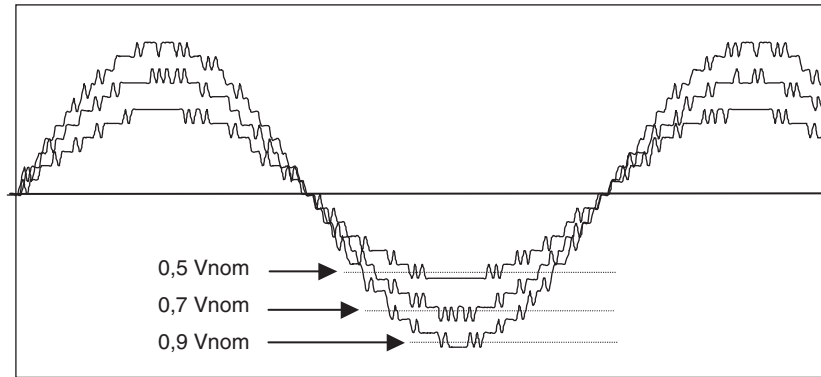
FIGURE 12.65   Amplitude modulation of the "H" bridges of Fig. 12.62.

0,5 Vnom
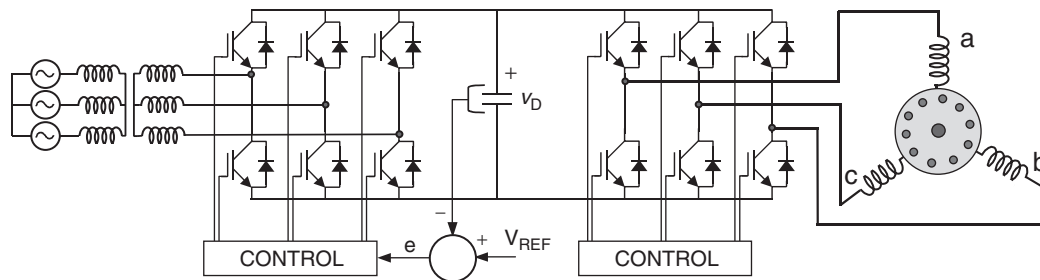0,7 Vnom
0,9 Vnom

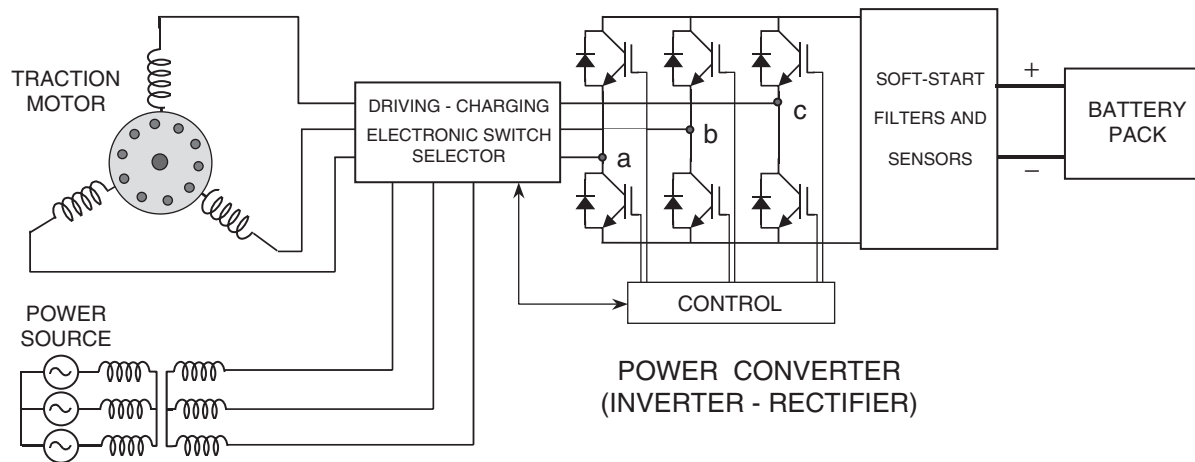**FIGURE 12.66**   Frequency converter with force-commutated converters.

FIGURE 12.67   Electric bus system with regenerative braking and battery charger.

torque angle. The inverter will become a rectifier during regenerative braking, which is possible by making slip negative in an induction machine, or by making the torque angle negative in synchronous and brushless *dc* machines.

A variation of the drive of Fig. 12.66 is found in electric traction applications. Battery powered vehicles use the inverter as a rectifier during regenerative braking, and sometimes the inverter is also used as a battery charger. In this case, the rectifier can be fed by a single-phase or three-phase system.

Figure 12.67 shows a battery-powered electric bus system. This system uses the power inverter of the traction motor as rectifier for two purposes: regenerative braking and as a battery charger fed by a three-phase power source.

12.3.5.5 Variable Speed Power Generation

Power generation at 50 or 60 Hz requires constant speed machines. In addition, induction machines are not currently
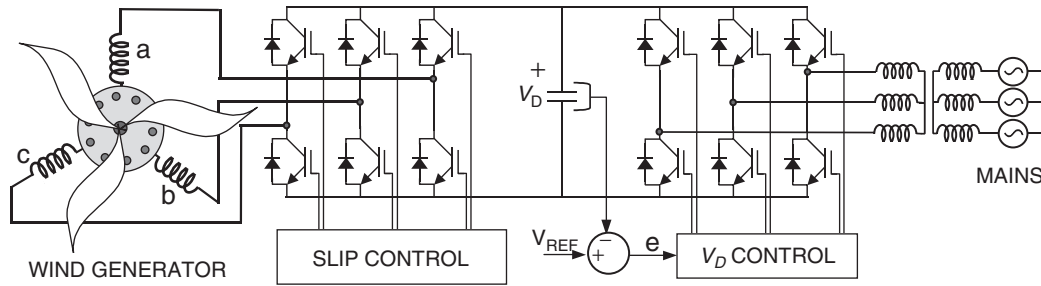
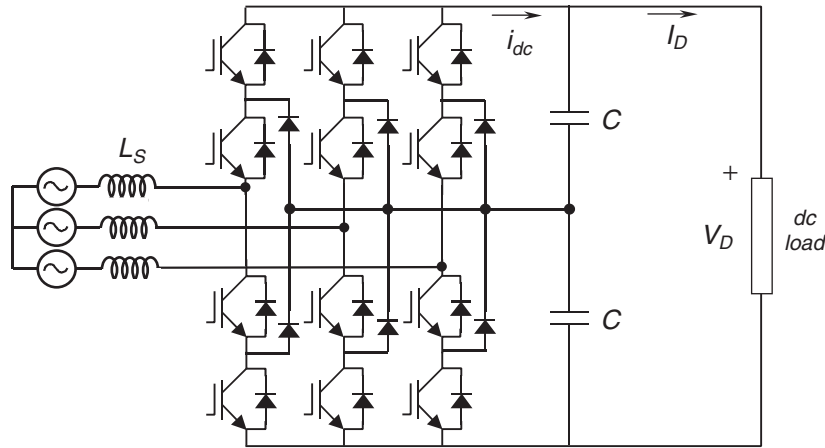**FIGURE 12.68**   Variable-speed constant-frequency wind generator.

FIGURE 12.69   Voltage-source rectifier using three-level converter.

used in power plants because of magnetization problems. With the use of frequency-link force-commutated converters, variable-speed constant-frequency generation becomes possible even with induction generators. The power plant in Fig. 12.68 shows a wind generator implemented with an induction machine, and a rectifier–inverter frequency link connected to the utility. The *dc* link voltage is kept constant with the converter located at the mains side. The converter connected at the machine side controls the slip of the generator and adjusts it according to the speed of wind or power requirements. The utility is not affected by the power factor of the generator, because the two converters keep the $\cos\varphi$ of the machine independent of the mains supply. The converter at the mains side can even be adjusted to operate at leading power factor.

Varible-speed constant-frequency generation also can be used in either hydraulic or thermal plants. This allows for optimal adjustment of the efficiency-speed characteristics of the machines. In many places, wound rotor induction generators working as variable speed synchronous machines are being used as constant frequency generators. They operate in hydraulic plants that are able to store water during low demand periods. A power converter is connected at the slip rings of the generator. The rotor is then fed with variable frequency excitation. This allows the generator to generate at different speeds around the synchronous rotating flux.

12.3.5.6 Power Rectifiers Using Multilevel Topologies

Almost all voltage source rectifiers already described are two-level configurations. Today, multilevel topologies are becoming very popular, mainly three-level converters. The most popular three-level configuration is called diode clamped converter, which is shown in Fig. 12.69. This topology is today the standard solution for high power steel rolling mills, which uses back-to-back three-phase rectifier–inverter link configuration. In addition, this solution has been recently introduced in high power downhill conveyor belts which operate almost permanently in the regeneration mode or rectifier operation. The more important advantage of three-level rectifiers is that voltage and current harmonics are reduced due to the increased number of levels.

Higher number of levels can be obtained using the same diode clamped strategy, as shown in Fig. 12.70, where only one phase of a general approach is displayed. However, this topology becomes more and more complex with the increase of number of levels. For this reason, new topologies are being
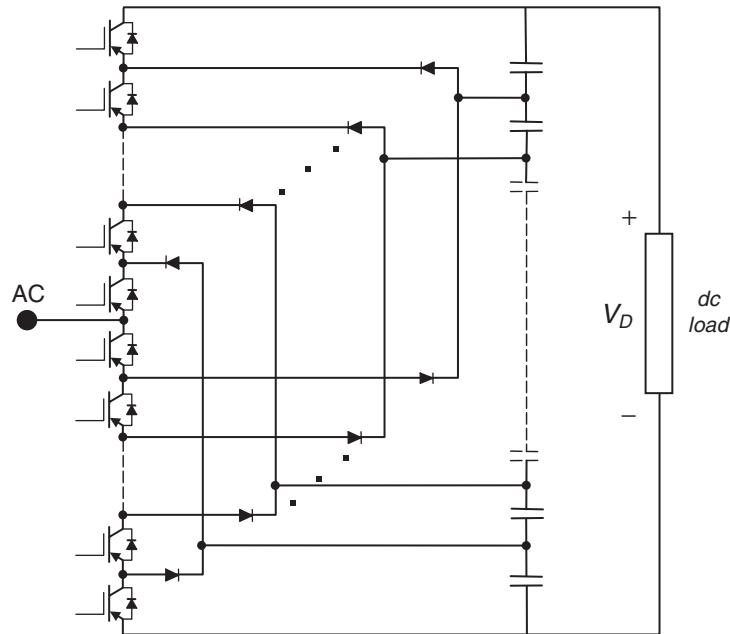
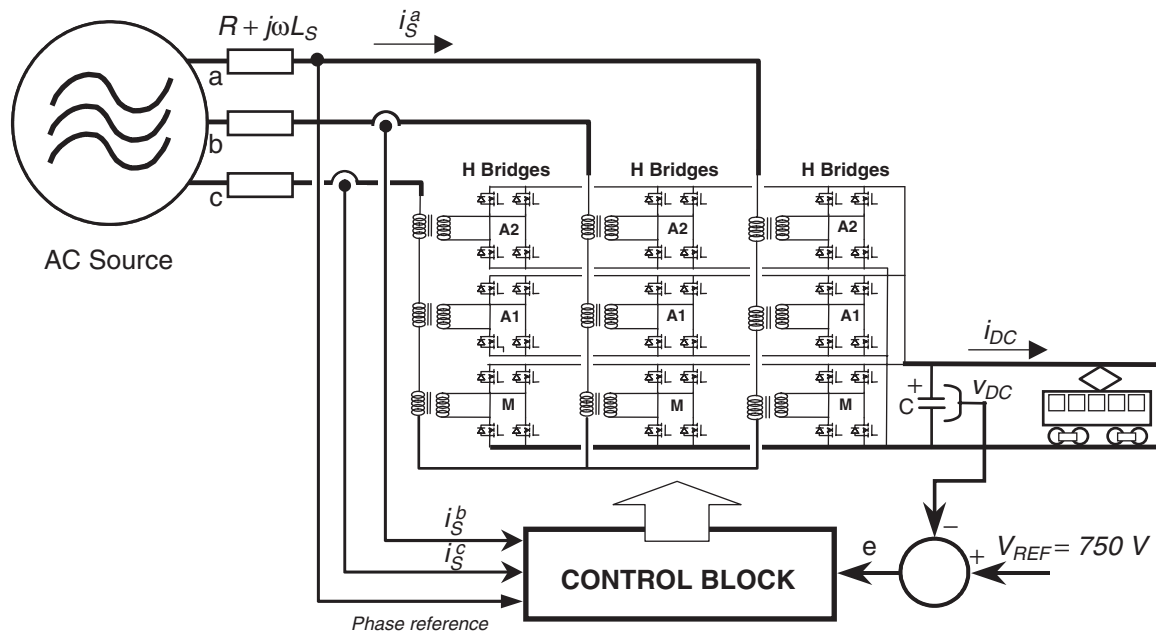**FIGURE 12.70**   Multilevel rectifier using diode clamped topology.

FIGURE 12.71   27-Level rectifier for railways, using H-bridges scaled in power of three.

studied to get a large number of levels with less power transistors. One example of such of these topologies is the multistage, 27-level converter shown in Fig. 12.71. This special 27-level, four-quadrant rectifier, uses only three H-bridges per phase with independent input transformers for each H-bridge. The transformers allow galvanic isolation and power escalation to get high quality voltage waveforms, with *THD* of less than 1%.

The power scalation consists on increasing the voltage rates of each transformer making use of the "three-level" characteristics of H-bridges. Then, the number of levels is optimized when transformers are scaled in power of three. Some advantages of this 27-level topology are: (a) only one of the three H-bridges, called "main converter," manages more than 80% of the total active power in each phase and (b) this main
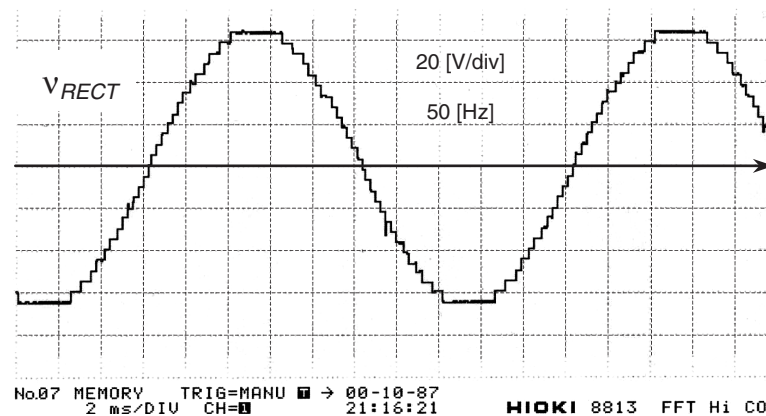
FIGURE 12.72 *AC voltage waveform generated by the 27-level rectifier.*

converter switches at fundamental frequency reducing the switching losses at a minimum value. The rectifier of Fig. 12.71 is a current-controlled voltage source type, with a conventional feedback control loop, which is being used as a rectifier in a subway substation. It includes fast reversal of power and the ability to produce clean *ac* and *dc* waveforms with negligible ripple. This rectifier can also compensate power factor and eliminate harmonics produced by other loads in the *ac* line. Figure 12.72 shows the *ac* voltage waveform obtained with this rectifier from an experimental prototype. If one more H-bridge is added, 81 levels are obtained, because the number of levels increases according with $N = 3^k$, where N is the number of levels or voltage steps and k the number of H-bridges used per phase.

Many other high-level topologies are under study but this matter is beyond the main topic of this chapter.

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