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Inverters

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15.1 Introduction

The main objective of static power converters is to produce an ac output waveform from a dc power supply. These are the types of waveforms required in adjustable speed drives (ASDs), uninterruptible power supplies (UPSs), static var compensators, active filters, flexible ac transmission systems (FACTSs), and voltage compensators, which are only a few applications. For sinusoidal ac outputs, the magnitude, frequency, and phase should be controllable. According to the type of ac output waveform, these topologies can be considered as voltage-source inverters (VSIs), where the independently controlled ac output is a voltage waveform. These structures are the most widely used because they naturally behave as voltage sources as required by many industrial applications, such as ASDs, which are the most popular application of inverters (Fig. 15.1a). Similarly, these topologies can be found as current-source inverters (CSIs), where the independently controlled ac output is a current waveform. These structures are still widely used in medium-voltage industrial applications, where high-quality voltage waveforms are required.

Static power converters, specifically inverters, are constructed from power switches and the ac output waveforms are therefore made up of discrete values. This leads to the generation of waveforms that feature fast transitions rather than smooth ones. For instance, the ac output voltage produced by the VSI of a three-level ASD is a, Pulse Width Modulation (PWM) type of waveform (Fig. 15.1c). Although this waveform is not sinusoidal as expected (Fig. 15.1b), its fundamental component behaves as such. This behavior should be ensured by a modulating technique that controls

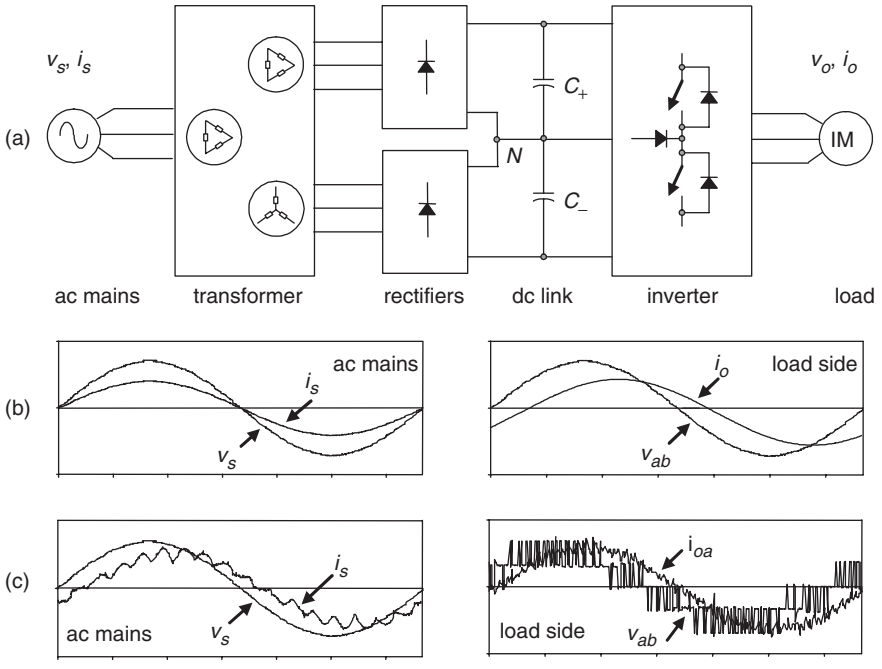

FIGURE 15.1 A three-level adjustable speed drive scheme and associated waveforms: (a) the electrical power conversion topology; (b) the ideal input (ac mains) and output (load) waveforms; and (c) the actual input (ac mains) and output (load) waveforms.

the amount of time and the sequence used to switch the power valves on and off. The modulating techniques most used are the carrier-based technique (e.g. sinusoidal pulsewidth modulation, SPWM), the space-vector (SV) technique, and the selective-harmonic-elimination (SHE) technique.

The discrete shape of the ac output waveforms generated by these topologies imposes basic restrictions on the applications of inverters. The VSI generates an ac output voltage waveform composed of discrete values (high dv/dt); therefore, the load should be inductive at the harmonic frequencies in order to produce a smooth current waveform. A capacitive load in the VSIs will generate large current spikes. If this is the case, an inductive filter between the VSI ac side and the load should be used. On the other hand, the CSI generates an ac output current waveform composed of discrete values (high di/dt); therefore, the load should be capacitive at the harmonic frequencies in order to produce a smooth voltage waveform. An inductive load in CSIs will generate large voltage spikes. If this is the case, a capacitive filter between the CSI ac side and the load should be used.

A three-level voltage waveform is not recommended for medium-voltage ASDs due to the high dv/dt that would apply to the motor terminals. Several negative side effects of this approach have been reported (bearing and isolation problems). As alternatives, to improve the ac output waveforms in VSIs are the multistage topologies (multilevel and multicell). The basic principle is to construct the required ac output waveform from various voltage levels, which achieves medium-voltage waveforms at reduced dv/dt. Although these topologies are well developed in ASDs, they are also suitable for static var compensators, active filters, and voltage compensators. Specialized modulating techniques have been developed to switch the higher number of power valves involved in these topologies. Among others, the carrier-based (SPWM) and SV-based techniques have been naturally extended to these applications.

In many applications, it is required to take energy from the ac side of the inverter and send it back into the dc side. For instance, whenever ASDs need to either brake or slow down the motor speed, the kinetic energy is sent into the voltage dc link (Fig. 15.1a). This is known as the regenerative operating mode and, in contrast to the motoring mode, the dc link current direction is reversed due to the fact that the dc link voltage is fixed. If a capacitor is used to maintain the dc link voltage (as in standard ASDs) the energy must either be dissipated or fed back into the distribution system, otherwise, the dc link voltage gradually increases. The first approach requires the dc link capacitor be connected in parallel with a resistor, which must be properly switched only when the energy flows from the motor into the dc link. A better alternative is to feed back such energy into the distribution system. However, this alternative requires a reversible-current topology connected between the distribution system and the dc link capacitor. A modern approach to such a requirement is to use the active front-end rectifier technologies, where the regeneration mode is a natural operating mode of the system.

In this chapter, single- and three-phase inverters in their voltage and current source alternatives will be reviewed. The dc link will be assumed to be a perfect dc, either voltage or current source that could be fixed as the dc link voltage in standard ASDs, or variable as the dc link current in some medium-voltage current source drives. Specifically, the topologies, modulating techniques and control aspects oriented to standard applications, are analyzed. In order to simplify the analysis, the inverters are considered lossless topologies, which are composed of ideal power valves. Nevertheless, some practical non-ideal conditions are also considered.

15.2 Single-phase Voltage Source Inverters

Single-phase VSI can be found as half-bridge and full-bridge topologies. Although, the power range they cover is the low one, they are widely used in power supplies, single-phase UPSs, and currently to form high-power static power topologies, such as the multicell configurations that are reviewed in Section 15.7. The main features of both approaches are reviewed and presented in the following.

15.2.1 Half-bridge VSI

Figure 15.2 shows the power topology of a half-bridge VSI, where two large capacitors are required to provide a neutral point N, such that each capacitor maintains a constant voltage $v_i/2$. Because the current harmonics injected by the operation of the inverter are low-order harmonics, a set of large capacitors (C_+ and C_-) is required. It is clear that both switches S_+ and S_- cannot be on simultaneously because a short circuit across the dc link voltage source v_i would be produced. There are two defined (states 1 and 2) and one undefined (state 3) switch state as shown in Table 15.1. In order to avoid the short circuit across the dc bus and the undefined ac output-voltage condition, the modulating technique should always ensure that at any instant either the top or the bottom switch of the inverter leg is on.

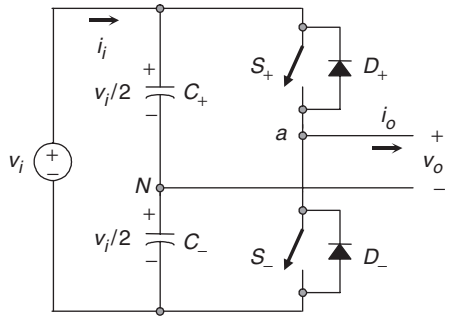

FIGURE 15.2 Single-phase half-bridge VSI.

TABLE 15.1 Switch states for a half-bridge single-phase VSI

State	State #	v_o	Components conducting
S_+ is on and S_- is off	1	$v_i/2$	S_+ if $i_o > 0$ D_+ if $i_o < 0$
S_- is on and S_+ is off	2	$-v_i/2$	D_- if $i_o > 0$ S_- if $i_o < 0$
S_+ and S_- are all off	3	$-v_i/2$ $v_i/2$	D_- if $i_o > 0$ D_+ if $i_o < 0$

Figure 15.3 shows the ideal waveforms associated with the half-bridge inverter shown in Fig. 15.2. The states for the switches S_+ and S_- are defined by the modulating technique, which in this case is a carrier-based PWM.

A. The Carrier-based Pulse Width Modulation (PWM) Technique

As mentioned earlier, it is desired that the ac output voltage, $v_o = v_{aN}$, follow a given waveform (e.g. sinusoidal) on a continuous basis by properly switching the power valves. The carrier-based PWM technique fulfills such a requirement as it defines the on- and off-states of the switches of one leg of a VSI by comparing a modulating signal v_c (desired ac output voltage) and a triangular waveform v_Δ (carrier signal). In practice, when $v_c > v_\Delta$ the switch S_+ is on and the switch S_- is off; similarly, when $v_c < v_\Delta$ the switch S_+ is off and the switch S_- is on.

A special case is when the modulating signal v_c is a sinusoidal at frequency f_c and amplitude $\hat{v}_c$, and the triangular signal v_Δ is at frequency f_Δ and amplitude $\hat{v}_\Delta$. This is the sinusoidal PWM (SPWM) scheme. In this case, the modulation index m_a (also known as the amplitude-modulation ratio) is defined as

$$m_a = \frac{\hat{v}_c}{\hat{v}_\Delta} \tag{15.1}$$

and the normalized carrier frequency m_f (also known as the frequency-modulation ratio) is

$$m_f = \frac{f_\Delta}{f_c} \tag{15.2}$$

Figure 15.3e clearly shows that the ac output voltage $v_o = v_{aN}$ is basically a sinusoidal waveform plus harmonics, which features: (a) the amplitude of the fundamental component of the ac output voltage $\hat{v}_{o1}$ satisfying the following expression:

$$\hat{v}_{o1} = \hat{v}_{aN1} = \frac{v_i}{2} m_a \tag{15.3}$$

for $m_a \leq 1$, which is called the linear region of the modulating technique (higher values of m_a leads to overmodulation that

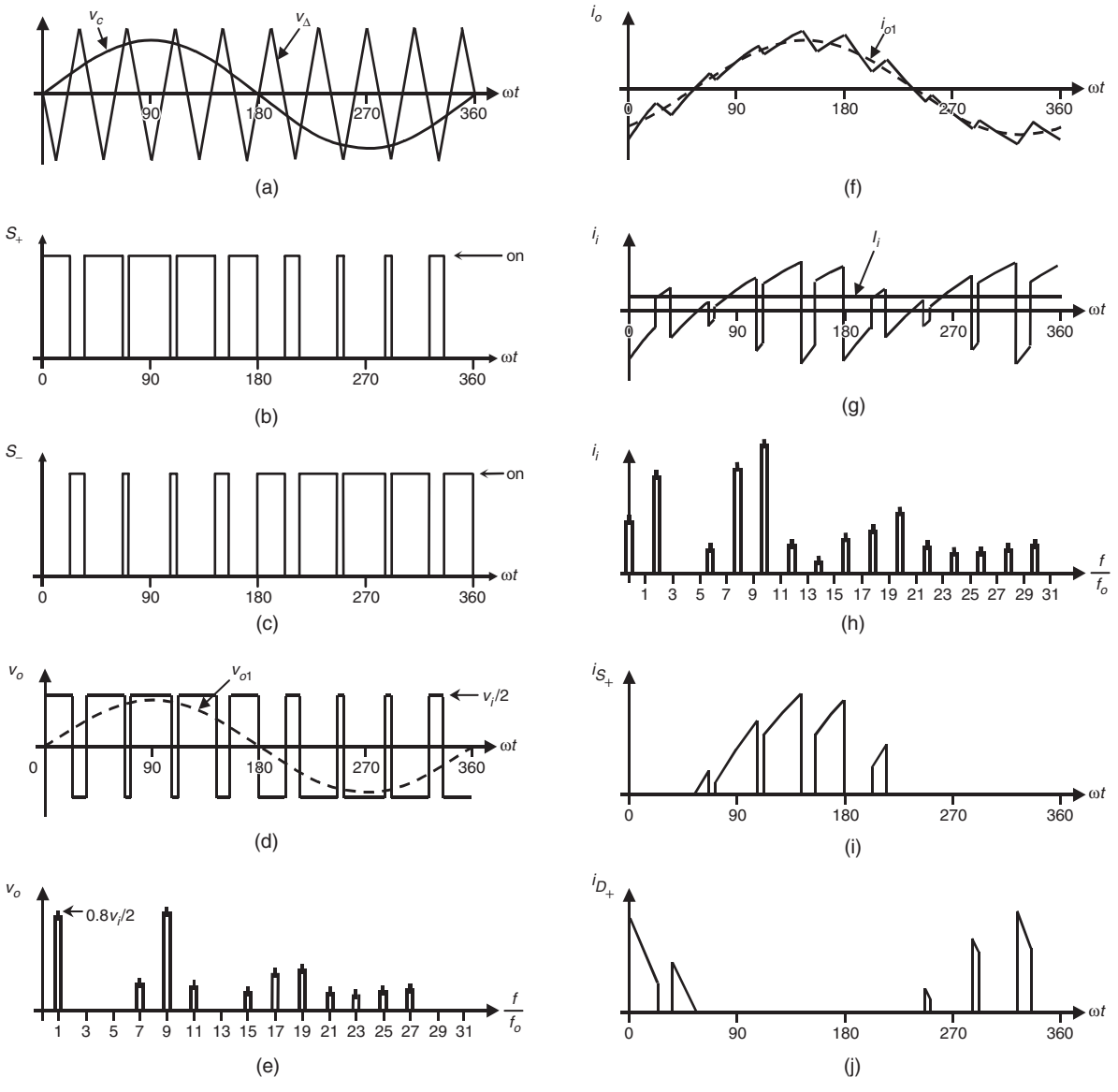

FIGURE 15.3 The half-bridge VSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) switch S_+ state; (c) switch S_- state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_+ current; and (j) diode D_+ current.

will be discussed later); (b) for odd values of the normalized carrier frequency m_f the harmonics in the ac output voltage appear at normalized frequencies f_h centered around m_f and its multiples, specifically,

$$h = l\,m_f \pm k \quad l = 1, 2, 3, \ldots \tag{15.4}$$

where $k = 2, 4, 6, \ldots$ for $l = 1, 3, 5, \ldots$; and $k = 1, 3, 5, \ldots$ for $l = 2, 4, 6, \ldots$; (c) the amplitude of the ac output voltage harmonics is a function of the modulation index m_a and is independent of the normalized carrier frequency m_f for $m_f > 9$; (d) the harmonics in the dc link current (due to the modulation) appear at normalized frequencies f_p centered around the normalized carrier frequency m_f and its multiples, specifically,

$$p = l\,m_f \pm k \pm 1 \quad l = 1, 2, \ldots \tag{15.5}$$

where $k = 2, 4, 6, \ldots$ for $l = 1, 3, 5, \ldots$; and $k = 1, 3, 5, \ldots$ for $l = 2, 4, 6, \ldots$. Additional important issues are: (a) for small values of m_f ($m_f < 21$), the carrier signal v_Δ and the signal v_c should be synchronized to each other (m_f integer), which is required to hold the previous features; if this is not the case, subharmonics will be present in the ac output voltage;

(b) for large values of m_f ($m_f > 21$), the subharmonics are negligible if an asynchronous PWM technique is used, however, due to potential very low-order subharmonics, its use should be avoided; finally (c) in the overmodulation region ($m_a > 1$) some intersections between the carrier and the modulating signal are missed, which leads to the generation of low-order harmonics but a higher fundamental ac output voltage is obtained; unfortunately, the linearity between m_a and $\hat{v}_{o1}$ achieved in the linear region does not hold in the overmodulation region, moreover, a saturation effect can be observed (Fig. 15.4).

The PWM technique allows an ac output voltage to be generated that tracks a given modulating signal. A special case is the SPWM technique (the modulating signal is a sinusoidal) that provides, in the linear region, an ac output voltage that varies linearly as a function of the modulation index, and the harmonics are at well-defined frequencies and amplitudes. These features simplify the design of filtering components. Unfortunately, the maximum amplitude of the fundamental ac voltage is $v_i/2$ in this operating mode. Higher voltages are obtained by using the overmodulation region ($m_a > 1$); however, low-order harmonics appear in the ac output voltage. Very large values of the modulation index ($m_a > 3.24$) lead to a totally square ac output voltage that is considered as the square-wave modulating technique.

B. Square-wave Modulating Technique

Both switches S_+ and S_- are on for one half-cycle of the ac output period. This is equivalent to the SPWM technique with an infinite modulation index m_a. Figure 15.5 shows the following: (a) the normalized ac output voltage harmonics are

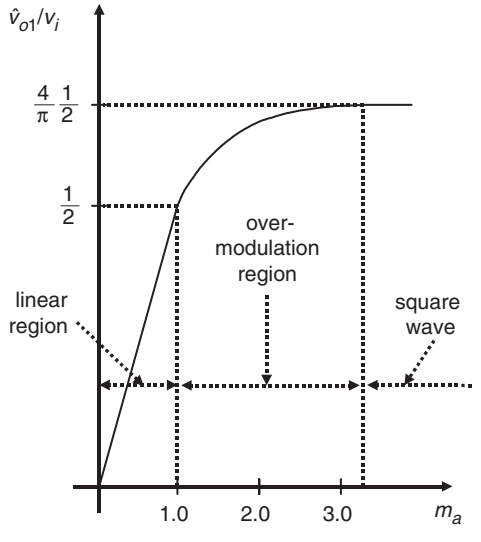

FIGURE 15.4 Normalized fundamental ac component of the output voltage in a half-bridge VSI SPWM modulated.

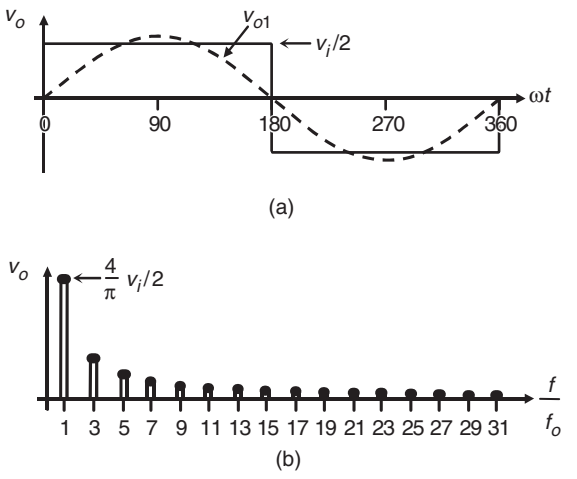

FIGURE 15.5 The half-bridge VSI. Ideal waveforms for the square-wave modulating technique: (a) ac output voltage and (b) ac output voltage spectrum.

at frequencies $h = 3, 5, 7, 9, \ldots$, and for a given dc link voltage; (b) the fundamental ac output voltage features an amplitude given by

$$\hat{v}_{o1} = \hat{v}_{aN1} = \frac{4}{\pi}\frac{v_i}{2} \tag{15.6}$$

and the harmonics feature an amplitude given by

$$\hat{v}_{oh} = \frac{\hat{v}_{o1}}{h} \tag{15.7}$$

It can be seen that the ac output voltage cannot be changed by the inverter. However, it could be changed by controlling the dc link voltage v_i. Other modulating techniques that are applicable to half-bridge configurations (e.g., selective harmonic elimination) are reviewed here as they can easily be extended to modulate other topologies.

C. Selective Harmonic Elimination

The main objective is to obtain a sinusoidal ac output voltage waveform where the fundamental component can be adjusted arbitrarily within a range and the intrinsic harmonics selectively eliminated. This is achieved by mathematically generating the exact instant of the turn-on and turn-off of the power valves. The ac output voltage features odd half- and quarter-wave symmetry; therefore, even harmonics are not present ($v_{oh} = 0$, $h = 2, 4, 6, \ldots$). Moreover, the phase voltage waveform ($v_o = v_{aN}$ in Fig. 15.2), should be chopped N times per half-cycle in order to adjust the fundamental and eliminate $N - 1$ harmonics in the ac output voltage waveform. For instance, to eliminate the third and fifth harmonics

and to perform fundamental magnitude control ($N = 3$), the equations to be solved are the following:

$$\begin{aligned}
&\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) = (2 + \pi\hat{v}_{o1}/v_i)/4 \\
&\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) = 1/2 \\
&\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 1/2
\end{aligned} \tag{15.8}$$

where the angles α_1, α_2 and α_3 are defined as shown in Fig. 15.6a. The angles are found by means of iterative algorithms as no analytical solutions can be derived. The angles α_1, α_2, and α_3 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 15.7a. The general expressions to eliminate an even $N-1$ $(N-1 = 2, 4, 6, \ldots)$ number of harmonics are

$$\begin{aligned}
&-\sum_{k=1}^{N}(-1)^k \cos(\alpha_k) = \frac{(2 + \pi\hat{v}_{o1})/v_i}{4} \\
&-\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k) = \frac{1}{2} \quad \text{for } n = 3, 5, \ldots, 2N-1
\end{aligned} \tag{15.9}$$

where α_1, α_2,..., α_N should satisfy $\alpha_1 < \alpha_2 < \cdots < \alpha_N < \pi/2$. Similarly, to eliminate an odd number of harmonics, for instance the third, fifth, and seventh, and to perform the

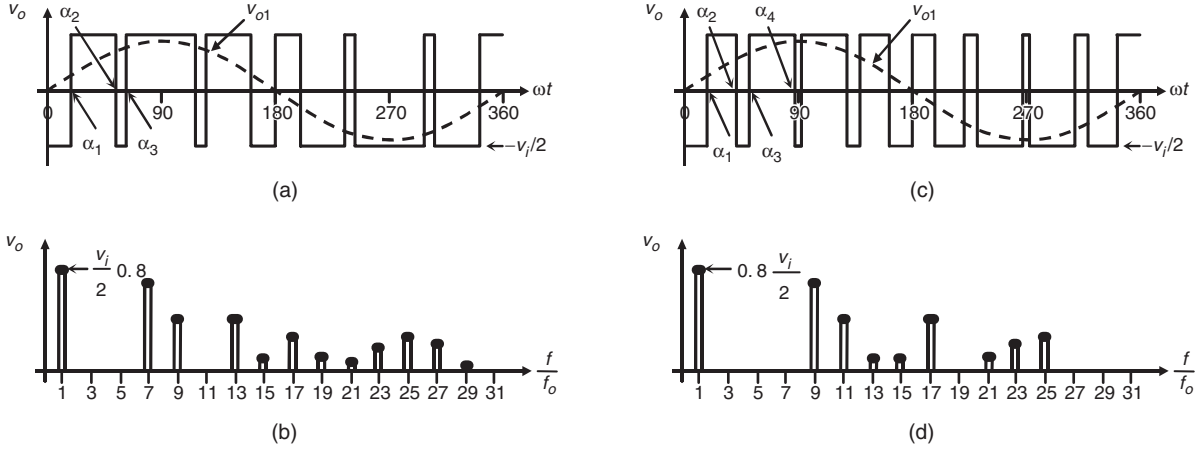

FIGURE 15.6 The half-bridge VSI. Ideal waveforms for the SHE technique: (a) ac output voltage for third and fifth harmonic elimination; (b) spectrum of (a); (c) ac output voltage for third, fifth, and seventh harmonic elimination; and (d) spectrum of (c).

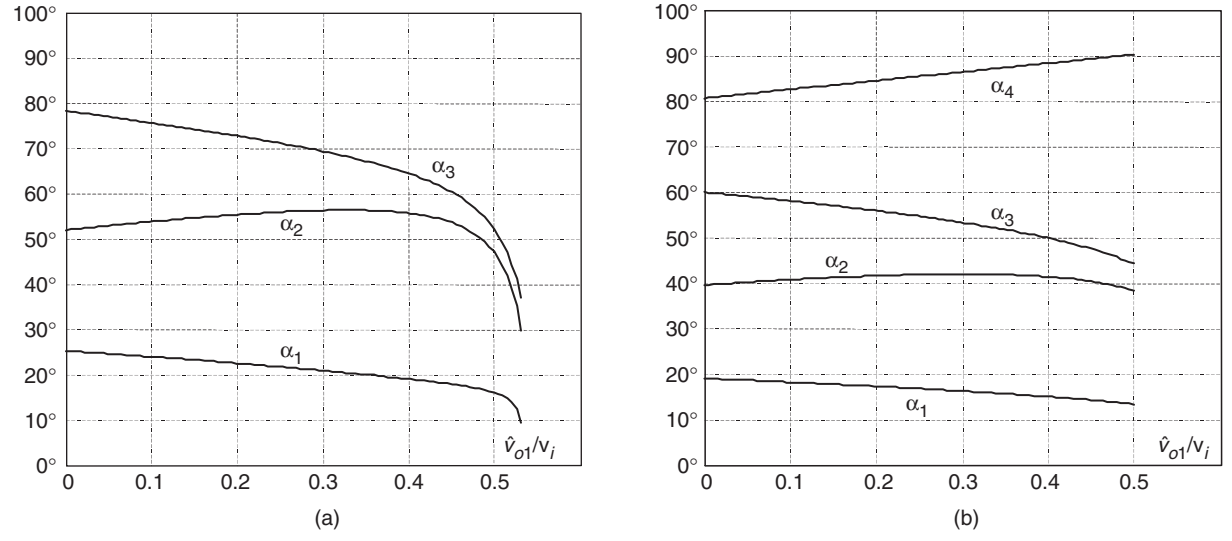

FIGURE 15.7 Chopping angles for SHE and fundamental voltage control in half-bridge VSIs: (a) third and fifth harmonic elimination and (b) third, fifth, and seventh harmonic elimination.

fundamental magnitude control ($N-1=3$), the equations to be solved are:

$$\begin{aligned}
&\cos(1\alpha_1)-\cos(1\alpha_2)+\cos(1\alpha_3)-\cos(1\alpha_4)=(2-\pi\hat{v}_{o1}/v_i)/4\\
&\cos(3\alpha_1)-\cos(3\alpha_2)+\cos(3\alpha_3)-\cos(3\alpha_4)=1/2\\
&\cos(5\alpha_1)-\cos(5\alpha_2)+\cos(5\alpha_3)-\cos(5\alpha_4)=1/2\\
&\cos(7\alpha_1)-\cos(7\alpha_2)+\cos(7\alpha_3)-\cos(7\alpha_4)=1/2
\end{aligned} \tag{15.10}$$

where the angles α_1, α_2, α_3, and α_4 are defined as shown in Fig. 15.6b. The angles α_1, α_2, and α_3 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 15.7b. The general expressions to eliminate an odd $N-1$ ($N-1=3,5,7,\ldots$) number of harmonics are given by

$$\begin{aligned}
&-\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k)=\frac{(2-\pi\hat{v}_{o1})/v_i}{4}\\
&-\sum_{k=1}^{N}(-1)^k\cos(n\alpha_k)=\frac{1}{2}\quad \text{for } n=3,5,\ldots,2N-1
\end{aligned} \tag{15.11}$$

where $\alpha_1,\alpha_2,\ldots,\alpha_N$ should satisfy $\alpha_1<\alpha_2<\cdots<\alpha_N<\pi/2$.

To implement the SHE modulating technique, the modulator should generate the gating pattern according to the angles as shown in Fig. 15.7. This task is usually performed by digital systems that normally store the angles in look-up tables.

D. DC Link Current

The split capacitors are considered a part of the inverter and therefore an instantaneous power balance cannot be considered due to the storage energy components (C_+ and C_-). However, if a lossless inverter is assumed, the average power absorbed in one period by the load must be equal to the average power supplied by the dc source. Thus, we can write

$$\int_0^T v_i(t)\cdot i_i(t)\cdot dt=\int_0^T v_o(t)\cdot i_o(t)\cdot dt \tag{15.12}$$

where T is the period of the ac output voltage. For an inductive load and a relatively high switching frequency, the load current i_o is nearly sinusoidal and therefore, only the fundamental component of the ac output voltage provides power to the load. On the other hand, if the dc link voltage remains constant $v_i(t)=V_i$, Eq. (15.12) can be simplified to

$$\int_0^T i_i(t)\cdot dt=\frac{1}{V_i}\int_0^T \sqrt{2}V_{o1}\sin(\omega t)\cdot\sqrt{2}I_o\sin(\omega t-\phi)\cdot dt=I_i \tag{15.13}$$

where V_{o1} is the fundamental rms ac output voltage, I_o is the rms load current, ϕ is an arbitrary inductive load power factor, and I_i is the dc link current that can be further simplified to

$$I_i=\frac{V_{o1}}{V_i}I_o\cos(\phi) \tag{15.14}$$

15.2.2 Full-bridge VSI

Figure 15.8 shows the power topology of a full-bridge VSI. This inverter is similar to the half-bridge inverter; however, a second leg provides the neutral point to the load. As expected, both switches S_{1+} and S_{1-} (or S_{2+} and S_{2-}) cannot be on simultaneously because a short circuit across the dc link voltage source v_i would be produced. There are four defined (states 1, 2, 3, and 4) and one undefined (state 5) switch state as shown in Table 15.2.

The undefined condition should be avoided so as to be always capable of defining the ac output voltage always. In order to avoid the short circuit across the dc bus and the undefined ac output voltage condition, the modulating technique should ensure that either the top or the bottom switch of each leg is on at any instant. It can be observed that the ac output voltage can take values up to the dc link value v_i, which is twice that obtained with half-bridge VSI topologies.

Several modulating techniques have been developed that are applicable to full-bridge VSIs. Among them are the PWM (bipolar and unipolar) techniques.

A. Bipolar PWM Technique

States 1 and 2 (Table 15.2) are used to generate the ac output voltage in this approach. Thus, the ac output voltage waveform features only two values, which are v_i and $-v_i$. To generate the

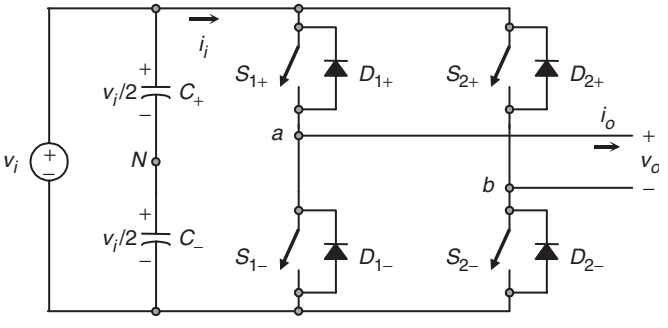

FIGURE 15.8 Single-phase full-bridge VSI.

TABLE 15.2 Switch states for a full-bridge single-phase VSI

State	State #	v_{aN}	v_{bN}	v_o	Components conducting	
S_{1+} and S_{2-} are on and S_{1-} and S_{2+} are off	1	$v_i/2$	$-v_i/2$	v_i	S_{1+} and S_{2-} D_{1+} and D_{2-}	if $i_o > 0$ if $i_o < 0$
S_{1-} and S_{2+} are on and S_{1+} and S_{2-} are off	2	$-v_i/2$	$v_i/2$	$-v_i$	D_{1-} and D_{2+} S_{1-} and S_{2+}	if $i_o > 0$ if $i_o < 0$
S_{1+} and S_{2+} are on and S_{1-} and S_{2-} are off	3	$v_i/2$	$v_i/2$	0	S_{1+} and D_{2+} D_{1+} and S_{2+}	if $i_o > 0$ if $i_o < 0$
S_{1-} and S_{2-} are on and S_{1+} and S_{2+} are off	4	$-v_i/2$	$-v_i/2$	0	D_{1-} and S_{2-} S_{1-} and D_{2-}	if $i_o > 0$ if $i_o < 0$
S_{1-}, S_{2-}, S_{1+}, and S_{2+} are all off	5	$-v_i/2$ $v_i/2$	$v_i/2$ $-v_i/2$	v_i $-v_i$	D_{1-} and D_{2+} D_{1+} and D_{2-}	if $i_o > 0$ if $i_o < 0$

states, a carrier-based technique can be used as in half-bridge configurations (Fig. 15.3), where only one sinusoidal modulating signal has been used. It should be noted that the on-state in switch S_+ in the half-bridge corresponds to both switches S_{1+} and S_{2-} being in the on-state in the full-bridge configuration. Similarly, S_- in the on-state in the half-bridge corresponds to both switches S_{1-} and S_{2+} being in the on-state in the full-bridge configuration. This is called bipolar carrier-based SPWM. The ac output voltage waveform in a full-bridge VSI is basically a sinusoidal waveform that features a fundamental component of amplitude $\hat{v}_{o1}$ that satisfies the expression

$$\hat{v}_{o1} = \hat{v}_{ab1} = v_i m_a \tag{15.15}$$

in the linear region of the modulating technique ($m_a \leq 1$), which is twice that obtained in the half-bridge VSI. Identical conclusions can be drawn for the frequencies and the amplitudes of the harmonics in the ac output voltage and dc link current, and for operations at smaller and larger values of odd m_f (including the overmodulation region ($m_a > 1$)), than in half-bridge VSIs, but considering that the maximum ac output voltage is the dc link voltage v_i. Thus, in the overmodulation region the fundamental component of amplitude $\hat{v}_{o1}$ satisfies the expression

$$v_i < \hat{v}_{o1} = \hat{v}_{ab1} < \frac{4}{\pi} v_i \tag{15.16}$$

B. Unipolar PWM Technique

In contrast to the bipolar approach, the unipolar PWM technique uses the states 1, 2, 3, and 4 (Table 15.2) to generate the ac output voltage. Thus, the ac output voltage waveform can instantaneously take one of the three values, namely v_i, $-v_i$, and 0. To generate the states, a carrier-based technique can be used as shown in Fig. 15.9, where two sinusoidal modulating signals (v_c and $-v_c$) are used. The signal v_c is used to generate v_{aN}, and $-v_c$ is used to generate v_{bN}; thus $v_{bN1} = -v_{aN1}$. On the other hand, $v_{o1} = v_{aN1} - v_{bN1}, = 2 \cdot v_{aN1}$; thus $\hat{v}_{o1} = 2 \cdot \hat{v}_{aN1} = m_a \cdot v_i$ This is called unipolar carrier-based SPWM.

Identical conclusions can be drawn for the amplitude of the fundamental component and harmonics in the ac output voltage and dc link current, and for operations at smaller and larger values of m_f (including the overmodulation region ($m_a > 1$)) than in full-bridge VSIs modulated by the bipolar SPWM. However, because the phase voltages (v_{aN} and v_{bN}) are identical but 180° out of phase, the output voltage ($v_o = v_{ab} = v_{aN} - v_{bN}$) will not contain even harmonics. Thus, if m_f is taken even, the harmonics in the ac output voltage appear at normalized odd frequencies f_h centered around twice the normalized carrier frequency m_f and its multiples. Specifically,

$$h = l\, m_f \pm k \quad l = 2, 4, \ldots \tag{15.17}$$

where $k = 1, 3, 5, \ldots$ and the harmonics in the dc link current appear at normalized frequencies f_p centered around twice the normalized carrier frequency m_f and its multiples. Specifically,

$$p = l\, m_f \pm k \pm 1 \quad l = 2, 4, \ldots \tag{15.18}$$

where $k = 1, 3, 5, \ldots$ This feature is considered to be an advantage because it allows the use of smaller filtering components to obtain high-quality voltage and current waveforms while using the same switching frequency as in VSIs modulated by the bipolar approach.

C. Selective Harmonic Elimination

In contrast to half-bridge VSIs, this approach is applied in a per-line fashion for full-bridge VSIs. The ac output voltage features odd half- and quarter-wave symmetry; therefore, even harmonics are not present ($\hat{v}_{oh} = 0$, $h = 2, 4, 6, \ldots$). Moreover, the ac output voltage waveform ($v_o = v_{ab}$ in Fig. 15.8), should feature N pulses per half-cycle in order to adjust the fundamental component and eliminate $N - 1$ harmonics. For instance, to eliminate the third, fifth, and the seventh harmonics and to perform fundamental component magnitude

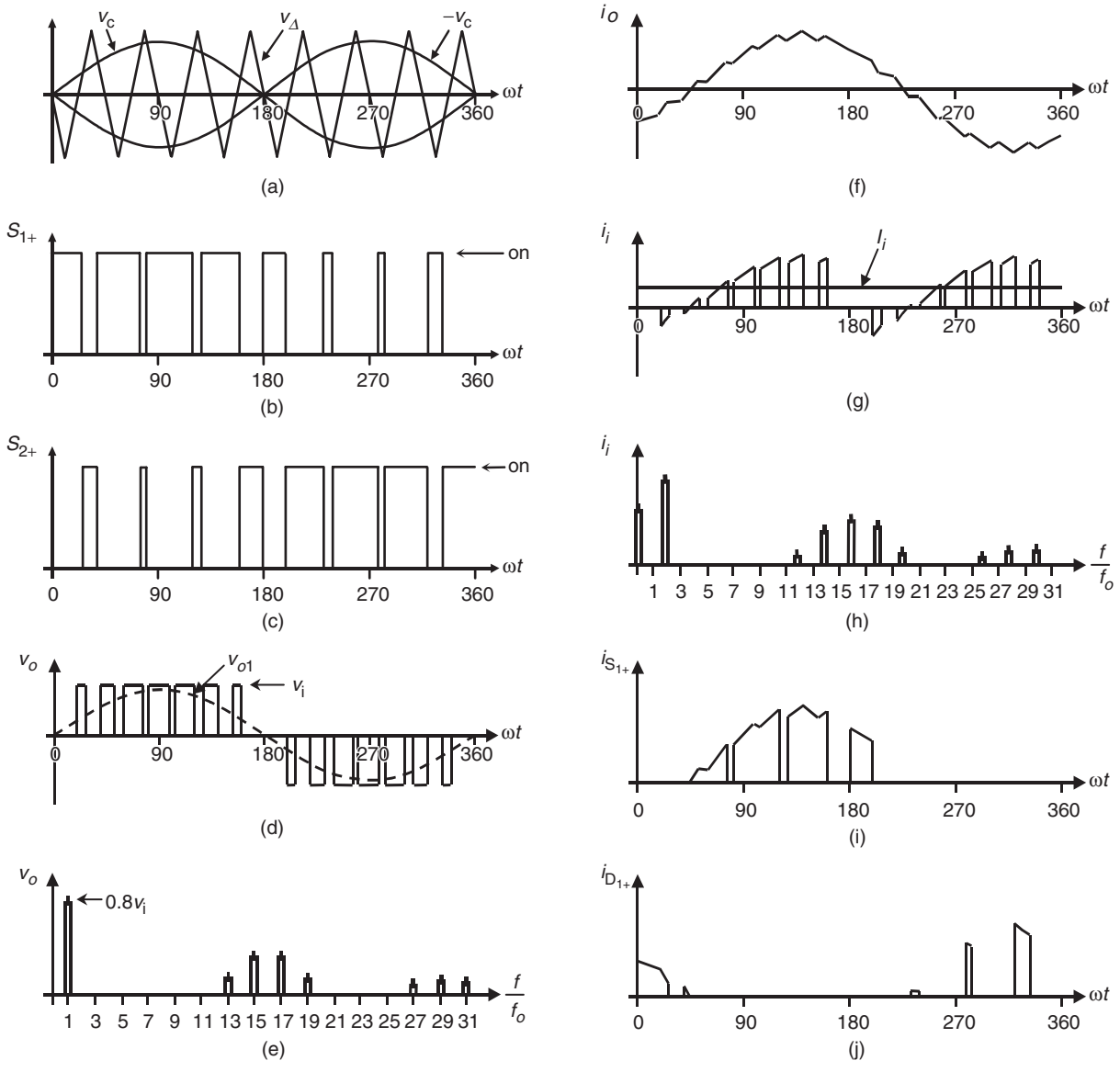

FIGURE 15.9 The full-bridge VSI. Ideal waveforms for the unipolar SPWM ($m_a = 0.8$, $m_f = 8$): (a) carrier and modulating signals; (b) switch S_{1+} state; (c) switch S_{2+} state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_{1+} current; and (j) diode D_{1+} current.

control ($N = 4$), the equations to be solved are:

$$\begin{aligned}
&\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) - \cos(1\alpha_4) = \pi\hat{v}_{o1}/(v_i 4)\\
&\cos(3\alpha_1) - \cos(3\alpha_2) + \cos(3\alpha_3) - \cos(3\alpha_4) = 0\\
&\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) = 0\\
&\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) = 0
\end{aligned} \tag{15.19}$$

where the angles α_1, α_2, α_3, and α_4 are defined as shown in Fig. 15.10a. The angles α_1, α_2, α_3, and α_4 are plotted for different values of $\hat{v}_{o1}/v_i$ in Fig. 15.11a. The general expressions to eliminate an arbitrary $N-1$ ($N-1 = 3, 5, 7, \ldots$) number of harmonics are given by

$$\begin{aligned}
&-\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k) = \frac{\pi}{4}\left(\frac{\hat{v}_{o1}}{v_i}\right)\\
&-\sum_{k=1}^{N}(-1)^k \cos(n\alpha_k) = 0 \quad \text{for } n = 3, 5, \ldots, 2N-1
\end{aligned} \tag{15.20}$$

where $\alpha_1, \alpha_2, \ldots, \alpha_N$ should satisfy $\alpha_1 < \alpha_2 < \cdots < \alpha_N < \pi/2$.

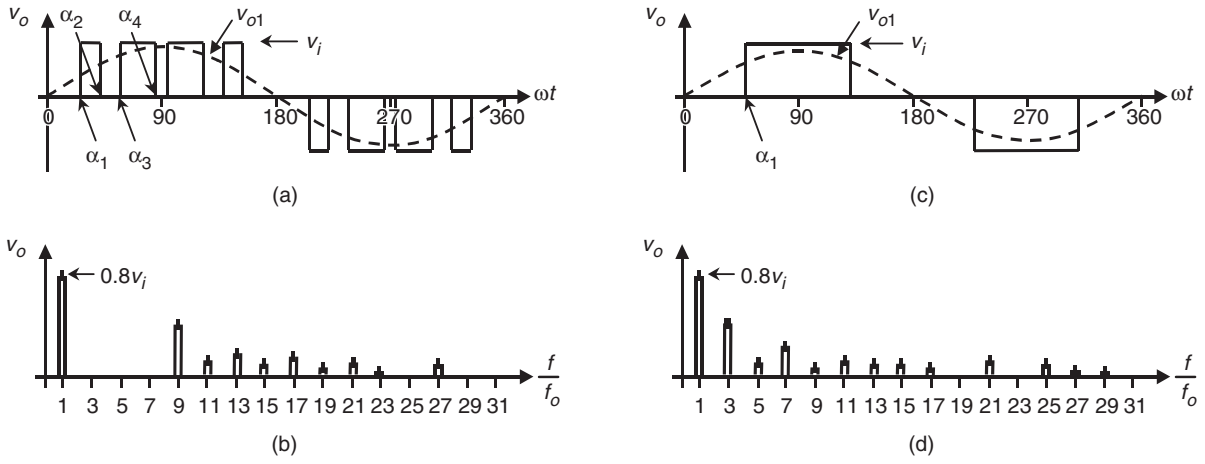

FIGURE 15.10 The half-bridge VSI. Ideal waveforms for the SHE technique: (a) ac output voltage for third, fifth, and seventh harmonic elimination; (b) spectrum of (a); (c) ac output voltage for fundamental control; and (d) spectrum of (c).

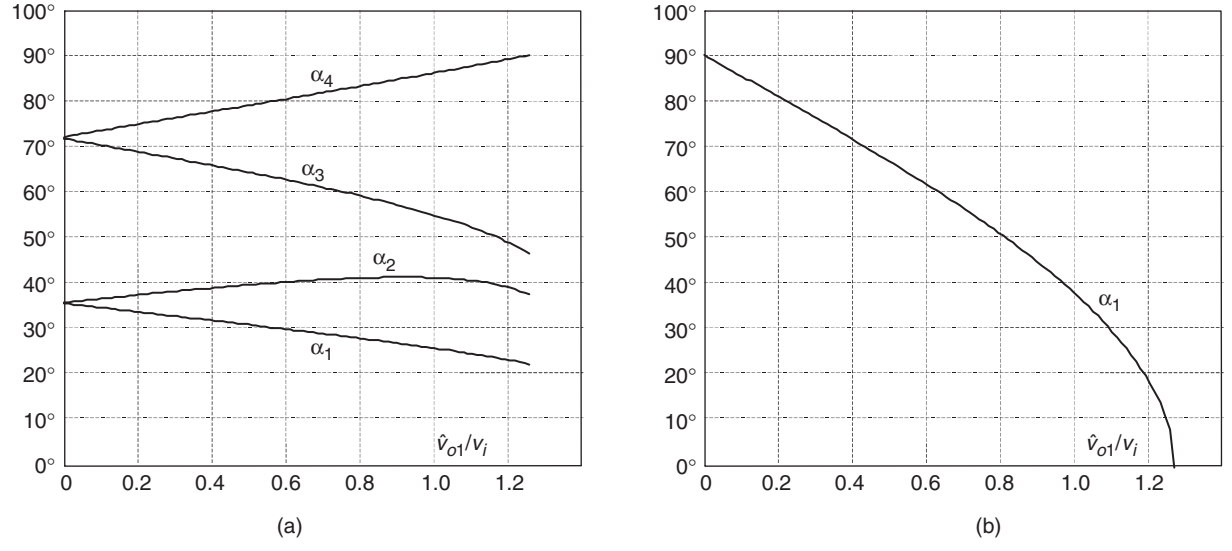

FIGURE 15.11 Chopping angles for SHE and fundamental voltage control in half-bridge VSIs: (a) fundamental control and third, fifth, and seventh harmonic elimination and (b) fundamental control.

Figure 15.10c shows a special case where only the fundamental ac output voltage is controlled. This is known as output control by voltage cancellation, which derives from the fact that its implementation is easily attainable by using two phase-shifted square-wave switching signals as shown in Fig. 15.12. The phase-shift angle becomes $2 \cdot \alpha_1$ (Fig. 15.11b). Thus, the amplitude of the fundamental component and harmonics in the ac output voltage are given by

$$\hat{v}_{oh} = \frac{4}{\pi} v_i \frac{(-1)^{(h-1)/2}}{h} \cos(h\alpha_1) \quad h = 1, 3, 5, \ldots \tag{15.21}$$

It can also be observed in Fig. 15.12c that for $\alpha_1 = 0$ square-wave operation is achieved. In this case, the fundamental ac output voltage is given by

$$\hat{v}_{o1} = \frac{4}{\pi} v_i \tag{15.22}$$

where the fundamental load voltage can be controlled by the manipulation of the dc link voltage.

D. DC Link Current

Due to the fact that the inverter is assumed lossless and constructed without storage energy components, the instantaneous power balance indicates that,

$$v_i(t) \cdot i_i(t) = v_o(t) \cdot i_o(t) \tag{15.23}$$

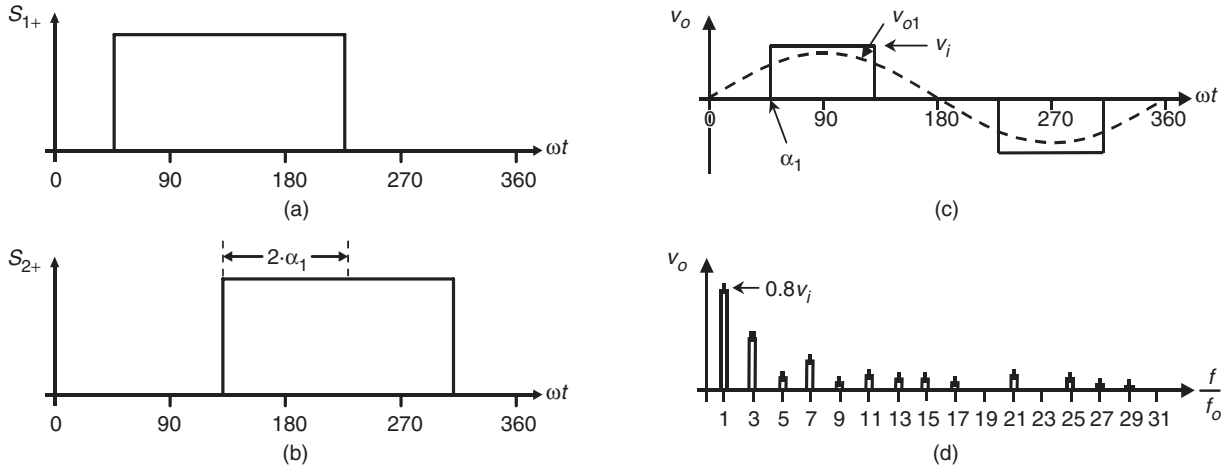

FIGURE 15.12 The full-bridge VSI. Ideal waveforms for the output control by voltage cancellation: (a) switch S_{1+} state; (b) switch S_{2+} state; (c) ac output voltage; and (d) ac output voltage spectrum.

For inductive load and relatively high switching frequencies, the load current i_o is nearly sinusoidal. As a first approximation, the ac output voltage can also be considered sinusoidal. On the other hand, if the dc link voltage remains constant $v_i(t) = V_i$, Eq. (15.23) can be simplified to

$$i_i(t) = \frac{1}{V_i}\sqrt{2}V_{o1}\sin(\omega t)\cdot\sqrt{2}I_o\sin(\omega t - \phi) \qquad (15.24)$$

where V_{o1} is the fundamental rms ac output voltage, I_o is the rms load current, and ϕ is an arbitrary inductive load power factor. Thus, the dc link current can be further simplified to

$$i_i(t) = \frac{V_{o1}}{V_i}I_o\cos(\phi) - \frac{V_{o1}}{V_i}I_o\cos(2\omega t - \phi) \qquad (15.25)$$

The preceding expression reveals an important issue, that is, the presence of a large second-order harmonic in the dc link current (its amplitude is similar to the dc link current). This second harmonic is injected back into the dc voltage source, thus its design should consider it in order to guarantee a nearly constant dc link voltage. In practical terms, the dc voltage source is required to feature large amounts of capacitance, which is costly and demands space, both undesired features, especially in medium- to high-power supplies.

15.3 Three-phase Voltage Source Inverters

Single-phase VSIs cover low-range power applications and three-phase VSIs cover medium- to high-power applications. The main purpose of these topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms (e.g. ASDs, UPSs, FACTS, var compensators), arbitrary voltages are also required in some emerging applications (e.g. active filters, voltage compensators).

The standard three-phase VSI topology is shown in Fig. 15.13 and the eight valid switch states are given in Table 15.3. As in single-phase VSIs, the switches of any leg

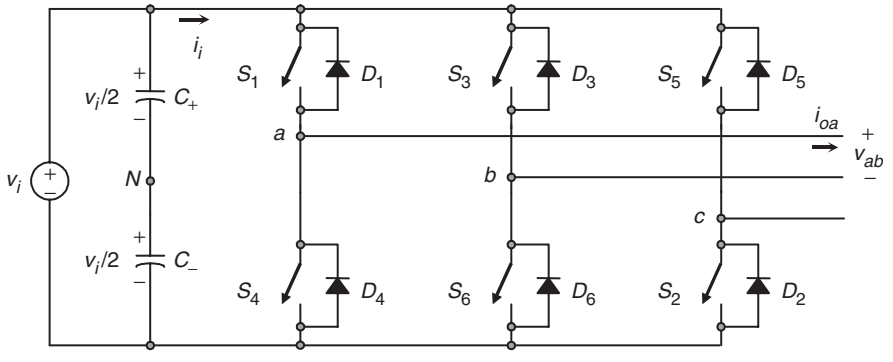

FIGURE 15.13 Three-phase VSI topology.

TABLE 15.3 Valid switch states for a three-phase VSI

State	State #	v_{ab}	v_{bc}	v_{ca}	Space vector
S_1, S_2, and S_6 are on and S_4, S_5, and S_3 are off	1	v_i	0	$-v_i$	$\vec{\mathbf{v}}_1 = 1 + j0.577$
S_2, S_3, and S_1 are on and S_5, S_6, and S_4 are off	2	0	v_i	$-v_i$	$\vec{\mathbf{v}}_2 = j1.155$
S_3, S_4, and S_2 are on and S_6, S_1, and S_5 are off	3	$-v_i$	v_i	0	$\vec{\mathbf{v}}_3 = -1 + j0.577$
S_4, S_5, and S_3 are on and S_1, S_2, and S_6 are off	4	$-v_i$	0	v_i	$\vec{\mathbf{v}}_4 = -1 - j0.577$
S_5, S_6, and S_4 are on and S_2, S_3, and S_1 are off	5	0	$-v_i$	v_i	$\vec{\mathbf{v}}_5 = -j1.155$
S_6, S_1, and S_5 are on and S_3, S_4, and S_2 are off	6	v_i	$-v_i$	0	$\vec{\mathbf{v}}_6 = 1 - j0.577$
S_1, S_3, and S_5 are on and S_4, S_6, and S_2 are off	7	0	0	0	$\vec{\mathbf{v}}_7 = 0$
S_4, S_6, and S_2 are on and S_1, S_3, and S_5 are off	8	0	0	0	$\vec{\mathbf{v}}_8 = 0$

of the inverter (S_1 and S_4, S_3 and S_6, or S_5 and S_2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity.

Of the eight valid states, two of them (7 and 8 in Table 15.3) produce zero ac line voltages. In this case, the ac line currents freewheel through either the upper or lower components. The remaining states (1 to 6 in Table 15.3) produce non-zero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus the resulting ac output line voltages consist of discrete values of voltages that are v_i, 0, and $-v_i$ for the topology shown in Fig. 15.13. The selection of the states in order to generate the given waveform is done by the modulating technique that should ensure the use of only the valid states.

15.3.1 Sinusoidal PWM

This is an extension of the one introduced for single-phase VSIs. In this case and in order to produce 120° out-of-phase load voltages, three modulating signals that are 120° out-of-phase are used. Figure 15.14 shows the ideal waveforms of three-phase VSI SPWM. In order to use a single carrier signal and preserve the features of the PWM technique, the normalized carrier frequency m_f should be an odd multiple of 3. Thus, all phase voltages (v_{aN}, v_{bN}, and v_{cN}) are identical, but 120° out-of-phase without even harmonics; moreover, harmonics at frequencies, a multiple of 3, are identical in amplitude and phase in all phases. For instance, if the ninth harmonic in phase aN is

$$v_{aN9}(t) = \hat{v}_9 \sin(9\omega t) \tag{15.26}$$

the ninth harmonic in phase bN will be

$$\begin{aligned} v_{bN9}(t) &= \hat{v}_9 \sin\left[9(\omega t - 120^\circ)\right] \\ &= \hat{v}_9 \sin(9\omega t - 1080^\circ) = \hat{v}_9 \sin(9\omega t) \end{aligned} \tag{15.27}$$

Thus, the ac output line voltage $v_{ab} = v_{aN} - v_{bN}$ will not contain the ninth harmonic. Therefore, for odd multiple of 3 values of the normalized carrier frequency m_f, the harmonics in the ac output voltage appear at normalized frequencies f_h centered around m_f and its multiples, specifically, at

$$h = l\, m_f \pm k \quad l = 1, 2, \ldots \tag{15.28}$$

where $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$ and $l = 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$ such that h is not a multiple of 3. Therefore, the harmonics will be at $m_f \pm 2$, $m_f \pm 4, \ldots$, $2m_f \pm 1$, $2m_f \pm 5, \ldots, 3m_f \pm 2$, $3m_f \pm 4, \ldots, 4m_f \pm 1$, $4m_f \pm 5, \ldots$. For nearly sinusoidal ac load current, the harmonics in the dc link current are at frequencies given by

$$h = l\, m_f \pm k \pm 1 \quad l = 1, 2, \ldots \tag{15.29}$$

where $l = 0, 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$ and $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$ such that $h = l \cdot m_f \pm k$ is positive and not a multiple of 3. For instance, Fig. 15.14h shows the sixth harmonic ($h = 6$), which is due to $h = 1 \cdot 9 - 2 - 1 = 6$.

The identical conclusions can be drawn for the operation at small and large values of m_f as for the single-phase configurations. However, because the maximum amplitude of the fundamental phase voltage in the linear region ($m_a \leq 1$) is $v_i/2$, the maximum amplitude of the fundamental ac output line voltage is $\sqrt{3}v_i/2$. Therefore, one can write

$$\hat{v}_{ab1} = m_a \sqrt{3} \frac{v_i}{2} \quad 0 < m_a \leq 1 \tag{15.30}$$

To further increase the amplitude of the load voltage, the amplitude of the modulating signal $\hat{v}_c$ can be made higher than the amplitude of the carrier signal $\hat{v}_\Delta$, which leads to overmodulation. The relationship between the amplitude of the fundamental ac output line voltage and the dc link voltage becomes non-linear as in single-phase VSIs. Thus, in the overmodulation region, the line voltages range is

$$\sqrt{3}\frac{v_i}{2} < \hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} < \frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{15.31}$$

15.3.2 Square-wave Operation of Three-phase VSIs

Large values of m_a in the SPWM technique lead to full overmodulation. This is known as square-wave operation as illustrated in Fig. 15.15, where the power valves are on for 180°.

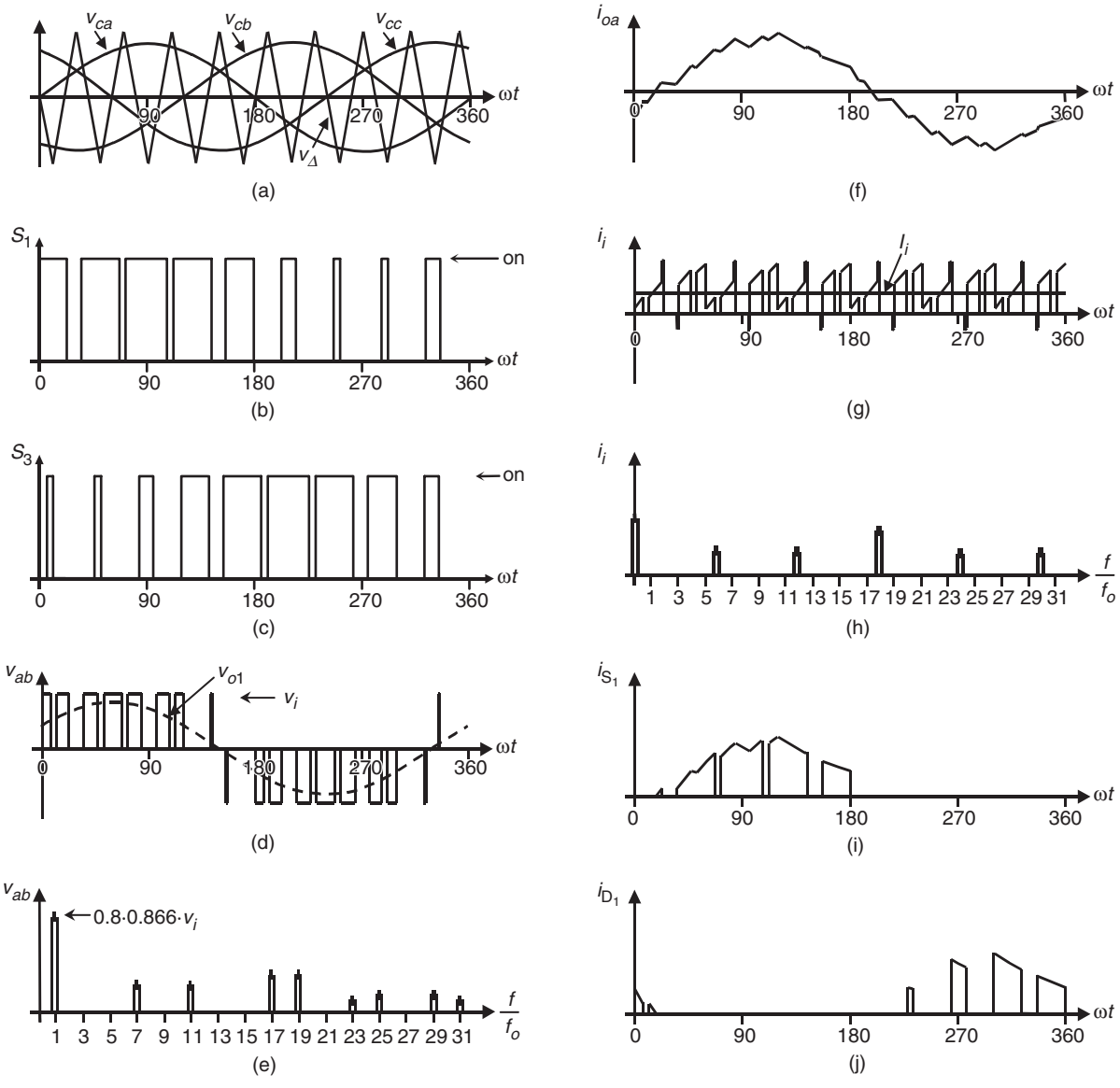

FIGURE 15.14 The three-phase VSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_1 current; and (j) diode D_1 current.

In this operation mode, the VSI cannot control the load voltage except by means of the dc link voltage v_i. This is based on the fundamental ac line-voltage expression

$$\hat{v}_{ab\,1} = \frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{15.32}$$

The ac line output voltage contains the harmonics f_h, where $h = 6 \cdot k \pm 1$ ($k = 1, 2, 3, \ldots$) and they feature amplitudes that are inversely proportional to their harmonic order (Fig. 15.15d). Their amplitudes are

$$\hat{v}_{ab\,h} = \frac{1}{h}\frac{4}{\pi}\sqrt{3}\frac{v_i}{2} \tag{15.33}$$

15.3.3 Sinusoidal PWM with Zero Sequence Signal Injection

The restriction for m_a ($m_a \leq 1$) can be relaxed if a zero sequence signal is added to the modulating signals before they are compared to the carrier signal. Figure 15.16 shows the block diagram of the technique. Clearly, the addition of

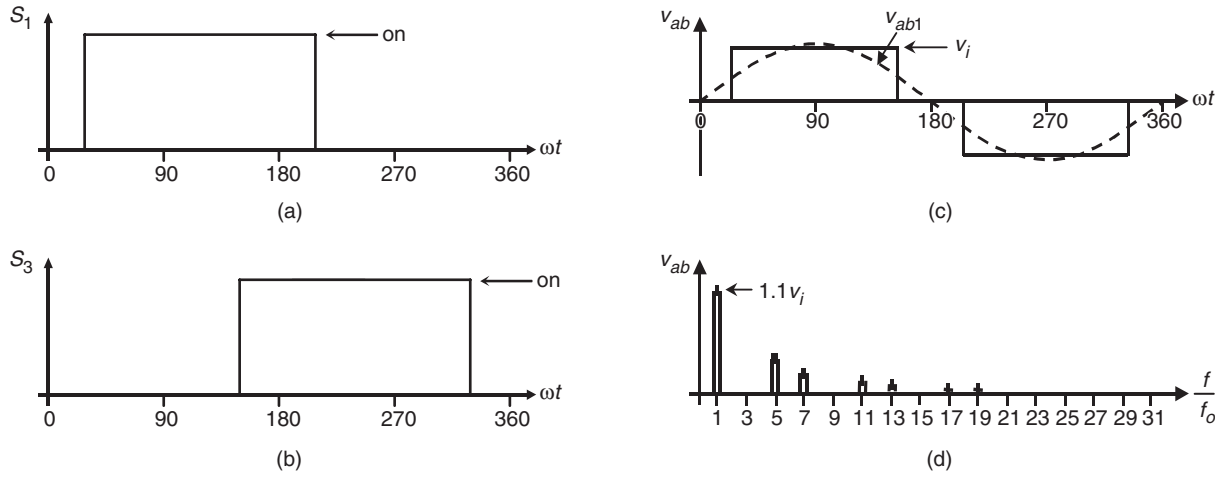

FIGURE 15.15 The three-phase VSI. Square-wave operation: (a) switch S_1 state; (b) switch S_3 state; (c) ac output voltage; and (d) ac output voltage spectrum.

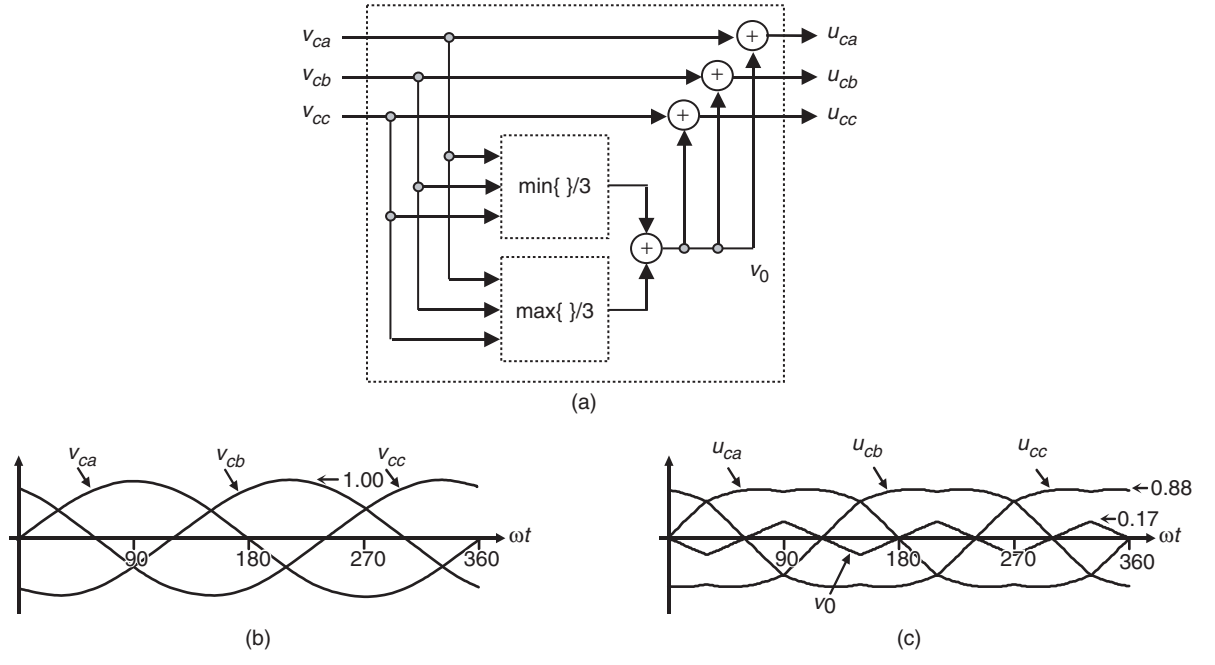

FIGURE 15.16 Zero sequence signal generator ($m_a = 1.0$, $m_f = 9$): (a) block diagram; (b) modulating signals; and (c) zero sequence and modulating signals with zero sequence injection.

the zero sequence reduces the peak amplitude of the resulting modulating signals (u_{ca}, u_{cb}, u_{cc}), while the fundamental components remain unchanged. This approach expands the range of the linear region as it allows the use of modulation indexes m_a up to $2/\sqrt{3}$ without getting into the overmodulating region.

The maximum amplitude of the fundamental phase voltage in the linear region $\left(m_a \leq 2/\sqrt{3}\right)$ is $v_i/2$, thus, the maximum amplitude of the fundamental ac output line voltage is v_i. Therefore, one can write

$$\hat{v}_{ab1} = m_a\sqrt{3}\frac{v_i}{2} \quad \left(0 < m_a \leq 2/\sqrt{3}\right) \tag{15.34}$$

Figure 15.17 shows the ideal waveforms of a three-phase VSI SPWM with zero injection for $m_a = 0.8$.

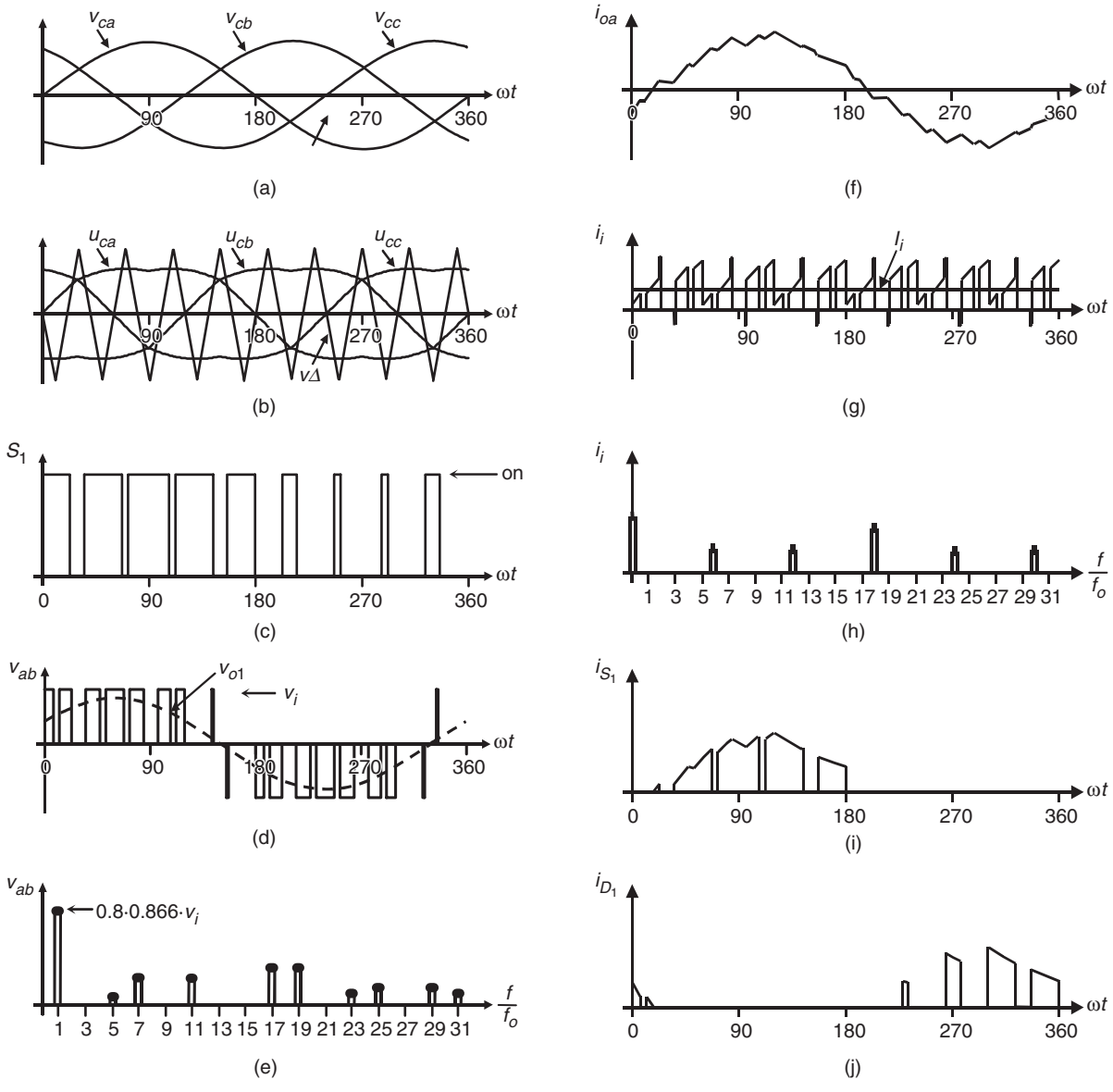

FIGURE 15.17 The three-phase VSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$) with zero sequence signal injection: (a) modulating signals; (b) carrier and modulating signals with zero sequence signal injection; (c) switch S_1 state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_1 current; and (j) diode D_1 current.

15.3.4 Selective Harmonic Elimination in Three-phase VSIs

As in single-phase VSIs, the SHE technique can be applied to three-phase VSIs. In this case, the power valves of each leg of the inverter are switched so as to eliminate a given number of harmonics and to control the fundamental phase-voltage amplitude. Considering that in many applications, the required line output voltages should be balanced and 120° out of phase, the harmonics multiples of 3 ($h = 3, 9, 15, \ldots$), which could be present in the phase voltages (v_{aN}, v_{bN}, and v_{cN}), will not be present in the load voltages (v_{ab}, v_{bc}, and v_{ca}). Therefore, these harmonics are not required to be eliminated, thus the chopping angles are used to eliminate only the harmonics at frequencies $h = 5, 7, 11, 13, \ldots$ as required.

The expressions to eliminate a given number of harmonics are the same as those used in single-phase inverters. For instance, to eliminate the fifth and seventh harmonics and perform fundamental magnitude control ($N = 3$), the equations

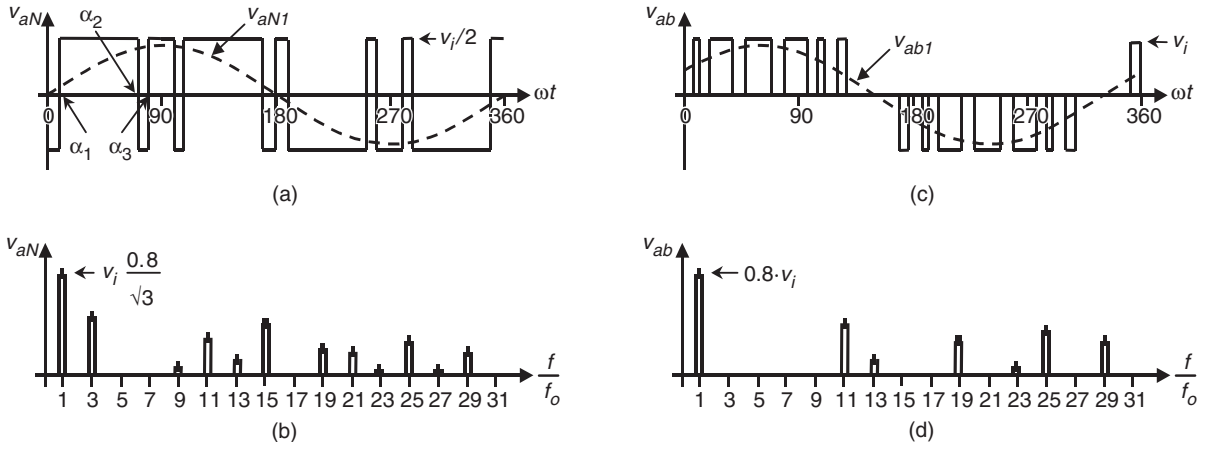

FIGURE 15.18 The three-phase VSI. Ideal waveforms for the SHE technique: (a) phase voltage v_{aN} for fifth and seventh harmonic elimination; (b) spectrum of (a); (c) line voltage v_{ab} for fifth and seventh harmonic elimination; and (d) spectrum of (c).

to be solved are:

$$\begin{aligned}
&\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) = (2 + \pi \hat{v}_{aN1}/v_i)/4 \\
&\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 1/2 \\
&\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) = 1/2
\end{aligned} \tag{15.35}$$

where the angles α_1, α_2, and α_3 are defined as shown in Fig. 15.18a and plotted in Fig. 15.19. Figure 15.18b shows that the third, ninth, fifteenth, ... harmonics are all present in the phase voltages; however, they are not in the line voltages (Fig. 15.18d).

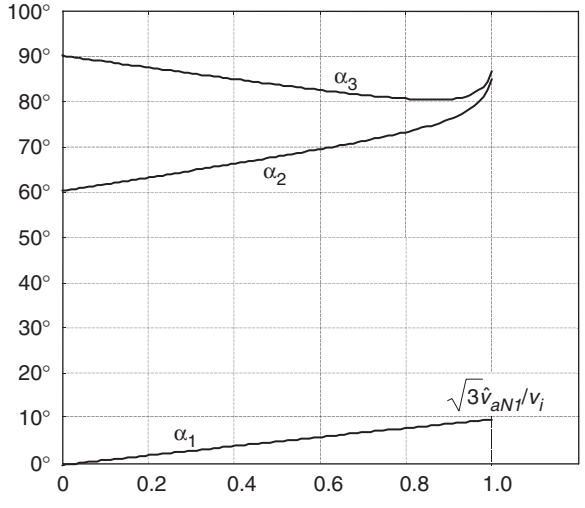

FIGURE 15.19 Chopping angles for SHE and fundamental voltage control in three-phase VSIs: fifth and seventh harmonic elimination.

15.3.5 Space-vector (SV)-based Modulating Techniques

At present, the control strategies are implemented in digital systems, and therefore digital modulating techniques are also available. The SV-based modulating technique is a digital technique in which the objective is to generate PWM load line voltages that are on average equal to given load line voltages. This is done in each sampling period by properly selecting the switch states from the valid ones of the VSI (Table 15.3) and by proper calculation of the period of times they are used. The selection and calculation times are based upon the SV transformation.

A. Space-vector Transformation

Any three-phase set of variables that add up to zero in the stationary *abc* frame can be represented in a complex plane by a complex vector that contains a real (α) and an imaginary (β) component. For instance, the vector of three-phase line-modulating signals $\mathbf{v_c^{abc}} = [v_{ca} v_{cb} v_{cc}]^T$ can be represented by the complex vector $\vec{\mathbf{v}}_\mathbf{c} = \mathbf{v_c^{\alpha\beta}} = [v_{c\alpha} v_{c\beta}]^T$ by means of the following transformation:

$$v_{c\alpha} = \frac{2}{3}\left[v_{ca} - 0.5\,(v_{cb} + v_{cc})\right] \tag{15.36}$$

$$v_{c\beta} = \frac{\sqrt{3}}{3}\,(v_{cb} - v_{cc}) \tag{15.37}$$

If the line-modulating signals $\mathbf{v_c^{abc}}$ are three balanced sinusoidal waveforms that feature an amplitude $\hat{v}_c$ and an angular frequency ω, the resulting modulating signals in the $\alpha\beta$ stationary frame become a vector $\vec{\mathbf{v}}_\mathbf{c} = \mathbf{v_c^{\alpha\beta}}$ of fixed module $\hat{v}_c$, which rotates at frequency ω (Fig. 15.20). Similarly, the SV transformation is applied to the line voltages of the eight states of the

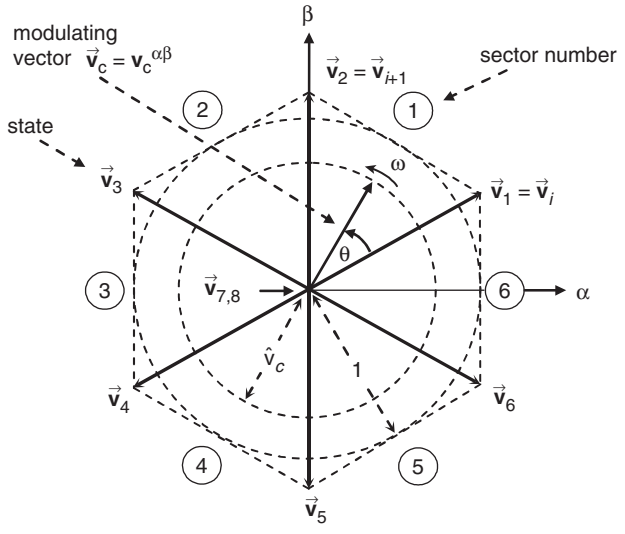

FIGURE 15.20 The space-vector representation.

VSI normalized with respect to v_i (Table 15.3), which generates the eight space vectors ($\vec{\mathbf{v}}_i$, $i = 1, 2, \ldots, 8$) in Fig. 15.20. As expected, $\vec{\mathbf{v}}_1$ to $\vec{\mathbf{v}}_6$ are non-null line-voltage vectors and $\vec{\mathbf{v}}_7$ and $\vec{\mathbf{v}}_8$ are null line-voltage vectors.

The objective of the SV technique is to approximate the line-modulating signal space vector $\vec{\mathbf{v}}_\mathbf{c}$ with the eight space vectors ($\vec{\mathbf{v}}_i$, $i = 1, 2, \ldots, 8$) available in VSIs. However, if the modulating signal $\vec{\mathbf{v}}_\mathbf{c}$ is laying between the arbitrary vectors $\vec{\mathbf{v}}_i$ and $\vec{\mathbf{v}}_{i+1}$, only the nearest two non-zero vectors ($\vec{\mathbf{v}}_i$ and $\vec{\mathbf{v}}_{i+1}$) and one zero SV ($\vec{\mathbf{v}}_z = \vec{\mathbf{v}}_7$ or $\vec{\mathbf{v}}_8$) should be used. Thus, the maximum load line voltage is maximized and the switching frequency is minimized. To ensure that the generated voltage in one sampling period T_s (made up of the voltages provided by the vectors $\vec{\mathbf{v}}_i$, $\vec{\mathbf{v}}_{i+1}$, and $\vec{\mathbf{v}}_z$ used during times T_i, T_{i+1}, and T_z) is on average equal to the vector $\vec{\mathbf{v}}_\mathbf{c}$ the following expression should hold:

$$\vec{\mathbf{v}}_\mathbf{c} \cdot T_s = \vec{\mathbf{v}}_i \cdot T_s + \vec{\mathbf{v}}_{i+1} \cdot T_{i+1} + \vec{\mathbf{v}}_z \cdot T_z \tag{15.38}$$

The solution of the real and imaginary parts of Eq. (15.37) for a line-load voltage that features an amplitude restricted to $0 \leq \hat{v}_c \leq 1$ gives

$$T_i = T_s \cdot \hat{v}_c \cdot \sin(\pi/3 - \theta) \tag{15.39}$$

$$T_{i+1} = T_s \cdot \hat{v}_c \cdot \sin(\theta) \tag{15.40}$$

$$T_z = T_s - T_i - T_{i+1} \tag{15.41}$$

The preceding expressions indicate that the maximum fundamental line-voltage amplitude is unity as $0 \leq \theta \leq \pi/3$. This is an advantage over the SPWM technique which achieves a $\sqrt{3}/2$ maximum fundamental line-voltage amplitude in the linear operating region. Although, the space vector modulation (SVM) technique selects the vectors to be used and their respective on-times, the sequence in which they are used, the selection of the zero space vector, and the normalized sampled frequency remain undetermined.

For instance, if the modulating line-voltage vector is in sector 1 (Fig. 15.20), the vectors $\vec{\mathbf{v}}_1$, $\vec{\mathbf{v}}_2$, and $\vec{\mathbf{v}}_z$ should be used within a sampling period by intervals given by T_1, T_2, and T_z, respectively. The question that remains is whether the sequence (i) $\vec{\mathbf{v}}_1 - \vec{\mathbf{v}}_2 - \vec{\mathbf{v}}_z$, (ii) $\vec{\mathbf{v}}_z - \vec{\mathbf{v}}_1 - \vec{\mathbf{v}}_2 - \vec{\mathbf{v}}_z$, (iii) $\vec{\mathbf{v}}_z - \vec{\mathbf{v}}_1 - \vec{\mathbf{v}}_2 - \vec{\mathbf{v}}_1 - \vec{\mathbf{v}}_z$, (iv) $\vec{\mathbf{v}}_z - \vec{\mathbf{v}}_1 - \vec{\mathbf{v}}_2 - \vec{\mathbf{v}}_z - \vec{\mathbf{v}}_2 - \vec{\mathbf{v}}_1 - \vec{\mathbf{v}}_z$, or any other sequence should actually be used. Finally, the technique does not indicate whether $\vec{\mathbf{v}}_z$ should be $\vec{\mathbf{v}}_7$, $\vec{\mathbf{v}}_8$, or a combination of both.

B. Space-vector Sequences and Zero Space-vector Selection

The sequence to be used should ensure load line-voltages that feature quarter-wave symmetry in order to reduce unwanted harmonics in their spectra (even harmonics). Additionally, the zero SV selection should be done in order to reduce the switching frequency. Although there is not a systematic approach to generate a SV sequence, a graphical representation shows that the sequence $\vec{\mathbf{v}}_i, \vec{\mathbf{v}}_{i+1}, \vec{\mathbf{v}}_z$ (where $\vec{\mathbf{v}}_z$ is alternately chosen among $\vec{\mathbf{v}}_7$ and $\vec{\mathbf{v}}_8$) provides high performance in terms of minimizing unwanted harmonics and reducing the switching frequency.

C. The Normalized Sampling Frequency

The normalized carrier frequency m_f in three-phase carrier-based PWM techniques is chosen to be an odd integer number multiple of 3 ($m_f = 3 \cdot n$, $n = 1, 3, 5, \ldots$). Thus, it is possible to minimize parasitic or non-intrinsic harmonics in the PWM waveforms. A similar approach can be used in the SVM technique to minimize uncharacteristic harmonics. Hence, it is found that the normalized sampling frequency f_{sn} should be an integer multiple of 6. This is due to the fact that in order to produce symmetrical line voltages, all the sectors (a total of 6) should be used equally in one period. As an example, Fig. 15.21 shows the relevant waveforms of a VSI SVM for $f_{sn} = 18$ and $\hat{v}_c = 0.8$. Figure 15.21 confirms that the first set of relevant harmonics in the load line voltage are at f_{sn} which is also the switching frequency.

15.3.6 DC Link Current in Three-phase VSIs

Due to the fact that the inverter is assumed to be lossless and constructed without storage energy components, the instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_{ab}(t) \cdot i_a(t) + v_{bc}(t) \cdot i_b(t) + v_{ca}(t) \cdot i_c(t) \tag{15.42}$$

where $i_a(t)$, $i_b(t)$, and $i_c(t)$ are the phase-load currents as shown in Fig. 15.22. If the load is balanced and inductive, and a relatively high switching frequency is used, the load currents become nearly sinusoidal balanced waveforms. On the other

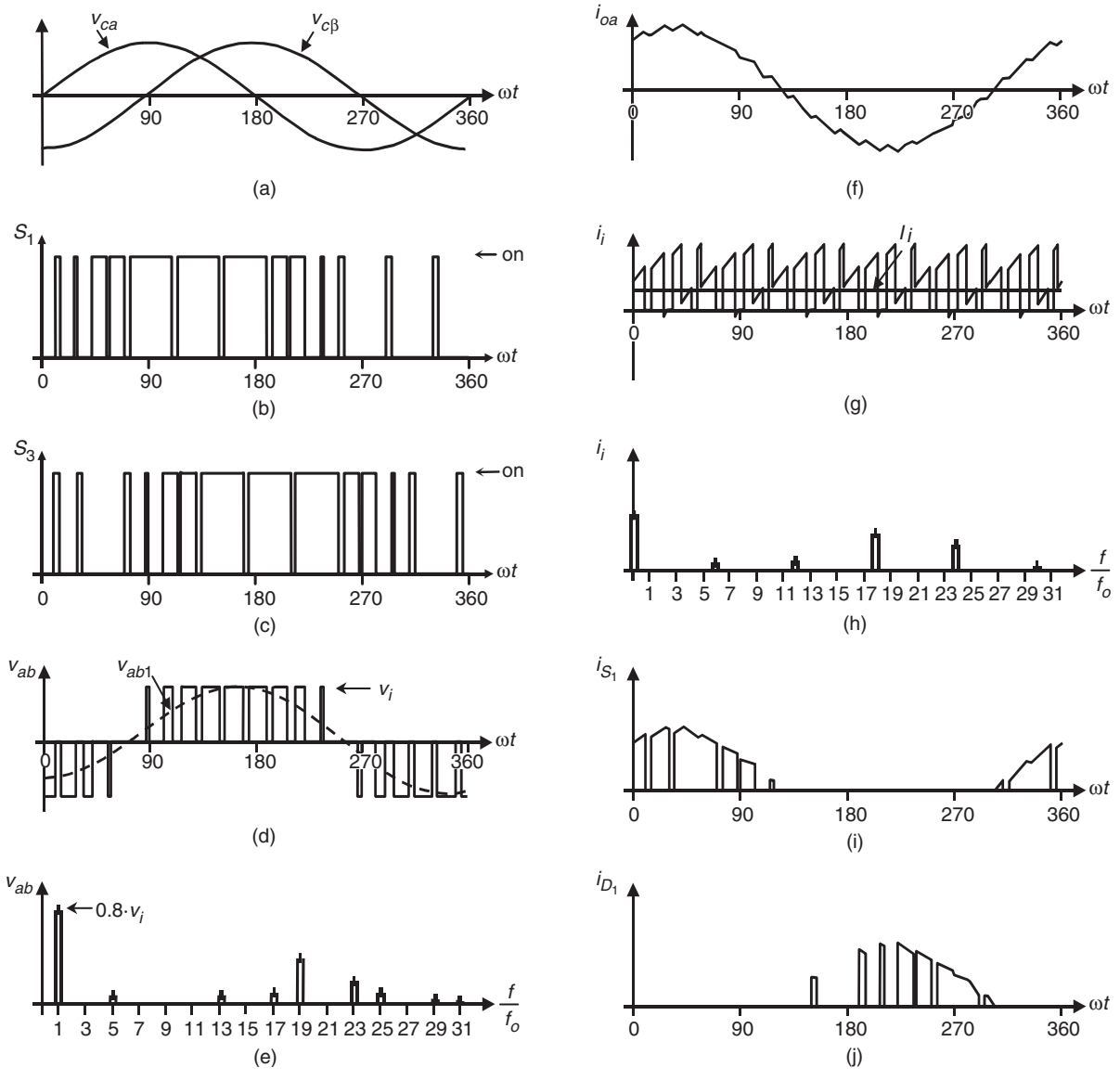

FIGURE 15.21 The three-phase VSI. Ideal waveforms for space-vector modulation ($\hat{v}_c = 0.8$, $f_{sn} = 18$): (a) modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output voltage; (e) ac output voltage spectrum; (f) ac output current; (g) dc current; (h) dc current spectrum; (i) switch S_1 current; and (j) diode D_1 current.

hand, if the ac output voltages are considered sinusoidal and the dc link voltage is assumed constant $v_i(t) = V_i$, Eq. (15.42) can be simplified to

$$i_i(t) = \frac{1}{V_i}\left\{\begin{array}{l} \sqrt{2}V_{o1}\sin(\omega t)\cdot\sqrt{2}I_o\sin(\omega t-\phi) \\ +\sqrt{2}V_{o1}\sin(\omega t-120^\circ)\cdot\sqrt{2}I_o\sin(\omega t-120^\circ-\phi) \\ +\sqrt{2}V_{o1}\sin(\omega t-240^\circ)\cdot\sqrt{2}I_o\sin(\omega t-240^\circ-\phi) \end{array}\right\} \tag{15.43}$$

where V_{o1} is the fundamental rms ac output line voltage, I_o is the rms load-phase current, and ϕ is an arbitrary inductive load power factor. Hence, the dc link current expression can be further simplified to

$$i_i(t) = 3\frac{V_{o1}}{V_i}I_o\cos(\phi) = \sqrt{3}\frac{V_{o1}}{V_i}I_l\cos(\phi) \tag{15.44}$$

where $I_l = \sqrt{3}I_o$ is the rms load line current. The resulting dc link current expression indicates that under harmonic-free load voltages, only a clean dc current should be expected in the dc bus and, compared to single-phase VSIs, there is no presence of second harmonic. However, as the ac load line voltages contain harmonics around the normalized sampling

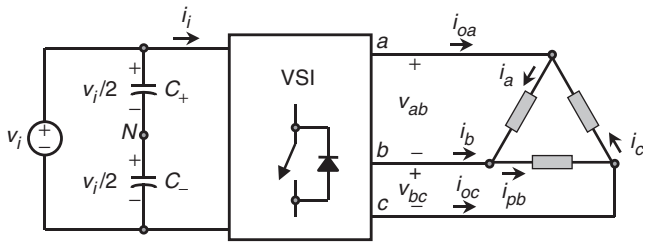

FIGURE 15.22 Phase-load currents definition in a delta-connected load.

frequency f_{sn}, the dc link current will contain harmonics but around f_{sn} as shown in Fig. 15.21h.

15.3.7 Load-phase Voltages in Three-phase VSIs

The load is sometimes wye-connected and the phase-load voltages v_{an}, v_{bn}, and v_{cn} may be required (Fig. 15.23). To obtain them, it should be considered that the line-voltage vector is

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{an} - v_{bn} \\ v_{bn} - v_{cn} \\ v_{cn} - v_{an} \end{bmatrix} \tag{15.45}$$

which can be written as a function of the phase-voltage vector $[v_{an} v_{bn} v_{cn}]^T$ as

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{15.46}$$

Expression (15.46) represents a linear system where the unknown quantity is the vector $[v_{an} v_{bn} v_{cn}]^T$. Unfortunately, the system is singular as the rows add up to zero (line voltages add up to zero), therefore, the phase-load voltages cannot be obtained by matrix inversion. However, if the phase-load voltages add up to zero, Eq. (15.46) can be rewritten as

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{15.47}$$

which is not singular and hence,

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 1 & 1 \\ -1 & 1 & 1 \\ -1 & -2 & 1 \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} \tag{15.48}$$

that can be further simplified to

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \end{bmatrix} \tag{15.49}$$

The final expression for the phase-load voltages is only a function of v_{ab} and v_{bc}, which is due to fact that the last row in Eq. (15.46) is chosen to be only ones. Figure 15.24 shows the line- and phase-voltages obtained using Eq. (15.49).

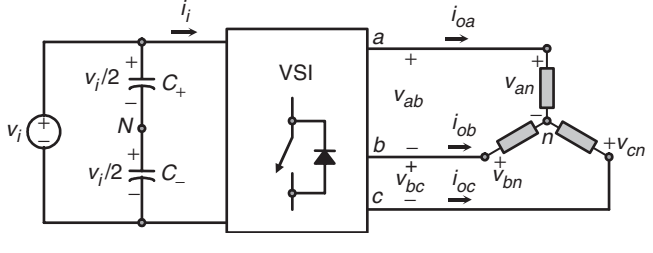

FIGURE 15.23 Phase-load voltages definition in a wye-connected load.

15.4 Current Source Inverters

The main objective of these static power converters is to produce an ac output current waveforms from a dc current power supply. For sinusoidal ac outputs, its magnitude, frequency, and phase should be controllable. Due to the fact that the ac line currents i_{oa}, i_{ob}, and i_{oc} (Fig. 15.25) feature high di/dt, a capacitive filter should be connected at the ac terminals in inductive load applications (such as ASDs). Thus, nearly sinusoidal load voltages are generated that justifies the use of these topologies in medium-voltage industrial applications, where high-quality voltage waveforms are required. Although single-phase CSIs can in the same way as three-phase CSIs topologies, be developed under similar principles, only three-phase applications are of practical use and are analyzed below.

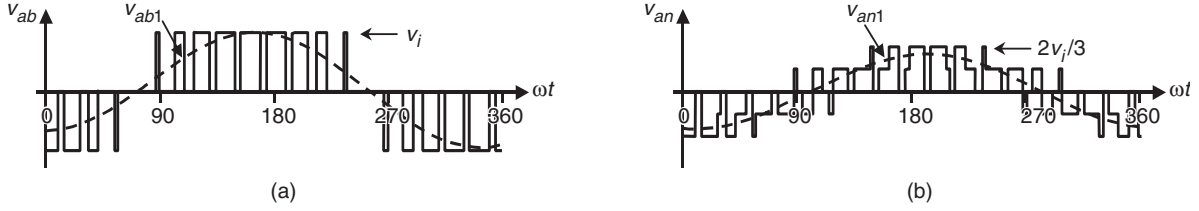

FIGURE 15.24 The three-phase VSI. Line- and phase-load voltages: (a) line-load voltage v_{ab}; and (b) phase-load voltage v_{an}.

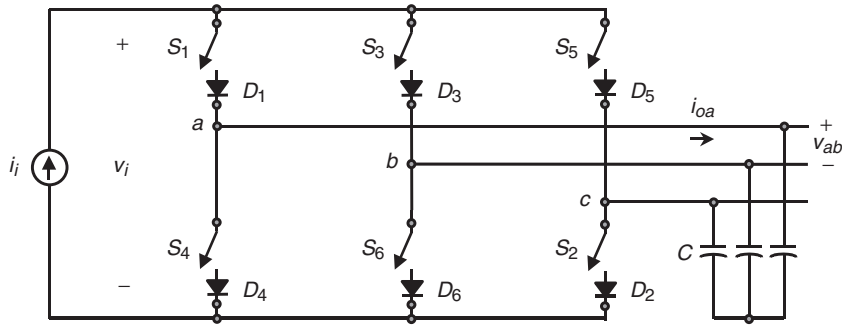

FIGURE 15.25 Three-phase CSI topology.

In order to properly gate the power switches of a three-phase CSI, two main constraints must always be met: (a) the ac side is mainly capacitive, thus, it must not be short-circuited; this implies that, at most one top switch (1, 3, or 5 (Fig. 15.25)) and one bottom switch (4, 6, or 2 (Fig. 15.25)) should be closed at any time; and (b) the dc bus is of the current-source type and thus it cannot be opened; therefore, there must be at least one top switch (1, 3, or 5) and one bottom switch (4, 6, or 2) closed at all times. Note that both constraints can be summarized by stating that at any time, only one top switch and one bottom switch must be closed.

There are nine valid states in three-phase CSIs. The states 7, 8, and 9 (Table 15.4) produce zero ac line currents. In this case, the dc link current freewheels through either the switches S_1 and S_4, switches S_3 and S_6, or switches S_5 and S_2. The remaining states (1 to 6 in Table 15.4) produce non-zero ac output line currents. In order to generate a given set of ac line current waveforms, the inverter must move from one state to another. Thus, the resulting line currents consist of discrete values of current, which are i_i, 0, and $-i_i$. The selection of the states in order to generate the given waveforms is done by the modulating technique that should ensure the use of only the valid states.

TABLE 15.4 Valid switch states for a three-phase CSI

State	State #	i_{oa}	i_{ob}	i_{oc}	Space vector
S_1 and S_2 are on and S_3, S_4, S_5, and S_6 are off	1	i_i	0	$-i_i$	$\vec{\mathbf{i}}_1 = 1 + j0.577$
S_2 and S_3 are on and S_4, S_5, S_6, and S_1 are off	2	0	i_i	$-i_i$	$\vec{\mathbf{i}}_2 = j1.155$
S_3 and S_4 are on and S_5, S_6, S_1, and S_2 are off	3	$-i_i$	i_i	0	$\vec{\mathbf{i}}_3 = -1 + j0.577$
S_4 and S_5 are on and S_6, S_1, S_2, and S_3 are off	4	$-i_i$	0	i_i	$\vec{\mathbf{i}}_4 = -1 - j0.577$
S_5 and S_6 are on and S_1, S_2, S_3, and S_4 are off	5	0	$-i_i$	i_i	$\vec{\mathbf{i}}_5 = -j1.155$
S_6 and S_1 are on and S_2, S_3, S_4, and S_5 are off	6	i_i	$-i_i$	0	$\vec{\mathbf{i}}_6 = 1 - j0.577$
S_1 and S_4 are on and S_2, S_3, S_5, and S_6 are off	7	0	0	0	$\vec{\mathbf{i}}_7 = 0$
S_3 and S_6 are on and S_1, S_2, S_4, and S_5 are off	8	0	0	0	$\vec{\mathbf{i}}_8 = 0$
S_5 and S_2 are on and S_6, S_1, S_3, and S_4 are off	9	0	0	0	$\vec{\mathbf{i}}_9 = 0$

There are several modulating techniques that deal with the special requirements of CSIs and can be implemented online. These techniques are classified into three categories: (a) the carrier-based; (b) the SHE-based; and (c) the SV-based techniques. Although they are different, they generate gating signals that satisfy the special requirements of CSIs. To simplify the analysis, a constant dc link-current source is considered ($i_i = I_i$).

15.4.1 Carrier-based PWM Techniques in CSIs

It has been shown that the carrier-based PWM techniques that were initially developed for three-phase VSIs can be extended to three-phase CSIs. The circuit shown in Fig. 15.26 obtains the gating pattern for a CSI from the gating pattern developed for a VSI. As a result, the line current appears to be identical to the line voltage in a VSI for similar carrier and modulating signals.

It is composed of a *switching pulse generator*, a *shorting pulse generator*, a *shorting pulse distributor*, and a *switching and shorting pulse combinator*. The circuit basically produces the gating signals ($\mathbf{s} = [s_1 \dots s_6]^T$) according to a carrier i_Δ and three modulating signals $\mathbf{i}_\mathbf{c}^{\text{abc}} = [i_{ca}\, i_{cb}\, i_{ca}]^T$. Therefore, any set of modulating signals which when combined result in a sinusoidal line-to-line set of signals, will satisfy the requirement for a sinusoidal line current pattern. Examples of such a modulating signals are the standard sinusoidal, sinusoidal with third harmonic injection, trapezoidal, and deadband waveforms.

The first component of this stage (Fig. 15.26) is the *switching pulse generator*, where the signals $\mathbf{s}_\mathbf{a}^{123}$ are generated according to:

$$\mathbf{s}_\mathbf{a}^{123} = \begin{cases} \text{HIGH} = 1 & \textit{if} \quad \mathbf{i}_\mathbf{c}^{\text{abc}} > v_c \\ \text{LOW} = 0 & \textit{otherwise} \end{cases} \tag{15.50}$$

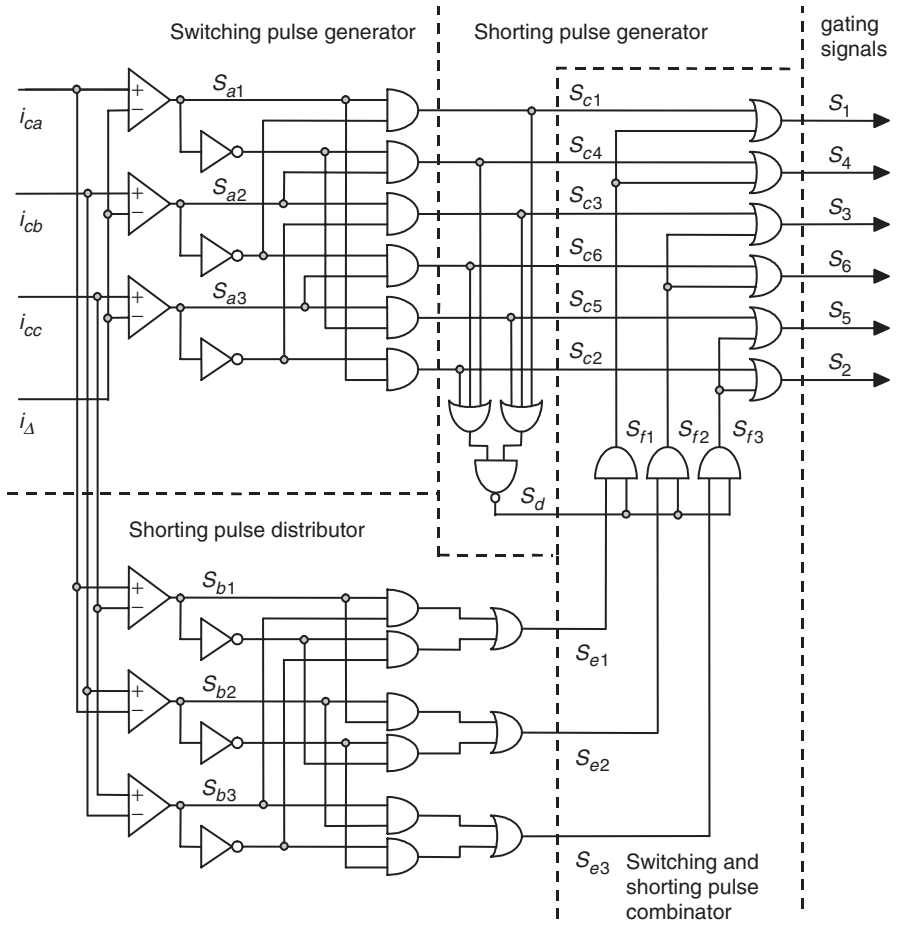

FIGURE 15.26 The three-phase CSI. Gating pattern generator for analog on-line carrier-based PWM.

The outputs of the *switching pulse generator* are the signals $\mathbf{s_c}$, which are basically the gating signals of the CSI without the shorting pulses. These are necessary to freewheel the dc link current i_i when zero ac output currents are required. Table 15.5 shows the truth table of $\mathbf{s_c}$ for all combinations of their inputs $\mathbf{s_a^{123}}$. It can be clearly seen that at most one top switch and one bottom switch is on, which satisfies the first constraint of the gating signals as stated before.

In order to satisfy the second constraint, the shorting pulse (s_d =1) (s_d = 1) is generated (*shorting pulse generator* (Fig. 15.26)) the top switches ($s_{c1} = s_{c3} = s_{c5} = 0$) or none of the bottom switches ($s_{c4} = s_{c6} = s_{c2} = 0$) are gated. Then, this pulse is added (using OR gates) to only one leg of the CSI (either to the switches 1 and 4, 3 and 6, or 5 and 2) by means of the *switching and shorting pulse combinator* (Fig. 15.26). The signals generated by the *shorting pulse generator* $\mathbf{s_e^{123}}$ ensure that: (a) only one leg of the CSI is shorted, as only one of the signals is HIGH at any time; and (b) there is an even distribution of the shorting pulse, as $\mathbf{s_e^{123}}$ is high for 120° in each period. This ensures that the rms currents are equal in all legs.

TABLE 15.5 Truth table for the switching pulse generator stage (Fig. 15.26)

s_{a1}	s_{a2}	s_{a3}	Top switches			Bottom switches		
			s_{c1}	s_{c3}	s_{c5}	s_{c4}	s_{c6}	s_{c2}
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	1	0
0	1	0	0	1	0	1	0	0
0	1	1	0	0	1	1	0	0
1	0	0	1	0	0	0	0	1
1	0	1	1	0	0	0	1	0
1	1	0	0	1	0	0	0	1
1	1	1	0	0	0	0	0	0

Figure 15.27 shows the relevant waveforms if a triangular carrier i_{Δ} and sinusoidal modulating signals $\mathbf{i_c^{abc}}$ are used in combination with the gating pattern generator circuit (Fig. 15.26); this is SPWM in CSIs. It can be observed that some of the waveforms (Fig. 15.27) are identical to those

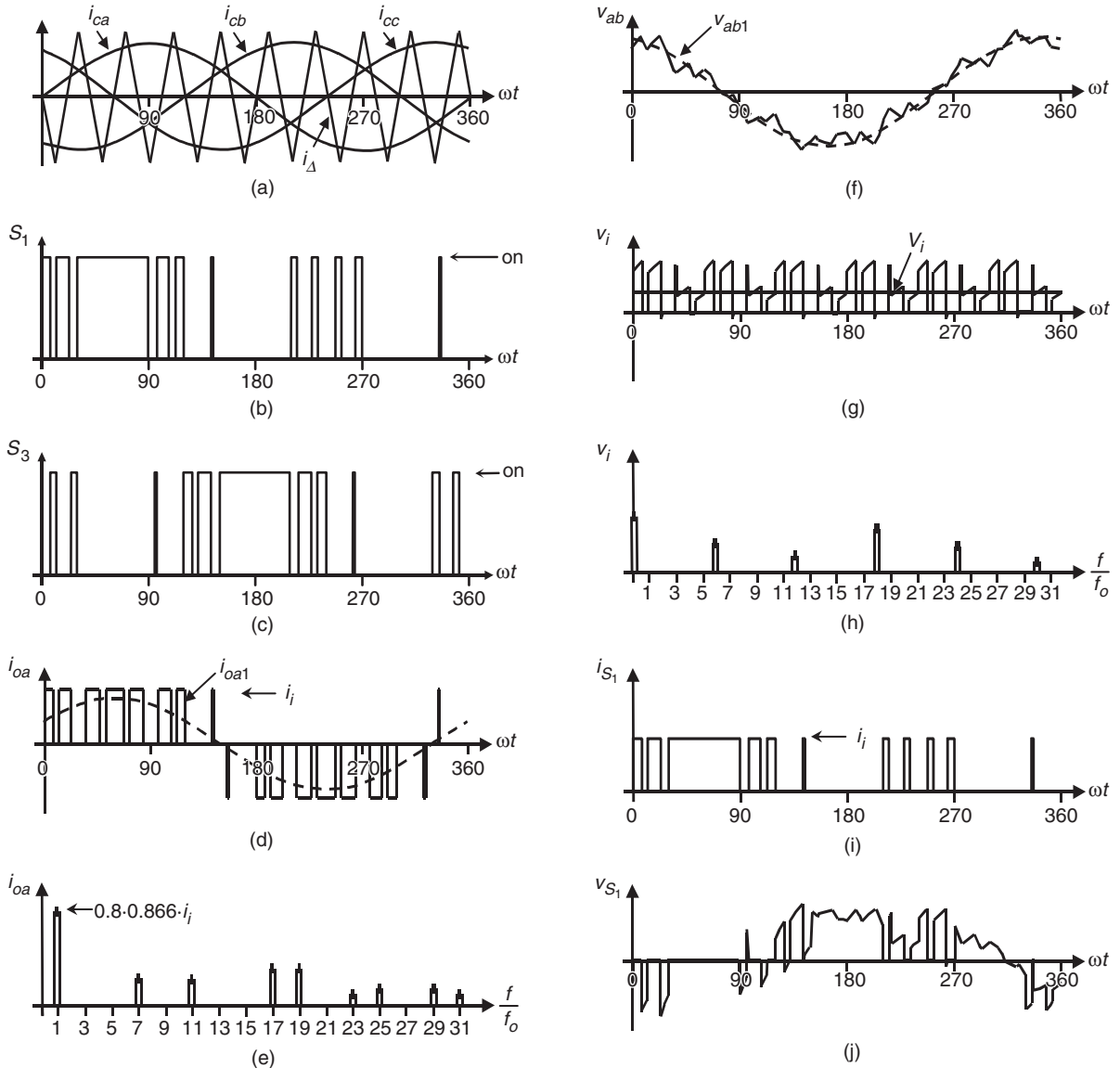

FIGURE 15.27 The three-phase CSI. Ideal waveforms for the SPWM ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output current; (e) ac output current spectrum; (f) ac output voltage; (g) dc voltage; (h) dc voltage spectrum; (i) switch S_1 current; and (j) switch S_1 voltage.

obtained in three-phase VSIs, where a SPWM technique is used (Fig. 15.15). Specifically: (i) the load line voltage (Fig. 15.15d) in the VSI is identical to the load line current (Fig. 15.27d) in the CSI; and (ii) the dc link current (Fig. 15.15g) in the VSI is identical to the dc link voltage (Fig. 15.27g) in the CSI.

This brings up the duality issue between both the topologies when similar modulation approaches are used. Therefore, for odd multiples of 3 values of the normalized carrier frequency m_f, the harmonics in the ac output current appear at normalized frequencies f_h centered around m_f and its multiples, specifically, at

$$h = l\,m_f \pm k \quad l = 1, 2, \ldots \tag{15.51}$$

where $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$ and $l = 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$ such that h is not a multiple of 3. Therefore, the harmonics will be at $m_f \pm 2$, $m_f \pm 4, \ldots$, $2m_f \pm 1$, $2m_f \pm 5, \ldots$, $3m_f \pm 2$, $3m_f \pm 4, \ldots$, $4m_f \pm 1$, $4m_f \pm 5, \ldots$. For nearly sinusoidal ac load voltages, the harmonics in the dc link voltage are at frequencies given by

$$h = l\,m_f \pm k \pm 1 \quad l = 1, 2, \ldots \tag{15.52}$$

where $l = 0, 2, 4, \ldots$ for $k = 1, 5, 7, \ldots$ and $l = 1, 3, 5, \ldots$ for $k = 2, 4, 6, \ldots$ such that $h = l \cdot m_f \pm k$ is positive and not a multiple of 3. For instance, Fig. 15.27h shows the sixth harmonic ($h = 6$), which is due to $h = 1 \cdot 9 - 2 - 1 = 6$. Identical conclusions can be drawn for the small and large values of m_f in the same way as for three-phase VSI configurations. Thus, the maximum amplitude of the fundamental ac output line current is $\hat{i}_{oa1} = \sqrt{3} i_i/2$ and therefore one can write

$$\hat{i}_{oa1} = m_a \frac{\sqrt{3}}{2} i_i \quad 0 < m_a \leq 1 \tag{15.53}$$

To further increase the amplitude of the load current, the overmodulation approach can be used. In this region, the fundamental line currents range in

$$\frac{\sqrt{3}}{2} i_i < \hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} < \frac{4}{\pi} \frac{\sqrt{3}}{2} i_i \tag{15.54}$$

To further test the gating signal generator circuit (Fig. 15.26), a sinusoidal set with third and ninth harmonic injection modulating signals are used. Figure 15.28 shows the relevant waveforms.

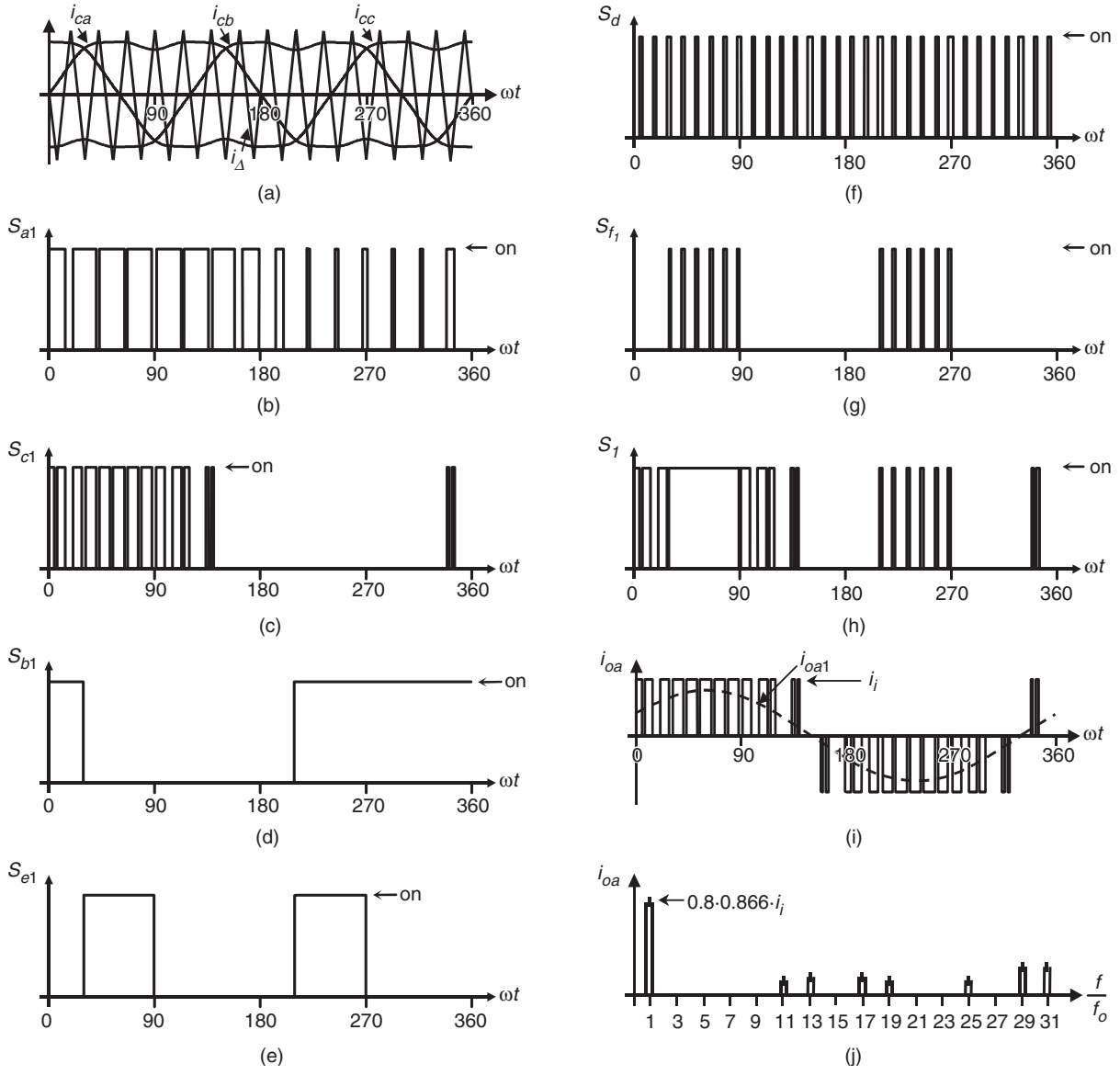

FIGURE 15.28 Gating pattern generator. Waveforms for third and ninth harmonic injection PWM ($m_a = 0.8$, $m_f = 15$): signals as described in Fig. 15.26.

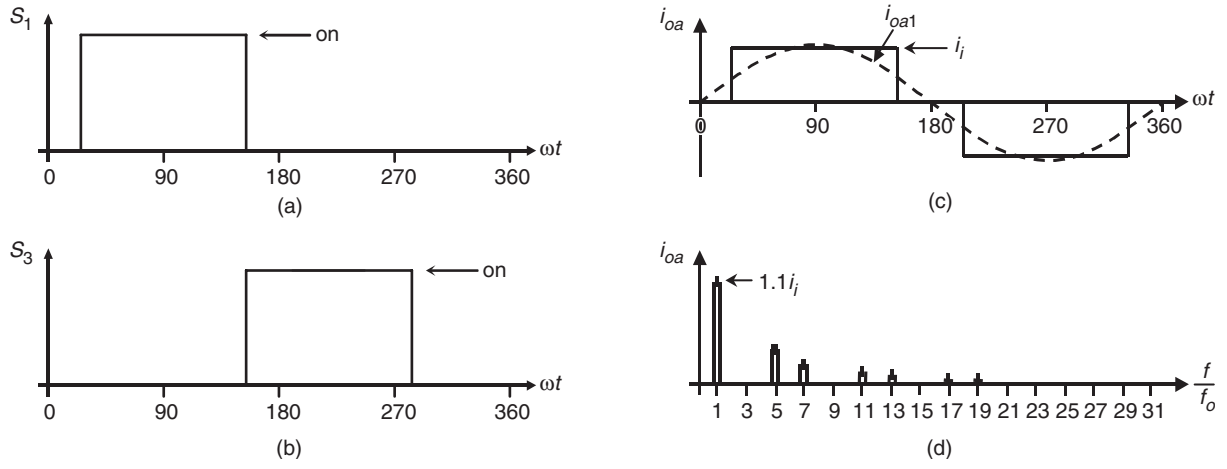

FIGURE 15.29 The three-phase CSI. Square-wave operation: (a) switch S_1 state; (b) switch S_3 state; (c) ac output current; and (d) ac output current spectrum.

15.4.2 Square-wave Operation of Three-phase CSIs

As in VSIs, large values of m_a in the SPWM technique lead to full overmodulation. This is known as square-wave operation. Figure 15.29 depicts this operating mode in a three-phase CSI, where the power valves are on for 120°. As presumed, the CSI cannot control the load current except by means of the dc link current i_i. This is due to the fact that the fundamental ac line current expression is

$$\hat{i}_{oa1} = \frac{4}{\pi}\frac{\sqrt{3}}{2} i_i \tag{15.55}$$

The ac line current contains the harmonics f_h, where $h = 6 \cdot k \pm 1$ ($k = 1, 2, 3, \ldots$), and they feature amplitudes that is inversely proportional to their harmonic order (Fig. 15.29d). Thus,

$$\hat{i}_{oah} = \frac{1}{h}\frac{4}{\pi}\frac{\sqrt{3}}{2} i_i \tag{15.56}$$

The duality issue among both the three-phase VSI and CSI should be noted especially in terms of the line-load waveforms. The line-load voltage produced by a VSI is identical to the load line current produced by the CSI when both are modulated using identical techniques. The next section will show that this also holds for SHE-based techniques.

15.4.3 Selective Harmonic Elimination in Three-phase CSIs

The SHE-based modulating techniques in VSIs define the gating signals such that a given number of harmonics are eliminated and the fundamental phase-voltage amplitude is controlled. If the required line output voltages are balanced and 120° out-of-phase, the chopping angles are used to eliminate only the harmonics at frequencies $h = 5, 7, 11, 13, \ldots$ as required.

The circuit shown in Fig. 15.30 uses the gating signals $\mathbf{s}_\mathbf{a}^{123}$ developed for a VSI and a set of synchronizing signals $\mathbf{i}_\mathbf{c}^{abc}$ to obtain the gating signals $\mathbf{s}$ for a CSI. The synchronizing signals $\mathbf{i}_\mathbf{c}^{abc}$ are sinusoidal balanced waveforms that are synchronized with the signals $\mathbf{s}_\mathbf{a}^{123}$ in order to symmetrically distribute the shorting pulse and thus generate symmetrical gating patterns. The circuit ensures line current waveforms as the line voltages in a VSI. Therefore, any arbitrary number of harmonics can be eliminated and the fundamental line current can be controlled in CSIs. Moreover, the same chopping angles obtained for VSIs can be used in CSIs.

For instance, to eliminate the fifth and seventh harmonics, the chopping angles are shown in Fig. 15.31, which are identical to that obtained for a VSI using Eq. (15.9). Figure 15.32 shows that the line current does not contain the fifth and the seventh harmonics as expected. Hence, any number of harmonics can be eliminated in three-phase CSIs by means of the circuit (Fig. 15.30) without the hassle of how to satisfy the gating signal constrains.

15.4.4 Space-vector-based Modulating Techniques in CSIs

The objective of the SV-based modulating technique is to generate PWM load line currents that are on average equal to given load line currents. This is done digitally in each sampling period by properly selecting the switch states from the valid ones of the CSI (Table 15.4) and the proper calculation of the period of times they are used. As in VSIs, the selection and time calculations are based upon the space-vector transformation.

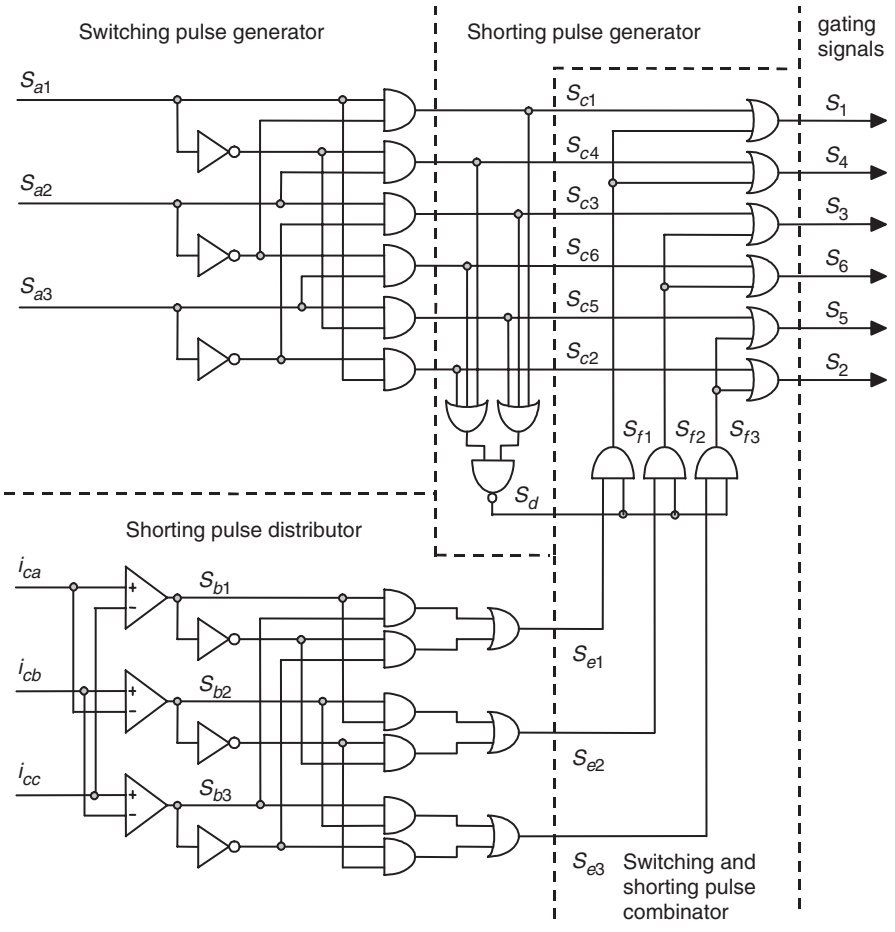

FIGURE 15.30 The three-phase CSI. Gating pattern generator for SHE PWM techniques.

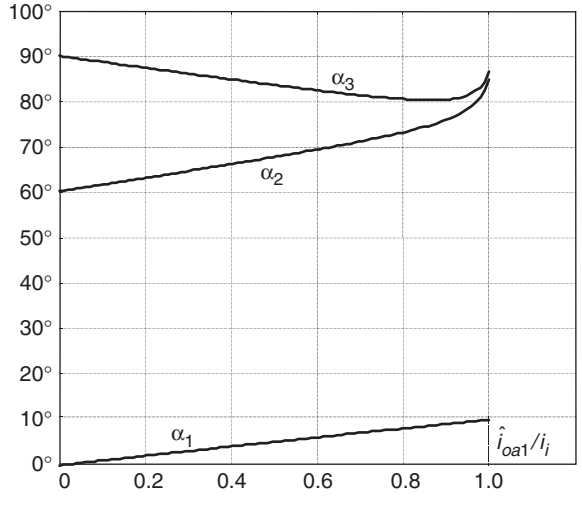

FIGURE 15.31 Chopping angles for SHE and fundamental current control in three-phase CSIs: fifth and seventh harmonic elimination.

A. Space-vector Transformation in CSIs

Similarly to VSIs, the vector of three-phase line-modulating signals $\mathbf{i}_\mathbf{c}^{abc} = [i_{ca}\, i_{cb}\, i_{cc}]^T$ can be represented by the complex vector $\vec{\mathbf{i}}_\mathbf{c} = \mathbf{i}_\mathbf{c}^{\alpha\beta} = [i_{c\alpha}\, i_{c\beta}]^T$ by means of Eqs. (15.36) and (15.37). For three-phase balanced sinusoidal modulating waveforms, which feature an amplitude $\hat{i}_c$ and an angular frequency ω, the resulting modulating signals complex vector $\vec{\mathbf{i}}_\mathbf{c} = \mathbf{i}_\mathbf{c}^{\alpha\beta}$ becomes a vector of fixed module $\hat{i}_c$, which rotates at frequency ω (Fig. 15.33). Similarly, the SV transformation is applied to the line currents of the nine states of the CSI normalized with respect to i_i, which generates nine space vectors ($\vec{\mathbf{i}}_\mathbf{i}$, $i = 1, 2, \ldots, 9$ in Fig. 15.33). As expected, $\vec{\mathbf{i}}_1$ to $\vec{\mathbf{i}}_6$ are non-null line current vectors and $\vec{\mathbf{i}}_7$, $\vec{\mathbf{i}}_8$, and $\vec{\mathbf{i}}_9$ are null line current vectors.

The SV technique approximates the line-modulating signal space vector $\vec{\mathbf{i}}_\mathbf{c}$ by using the nine space vectors ($\vec{\mathbf{i}}_i$, $i = 1, 2, \ldots, 9$) available in CSIs. If the modulating signal vector $\vec{\mathbf{i}}_\mathbf{c}$ is between the arbitrary vectors $\vec{\mathbf{i}}_i$ and $\vec{\mathbf{i}}_{i+1}$, then $\vec{\mathbf{i}}_i$ and $\vec{\mathbf{i}}_{i+1}$ combined with one zero SV ($\vec{\mathbf{i}}_z = \vec{\mathbf{i}}_7$ or $\vec{\mathbf{i}}_8$ or $\vec{\mathbf{i}}_9$) should be used to generate $\vec{\mathbf{i}}_\mathbf{c}$. To ensure that the generated current in

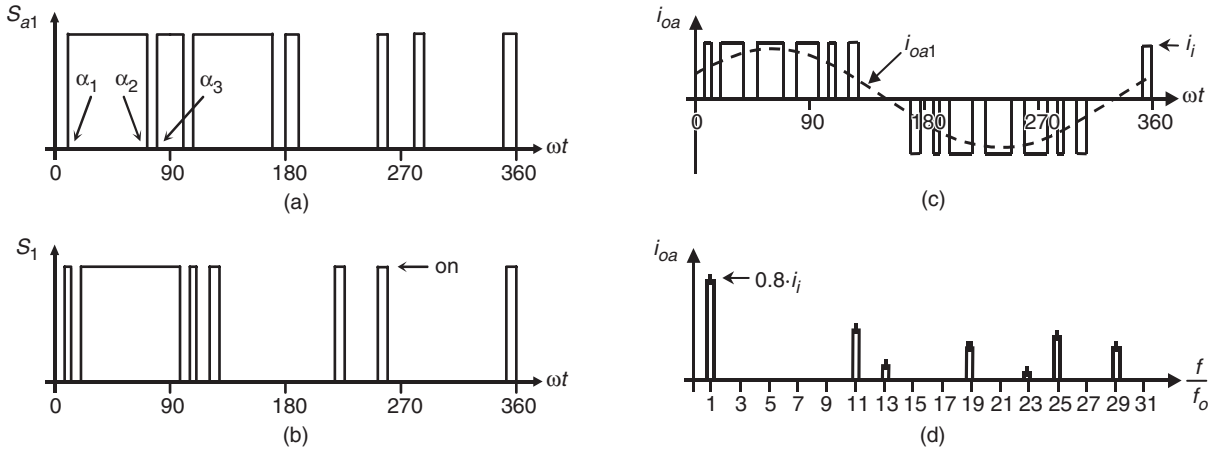

FIGURE 15.32 The three-phase CSI. Ideal waveforms for the SHE technique: (a) VSI gating pattern for fifth and seventh harmonic elimination; (b) CSI gating pattern for fifth and seventh harmonic elimination; (c) line current i_{oa} for fifth and seventh harmonic elimination; and (d) spectrum of (c).

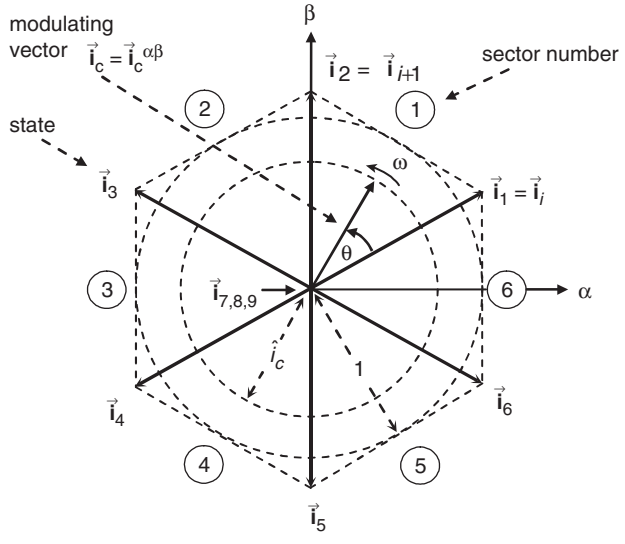

FIGURE 15.33 The space-vector representation in CSIs.

one sampling period T_s (made up of the currents provided by the vectors $\vec{\mathbf{i}}_i$, $\vec{\mathbf{i}}_{i+1}$, and $\vec{\mathbf{i}}_z$ used during times T_i, T_{i+1}, and T_z) is on average equal to the vector $\vec{\mathbf{i}}_\mathbf{c}$, the following expressions should hold:

$$T_i = T_s \cdot \hat{i}_c \cdot \sin(\pi/3 - \theta) \tag{15.57}$$

$$T_{i+1} = T_s \cdot \hat{i}_c \cdot \sin(\theta) \tag{15.58}$$

$$T_z = T_s - T_i - T_{i+1} \tag{15.59}$$

where $0 \leq \hat{i}_c \leq 1$. Although, the SVM technique selects the vectors to be used and their respective on-times, the sequence in which they are used, the selection of the zero space vector, and the normalized sampled frequency remain undetermined.

B. Space-vector Sequences and Zero Space-vector Selection

Although there is no systematic approach to generate a SV sequence, a graphical representation shows that the sequence $\vec{\mathbf{i}}_i$, $\vec{\mathbf{i}}_{i+1}$, $\vec{\mathbf{i}}_z$ (where the chosen $\vec{\mathbf{i}}_z$ depends upon the sector) provides high performance in terms of minimizing unwanted harmonics and reducing the switching frequency. To obtain the zero SV that minimizes the switching frequency, it is assumed that $\mathbf{I_c}$ is in Sector ②. Then Fig. 15.34 shows all

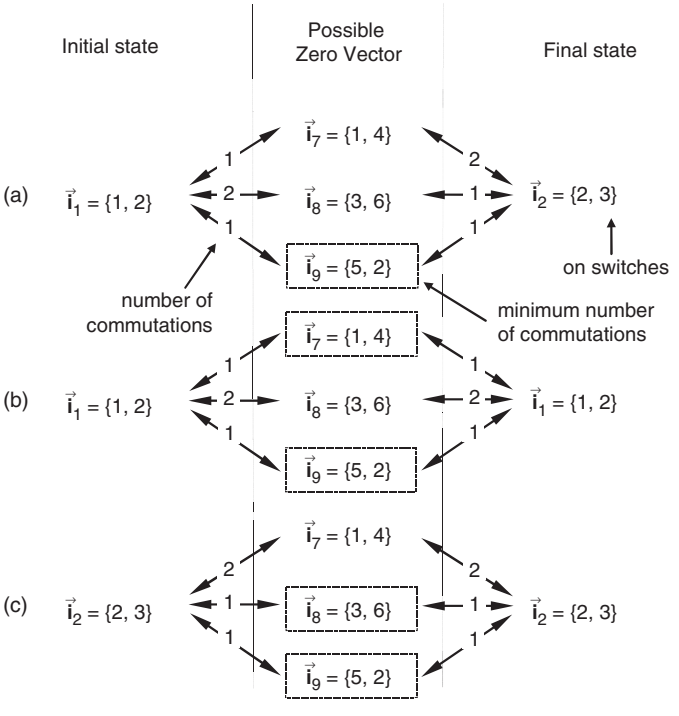

FIGURE 15.34 Possible state transitions in Sector ② involving a zero SV: (a) transition: $\vec{\mathbf{i}}_1 \Leftrightarrow \vec{\mathbf{i}}_z \Leftrightarrow \vec{\mathbf{i}}_2$ or $\vec{\mathbf{i}}_2 \Leftrightarrow \vec{\mathbf{i}}_z \Leftrightarrow \vec{\mathbf{i}}_1$; (b) transition: $\vec{\mathbf{i}}_1 \Leftrightarrow \vec{\mathbf{i}}_z \Leftrightarrow \vec{\mathbf{i}}_1$; and (c) transition: $\vec{\mathbf{i}}_2 \Leftrightarrow \vec{\mathbf{i}}_z \Leftrightarrow \vec{\mathbf{i}}_2$.

TABLE 15.6 Zero SV for minimum switching frequency in CSI and sequence $\vec{\mathbf{i}}_i$, $\vec{\mathbf{i}}_{i+1}$, $\vec{\mathbf{i}}_z$

Sector	$\vec{\mathbf{i}}_i$	$\vec{\mathbf{i}}_{i+1}$	$\vec{\mathbf{i}}_z$
①	$\vec{\mathbf{i}}_6$	$\vec{\mathbf{i}}_1$	$\vec{\mathbf{i}}_7$
②	$\vec{\mathbf{i}}_1$	$\vec{\mathbf{i}}_2$	$\vec{\mathbf{i}}_9$
③	$\vec{\mathbf{i}}_2$	$\vec{\mathbf{i}}_3$	$\vec{\mathbf{i}}_8$
④	$\vec{\mathbf{i}}_3$	$\vec{\mathbf{i}}_4$	$\vec{\mathbf{i}}_7$
⑤	$\vec{\mathbf{i}}_4$	$\vec{\mathbf{i}}_5$	$\vec{\mathbf{i}}_9$
⑥	$\vec{\mathbf{i}}_5$	$\vec{\mathbf{i}}_6$	$\vec{\mathbf{i}}_8$

the possible transitions that could be found in Sector ②. It can be seen that the zero vector $\vec{\mathbf{i}}_9$ should be chosen to minimize the switching frequency. Table 15.6 gives a summary of the zero space vector to be used in each sector in order to minimize the switching frequency. However, should be noted that Table 15.6 is valid only for the sequence $\vec{\mathbf{i}}_i$, $\vec{\mathbf{i}}_{i+1}$, $\vec{\mathbf{i}}_z$. Another sequence will require reformulating the zero space-vector selection algorithm.

C. The Normalized Sampling Frequency

As in VSIs modulated by a SV approach, the normalized sampling frequency f_{sn} should be an integer multiple of 6 to minimize uncharacteristic harmonics. As an example, Fig. 15.35 shows the relevant waveforms of a CSI SVM for $f_{sn} = 18$ and $\hat{i}_c = 0.8$. Figure 15.35 also shows that the first set of relevant harmonics load line current are at f_{sn}.

15.4.5 DC Link Voltage in Three-phase CSIs

An instantaneous power balance indicates that

$$v_i(t) \cdot i_i(t) = v_{an}(t) \cdot i_{oa}(t) + v_{bn}(t) \cdot i_{ob}(t) + v_{cn}(t) \cdot i_{oc}(t) \tag{15.60}$$

where $v_{an}(t)$, $v_{bn}(t)$, and $v_{cn}(t)$ are the phase filter voltages as shown in Fig. 15.36. If the filter is large enough and a relatively high switching frequency is used, the phase voltages become nearly sinusoidal balanced waveforms. On the other hand, if the ac output currents are considered sinusoidal and the dc link current is assumed constant $i_i(t) = I_i$, Eq. (15.60) can be simplified to

$$v_i(t) = \frac{1}{I_i} \left\{ \begin{array}{l} \sqrt{2} V_{on} \sin(\omega t) \cdot \sqrt{2} I_{o1} \sin(\omega t - \phi) \\ + \sqrt{2} V_{on} \sin(\omega t - 120^\circ) \cdot \sqrt{2} I_{o1} \sin(\omega t - 120^\circ - \phi) \\ + \sqrt{2} V_{on} \sin(\omega t - 240^\circ) \cdot \sqrt{2} I_{o1} \sin(\omega t - 240^\circ - \phi) \end{array} \right\} \tag{15.61}$$

where V_{on} is the rms ac output phase voltage, I_{o1} is the rms fundamental line current, and ϕ is an arbitrary filter-load angle. Hence, the dc link voltage expression can be further simplified to the following:

$$v_i(t) = 3 \frac{I_{o1}}{I_i} V_{on} \cos(\phi) = \sqrt{3} \frac{I_{o1}}{I_i} V_o \cos(\phi) \tag{15.62}$$

where $V_o = \sqrt{3} V_{on}$ is the rms load line voltage. The resulting dc link voltage expression indicates that the first line-current harmonic I_{o1} generates a clean dc current. However, as the load line currents contain harmonics around the normalized sampling frequency f_{sn}, the dc link current will contain harmonics but around f_{sn} as shown in Fig. 15.35h. Similarly, in carrier-based PWM techniques, the dc link current will contain harmonics around the carrier frequency m_f (Fig. 15.27).

In practical implementations, a CSI requires a dc current source that should behave as a constant (as required by PWM CSIs) or variable (as square-wave CSIs) current source. Such current sources should be implemented as separate units and they are described earlier in this book.

15.5 Closed-loop Operation of Inverters

Inverters generate variable ac waveforms from a dc power supply to feed, for instance, ASDs. As the load conditions usually change, the ac waveforms should be adjusted to these new conditions. Also, as the dc power supplies are not ideal and the dc quantities are not fixed, the inverter should compensate for such variations. Such adjustments can be done automatically by means of a closed-loop approach. Inverters also provide an alternative to changing the load operating conditions (i.e. speed in an ASD).

There are two alternatives for closed-loop operation the feedback and the feedforward approaches. It is known that the feedback approach can compensate for both the perturbations (dc power variations) and the load variations (load torque changes). However, the feedforward strategy is more effective in mitigating perturbations as it prevents its negative effects at the load side. These cause-effect issues are analyzed in three-phase inverters in the following, although similar results are obtained for single-phase VSIs.

15.5.1 Feedforward Techniques in Voltage Source Inverters

The dc link bus voltage in VSIs is usually considered a constant voltage source v_i. Unfortunately, and due to the fact that most practical applications generate the dc bus voltage by means of a diode rectifier (Fig. 15.37), the dc bus voltage contains low-order harmonics such as the sixth, twelfth, ... (due to six-pulse

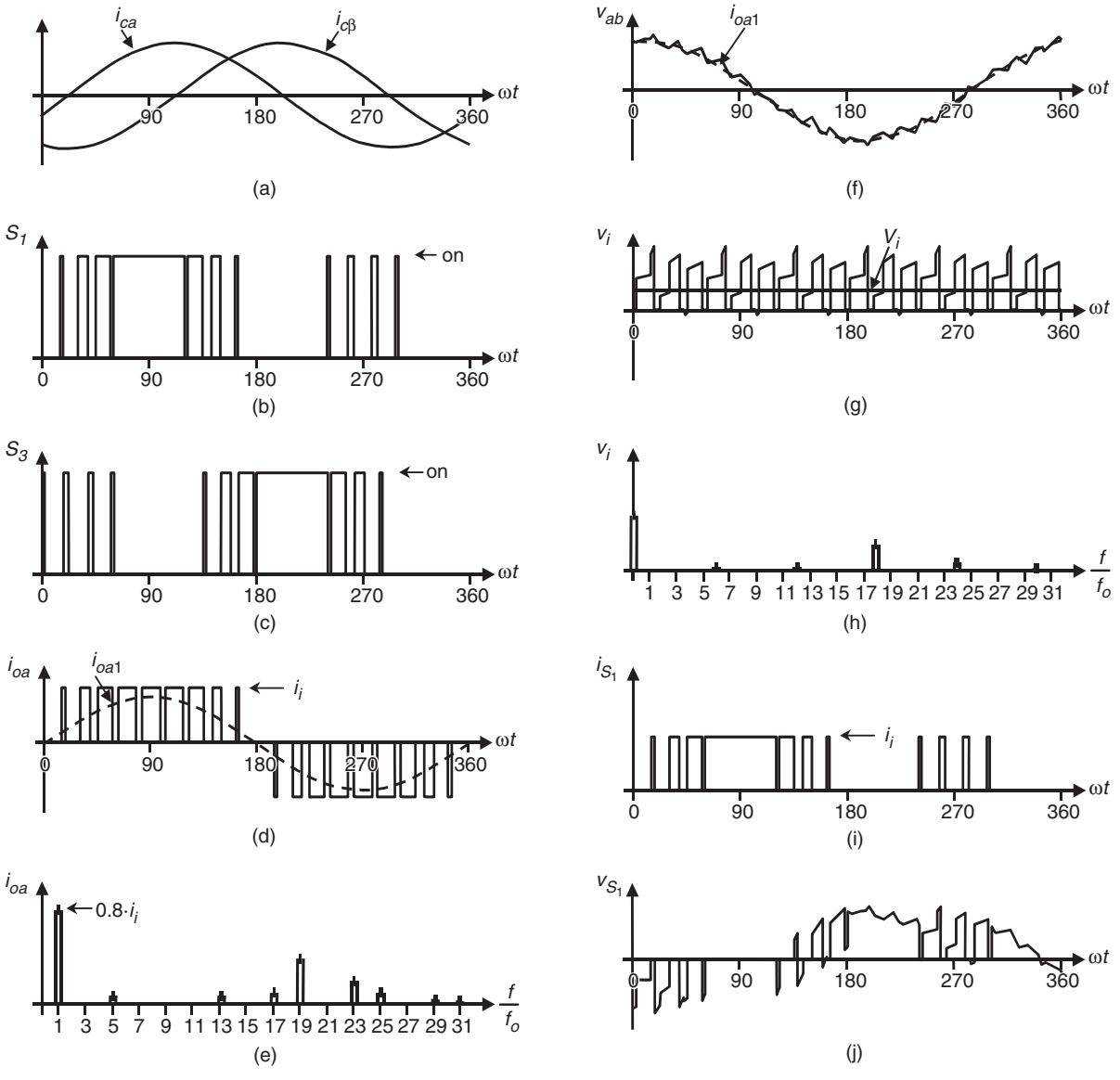

FIGURE 15.35 The three-phase CSI. Ideal waveforms for space-vector modulation ($\hat{i}_c = 0.8$, $f_{sn} = 18$): (a) modulating signals; (b) switch S_1 state; (c) switch S_3 state; (d) ac output current; (e) ac output current spectrum; (f) ac output voltage; (g) dc voltage; (h) dc voltage spectrum; (i) switch S_1 current; and (j) switch S_1 voltage.

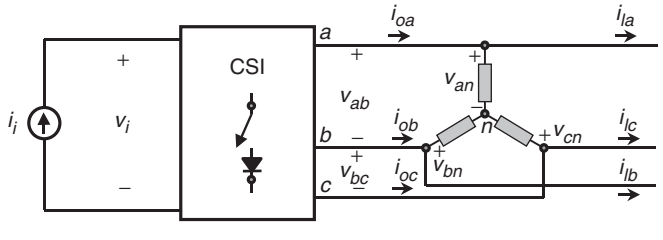

FIGURE 15.36 Phase-voltage definition in a wye-connected filter.

diode rectifiers), and the second if the ac voltage supply features an unbalance, which is usually the case. Additionally, if the three-phase load is unbalanced, as in UPS applications, the dc input current in the inverter i_i also contains the second harmonic, which in turn contributes to the generation of a second voltage harmonic in the dc bus.

The basic principle of feedforward approaches is to sense the perturbation and then modify the input in order to compensate for its effect. In this case, the dc link voltage should be sensed and the modulating technique should accordingly be modified. The fundamental *ab* line voltage in a VSI SPWM

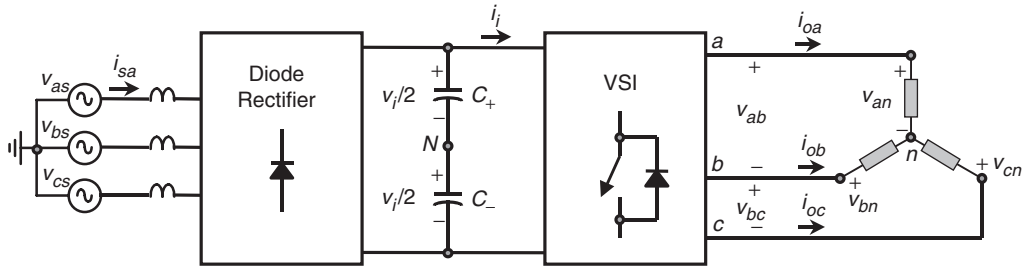

FIGURE 15.37 Three-phase VSI topology with a diode-based front-end rectifier.

can be written as

$$v_{ab1}(t) = \left\{ \frac{v_{ca1}(t)}{\hat{v}_\Delta} - \frac{v_{cb1}(t)}{\hat{v}_\Delta} \right\} \frac{\sqrt{3}}{2} v_i(t) \quad \hat{v}_\Delta > \hat{v}_{ca1}, \hat{v}_{cb1} \tag{15.63}$$

where $\hat{v}_\Delta$ is the carrier signal peak, $\hat{v}_{ca1}$ and $\hat{v}_{cb1}$ are the modulating signal peaks, and $v_{ca}(t)$ and $v_{ca}(t)$ are the modulating signals. If the dc bus voltage v_i varies around a nominal V_i value, then the fundamental line voltage varies proportionally; however, if the carrier signal peak $\hat{v}_\Delta$ is redefined as

$$\hat{v}_\Delta = \hat{v}_{\Delta m} \frac{v_i(t)}{V_i} \tag{15.64}$$

where $\hat{v}_{\Delta m}$ is the carrier signal peak (Fig. 15.38), then the resulting fundamental *ab* line voltage in a VSI SPWM is

$$v_{ab1}(t) = \left\{ \frac{v_{ca1}(t)}{\hat{v}_{\Delta m}} - \frac{v_{cb1}(t)}{\hat{v}_{\Delta m}} \right\} \frac{\sqrt{3}}{2} V_i \tag{15.65}$$

where, clearly, the result does not depend upon the variations of the dc bus voltage.

Figure 15.39 shows the waveforms generated by the SPWM under a severe dc bus voltage variation (a second harmonic has been added manually to a constant V_i). As a consequence, the ac line voltage generated by the VSI is distorted as it contains

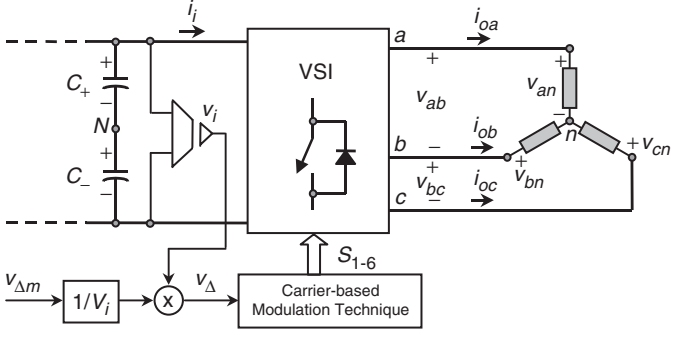

FIGURE 15.38 The three-phase VSI. Feedforward control technique to reject dc bus voltage variations.

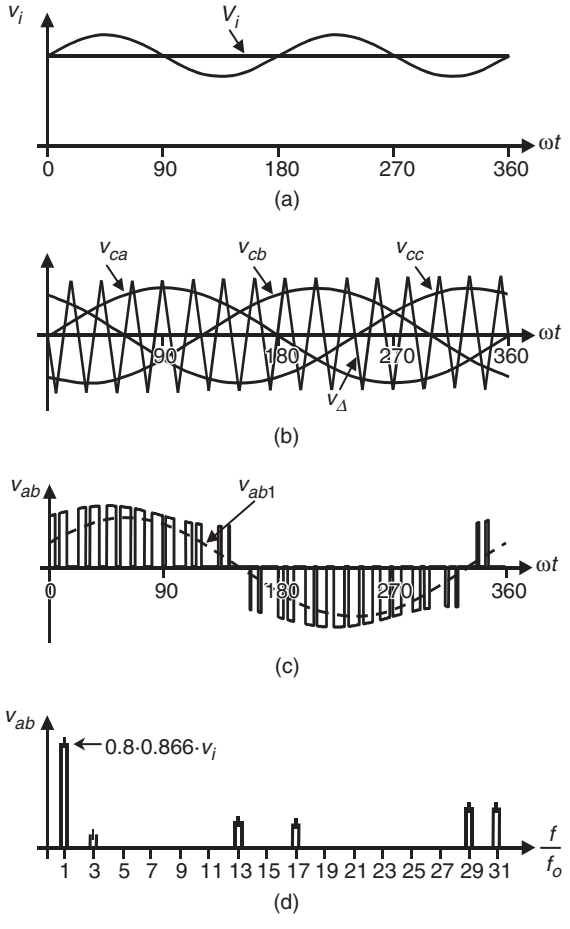

FIGURE 15.39 The three-phase VSI. Waveforms for regular SPWM ($m_a = 0.8$, $m_f = 9$): (a) dc bus voltage; (b) carrier and modulating signals; (c) ac output voltage; and (d) ac output voltage spectrum.

low-order harmonics (Fig. 15.39e). These operating conditions may not be acceptable in standard applications such as ASDs because the load will draw distorted three-phase currents as well. The feedforward loop performance is illustrated in Fig. 15.40. As expected, the carrier signal is modified so as to compensate for the dc bus voltage variation (Fig. 15.40b). This is probed by the spectrum of the ac line voltage that does not

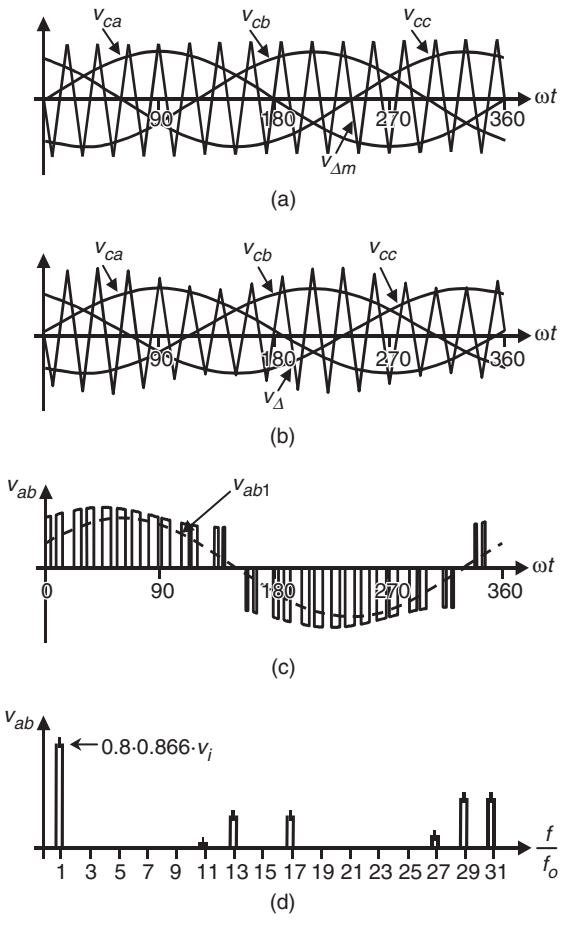

FIGURE 15.40 The three-phase VSI. Waveforms for SPWM including a feedforward loop ($m_a = 0.8$, $m_f = 9$): (a) carrier and modulating signals; (b) modified carrier and modulating signals; (c) ac output voltage; and (d) ac output voltage spectrum.

contain low-order harmonics (Fig. 15.40e). It should be noted that $\hat{v}_{\Delta} > \hat{v}_{ca1}, \hat{v}_{cb1}$; therefore, the compensation capabilities are limited by the required ac line voltage.

The performance of the feedforward approach depends upon the frequency of the harmonics present in the dc bus voltage and the carrier signal frequency. Fortunately, the relevant unwanted harmonics to be found in the dc bus voltage are the second, due to unbalanced supply voltages, and/or the sixth as the dc bus voltage is generated by means of a six-pulse diode rectifier. Therefore, a carrier signal featuring a 15-pu frequency is found to be sufficient to properly compensate for dc bus voltage variations.

Unbalanced loads generate a dc input current i_i that contains a second harmonic, which contributes to the dc bus voltage variation. The previous feedforward approach can compensate for such perturbation and maintain balanced ac load voltages.

Digital techniques can also be modified in order to compensate for dc bus voltage variations by means of a feedforward approach. For instance, the SVM techniques indicate that the on-times of the vectors $\vec{\mathbf{v}}_i$, $\vec{\mathbf{v}}_{i+1}$, and $\vec{\mathbf{v}}_z$ are

$$T_i = T_s \cdot \hat{v}_c \cdot \sin(\pi/3 - \theta) \tag{15.66}$$

$$T_{i+1} = T_s \cdot \hat{v}_c \cdot \sin(\theta) \tag{15.67}$$

$$T_z = T_s - T_i - T_{i+1} \tag{15.68}$$

respectively, where $\hat{v}_c$ is the amplitude of the desired ac line voltage, as shown in Fig. 15.18. By redefining this quantity to

$$0 \leq \hat{v}_c = \hat{v}_{cm} \frac{V_i}{v_i(t)} \leq 1 \tag{15.69}$$

where V_i is the nominal dc bus voltage and $v_i(t)$ is the actual dc bus voltage. Thus, the on-times become

$$T_i = T_s \cdot \hat{v}_{cm} \frac{V_i}{v_i(t)} \cdot \sin(\pi/3 - \theta) \tag{15.70}$$

$$T_{i+1} = T_s \cdot \hat{v}_{cm} \frac{V_i}{v_i(t)} \cdot \sin(\theta) \tag{15.71}$$

$$T_z = T_s - T_i - T_{i+1} \tag{15.72}$$

where $\hat{v}_{cm}$ is the desired maximum ac line voltage. The previous expressions account for dc bus voltage variations and behave as a feedforward loop as it needs to sense the perturbation in order to be implemented. The previous expressions are valid for the linear region, thus $\hat{v}_c$ is restricted to $0 \leq \hat{v}_c \leq 1$, which indicates that the compensation is indeed limited.

15.5.2 Feedforward Techniques in Current Source Inverters

The duality principle between the voltage and the current source inverters indicates that, as described previously, the feedforward approach can be used for CSIs as well as for VSIs. Therefore, low-order harmonics present in the dc bus current can be compensated for before they appear at the load side. This can be done for both analog-based (e.g. carrier-based) and digital-based (e.g. space-vector) modulating techniques.

15.5.3 Feedback Techniques in Voltage Source Inverters

Unlike the feedforward approach, the feedback techniques correct the input to the system (gating signals) depending upon the deviation of the output to the system (e.g. ac load line currents in VSIs). Another important difference is that feedback techniques need to sense the controlled variables. In general, the controlled variables (output to the system) are chosen according to the control objectives. For instance, in ASDs, it is usually necessary to keep the motor line currents equal to

a given set of sinusoidal references. Therefore, the controlled variables become the ac line currents. There are several alternatives to implement feedback techniques in VSIs, and three of them are discussed in the following.

A. Hysteresis Current Control

The main purpose here is to force the ac line current to follow a given reference. The status of the power valves S_1 and S_4 are changed whenever the actual i_{oa} current goes beyond a given reference $i_{oa,ref} \pm \Delta i/2$. Figure 15.41 shows the hysteresis current controller for phase *a*. Identical controllers are used in phase *b* and *c*. The implementation of this controller is simple as it requires an operational amplifier (op-amp) operating in the hysteresis mode, thus the controller and modulator are combined in one unit.

Unfortunately, there are several drawbacks associated with the technique itself. First, the switching frequency cannot be predicted as in carrier-based modulators and therefore the harmonic content of the ac line voltages and currents becomes random (Fig. 15.42d). This could be a disadvantage when designing the filtering components. Second, as three-phase loads do not have the neutral connected as in ASDs, the load currents add up to zero. This means that only two ac line currents can be controlled independently at any given instant. Therefore, one of the hysteresis controllers is redundant at a given time. This explains why the load current goes beyond the limits and introduces limit cycles (Fig. 15.42a). Finally, although the ac load currents add up to zero, the controllers cannot ensure that all load line currents feature a zero dc component in one load cycle.

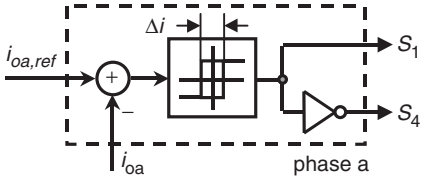

FIGURE 15.41 The three-phase VSI. Hysteresis current control (phase *a*).

B. Linear Control of VSIs

Proportional and proportional-integrative controllers can also be used in VSIs. The main purpose is to generate the modulating signals v_{ca}, v_{cb}, and v_{cc} in a closed-loop fashion as depicted in Fig. 15.43. The modulating signals can be used by a carrier-based technique such as the SPWM (as depicted in Fig. 15.43) or by space vector modulation. Because the load line currents add up to zero, the load line current references must add up to zero. Thus, the abc/αβγ transformation can be used to reduce to two controllers the overall implementation scheme as the γ component is always zero. This avoids limit cycles in the ac load currents.

The transformation of a set of variables in the stationary abc frame $\mathbf{x}^{abc}$ into a set of variables in the stationary αβ frame $\mathbf{x}^{\alpha\beta}$ is given by

$$\mathbf{x}^{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \mathbf{x}^{abc} \tag{15.73}$$

The selection of the controller (P, PI,...) is done according to the control procedures such as steady-state error, settling time, overshoot, and so forth. Figure 15.44 shows the relevant waveforms of a VSI SPWM controlled by means of a PI controller as shown in Fig. 15.43.

Although it is difficult to prove that no limit cycles are generated, the ac line current appears very much sinusoidal. Moreover, the ac line voltage generated by the VSI preserves the characteristics of such waveforms generated by SPWM modulators. This is confirmed by the harmonic spectrum

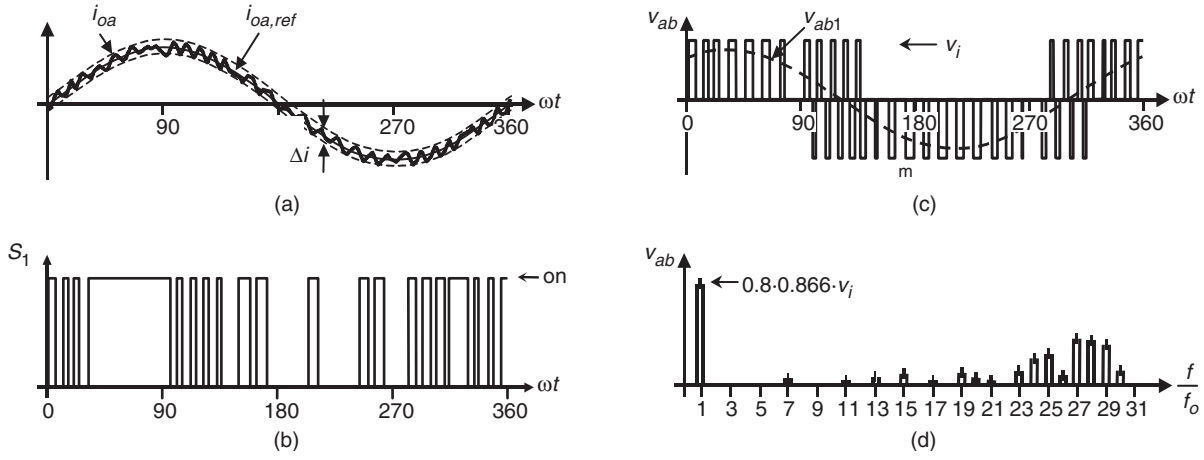

FIGURE 15.42 The three-phase VSI. Ideal waveforms for hysteresis current control: (a) actual ac load current and reference; (b) switch S_1 state; (c) ac output voltage; and (d) ac output voltage spectrum.

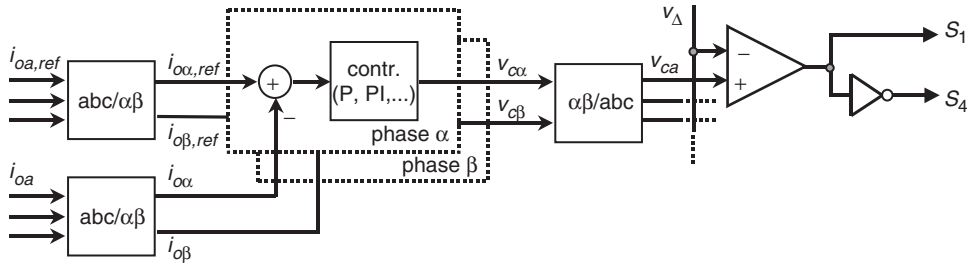

FIGURE 15.43 The three-phase VSI. Feedback control based on linear controllers.

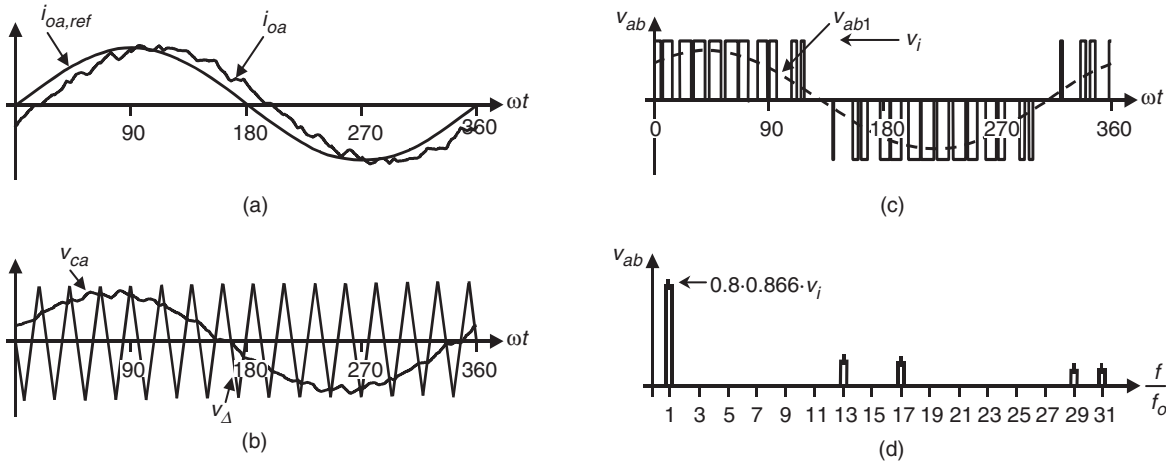

FIGURE 15.44 The three-phase VSI. Ideal waveforms for a PI controller in a feedback loop ($m_a = 0.8$, $m_f = 15$): (a) actual ac load current and reference; (b) carrier and modulating signals; (c) ac output voltage; and (d) ac output voltage spectrum.

shown in Fig. 15.44d, where the first set of characteristic harmonics are around the normalized carrier frequency $m_f = 15$.

However, an error between the actual i_{oa} and the ac line current reference $i_{oa,ref}$ can be observed (Fig. 15.44a). This error is inherent to linear controllers and cannot be totally eliminated, but it can be minimized by increasing the gain of the controller. However, the noise in the circuit is also increased, which could deteriorate the overall performance of the control scheme. The inherent presence of the error in this type of controllers is due to the fact that the controller needs a sinusoidal error to generate sinusoidal modulating signals v_{ca}, v_{cb}, and v_{cc}, as required by the modulator. Therefore, an error must exist between the actual and the ac line current references.

Nevertheless, as current-controlled VSIs are actually the inner loops in many control strategies, their inherent errors are compensated by the outer loop. This is the case of ASDs, where the outer speed loop compensates the inner current loops. In general, if the outer loop is implemented with dc quantities (such as speed), it can compensate the ac inner loops (such as ac line currents). If it is mandatory that a zero steady-state error be achieved with the ac quantities, then a stationary (abc frame) to rotating (dq frame) transformation is a valid alternative to use.

C. Linear Control of VSIs in a Rotating Frame

The rotating dq transformation allows ac three-phase circuits to be operated as if they were dc circuits. This is based upon a mathematical operation, that is the transformation of a set of variables in the stationary abc frame $\mathbf{x}^{abc}$ into a set of variables in the rotating dq0 frame $\mathbf{x}^{dq0}$. The transformation is given by

$$\mathbf{x}^{dq} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t - 4\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t - 4\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \mathbf{x}^{abc} \tag{15.74}$$

where ω is the angular frequency of the ac quantities. For instance, the current vector given by

$$\mathbf{i}^{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} I\sin(\omega t - \varphi) \\ I\sin(\omega t - 2\pi/3 - \varphi) \\ I\sin(\omega t - 4\pi/3 - \varphi) \end{bmatrix} \tag{15.75}$$

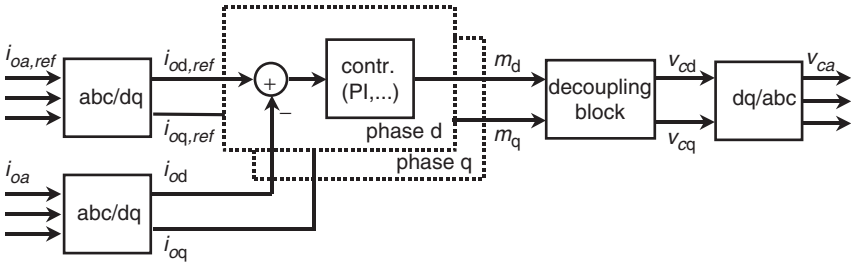

FIGURE 15.45 The three-phase VSI. Feedback control based on dq0 transformation.

becomes the vector

$$\mathbf{i}^{\mathrm{dq0}} = \begin{bmatrix} i_{\mathrm{d}} \\ i_{\mathrm{q}} \\ i_0 \end{bmatrix} = \begin{bmatrix} I\cos(\varphi) \\ -I\sin(\varphi) \\ 0 \end{bmatrix} \tag{15.76}$$

where I and φ are the amplitude and phase of the line currents, respectively. It can be observed that: (a) the zero component i_0 is always zero as the three-phase quantities add up to zero; and (b) the d and q components i_d, i_q are dc quantities. Thus, linear controllers should help to achieve zero steady-state error. The control strategy shown in Fig. 15.45 is an alternative where the zero-component controller has been eliminated due to fact that the line currents at the load side add up to zero.

The controllers in Fig. 15.45 include an integrator that generates the appropriate dc outputs m_d and m_q even if the actual and the line current references are identical. This ensures that the zero steady-state error is achieved. The decoupling block in Fig. 15.45 is used to eliminate the cross-coupling effect generated by the dq0 transformation and to allow an easier design of the parameters of the controllers.

The dq0 transformation requires the intensive use of multiplications and trigonometric functions. These operations can readily be done by means of digital microprocessors. Also, analog implementations would indeed be involved.

15.5.4 Feedback Techniques in Current Source Inverters

Duality indicates that CSIs should be controlled as equally as VSIs except that the voltages become currents and the currents become voltages. Thus, hystersis, linear and dq linear-based control strategies are also applicable to CSIs; however, the controlled variables are the load voltages instead of the load line currents.

For instance, the linear control of a CSI based on a dq transformation is depicted in Fig. 15.46. In this case, a passive balanced load is considered. In order to show that zero steady-state error is achieved, the per phase equations of the converter are written as

$$C\frac{d}{dt}\mathbf{v}_{\mathbf{p}}^{\mathrm{abc}} = \mathbf{i}_{\mathbf{o}}^{\mathrm{abc}} - \mathbf{i}_{\mathbf{l}}^{\mathrm{abc}} \tag{15.77}$$

$$L\frac{d}{dt}\mathbf{i}_{\mathbf{l}}^{\mathrm{abc}} = \mathbf{v}_{\mathbf{p}}^{\mathrm{abc}} - R\mathbf{i}_{\mathbf{l}}^{\mathrm{abc}} \tag{15.78}$$

the ac line currents are in fact imposed by the modulator and they satisfy

$$\mathbf{i}_{\mathbf{o}}^{\mathrm{abc}} = i_i\mathbf{i}_{\mathbf{c}}^{\mathrm{abc}} \tag{15.79}$$

Replacing Eq. (15.79) into the model of the converter Eqs. (15.77) and (15.78), using the dq0 transformation and assuming null zero component, the model of the converter becomes

$$\frac{d}{dt}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} = -\mathbf{W}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} + \frac{i_i}{C}\mathbf{i}_{\mathbf{c}}^{\mathrm{dq}} - \frac{1}{C}\mathbf{i}_{\mathbf{l}}^{\mathrm{dq}} \tag{15.80}$$

$$\frac{d}{dt}\mathbf{i}_{\mathbf{l}}^{\mathrm{dq}} = -\mathbf{W}\mathbf{i}_{\mathbf{l}}^{\mathrm{dq}} + \frac{1}{L}\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} - \frac{R}{L}\mathbf{i}_{\mathbf{l}}^{\mathrm{dq}} \tag{15.81}$$

where $\mathbf{W}$ is given by

$$\mathbf{W} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \tag{15.82}$$

A first approximation is to assume that the decoupling block is not there; in other words, $\mathbf{i}_{\mathbf{c}}^{\mathrm{dq}} = \mathbf{m}^{\mathrm{dq}}$. On the other hand, the model of the controllers can be written as

$$\mathbf{m}^{\mathrm{dq}} = k\left\{\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} - \mathbf{v}_{\mathbf{p}}^{\mathrm{dq}}\right\} + \frac{1}{T}\int_{-\infty}^{t}\left(\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} - \mathbf{v}_{\mathbf{p}}^{\mathrm{dq}}\right)dt \tag{15.83}$$

where k and T are the proportional and integrative gains of the PI controller that are chosen to achieve a desired dynamic response. Combining the model of the controllers and the model of the converter in dq coordinates and using

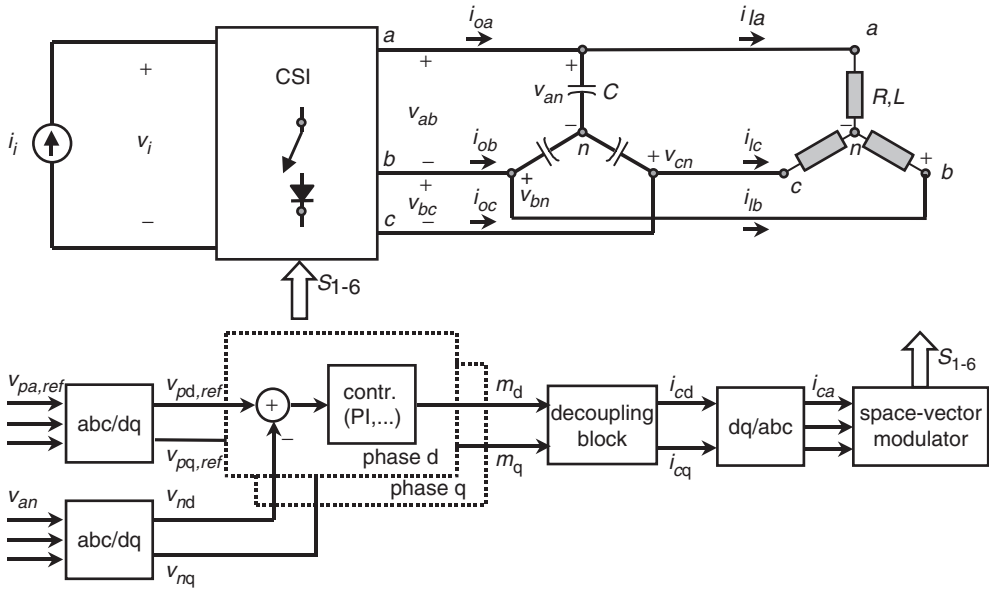

FIGURE 15.46 The three-phase CSI. Feedback control based on dq0 transformation.

the Laplace transform, the following relationship between the reference and actual load-phase voltages is found:

$$\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} = \frac{i_i}{C}\left\{sk + \frac{1}{T}\right\}\left\{s\mathbf{I} + \mathbf{W} + \frac{R}{L}\mathbf{I}\right\} \times \left[\left\{s\mathbf{I} + \mathbf{W} + \frac{R}{L}\mathbf{I}\right\}\left\{s^2\mathbf{I} + s\left(\mathbf{W} + \frac{i_i}{C}k\mathbf{I}\right) + \frac{i_i}{CT}\mathbf{I}\right\} + \frac{s}{LC}\mathbf{I}\right]^{-1}\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} \tag{15.84}$$

Finally, in order to prove that the zero steady-state error is achieved for step inputs in either the d or q component of the load-phase voltage reference, the previous expression is evaluated in $s = 0$. This results in the following:

$$\mathbf{v}_{\mathbf{p}}^{\mathrm{dq}} = \frac{i_i}{C}\left\{\frac{1}{T}\right\}\left\{\mathbf{W} + \frac{R}{L}\mathbf{I}\right\}\left[\left\{W + \frac{R}{L}\mathbf{I}\right\}\left\{\frac{i_i}{CT}\mathbf{I}\right\}\right]^{-1}\mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} = \mathbf{v}_{\mathbf{p,ref}}^{\mathrm{dq}} \tag{15.85}$$

As expected, the actual and reference values are identical. Finally, the relationship in Eq. (15.84) is a matrix that is not diagonal. This means that both the actual and the reference load-phase voltages are coupled. In order to obtain a decoupled control, the decoupling block in Fig. 15.46 should be properly chosen.

15.6 Regeneration in Inverters

Industrial applications are usually characterized by a power flow that goes from the ac distribution system to the load. This is, for example, the case of an ASD operating in the motoring mode. In this instance, the active power flows from the dc side to the ac side of the inverter. However, there are an important number of applications in which the load may supply power to the system. Moreover, this could be an occasional condition as well as a normal operating condition. This is known as the regenerative operating mode. For example, when an ASD reduces the speed of an electrical machine this can be considered a transient condition. Downhill belt conveyors in mining applications can be considered as a normal operating condition. In order to simplify the notation, it could be said that an inverter operates in the motoring mode when the power flows from the dc to the ac side, and in the regenerative mode when the power flows from the ac to the dc side.

15.6.1 Motoring Operating Mode in Three-phase VSIs

This is the case where the power flows from the dc side to the ac side of the inverter. Figure 15.47 shows a simplified scheme of an ASD where the motor has been modeled by three *RLe* branches, where the sources $\mathbf{e}^{\mathrm{abc}}$ are the back-emf. Because the ac line voltages applied by the inverter are imposed by the pulsewidth modulation technique being used, they can be adjusted according to specific requirements. In particular, Fig. 15.48 shows the relevant waveforms in steady state for the

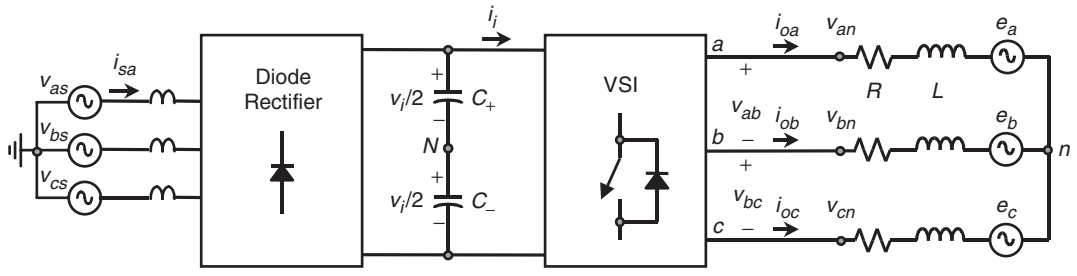

FIGURE 15.47 Three-phase VSI topology with a diode-based front-end rectifier.

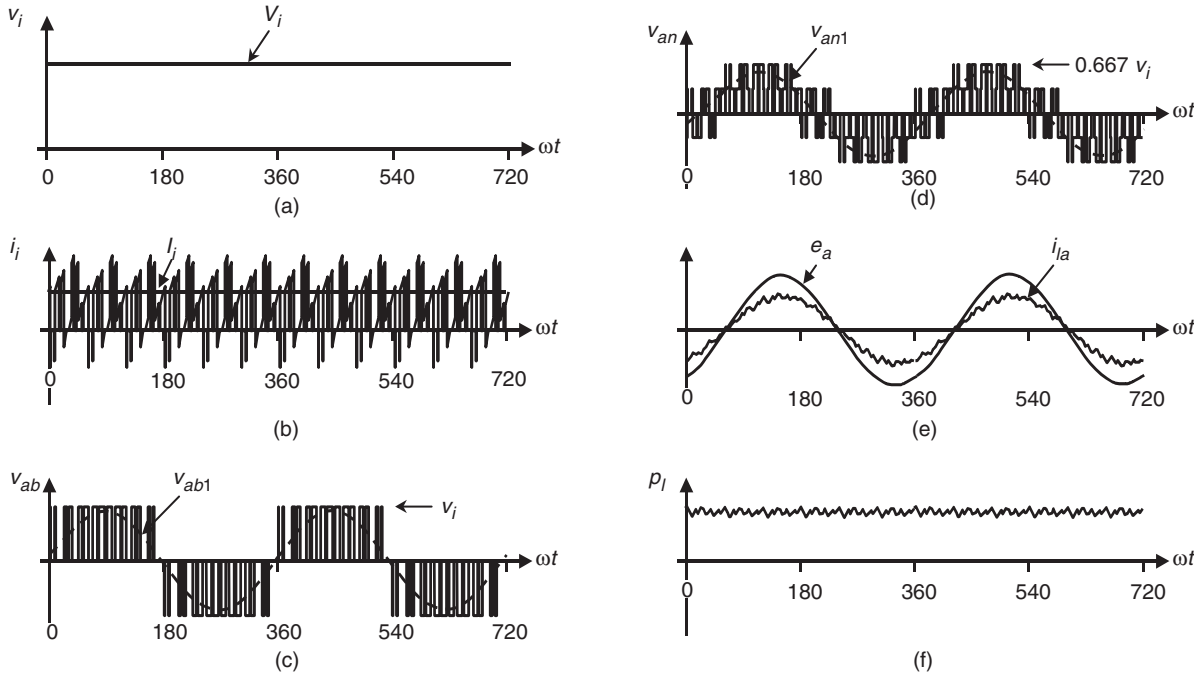

FIGURE 15.48 The ASD based on a VSI. Motoring mode: (a) dc bus voltage; (b) dc bus current; (c) ac line-load voltage; (d) ac phase-load voltage; (e) motor line current and back-emf; and (f) shaft power.

motoring operating mode of the ASD. To simplify the analysis, a constant dc bus voltage $v_i = V_i$ has been considered.

It can be observed that: (i) the dc bus current i_i features a dc value I_i that is positive; and (ii) the motor line current is in phase with the back-emf. Both features confirm that the active power flows from the dc source to the motor. This is also confirmed by the shaft power plot (Fig. 15.48f), which is obtained as:

$$p_l(t) = e_a(t)i_{la}(t) + e_b(t)i_{lb}(t) + e_c(t)i_{lc}(t) \qquad (15.86)$$

15.6.2 Regenerative Operating Mode in Three-phase VSIs

The back-emf sources $\mathbf{e}^{abc}$ are functions of the machine speed and as such they ideally change just as the speed changes. The regeneration operating mode can be achieved by properly modifying the ac line voltages applied to the machine. This is done by the speed outer loop that could be based on a scalar (e.g. V/f) or vectorial (e.g. field-oriented) control strategy. As indicated earlier, there are two cases of regenerative operating modes.

A. Occasional Regenerative Operating Mode

This mode is required during transient conditions such as in occasional braking of electrical machines (ASDs). Specifically, the speed needs to be reduced and the kinetic energy is taken into the dc bus. Because the motor line voltage is imposed by the VSI, the speed reduction should be done in such a way that the motor line currents do not exceed the maximum values. This boundary condition will limit the ramp-down speed to a minimum, but shorter braking times will require a mechanical braking system.

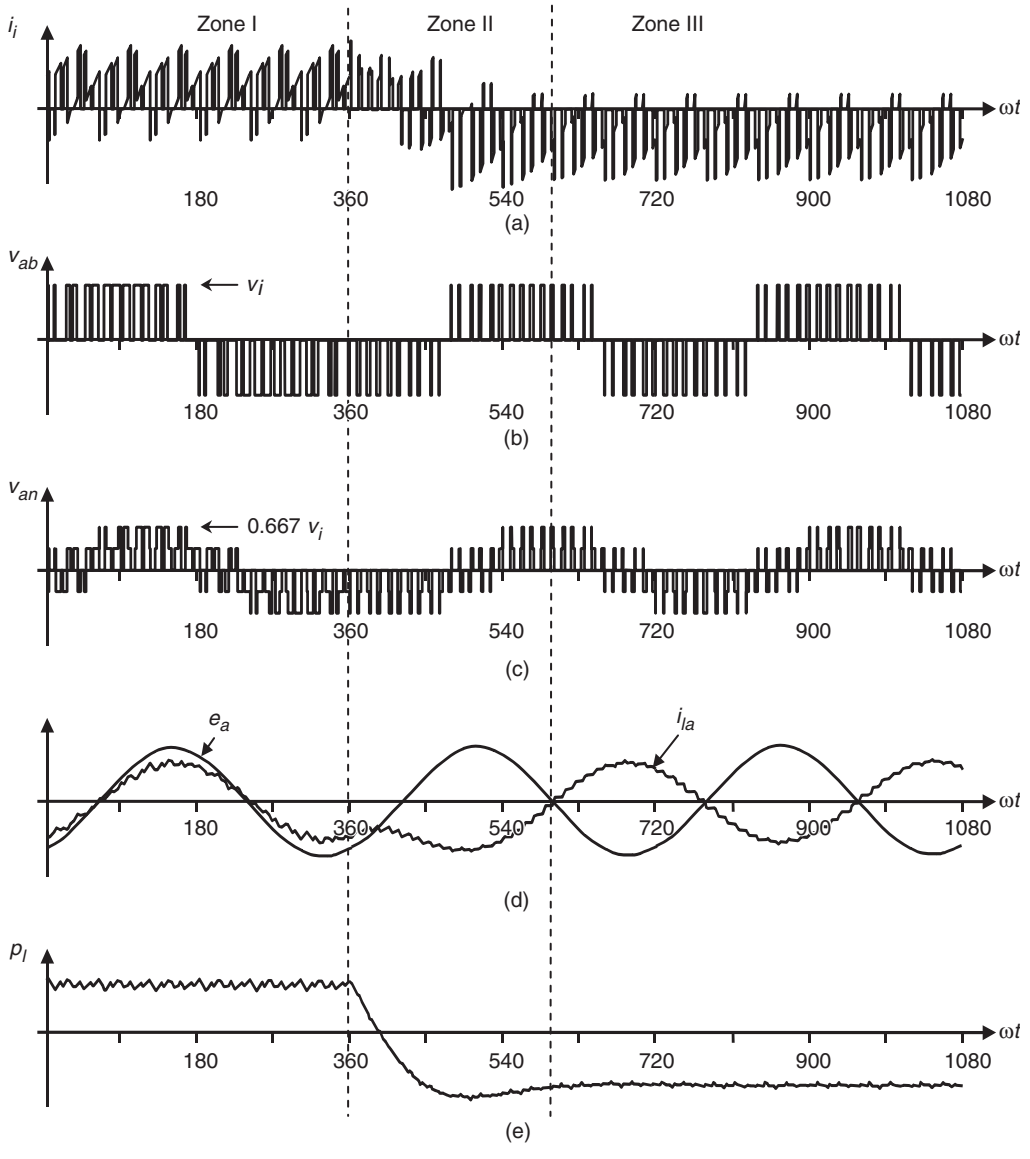

FIGURE 15.49 The ASD based on a VSI. Motoring to regenerative operating mode transition: (a) dc bus current; (b) ac line motor voltage; (c) ac phase motor voltage; (d) motor line current and back-emf; and (e) shaft power.

Figure 15.49 shows a transition from the motoring to regenerative operating mode for an ASD as shown in Fig. 15.47. Here, a stiff dc bus voltage has been used. Zone I in Fig. 15.49 is the motoring mode, Zone II is a transition condition, and Zone III is the regeneration mode. The line voltage is adjusted dynamically to obtain nominal motor line currents during regeneration (Fig. 15.49d). Zone III clearly shows that the shaft power gets reversed.

Occasional regeneration means that the drive rarely goes into this operating mode. Therefore, such energy can be: (a) left uncontrolled or (b) burned in resistors that are paralleled to the dc bus. The first option is used in low- to medium-power applications that use diode-based front-end rectifiers. Therefore, the dc bus current flows into the dc bus capacitor and the dc bus voltage rises accordingly to

$$\Delta v_i = \frac{1}{C} I_i \Delta t \tag{15.87}$$

where Δv_i is the dc bus voltage variation, C is the dc bus voltage capacitor, I_i is the average dc bus current during regeneration, and Δt is the duration of the regeneration operating mode. Usually, the drives have the capacitor C designed to allow a 10% overvoltage in the dc bus.

The second option uses burning resistors R_R that are paralleled in the dc bus as shown in Fig. 15.50 by means of the

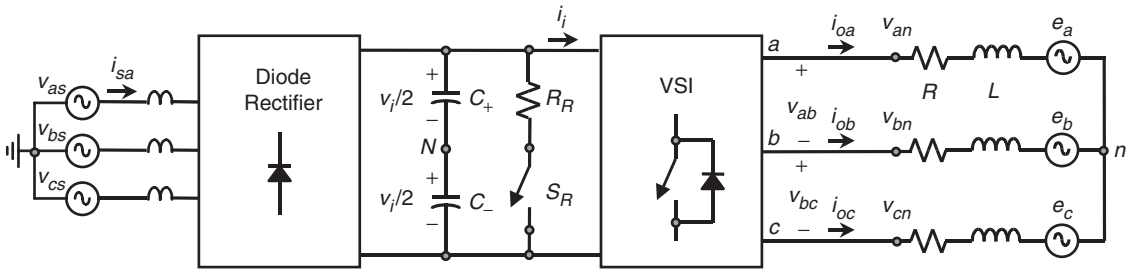

FIGURE 15.50 The ASD based on a VSI. Burning resistor strategy.

switch S_R. A closed-loop strategy based on the actual dc bus voltage modifies the duty cycle of the turn-on/turn-off of the switch S_R in order to keep such voltage under a given reference. This alternative is used when the energy recovered by the VSI would result in an acceptable dc bus voltage variation if an uncontrolled alternative is used.

There are some special cases where the regeneration operating mode is frequently used. For instance, electrical shovels in mining companies have repetitive working cycles and ≈15% of the energy is sent back into the dc bus. In this case, a valid alternative is to send back the energy into the ac distribution system.

The schematic shown in Fig. 15.51 is capable of taking the kinetic energy and sending it into the ac grid. As reviewed earlier, the regeneration operating mode reverses the polarity of the dc current i_i, and because the diode-based front-end converter cannot take negative currents, a thyristor-based front-end converter is added. Similarly to the burning-resistor approach, a closed-loop strategy based on the actual dc bus voltage v_i modifies the commutation angle α of the thyristor rectifier in order to keep such voltage under a given reference.

B. Regenerative Operating Mode as Normal operating Mode

Fewer industrial applications are capable of returning energy into the ac distribution system on a continuous basis. For instance, mining companies usually transport their product downhill for a few kilometers before processing it. In such cases, the drive maintains the transportation belt conveyor at constant speed and takes the kinetic energy. Due to the large amount of energy and the continuous operating mode, the drive should be capable of taking the kinetic energy, transforming it into electrical energy, and sending it into the ac distribution system. This would make the drive a generator that would compensate for the active power required by other loads connected to the electrical grid.

The schematic shown in Fig. 15.52 is a modern alternative for adding regeneration capabilities to the VSI-based drive on a continuous basis. In contrast to the previous alternatives, this scheme uses a VSI topology as an active front-end converter, which is generally called voltage-source rectifier (VSR). The VSR operates in two quadrants, that is, positive dc voltages and positive/negative dc currents as reviewed earlier. This feature makes it a perfect match for ASDs based on a VSI. Some of the advantages of using a VSR topology are: (i) the ac supply

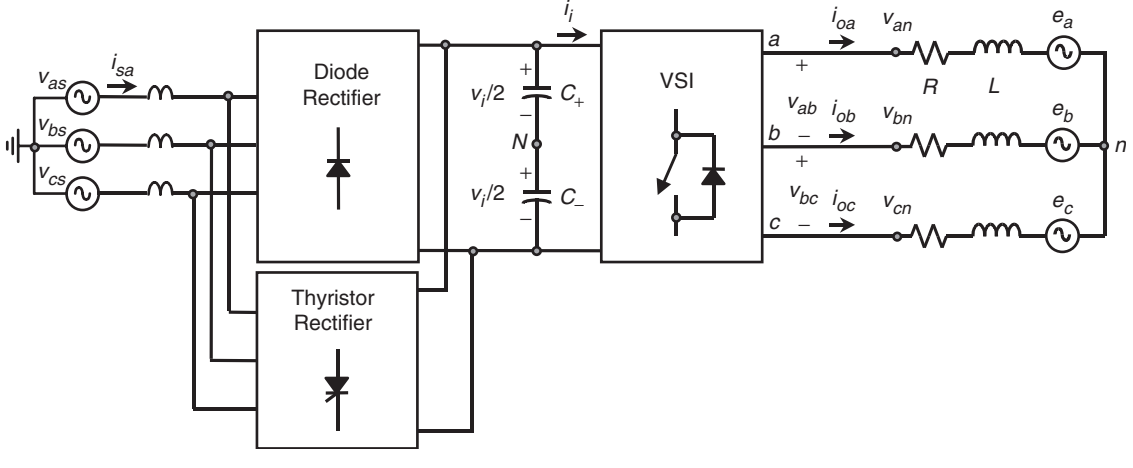

FIGURE 15.51 The ASD based on a VSI. Diode-thyristor-based front-end rectifier with regeneration capabilities.

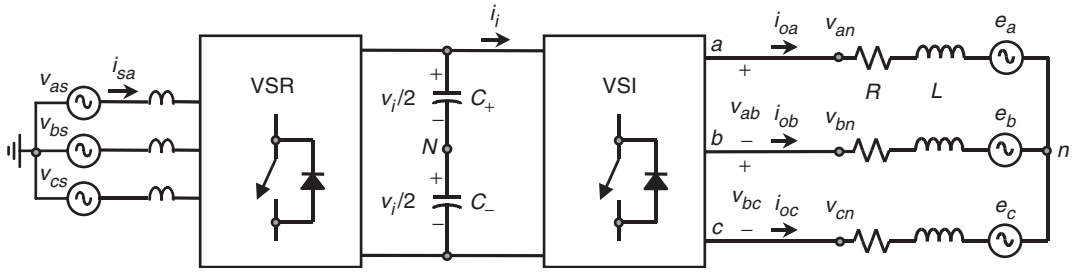

FIGURE 15.52 The ASD based on a VSI. Active front-end rectifier with regeneration capabilities.

current can be as sinusoidal as required (by increasing the switching frequency of the VSR or the ac line inductance); (ii) the operation can be done at a unity displacement power factor in both motoring and regenerative operating modes; and (iii) the control of the VSR is done in both motoring and regenerative operating modes by a single dc bus voltage loop.

15.6.3 Regenerative Operating Mode in Three-phase CSIs

There are drives where the motor side converter is a CSI. This is usually the case where near sinusoidal motor voltages are needed instead of the PWM type of waveform generated by VSIs. This is normally the case for medium-voltage applications. Such inverters require a dc current source that is constructed by means of a controlled rectifier.

Figure 15.53 shows a CSI-based ASD where the dc current source is generated by means of a thyristor-based rectifier in combination with a dc link inductor L_{dc}. In order to maintain a constant dc link current $i_i = I_i$, the thyristor-based rectifier adjusts the commutation angle α by means of a closed-loop control strategy. Assuming a constant dc link current, the regenerating operating mode is achieved when the dc link voltage v_i reverses its polarity. This can be done by modifying the PWM pattern applied to the CSI as in the VSI-based drive. To maintain the dc link current constant, the thyristor-based rectifier also reverses its dc link voltage v_r. Fortunately, the thyristor rectifier operates in two quadrant, that is, positive dc link currents and positive/ negative dc link voltages. Thus, no additional equipment is required to include regeneration capabilities in CSI-based drives.

Similarly, an active front-end rectifier could be used to improve the overall performance of the thyristor-based rectifier. A PWM current-source rectifier (CSR) could replace the thyristor-based rectifier with the following added advantages: (i) the ac supply current can be as sinusoidal as required (e.g. by increasing the switching frequency of the CSR); (ii) the operation can be done at a unity displacement power factor in both motoring and regenerative operating modes; and (iii) the control of the CSR is done in both motoring and regenerative operating modes by a single dc bus current loop.

15.7 Multistage Inverters

The most popular three-phase voltage source inverter (VSI) consists of a six-switch topology (Fig. 15.54a). The topology can generate a three-phase set of ac line voltages such that each line voltage v_{ab} (Fig. 15.54b) features a fundamental ac line voltage v_{ab1} and unwanted harmonics Fig. 15.54c. The fundamental ac line voltage is usually required as a sinusoidal waveform at variable amplitude and frequency, and the unwanted harmonics are located at high frequencies. These requirements are met by means of a modulating technique as shown earlier. Among the applications in low-voltage ranges of six-switch VSIs are the adjustable speed drives (ASDs). The range is in low voltages due to: (a) the high dv/dt present in the PWM ac line voltages (Fig. 15.54b), which will be unacceptable

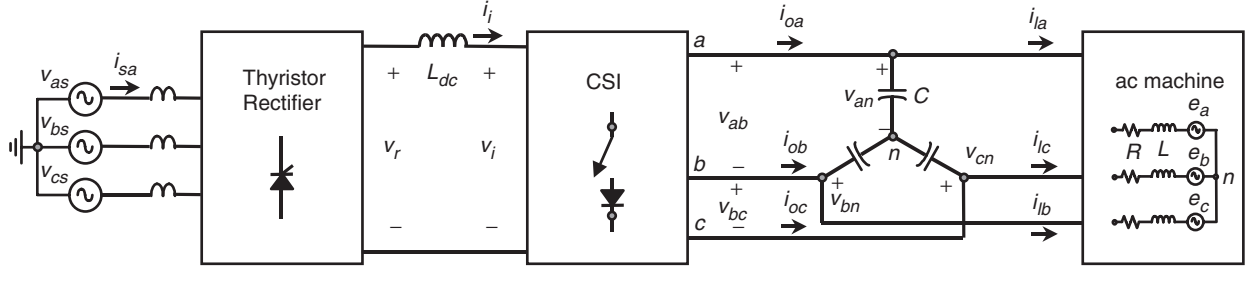

FIGURE 15.53 The ASD based on a CSI. Thyristor-based rectifier.

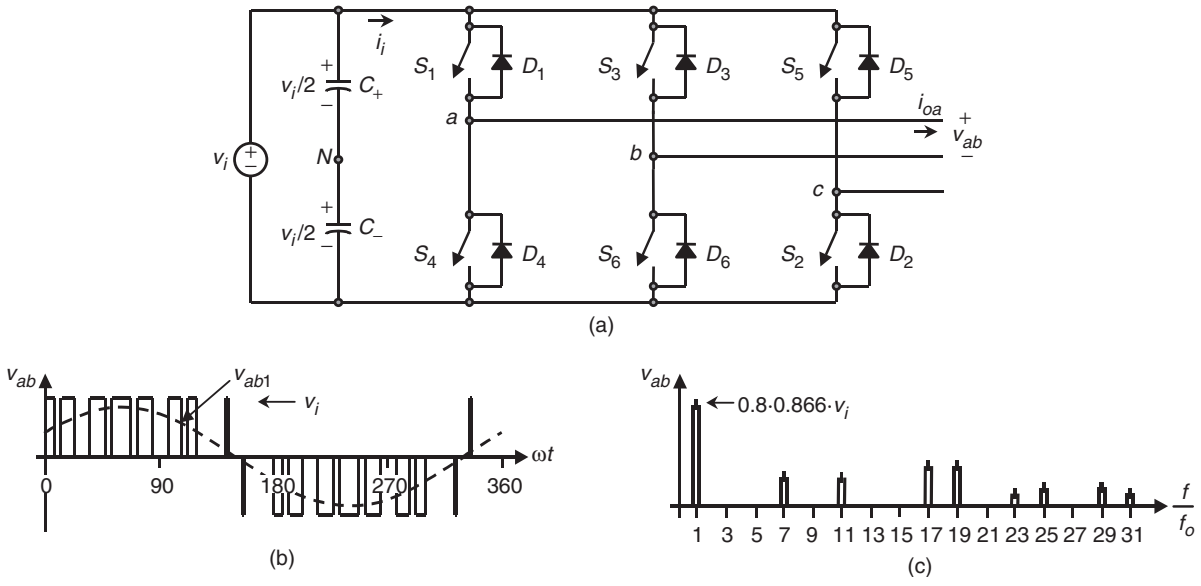

FIGURE 15.54 Six-switch voltage source inverter ($m_f = 9$, $m_a = 0.8$): (a) power topology; (b) ac output voltage; and (c) ac output voltage spectrum.

in the medium- to high-voltage ranges and (b) the load power would be shared only among six switches. This may require paralleling and series-connected power valves, an option usually avoided as symmetrical sharing of the power is not natural in these arrangements.

Two solutions are available to generate near-sinusoidal voltage waveforms while using six-switch topologies. The first is a topology based on a CSI in combination with a capacitive filter. The second solution is a topology based on a VSI including an inductive or inductive/capacitive filter at the load terminals. Although both alternatives generate near-sinusoidal voltage waveforms, both continue sharing the load power only among six power valves.

Solutions based on multistage voltage source topologies have been proposed. They provide medium voltages at the ac terminals while keeping low dv/dts and a large number of power valves that symmetrically share the total load power. The multistage VSIs can be classified in multicell and multilevel topologies.

15.7.1 Multicell Topologies

The goal is to develop a new structure with improved performance based on standard structures that are known as cells. For instance, Fig. 15.55a shows a cell featuring a three-phase input and a single-phase output. The front-end converter is a six-diode-based rectifier, and a single-phase VSI generates a single-phase ac voltage v_o. Figure 15.55b and c shows characteristic waveforms where a sinusoidal unipolar PWM ($m_f = 6$, $m_a = 0.8$) has been used to modulate the inverter.

Standard cells are meant to be used at low voltages, thus they can use standard components that are less expensive and widely available. The new structure should generate near-sinusoidal ac load voltages, draw near-sinusoidal ac line currents, and more importantly the load voltages should feature moderate dv/dts.

Figure 15.56 shows a multicell converter that generates a three-phase output voltage out of a three-phase ac distribution system. The structure uses three standard cells (as shown in Fig. 15.55) connected in series to form one phase; thus the phase-load voltages are the sum of the single-phase voltages generated by each cell. For instance, the phase voltage a is given by

$$v_{an} = v_{o\mathbf{11}} + v_{o\mathbf{21}} + v_{o\mathbf{31}} \tag{15.88}$$

In order to maximize the load-phase voltages, the ac voltages generated by the cells should feature identical fundamental components. On the other hand, each cell generates a PWM voltage waveform at the ac side, which contains unwanted voltage harmonics. If a carrier-based modulating technique is used, the harmonics generated by each cell are at well-defined frequencies (Fig. 15.55c). Some of these harmonics are not present in the phase-load voltage if the carrier signals of each cell are properly phase shifted.

In fact, Fig. 15.57 shows the voltages generated by cells c_{11}, c_{21}, and c_{31}, which are $v_{o\mathbf{11}}$, $v_{o\mathbf{21}}$, and $v_{o\mathbf{31}}$, respectively, and form the load-phase voltage a. They are generated using the unipolar SPWM approach, that is, one modulating signal v_{ca} and three carrier signals $v_{\Delta\mathbf{1}}$, $v_{\Delta\mathbf{2}}$, and $v_{\Delta\mathbf{3}}$ that are used by cells c_{11}, c_{21}, and c_{31}, respectively (Fig. 15.57a). The carrier signals have a normalized frequency m_f, which ensures an m_f switching frequency in each power valve and the lowest unwanted set of harmonics $\approx 2 \cdot m_f$ (m_f even) in the ac cell

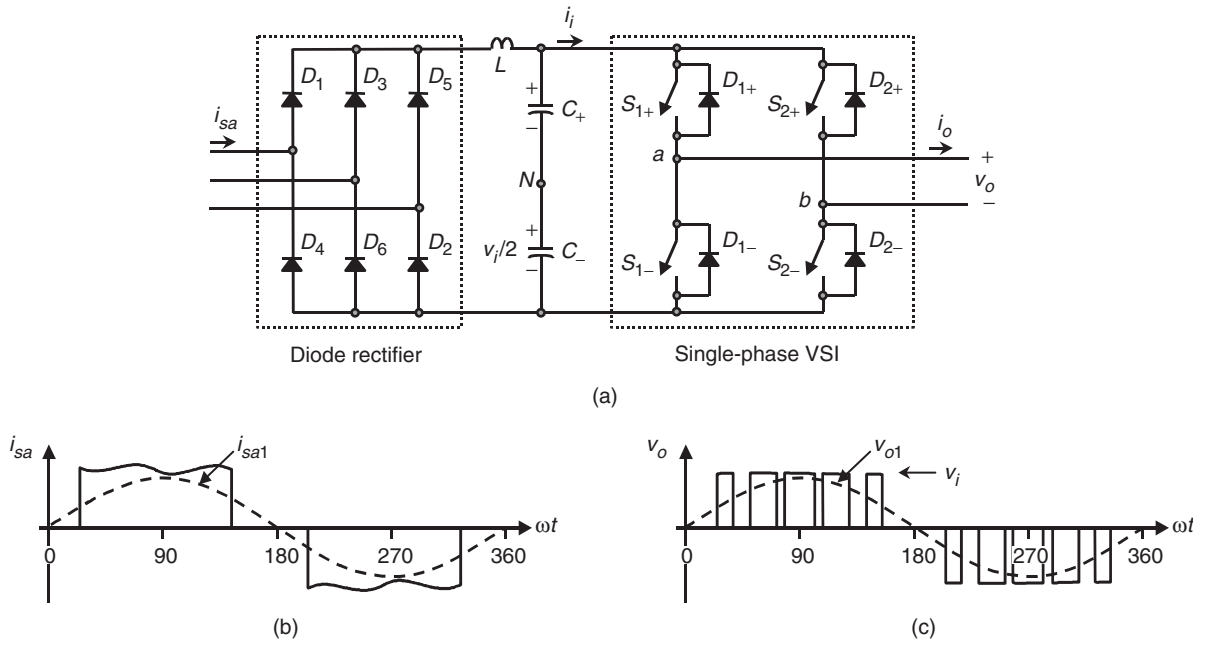

FIGURE 15.55 Three-phase-input single-phase output cell: (a) power topology; (b) ac input current, phase *a*; and (c) ac output voltage ($m_f = 6$, $m_a = 0.8$).

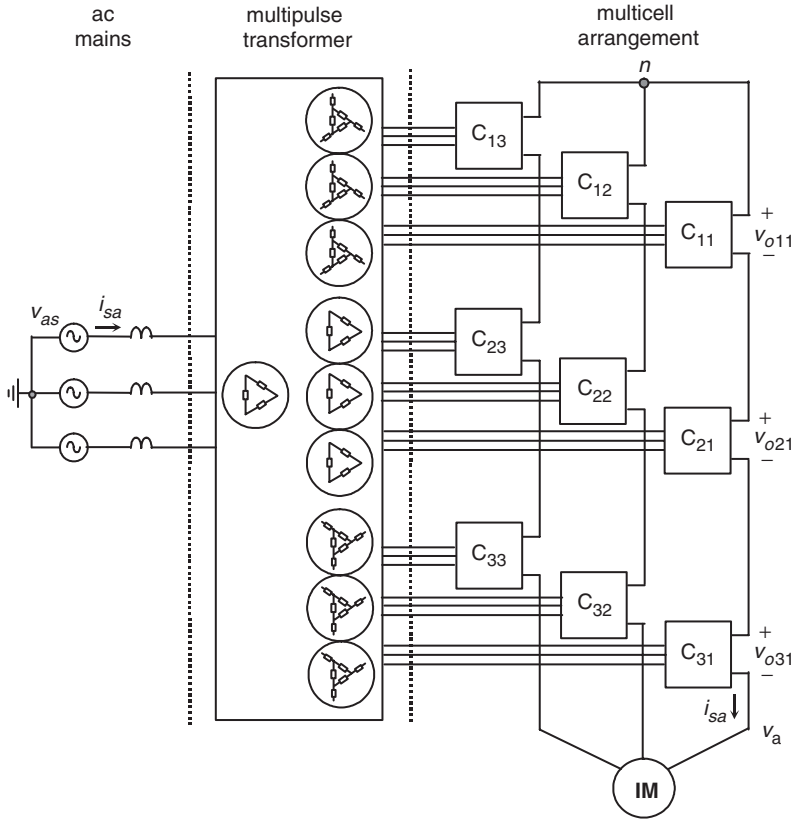

FIGURE 15.56 Multistage converter based on a multicell arrangement.

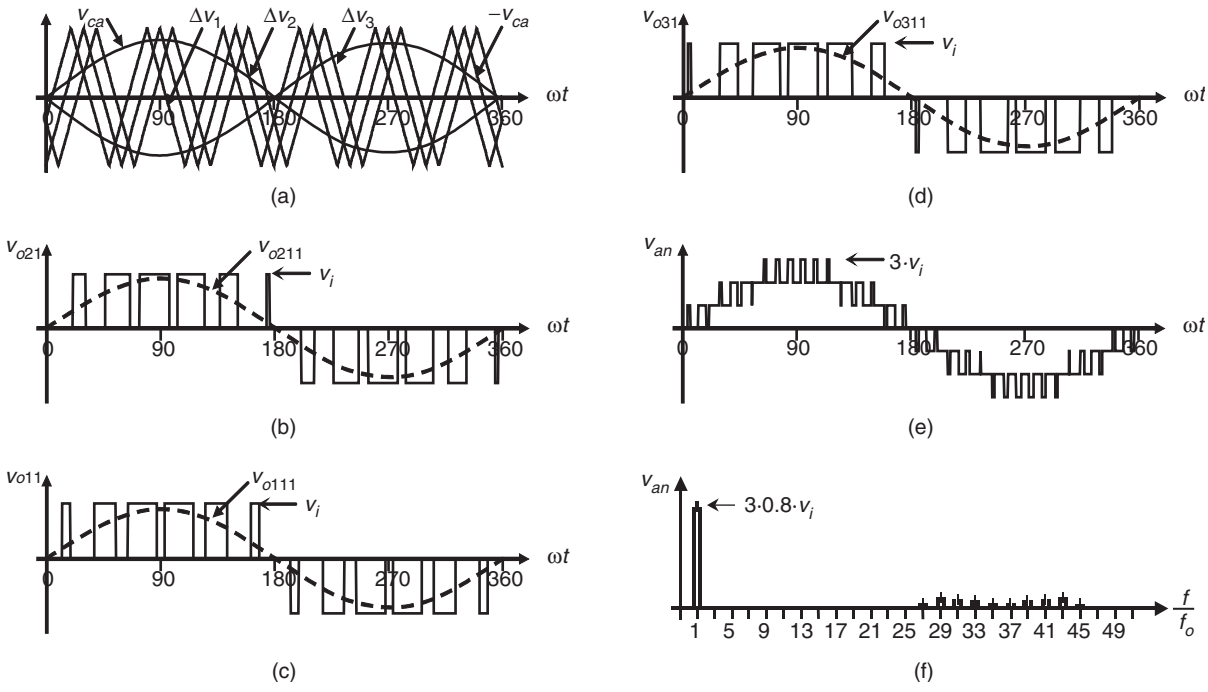

FIGURE 15.57 Multicell topology. Cell voltages in phase *a* using a unipolar SPWM ($m_f = 6$, $m_a = 0.8$): (a) modulating and carrier signals; (b) cell c_{11} ac output voltage; (c) cell c_{21} ac output voltage; (d) cell c_{31} ac output voltage; (e) phase *a* load voltage; and (f) phase *a* load-voltage spectrum.

voltages v_{o11}, v_{o21}, and v_{o31}. More importantly, the carrier signals are $\psi = 60°$ out-of-phase, which ensures the lowest unwanted set of voltage harmonics $\approx 6 \cdot m_f$ in the load-phase voltage v_{an}, that is, the lowest set of harmonics in Fig. 15.57f is $6 \cdot m_f = 6 \cdot 6 = 36$.

This can be explained as follows. The voltage harmonics present in the PWM voltage of each cell are at $l \cdot m_f \pm k$, $l = 2, 4, \ldots$ (where $k = 1, 3, 5, \ldots$); for instance, for $m_f = 6$, the first set of harmonics is at 12 ± 1, 12 ± 3, … in all cells. Because the cells in one phase use carrier signals that are 60° out-of-phase, all the voltage harmonics $\approx l \cdot m_f$ in all cells are $l \cdot 60°$ out-of-phase. Therefore, for $l = 2$, the cell c_{11} generates the harmonics $l \cdot m_f \pm k = 2 \cdot m_f \pm k$ at a given phase φ, the cell c_{21} generates the harmonics $2 \cdot m_f \pm k$ at a phase $\varphi + l \cdot 60° = \varphi + 2 \cdot 60° = \varphi + 120° = \varphi - 240°$, and the cell c_{21} generates the harmonics $2 \cdot m_f \pm k$ at a phase $\varphi - l \cdot 60° = \varphi - 2 \cdot 60° = \varphi - 120° = \varphi + 240°$; thus, if the voltages have identical amplitudes, the harmonics $\approx 2 \cdot m_f$ add up to zero. Similarly, for $l = 4$, the cell c_{11} generates the harmonics $l \cdot m_f \pm k = 4 \cdot m_f \pm k$ at a given phase φ, the cell c_{21} generates the harmonics $4 \cdot m_f \pm k$ at a phase $\varphi + l \cdot 60° = \varphi + 4 \cdot 60° = \varphi + 240° = \varphi - 120°$, and the cell c_{21} generates the harmonics $4 \cdot m_f \pm k$ at a phase $\varphi - l \cdot 60° = \varphi - 4 \cdot 60° = \varphi - 240° = \varphi + 120°$; thus, if the voltages have identical amplitudes, the harmonics $\approx 4 \cdot m_f$ add up to zero. However, for $l = 6$, the cell c_{11} generates the harmonics $l \cdot m_f \pm k = 6 \cdot m_f \pm k$ at a given phase φ, the cell c_{21} generates the harmonics $6 \cdot m_f \pm k$ at a phase $\varphi + l \cdot 60° = \varphi + 6 \cdot 60° = \varphi + 360° = \varphi$, and the cell c_{21} generates the harmonics $6 \cdot m_f \pm k$ at a phase $\varphi - l \cdot 60° = \varphi - 6 \cdot 60° = \varphi - 360° = \varphi$; thus, if the voltages have identical amplitudes, the harmonics $\approx 6 \cdot m_f$ become triplicated rather than cancelled out.

In general, due to the fact that $n_c = 3$, cells are connected in series in each phase, n_c carriers are required, which should be $\psi = 180°/n_c$ out-of-phase. The number of cells per phase n_c depends on the required phase voltage. For instance, a 600 V dc cell generates an ac voltage of $\approx 600/\sqrt{2} = 424$ V. Then three cells connected in series generate a phase voltage of $3 \cdot 424 = 1.27$ kV, which in turn generates a $1.27 \cdot \sqrt{3} = 2.2$ kV line-to-line voltage.

Phases *b* and *c* are generated similarly to phase *a*. However, the modulating signals v_{cb} and v_{cc} should be 120° out-of-phase. In order to use identical carrier signals in phases *b* and *c*, the carrier-normalized frequency m_f should be a multiple of 3. Thus, three modulating signals and n_c carrier signals are required to generate three phase voltages by means of a multicell approach, where n_c depends upon the required load line voltage and the dc bus voltage of each cell.

The ac supply current of each cell is a six-pulse type of current as shown in Fig. 15.58, which feature harmonics at $6 \cdot k \pm 1$ ($k = 1, 2, \ldots$). Similarly to the load side, the ac supply currents of each cell are combined so as to achieve high-performance overall supply currents. Because the front-end converter of

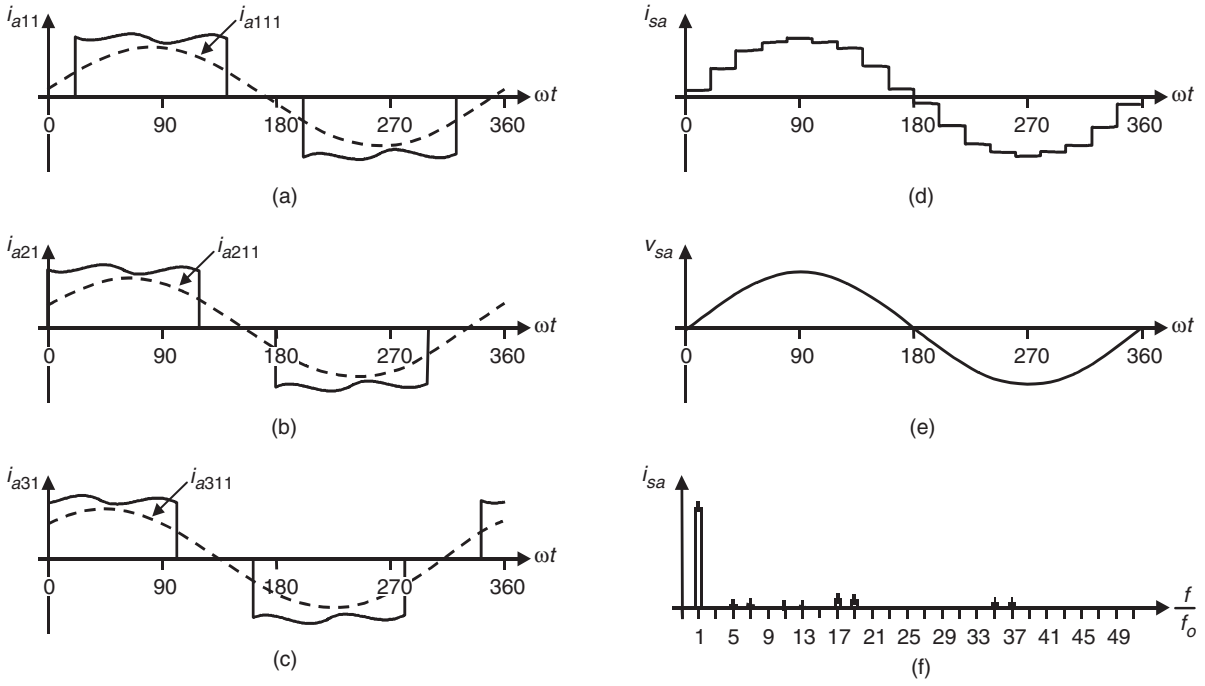

FIGURE 15.58 Multicell topology. Ac input current, phase *a*: (a) cell c_{11}; (b) cell c_{21}; (c) cell c_{31}; (d) overall supply current; (e) supply phase voltage; and (f) overall supply current spectrum.

each cell is a six-pulse diode rectifier, a multipulse approach is used. This is based on the natural harmonic cancellation when, for instance, a wye to delta/wye transformer is used to form an $N = 12$-pulse configuration from two six-pulse diode rectifiers. In this case, the fifth and seventh harmonics are cancelled out because the supply voltages applied to each six-pulse rectifier become 30° out-of-phase. In general, to form an $N = 6 \cdot n_s$ pulse configuration, n_s set of supply voltages that should be $60°/n_s$ out-of-phase is required. This would ensure the first set of unwanted current harmonics at $6 \cdot n_s \pm 1$.

The configuration depicted in Fig. 15.56 contains $n_c = 9$ cells, and a transformer capable of providing $n_s = 9$ sets of three-phase voltages that should be $60°/n_s = 60°/9$ out-of-phase to form an $N = 6 \cdot n_s = 6 \cdot 9 = 54$-pulse configuration is required. Although this alternative would provide a near-sinusoidal overall supply current, a fewer number of pulses are also acceptable that would reduce the transformer complexity. An $N = 18$-pulse configuration usually satisfies all the requirements. In the example, this configuration can be achieved by means of a transformer with $n_c = 9$ isolated secondaries; however, only $n_s = 3$ set of three-phase voltages that are $60°/n_s = 60°/3 = 20°$ out-of-phase are generated (Fig. 15.56). The configuration of the transformer restricts the connection of the cells in groups of three as shown in Fig. 15.56. In this case, the fifth, seventh, eleventh, and thirteenth harmonics are cancelled out and thus the first set of harmonics in the supply currents are the seventeenth and the nineteenth. Figure 15.58d shows the resulting supply current that is near-sinusoidal and Fig. 15.58f shows the corresponding spectrum. The fifth, seventh, eleventh, and thirteenth harmonics are still there, which is due to the fact that the ac input currents in each cell are not exactly the six-pulse type of waveforms as seen in Fig. 15.58a, b, and c. This is mainly because: (i) the dc link in the cells contains a small inductor L, which does not smooth out sufficiently the dc bus current (Fig. 15.55a) and (ii) the transformer leakage inductance (or added line inductance) smoothes out the edges of the current, which also contributes to the reactive power required by the cells. This last effect is not shown in Fig. 15.58a, b, and c.

15.7.2 Voltage Source-based Multilevel Topologies

The six-switch VSI is usually called a two-level VSI due to the fact that the inverter phase voltages v_{aN}, v_{bN}, and v_{cN} (Fig. 15.54a) are instantaneously either $v_i/2$ or $-v_i/2$. In other words, the phase voltages can take one of the two voltage levels. Multilevel topologies provide an alternative to these voltages to take one value out of N levels. For instance, Fig. 15.59 shows an $N = 3$-level topology, where the values of the inverter phase voltage are either $v_i/2$, 0, or $-v_i/2$ (Fig. 15.60d). An interesting problem is how to obtain the gating pattern for the 12 switches required in an $N = 3$-level topology. There are several modulating techniques to overcome this problem,

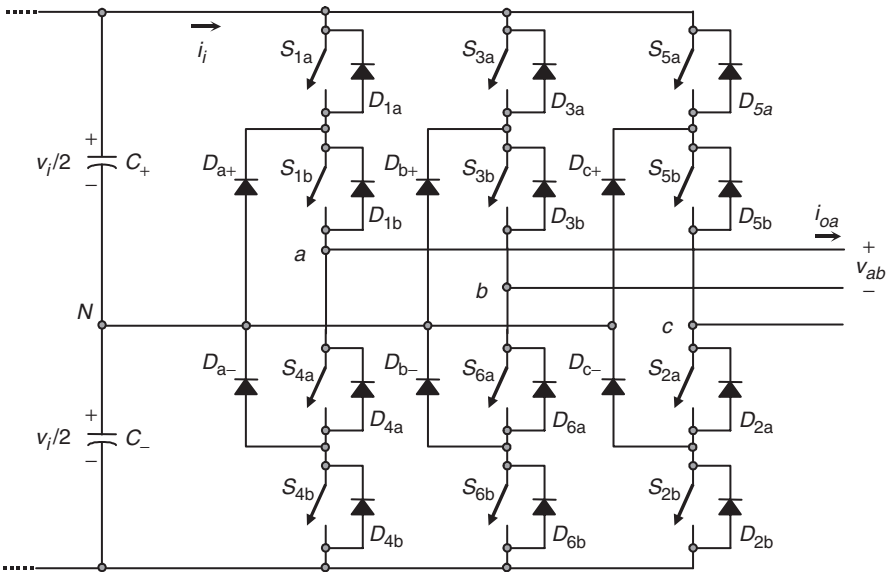

FIGURE 15.59 Three-phase three-level VSI topology.

which can be classified as analog (e.g. carrier-based) and digital (SV-based). Both approaches have to deal with the valid switch states of the inverter.

A. Valid Switch States in a Three-level VSI

The easiest way of obtaining the valid switch states is to analyze each phase separately. Phase a contains the switches S_{1a}, S_{1b}, S_{4a}, and S_{4b}, which cannot be on simultaneously because a short circuit across the dc bus would be produced, and cannot be off simultaneously because an undefined phase voltage v_{aN} would be produced. A summary of the valid switch combinations is given in Table 15.7. It is important to note that all valid switch combinations satisfy the condition that switch S_{1a} state is always the opposite to switch S_{4a} state, and that switch S_{1b} state is always the opposite to switch S_{4b} state. Any other switch-state combination would result in an undefined inverter phase a voltage because it will depend upon the load-phase current i_{oa} polarity. The switch states for phases b and c are identical to that of phase a; moreover, because they are paralleled, they can operate in an independent manner.

TABLE 15.7 Valid switch states for a three-level VSI, phase a

s_{1a}	s_{1b}	s_{4a}	s_{4b}	v_o	Components conducting	
1	1	0	0	$v_i/2$	S_{1a}, S_{1b}	if $i_{oa} > 0$
					D_{1a}, D_{1b}	if $i_{oa} < 0$
0	1	1	0	0	S_{1b}, D_{a+}	if $i_{oa} > 0$
					S_{4a}, D_{a-}	if $i_{oa} < 0$
0	0	1	1	$-v_i/2$	D_{4a}, D_{4b}	if $i_{oa} > 0$
					S_{4a}, S_{4b}	if $i_{oa} < 0$

B. The SPWM Technique in Three-level VSIs

The main objective is to generate the appropriate 12 gating signals so as to obtain fundamental inverter phase voltages equal to a given set of modulating signals. Specifically, the SPWM in three-level inverters uses a sinusoidal set of modulating signals (v_{ca}, v_{cb}, and v_{cc} for phases a, b, and c, respectively) and $N - 1 = 2$ triangular type of carrier signals ($v_{\Delta 1}$ and $v_{\Delta 2}$) as illustrated in Fig. 15.60a. The best results are obtained if the carrier signals are in-phase and feature an odd normalized frequency (e.g. $m_f = 15$). According to Fig. 15.60a, switch S_{1a} is either turned on if $v_{ca} > v_{\Delta 1}$ or off if $v_{ca} < v_{\Delta 1}$, and switch S_{1b} is either turned on if $v_{ca} > v_{\Delta 2}$ or off if $v_{ca} < v_{\Delta 2}$. Additionally, the switch S_{4a} status is obtained as the opposite to switch S_{1a}, and the switch S_{4b} status is obtained as the opposite to switch S_{1b}. In order to use the same set of carrier signals to generate the gating signals for phases b and c, the normalized frequency of the carrier signal m_f should be a multiple of 3. Thus, the possible values are $m_f = 3, 9, 15, 21, \ldots$.

Figure 15.60 shows the relevant waveforms for a three-level inverter modulated by means of a SPWM technique ($m_f = 15$, $m_a = 0.8$). Specifically, Fig. 15.60d shows the inverter phase voltage, which is clearly a three-level type of voltage, and Fig. 15.60f shows the load line voltage, which shows that the step voltages are at most $v_i/2$. More importantly, the inverter phase voltage (Fig. 15.60e) contains harmonics at $l \cdot m_f \pm k$ with $l = 1, 3, \ldots$ and $k = 0, 2, 4, \ldots$ and at $l \cdot m_f \pm k$ with $l = 2, 4, \ldots$ and $k = 1, 3, \ldots$ For instance, the first set of harmonics ($l = 1$, $m_f = 15$) are at 15, 15 ± 2, $15 \pm 4, \ldots$

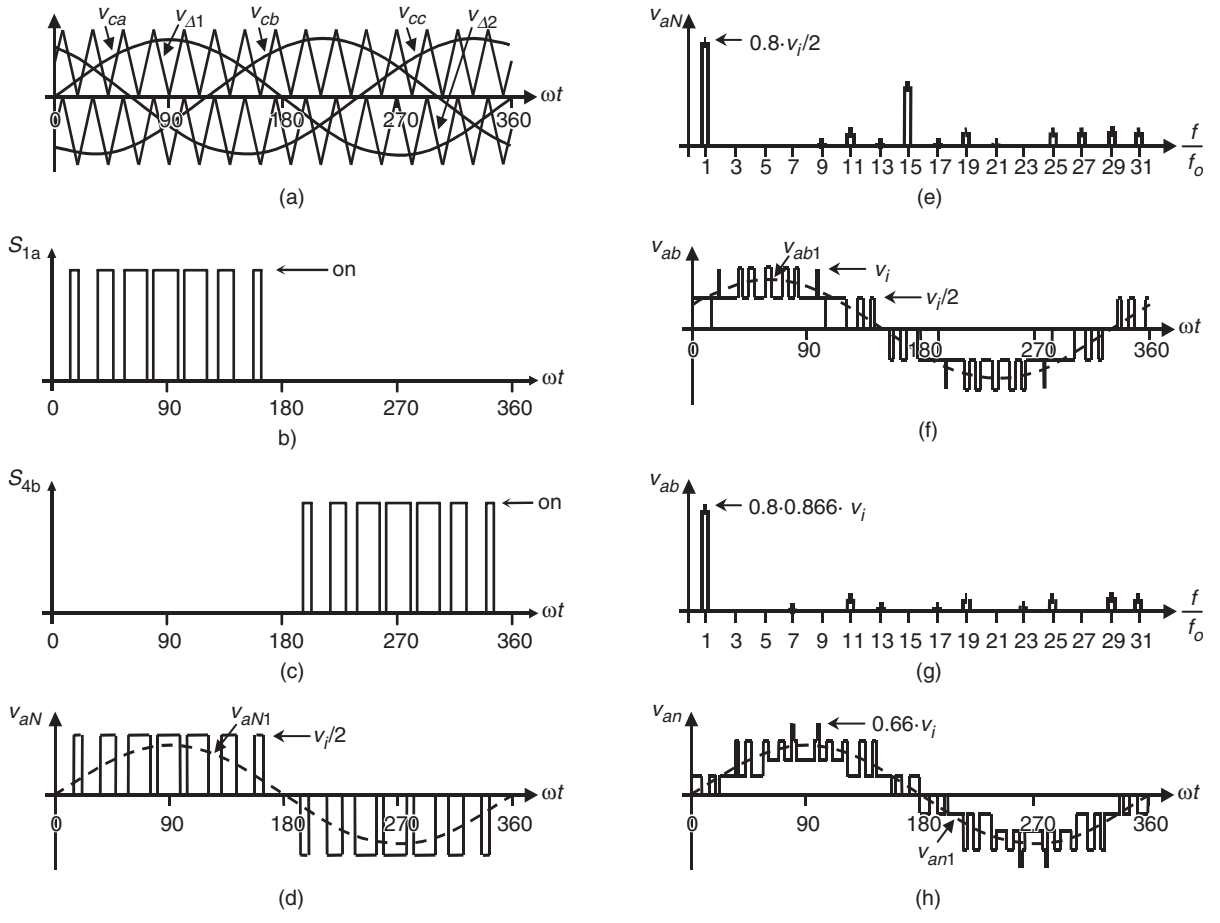

FIGURE 15.60 Three-level VSI topology. Relevant waveforms using a SPWM ($m_f = 15$, $m_a = 0.8$): (a) modulating and carrier signals; (b) switch S_{1a} status; (c) switch S_{4b} status; (d) inverter phase a voltage; (e) inverter phase a voltage spectrum; (f) load line voltage; (g) load line voltage spectrum; and (h) load phase a voltage.

The inverter line voltage (Fig. 15.60g) contains harmonics at $l \cdot m_f \pm k$ with $l = 1, 3, \ldots$ and $k = 2, 4, \ldots$ and at $l \cdot m_f \pm k$ with $l = 2, 4, \ldots$ and $k = 1, 3, \ldots$ For instance, the first set of harmonics in the line voltages ($l = 1$, $m_f = 15$) are at 15 ± 2, $15 \pm 4, \ldots$.

All the other features of carrier-based PWM techniques also apply in multilevel inverters. For instance, (I) the fundamental component of the inverter phase voltages satisfies

$$\hat{v}_{aN1} = \hat{v}_{bN1} = \hat{v}_{cN1} = m_a \frac{v_i}{2} \quad 0 < m_a \leq 1 \tag{15.89}$$

and thus the line voltages satisfy

$$\hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} = m_a \sqrt{3} \frac{v_i}{2} \quad 0 < m_a \leq 1 \tag{15.90}$$

where $0 < m_a \leq 1$ the linear operating region. To further increase the amplitude of the load voltages, the overmodulation operating region can be used by further increasing the modulating signal amplitudes ($m_a > 1$), where the line voltages range in

$$\sqrt{3} \frac{v_i}{2} < \hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} < \frac{4}{\pi} \sqrt{3} \frac{v_i}{2} \tag{15.91}$$

Also, (II) the modulating signals could be improved by adding a third harmonic (zero sequence), which will increase the linear region up to $m_a = 1.15$. This results in a maximum fundamental line-voltage component equal to v_i; (III) a nonsinusoidal set of modulating signals could also be used by the modulating technique. This is the case where nonsinusoidal line voltages are required as in active filter applications; and (IV) because of the two quadrants operation of VSIs, the multilevel inverter could equally be used in applications where the active power flow goes from the dc to the ac side or from the ac to the dc side.

In general, for an N-level inverter modulated by means of a carrier-based technique, the following conclusions can be drawn:

(a) three modulating signals 120° out of phase and $N-1$ carrier signals are required;
(b) the phase voltages in the inverters have a peak value of $v_i/(N-1)$;
(c) the phase voltages in the inverters are discrete waveforms constructed from the values

$$\frac{v_i}{2}, \frac{v_i}{2} - \frac{v_i}{N-1}, \frac{v_i}{2} - \frac{2 \cdot v_i}{N-1}, \cdots, -\frac{v_i}{2} \qquad (15.92)$$

(d) the maximum voltage step in the line voltages is

$$\frac{v_i}{N-1} \qquad (15.93)$$

for instance, an $N = 5$-level inverter requires four carrier signals, the discrete values of the phase voltages are: $v_i/2$, $v_i/4$, 0, $-v_i/4$, and $-v_i/2$, and the maximum step voltage at the load side is $v_i/4$. Key waveforms are shown in Fig. 15.61.

One of the drawbacks of the multilevel inverter is that the dc link capacitors should be equal. Unfortunately, this is not a natural operating condition mainly due to the fact that the currents required by the inverter in the dc bus are not symmetrical and therefore the capacitors will not equally share the total dc supply voltage v_i. To overcome this problem, two alternatives are developed later on.

C. The Space-vector Modulation in Three-level VSIs

Digital techniques are naturally extended to multilevel inverters. In fact, the SV modulating technique can be applied using the same principles used in two-level inverters. However, the higher number of voltage levels increases the complexity of the practical implementation of the technique. For instance, in $N = 3$-level inverters, each leg allows $N = 3$ different switch combinations as indicated in Table 15.7. Therefore, there are $N^3 = 27$ total valid switch combinations, which generate $N^3 = 27$ load line voltages that are represented by $N^3 = 27$ space vectors ($\vec{\mathbf{v}}_1, \vec{\mathbf{v}}_2, \ldots, \vec{\mathbf{v}}_{27}$) in Fig. 15.62. For instance, $\vec{\mathbf{v}}_2 = 0.5 + j0.866$ is due to the line voltages $v_{ab} = 0.5$, $v_{bc} = 0.5$, $v_{ca} = -1.0$ in pu. Thus, although the principle of operation is the same, the SV digital algorithm will have to deal with a higher number of states N^3. Moreover, because some space vectors (e.g. $\vec{\mathbf{v}}_{13}$ and $\vec{\mathbf{v}}_{14}$ in Fig. 15.62) produce the same load-voltage terminals, the algorithm will have to decide between the two based on additional criteria and that of the basic SV-approach. Clearly, as the number of level increases, the algorithm becomes more and more elaborate. However, the benefits are not evident as the number of level increases. The maximum number of levels used in practical applications is five. This is based on a compromise between the complexity of the implementation and the benefits of the resulting waveforms.

D. DC Link Voltage Balancing Issues

Figure 15.59 shows a three-level inverter and the ideal waveforms are shown in Fig. 15.60, which assume an even distribution of the voltage across the dc link capacitors. This even distribution is not naturally achieved and could be overcome by supplying both capacitors from independent supplies or properly gating the power valves of the inverter in order to minimize the unbalance.

Figure 15.63 shows an ASD based on a three-level VSI, where the dc link capacitors are feed from two different sources. This approach is being commercially used as it ensures a robust balanced dc link voltage distribution and operates with a high-performance type of ac mains current.

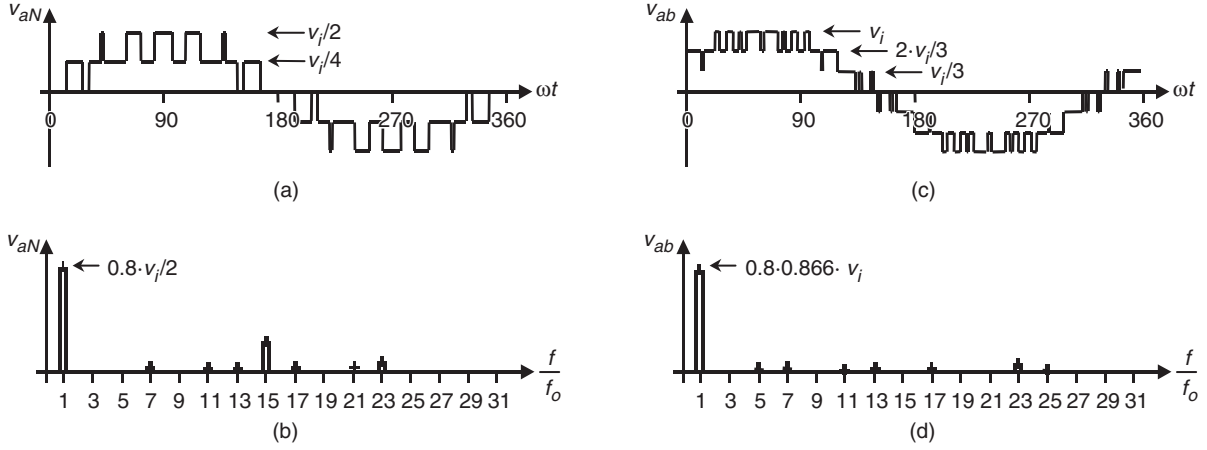

FIGURE 15.61 Five-level VSI topology. Relevant waveforms using a SPWM ($m_f = 15$, $m_a = 0.8$): (a) inverter phase *a* voltage; (b) inverter phase *a* voltage spectrum; (c) load line voltage; and (d) load line voltage spectrum.

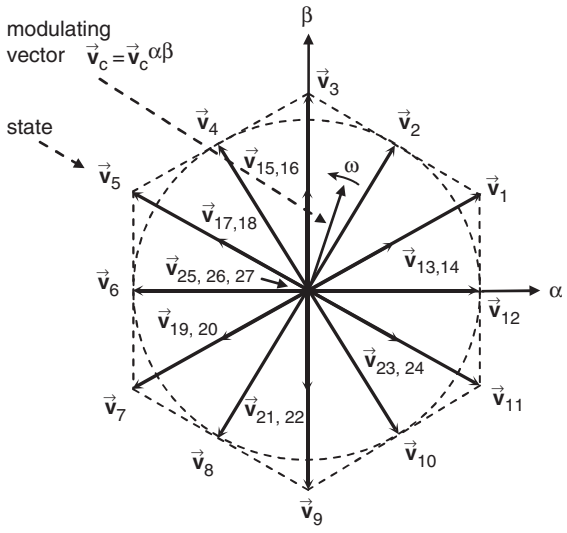

FIGURE 15.62 The space-vector representation in a three-level VSI.

Indeed, for a N level inverter, $N-1$ independent dc voltage supplies are required that could be provided by $N-1$ six-pulse rectifiers feed from an $N-1$ -pulse transformer. Therefore, the ac main currents is a $N-1$ level type of waveform.

This approach cannot be used when the inverter does not feature dc link voltage supplies. This is the case of static power reactive power compensators and static power active filters. In this case, the proper gating of the power valves becomes the only choice to keep and balance the dc link voltages. Figure 15.64a shows this case where the current added by the inverter i_o^{abc} provides the reactive power and current harmonics such that the ac mains current i_s^{abc} features a given power factor.

The SPWM modulating technique could be used as in Fig. 15.60; however, the zero level of the carriers δ is left as a manipulable variable Fig. 15.64b. In fact, it is used to control the difference of the upper and lower capacitor voltages $\Delta v_i = v_{i1} - v_{i2}$. A closed loop alternative is depicted in Fig. 15.64c to manipulate δ. The modulating signals $\mathbf{v_c^{abc}}$ are left to control the reactive power and current harmonics injected into the ac mains by regulating the currents $\mathbf{i_o^{abc}}$ and keep the total dc link voltage $v_i = v_{i1} + v_{i2}$ equal to a reference. Both loops are not included in Fig. 15.64c.

15.7.3 Current Source-based Multilevel Topologies

Duality is found in many aspects related to voltage and current source inverters. Perhaps, the most evident is the duality in terms of modulating techniques. Thus, current source based multilevel topologies are available as well. As expected, all the benefits and all the drawbacks found in voltage source topologies should be found in current source topologies.

Figure 15.65 shows a three-level $N = 3$ current source topology, which is formed by paralleling two standard six-switches topologies. The main goal is to share evenly the ac current $\mathbf{i_o^{abc}}$ among the two topologies ($\mathbf{i_o^{abc}}/2 = \mathbf{i_{o1}^{abc}} = \mathbf{i_{o2}^{abc}}$). This should be ensured by having equal dc link currents ($i_{i1} = i_{i2}$). Similarly to voltages source based mutlilevel topologies, this could be achieved by using either two independent dc link currents or by properly gating the power valves. Both alternatives are reviewed later on.

A. The SPWM Technique in Three-level CSIs

As in three-level VSIs, the main objective is to generate the appropriate 12 gating signals so as to obtain fundamental inverter line currents equal to a given set of modulating signals. Specifically, the SPWM in three-level inverters uses a sinusoidal set of modulating signals (i_{ca}, i_{cb}, and i_{cc} for phases a, b, and c, respectively) and $N-1=2$ triangular type of carrier signals ($i_{\Delta 1}$ and $i_{\Delta 2}$) as illustrated in Fig. 15.66a and 15.66e. The best results are obtained if the carrier signals are

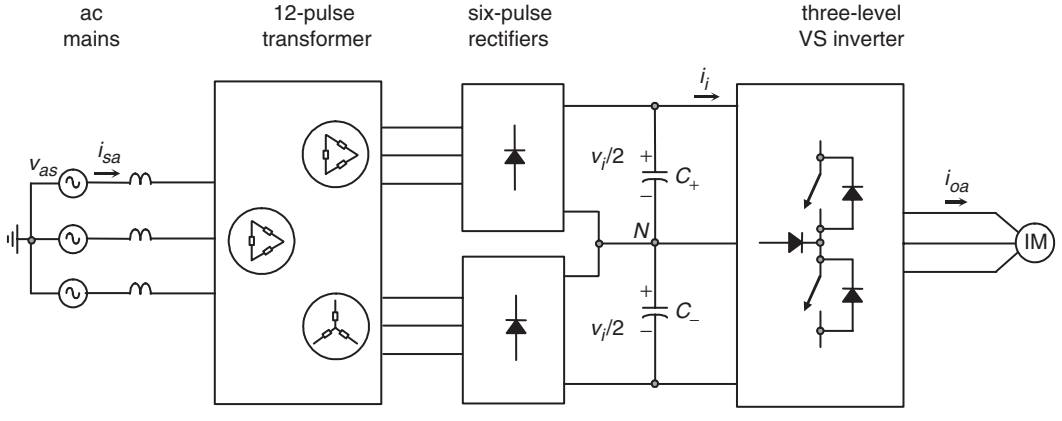

FIGURE 15.63 ASD based on a three-phase three-level VSI topology.

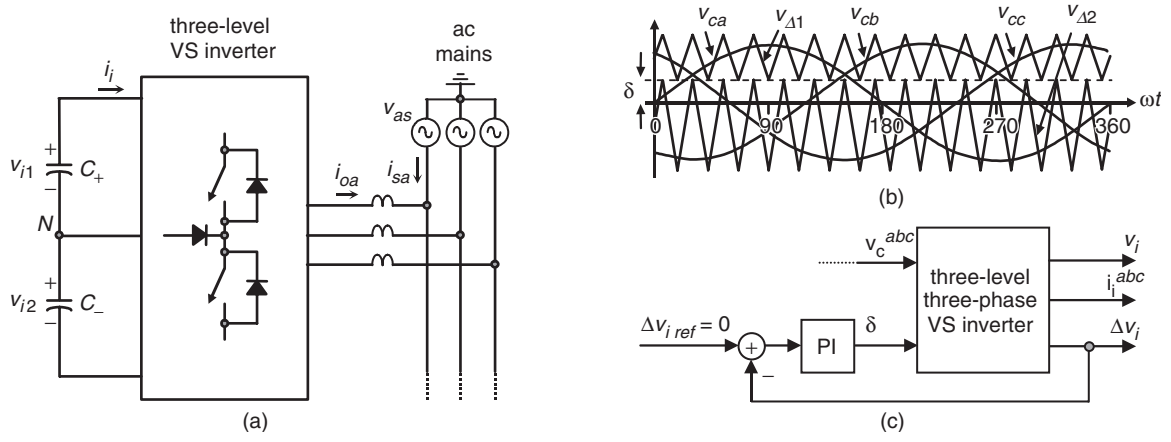

FIGURE 15.64 Reactive power and current harmonics compensator based on a three-phase three-level VSI topology: (a) power topology; (b) carrier and modulating signals; and (c) δ closed loop scheme.

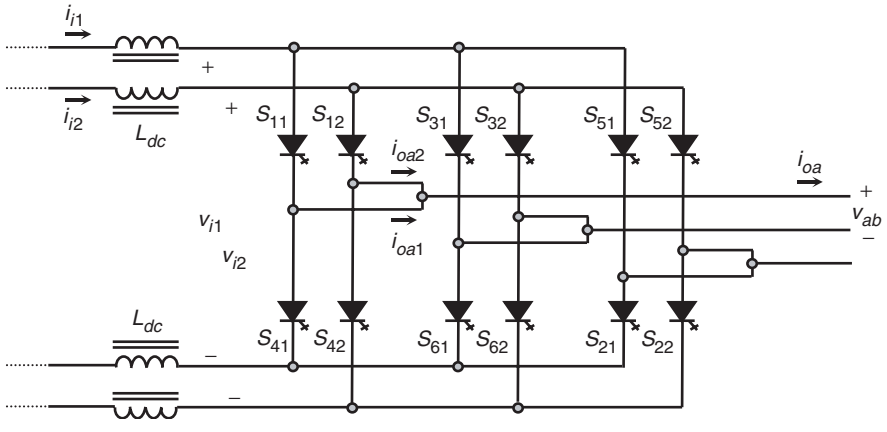

FIGURE 15.65 Three-phase three-level CSI topology.

180° out of phase and feature an odd normalized frequency (e.g. $m_f = 15$). In order to use the same set of carrier signals to generate the gating signals for phases b and c, the normalized frequency of the carrier signal m_f should be a multiple of 3. Thus, the possible values are $m_f = 3, 9, 15, 21, \ldots$.

Figure 15.66 shows the relevant waveforms for a three-level inverter modulated by means of a SPWM technique ($m_f = 15$, $m_a = 0.8$). Specifically, Fig. 15.66b and 15.66f show the gating signals obtained as described earlier in this chapter. The inverter line currents shown in 15.66c and 15.66g feature spectra shown in 15.66d and 15.66h, respectively. As expected, the inverter line currents contain harmonics at $l \cdot m_f \pm k$ with $l = 1, 3, \ldots$ and $k = 2, 4, \ldots$ and at $l \cdot m_f \pm k$ with $l = 2, 4, \ldots$ and $k = 1, 3, \ldots$. For instance, the first set of harmonics in the line currents (l =1, $m_f = 15$) are at 15 ± 2, $15 \pm 4, \ldots$.

The total inverter line current is shown in Fig. 15.67a, and features the first set of unwanted harmonics around $2m_f$ Fig. 15.67b. This becomes the first advantage of using a multilevel topology as the filtering component requirements become more relaxed. All the other features of carrier-based PWM techniques also apply in current source multilevel inverters. For instance: (I) the fundamental component of the line currents satisfy

$$\hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} = m_a \frac{\sqrt{3}}{2}(i_{i1} + i_{i2}) \quad 0 < m_a \leq 1 \quad (15.94)$$

where $0 < m_a \leq 1$ is the linear operating region. Also: (II) to further increase the amplitude of the load currents, a zero sequence signal could be injected to the modulating signals, in this case

$$\hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} = m_a \frac{\sqrt{3}}{2}(i_{i1} + i_{i2}) \quad 0 < m_a \leq 2/\sqrt{3} \quad (15.95)$$

the overmodulation operating region can be used by further increasing the modulating signal amplitudes ($m_a > 2/\sqrt{3}$),

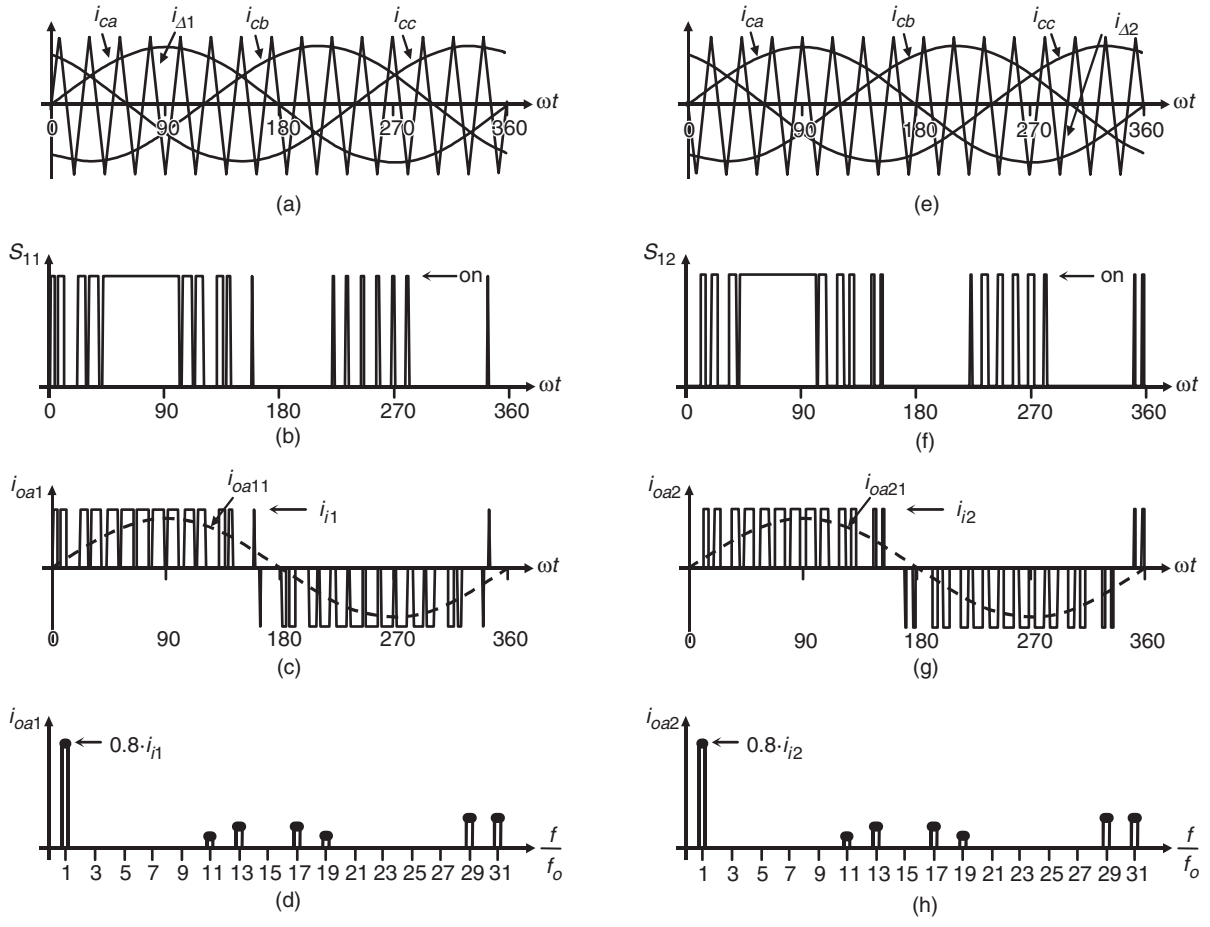

FIGURE 15.66 Three-level CSI topology. Relevant waveforms using a SPWM ($m_f = 15$, $m_a = 0.8$): (a) modulating signals and carrier signal 1; (b) switch S_{11} status; (c) inverter 1 linea current; (d) inverter 1 linea current spectrum; (e) modulating signals and carrier signal 2; (f) switch S_{12} status; (g) inverter 2 linea current; and (h) inverter 2 linea current spectrum.

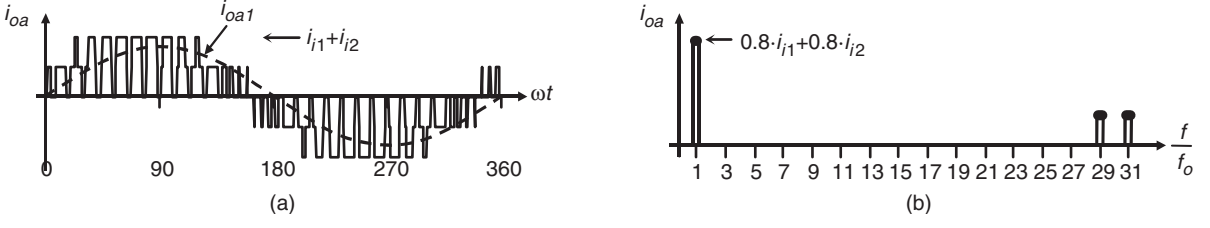

FIGURE 15.67 Three-level CSI topology. Relevant waveforms using a SPWM ($m_f = 15$, $m_a = 0.8$): (a) total inverter line current and (b) total inverter line current spectrum.

where the line currents range in

$$(i_{i1} + i_{i2}) < \hat{i}_{oa1} = \hat{i}_{ob1} = \hat{i}_{oc1} < \frac{4}{\pi}(i_{i1} + i_{i2}) \qquad (15.96)$$

Also: (III) a nonsinusoidal set of modulating signals could also be used by the modulating technique. This is the case where nonsinusoidal line currents are required as in active filter applications; and (IV) because of the two quadrants operation of CSIs, the multilevel inverter could equally be used in applications where the active power flow goes from the dc to the ac side or from the ac to the dc side. In general, for an N-level inverter modulated by means of a carrier-based technique, three modulating signals 120° out-of-phase and $N - 1$ carrier signals are required and the line currents in the inverters have a peak value of $i_i/(N - 1)$.

One of the drawbacks of the multilevel inverter is that the dc link capacitors cannot be supplied by a single dc voltage source. This is due to the fact that the currents required by the inverter in the dc bus are not symmetrical and therefore the capacitors will not equally share the dc supply voltage v_i. To overcome this problem, two alternatives are developed later on.

B. DC Link Voltage Balancing Issues

Figure 15.65 shows a three-level inverter and the ideal waveforms are shown in Fig. 15.66 and Fig. 15.67, which assume equal dc link currents, $i_{i1} = i_{i2}$. This even distribution is not naturally achieved and could be overcome by supplying the dc link inductors from independent supplies or properly gating the power valves of the inverter in order to minimize the unbalance.

Figure 15.68 shows an ASD based on a three-level current source inverter, where the dc link inductors are feed from two different sources. Unlike the VS topology, the scheme needs a closed loop control strategy to keep constant the dc link currents and equal to a given reference. This is achieved in commercial units by using either phase-controlled rectifiers or PWM rectifiers. Nevertheless, the multipulse transformer required to provide isolated dc link currents improves the ac mains current as in the VS multilevel topology.

This approach cannot be used when the inverter is not feed from an external power supply. This is the case of static series voltage compensators. In this case, the proper gating of the power valves becomes the only choice to keep and balance the dc link currents. Figure 15.64a shows this case where the voltage added by the inverter $n\mathbf{v}_\mathbf{o}^{abc}$ compensates the sags and/or swells present in the ac mains in order to provide a constant voltage to the load.

The SPWM modulating technique could be used as in Fig. 15.66 and Fig. 15.67; however, the peak amplitude of one triangular is amplified in the factor $1 + \delta$ and the peak amplitude of other triangular is amplified in the factor $1 - \delta$, where δ is left as a manipulable variable Fig. 15.69b. In fact, δ is used to control the difference of the dc link currents $\Delta i_i = i_{i1} - i_{i2}$.

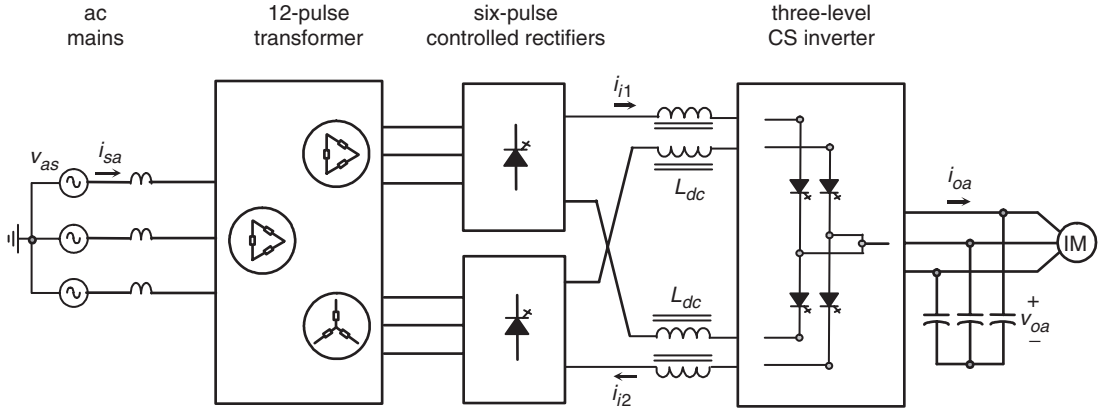

FIGURE 15.68 ASD based on a three-phase three-level CSI topology.

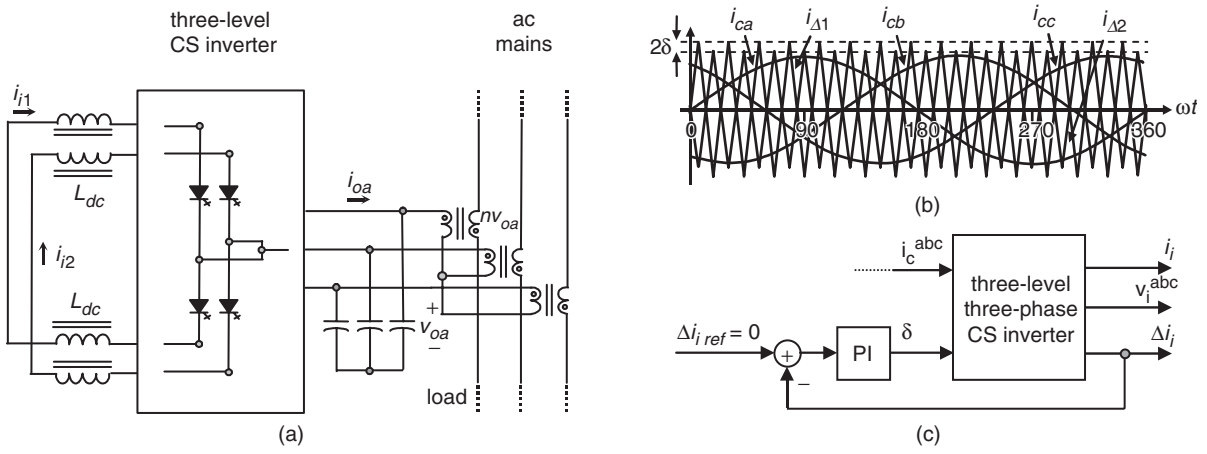

FIGURE 15.69 Reactive power and current harmonics compensator based on a three-phase three-level VSI topology: (a) power topology; (b) carrier and modulating signals; and (c) δ closed loop scheme.

A closed loop alternative is depicted in Fig. 15.69c to manipulate δ. The modulating signals $\mathbf{i}_\mathbf{c}^{abc}$ are left to control the series injected voltage into the ac mains by regulating the voltages $\mathbf{v}_\mathbf{o}^{abc}$ and keep the total dc link current $i_i = i_{i1} + i_{i2}$ equal to a reference. Both loops are not included in Fig. 15.69c.

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