ELE 432 PROJECT

Spring Semester 2020

Design of a 16-bit RISC Processor Using VHDL

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Dear Students,

This semester's project is based on "Design of a 16-bit RISC Processor Using VHDL" by Karansingh Pramodsingh Thakor e al. uploaded at HUZEM web site.

Procedure:

1- Gather 3-4 people as a group.
2- Publish this in https://docs.google.com/document/d/1WlcxnFXOLH F4px9CGPq_07NlOIzZ-1xfmcxIrIKaHXg/edit?usp=sharing
3- If you have no group add (your name+email) to in an empty slot or add it to groups with 1,2 or 3 people. Ask them first if they would accept you as a member
4- Your task is to implement version 3 of this RISC CPU
5- You will be graded as follows:
6- A) Implementing the exact schematic on Fig 12 on VHDL and showing this Will give you points +1-50; dependent on your report
   B) Implementing all the instructions of this CPU will give you +20-30 pts depending on how well you present this.
   C) Implementing a small program such as the one in TABLE V, will give you +10-20 pts depending on how well you present this.
7- Indicate the contributions of each member in the pd
8- For 6A,B and C put all information in a pdf file and return it by Jan 14th.
9- This will form a part of your Midterm Grade.
10- Please read the paper and for the items not describe clearly try to improvise and be creative.

GOOD LUCK !