

CSE 331/503

Computer Organization

Homework 4

In this project, you will use Altera Quartus II with Verilog. You will implement a different version of 32-bit MIPS processor. The block that you will design will get no inputs from outside. You will have two memories: Data Memory and Instruction Memory. The instructions must be loaded to the instruction memory and the data must be put in data memory. You will support **lw**, **sw**, **j**, **jal**, **jr**, **beq**, **bne**, **addn**, **subn**, **xorn**, **andn**, **orn**, **ori** and **lui** instructions.

But the R-type instructions will execute different than the conventional MIPS we have seen. This is why they have 'n' at the end (representing new). The new instructions have the same opcode and function fields as the conventional R-type instructions. For instance the opcode and function field of **orn** is same as **or**.

But the execution is different. For instance:

addn \$rd, \$rs, \$rt

RTL Representation

```
$rs <= $rs + $rt
if($rs + $rt == 0)
  $rd <= 1
else if($rs + $rt < 0)
  $rd <= 2
else
  $rd <= 3
```

In order to implement that, you must be able to write two different register addresses in one cycle Design your register accordingly.

You will write test bench and simulate your design for verification. You will write the register and memory contents before and after the execution of instructions using **writememh** in your test bench verilog code. You will initialize memory contents using **readmemh**.

The data memory size will be 256KB whereas the instruction memory size will be 16KB.

Other than registers and memory only structural Verilog is allowed. This means behavioral statements like always, if, etc are not allowed.