AARHUS UNIVERSITY

EIC

Integrerede kredsløb

IC Project - class AB Amplifier

Navn	Initialer	Studienummer	Retning
Jakob Bjerregaard Olsen	JBO	202109022	E
Alexander Nygaard Thomsen	AT	201911329	E

Underviser: Jamaac Hassan Hire

Afleveringsdato: 28/12/2025

1 introduction

The purpose of this project is to design and implement a Class AB audio power Amplifier, with some general requirements.
From the provided requirements of the project, the below states specifications are:

- **Output power** - This specification is a free choice and will be expanded later
- **Input Resistance** - $>= 10k\Omega$
- **Output Resistance** - $< 5\Omega$
- **Bandwidth** - bandwidth is specified to be in the human hearing range 20Hz - 20KHz
- **Design Structure** - must be based on a three stage topology, differential pre-amp, voltage amp stage and power amp stage.

From these given, overall requirements, our derived specifications are:

- **Output power** - $P_{out} = 200mW$
- **load size** - Giver the output power, the chosen load size is $R_{load} = 16\Omega$
- **Supply contrains** - given power requirements and load size, the supply rails of the Amplifier system is $\pm 15V$

From our on own requirements, it is possible to derive some other specifications about the system. The output voltage/current RMS

$$V_{outRMS} = \sqrt{P_{out} \cdot R_{load}} \tag{1}$$

$$I_{outRMS} = \sqrt{\frac{P_{out}}{R_{load}}} \tag{2}$$

We assume an input signal of $V_{inRMS} = 20mV$, this gives an overall gain of

$$\frac{V_{out}}{V_{in}} \approx 126 \tag{3}$$

To limit the Amplifier to the human hearing range, an lowpass filter is added to limit frequency content above 20KHz

$$f_C = 20KHz \tag{4}$$

$$C = 470\mu F \tag{5}$$

$$X_C = \frac{1}{2\pi f \cdot C} = 0.017\Omega \tag{6}$$

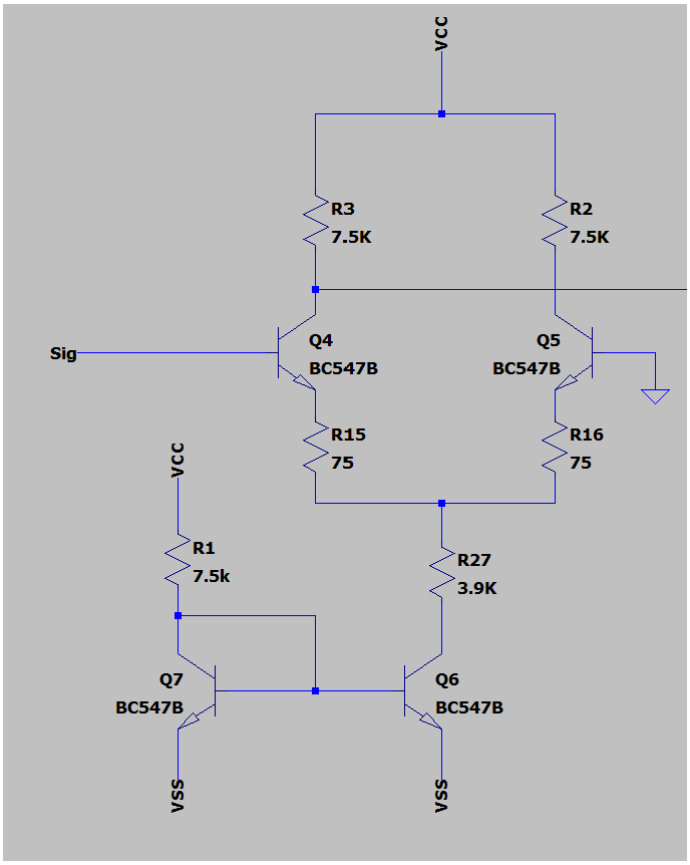
2 Input stage

The first part of the amplifier is the input stage, this specific implementation is build around a pair of NPN transistors. This particular implementation includes a tail current source, more specifcally a current mirror build as a sink.

2.1 topology

2.1.1 differential pair

Q4 and Q5 is an NPN differential pair, with R3 and R2 as collector loads and R15 and R16 as emitter degeneration resistors. This create a single-ended output differential amplifier. The emitter resistances are included to negate the temperature dependence of BJT's and to make the transistor have a more linear behavior. This however changes how the transistors transconductance is calculated from $gm = \frac{I_C}{V_T}$ to $gm \approx \frac{1}{R_E}$, if and only if $gmR_E \gg 1$.



DC analysis

It is assumed that the BC547 has an beta factor of $\beta = 325$ and we aim for a diff amp gain of roughly $A_{diff} \approx 42$. The current sink in bottom tries to draw 4mA of current, thus $I_{Ecm} = 2mA$ must run in each branch of the Amplifier. The collector resistance then becomes

$$V_{Ccm} = V_{CC} - R_{Ccm} \cdot I_{Ecm}\alpha \Rightarrow R_{Ccm} = \frac{V_{CC} - V_{Ccm}}{I_{Ecm}\alpha} = 7.774k\Omega \tag{7}$$

AC analysis

For AC analysis, the intrinsic emitter resistance is $r_e = \frac{V_T}{2mA} = 12.5\Omega$ and the external emitter resistance is $R_E = 75\Omega$ this yields a total emitter resistance of $r_{etot} = 12.5\Omega + 75\Omega = 87.5\Omega$. Thus changes to temperature only affects the term with V_T, which is $\approx \pm 2mV/C$

The goal here is to relate the differential input voltage V_d to the output voltage V_o, by elimintating the internal transistor current i_b, this will yield the gain. Since the desired gain for this Amplifier is chosen, we can use this to find the emitter resistance, which stated earlier is $R_E = 75\Omega$.

Since the other input of the differential amplifier is grounded, the differential voltage for Q4 becomes:

$$\frac{v_{Indiff}}{2} = i_b r_\pi + i_e R_E \tag{8}$$

$$r_\pi = \beta r_e \tag{9}$$

$$i_e = (\beta + 1) i_b \tag{10}$$

$$\Downarrow \tag{11}$$

$$v_d = 2 i_b (\beta r_e + (\beta + 1) R_E) \tag{12}$$

And the common mode voltage then becomes:

$$v_{Outdiff} = -\beta \cdot i_{bcm} \cdot R_{Ccm} \tag{13}$$

These two defines the differential gain:

$$A_{diff} = \frac{v_{Outdiff}}{v_{Indiff}} = -\frac{\beta R_C}{2(\beta r_e + (\beta + 1) R_E)} \tag{14}$$

Since the gain has already been chosen in the design stage, as mentioned ealier, $A_{diff} \approx 42$. The emitter resistance can be calculated, by solving for R_E:

$$A_{diff} \rightarrow R_E \approx 75\Omega \tag{15}$$

It should be noted that the expression for the differential gain gets rather lengthy when expanded, thus for gains much larger than $\beta \gg 1$, the 1 term in $(\beta + 1)$, can safely be ignored. This factors out β in both numerator and denominator:

$$2(\beta r_e + (\beta + 1) R_E) \Rightarrow\approx \beta (r_e + R_E) \tag{16}$$

$$A_{diff} \approx -\frac{R_C}{2(r_e + R_E)} \approx -42.726 \tag{17}$$

It is desirable to know the common mode rejections ratio, and in order to find that, the common mode gain is needed. The common mode gain is given by the common mode input voltage over the common mode output voltage. But in order to express them the value of R_{EE} needs to be known. R_{EE} is placed to reduce the stress on the transistor in the current mirror. An assumption of the collector emitter voltage being 0.3V is made to ensure that the transistor is operating in the active region. Based on this assumsion the expression for R_{EE} is given by

$$0V - V_{BE} - R_E \cdot I_E - 2 \cdot I_E \cdot R_{EE} - V_{CE} - V_{EE} = 0V \tag{18}$$

$$R_{EE} = \frac{V_{BE} - R_E \cdot I_E - V_{CE} - V_{EE}}{2 \cdot I_E} = 3.838k\Omega \approx 3.9k\Omega \tag{19}$$

Now the common mode input voltage can be expressed as:

$$v_{InCM} = i_b \cdot (\beta + 1) \cdot r_e + i_b \cdot (\beta + 1) \cdot R_E + 2 \cdot i_b \cdot (\beta + 1) \cdot R_{EE} \tag{20}$$

The times 2 comes from the fact that know there is a contribution from both branches. The output common mode is given by:

$$v_{OutCM} = -\beta \cdot i_b \cdot R_C \tag{21}$$

With the two above equations the common mode gain can be expressed as:

$$A_{CM} = \frac{v_{OutCM}}{v_{InCM}} = \frac{-\beta \cdot i_b \cdot R_C}{i_b \cdot (\beta + 1) \cdot r_e + i_b \cdot (\beta + 1) \cdot R_E + 2 \cdot i_b \cdot (\beta + 1)} \tag{22}$$

In the above equation i_b can be removed because it is multiplied on both the denominator and numerator. Then by combining common expressions in the denominator then the gain can be expressed as:

$$A_{CM} = \frac{-\beta \cdot i_b \cdot R_C}{(\beta + 1) \cdot (r_e + R_E + 2 \cdot R_{EE})} = -0.948 \tag{23}$$

Now that both the differential and common mode gain is known the common mode rejection ration can be calculated. It is given as:

$$CMRR = 20 \cdot \log(\frac{A_{diff}}{A_{CM}}) = 33.078dB \tag{24}$$

2.2 Current Sink

The pupose of the current mirror is to supply, or in this case "sink" the required current for the differential amplifier. This means that it should be specified to draw the sum of the currents leaving both branches of the diff amp. Thus the equations becomes:

$$I_{CQ6} = I_{EEcm} = 4mA \tag{25}$$

$$\tag{26}$$

Because it is a BC547 again, the same $\beta = 325$ is assumed, this means that current entering the base of Q6.

$$I_{BQ6} = \frac{I_{CQ6}}{\beta} \approx 12\mu A \tag{27}$$

$$\tag{28}$$

Since the current mirror is comprised to two NPN transistors, the current drawn should be the sum of the collector current I_{CQ5} and 2 base currents.

$$I_{RCQ5} = 2I_{BQ6} + I_{CQ5} = 4.025mA \tag{29}$$

Therefore the resistance to define the reference current becomes:

$$R_{ref} = \frac{V_{CC} - V_{EE}}{I_{RCQ5}} \approx 7.5k\Omega \tag{30}$$

3 Voltage Amplification Stage

Following the differential amplifier is a Voltage amplification stage. The purpose of this circuit is to gain the signal.

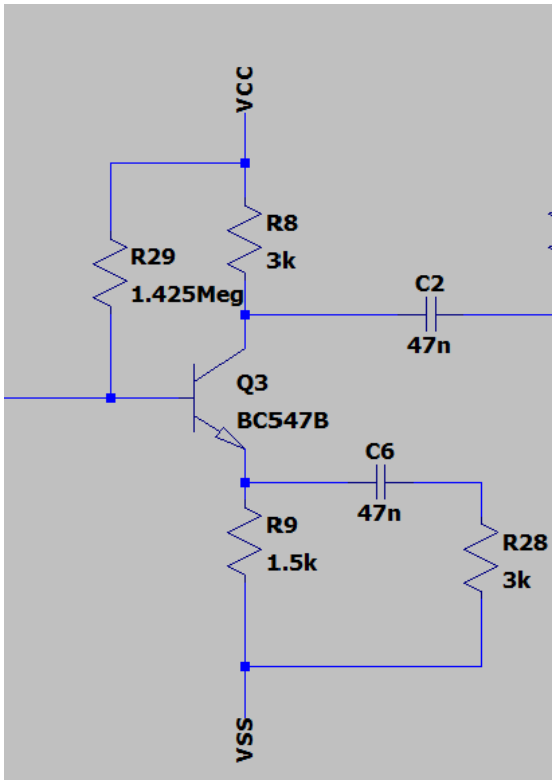


Figure 1: voltage amplification stage

The design goal of this stage is a gain of 3. And to realize this goal a few other contraints are chosen to make it easier, such as the emitter current should be $I_E = 5mA$ and $V_{CE} = 7.5V$, to ensure in the active region.

From these contrains the ratio of the emitter and collector resistor can be determined. Also note that this the current design is for DC, thus for the AC gain an additional impedance can be coupled in to reduce the emitter resistance in AC and increase the gain.

$$i_B = \frac{v_{in}}{R_{IN}} v_o = -R_C i_b \beta \tag{31}$$

subtituting

$$v_o = -R_C \frac{v_{in}}{R_{IN}} \beta \Rightarrow -\alpha \frac{R_C}{R_E} \tag{32}$$

Setting $R_C = 3k\Omega$, means that, at AC, $R_E = 1k\Omega$

To achieve the current at DC, the emitter resistance can be calculated:

$$R_{Edc} = \frac{V_{CC} - R_C I_E \alpha - VCE - V_{EE}}{I_E} \approx 1.5k\Omega \tag{33}$$

To compensate for this in AC, an impedance consisting of a resistance and a capacitor is set in parallel with the emitter resistance. This essentially shapes the gain when an AC input is given.

$$A_{Ndc} = \frac{R8}{R9} = 2 \tag{34}$$

$$A_{Nac} = \frac{R8}{R9||R28} = 3 \tag{35}$$

This happends when when the corner frequency of:

$$f_c = \frac{1}{2\pi R28C6} = \frac{1}{2\pi \cdot 3k\Omega \cdot 47nF} \approx 1.13Hz \tag{36}$$

is exceeded.

Other parameters for the stage:

$$V_C = V_{CC} - R_C I_E \alpha = 0.046V \tag{37}$$

$$V_E = I_E R_E + V_{EE} = -7.5V \tag{38}$$

$$V_B = V_E + V_{BE} = -6.8V \tag{39}$$

$$I_B = \frac{I_E}{(\beta + 1)} \approx 15.3\mu A \tag{40}$$

Biasing the stage then comes from a collector base resistor

$$R_C B = \frac{15V - (-6.8V)}{15.3\mu A} = 1.425M\Omega \tag{41}$$

4 Unity gain Buffer

To prevent loading of the voltage amplification stage into the output stage, a unity gain buffer is implemented to increase the perceived impedance, the output of the voltage amplification stage sees. This is implemented as a common collector amplifier with a gain of ≈ 1.

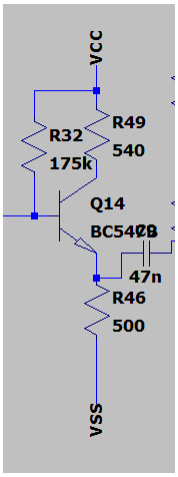


Figure 2: common collector unity gain buffer

To ensure that the buffer has low output impedance, so it does not affect the circuitry that comes after, a decently sized standing current is necessary. To drive the stage a ratherl large emitter current of 28mA is chosen.

$$V_E = V_{SS} + I_E R46 = -1V \tag{42}$$
$$V_B = V_B + 0.7V = -0.3V \tag{43}$$
$$I_B = \frac{I_E}{\beta + 1} \approx 85\mu A \tag{44}$$

The biasing resistor then becomes:

$$R32 = \frac{V_{SS} - V_B}{I_B} \approx 178k\Omega \tag{45}$$

The collector current then becomes:

$$I_C = \frac{\beta}{\beta + 1} I_E \approx 27.9mA \tag{46}$$

and to sanity check if the current is possible the voltage across the collector and emitter must be above 0.3V

$$V_C = Vcc - I_C R49 = -0.074V \tag{47}$$
$$V_{CE} = V_C - V_E = 0.926V \tag{48}$$

This shows that the unity gain buffer can drive this configuration.
The small signal parameters becomes:

$$r_e \approx \frac{V_T}{I_E} = \frac{25mV}{28mA} = 0.893\Omega \tag{49}$$
$$r_\pi = \beta r_e \approx 290\Omega \tag{50}$$

Output impedance, when looking into the emitter. The sources becomes AC ground, this means that the output impedance becomes

$$R_{out} \approx r_e || 500\Omega \approx r_e \tag{51}$$

5 Output Stage

The output stage consists mainly of circuitry to handle the final power amplification of the amplification, the purpose is to gain the currents and not the voltage signal. Because this is a Class AB, this means that two output transistors are driving each half of the signal cycle, however to change this from class B to AB, it requires transistor biasing, so that cross distortion is avoided.

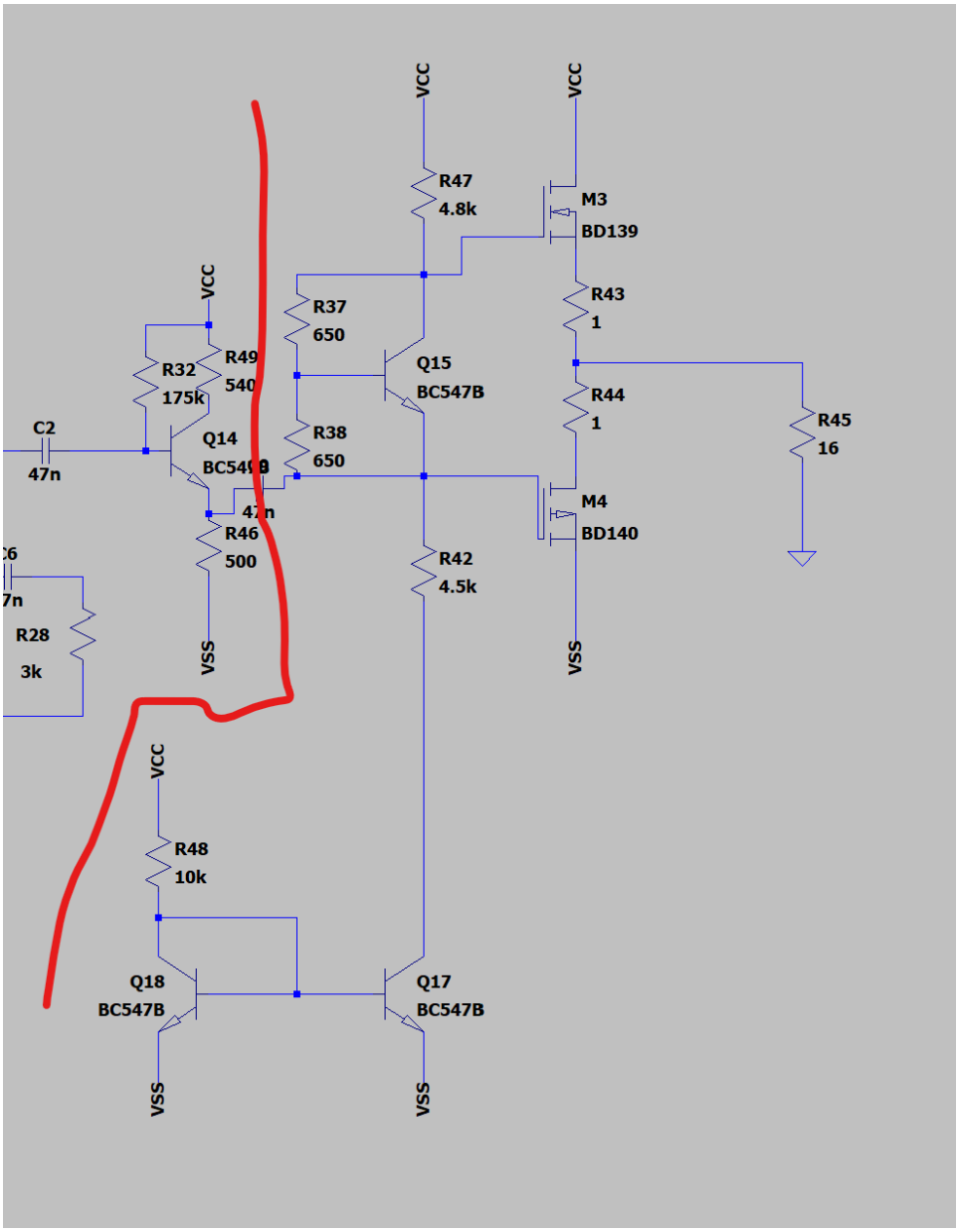


Figure 3: Output stage, everything to the right of the red line, is considered part of the output stage.

To bias the two output transistors, a Vbe multiplier has been implemented. Q15 and the two resistors R37/38 generate a controlled voltage, which is used to determine the working point of the output follow the expression:

$$V_{bias} \approx V_{beQ15} \cdot (1 + \frac{R37}{R38}) \approx 2V_{BE} \tag{52}$$

This then becomes a scale factor for the transistors base emitter voltage, meaning that the collector voltage will sit an additional drop above it, of $\approx 1.4V$ Practically this circuit also provides the ability to thermally track or follow

the output transistors, due the possibility to physically mount the circuit thermally close to the output.

The biasing part of the stage is driven by a current sink similar to the one found in the input stage, however this sinks $3mA$ of current. This means that the voltages at the output stages are.

$$V_{R47} = 3mA \cdot 4.8k\Omega = 14.4V \tag{53}$$
$$V_{Bm3} = 0.6V \tag{54}$$
$$V_{R42} = 3mA \cdot 4.5k\Omega = 13.5V \tag{55}$$
$$V_{Bm4} = -15V + 13.5V = -1.5V \tag{56}$$

Quiescent current through the output stage can then be expressed as:

$$I_Q \approx \frac{V_{bias} - (V_{BE,N} + |V_{BE,P|})}{R43 + R44} \tag{57}$$

This indicates that the output stage is somewhat sensitive to changes in changes in both transistors V_{be} due to fact that those resistances, R43 + R44 are so small.

The two emitter resistors linearize the transfer characteritics of the output transistors and limits thermal runaway. The main purpose of those transistors, is to turn small changes in Vbe into current chnages, therefore the small signal voltage gain is $A_N \approx 1$. The output impedance, can be approximated by

$$R_{out} \approx \frac{r_e}{\beta + 1} + R43 + R44 \tag{58}$$

Where $r_e \approx \frac{V_T}{I_E}$

5.1 Simulation

Using the calculated values from the analysis, the circuit was then simulated in LTspice. The complete circuit can be seen below. Using the *.tren* spice directive to test the circuit and checking for behavior.

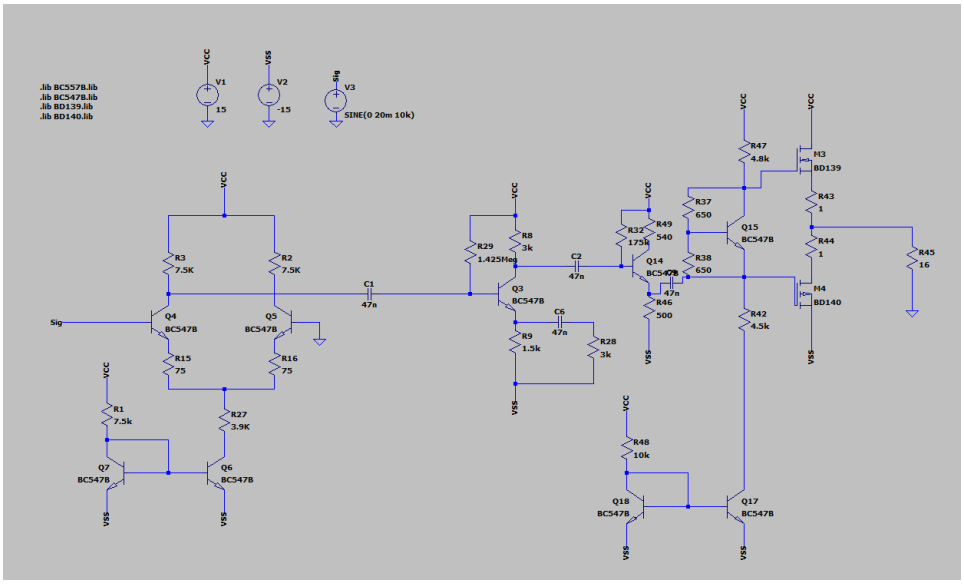


Figure 4: Complete circuit in LTspice.

Grounding both of the inputs and probing the simulation model, resulted in a measurement of 1.468V at the collector of Q4 and having its emitter sit a diode drop below ground, means that this transistor is in the active region.

At Dc the current sink through R27 is around 3.6mA.

As for the voltage amplification stage, the collector sits at 0.56V and the emitter at -7.76V, this means that this coupling also is in the active region. With an emitter current of roughly 4.8mA

In the output stage, the current drawn thought the vbe multiplier is roughly 2.94mA, which is close to the desired 3mA. The lower bias point sits at $\approx -474mV$, while the upper bias point is at $\approx 842mV$, this means that there is approximately a multiple of 2 base emitter voltage difference between the two points, which is intended.

Lastly the Quiescent current, at DC, running through R42 is 1.92mA. This current is flowing to load, as it seems to be strongly tied to ground. There is only 30mV at the collector of M4, so the Vbe of M4 is not high enough to draw the current at this stage.

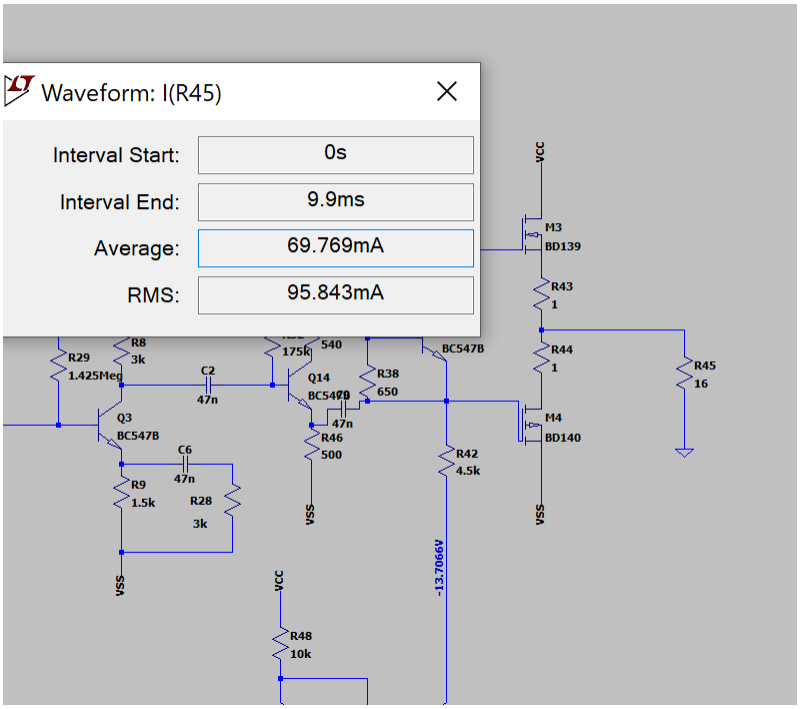


Figure 5: RMS current measurement at the output of the amplification, more specifically the current running in the load

With a RMS current of $I_{OUT} = 95.832mA$ running in the 16Ω load, the power can be calculated:

$$V_{OUT} = I_{RMS} \cdot R_{LOAD} = 95.832mA \cdot 16\Omega = 1.5328V_{RMS} \tag{59}$$

$$P_{OUT} = I_{RMS} \cdot V_{OUT} = 0.146W \tag{60}$$

This simulated power is a little lower than intended.

5.2 Realization

The circuit was the built and realized. The realized circuit can be seen on figure 6. The circuit was tested the same way the simulation was, the settinges for the signal used can be seen on figure 7

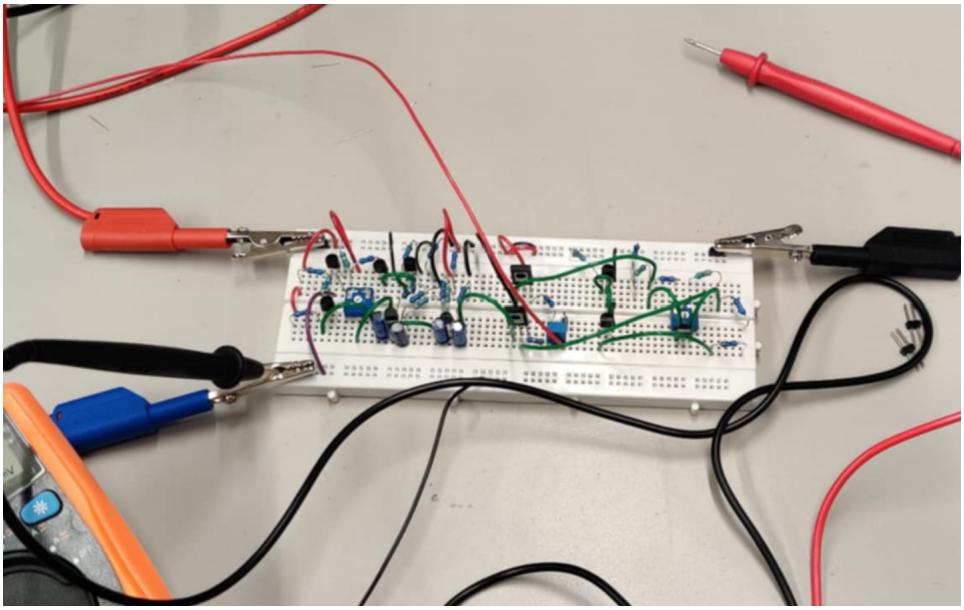


Figure 6: implementation on breadboard

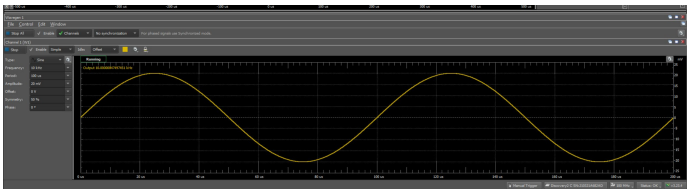


Figure 7: The chosen input signal is a pure signe wave with a 20mV amplitude at 10kHz

Table 1: Measured DC voltages of bias points in amplifier circuit

Class AB DC points	Diff sig[V]	Diff No sig[V]	CE amp[V]	C amp[V]	AB NPN[V]	AB NPN[V]
V_C	1.83	2.18	-0.15	0.88	15	-15.01
V_E	-0.644	-0.645	-6.75	-0.82	-0.76	-0.28
V_B	0	0	-5.6	-0.16	0.44	-1.02

On figure 8 the amplification results can be seen for after the common mode amplifier and the commen emitter amplifer(voltage amplification stage). The final gain for the amplifier is somewhat lower than expected. On table 1 the DC point for the diffrent transistors is shown, here it can be seen that the DC points are the with in resenable range and they are in the active region

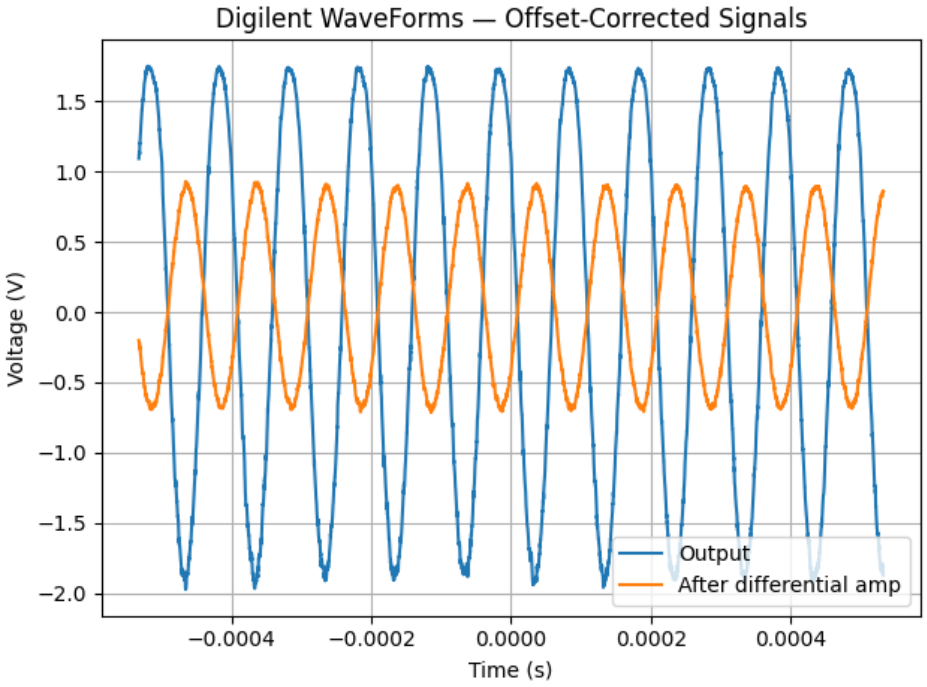


Figure 8: Measurements of the amplifier. The orange trace is from after the differential amplifier, to show much the signal is gained. The blue trace is from the output of the amplifier itself.

6 conclusion

It can then be concluded that the audio amplifier works as intended and that it mostly satisfies our requirements, set in the specification. However, we fell short of the gain goal of $\approx= 126$, we achieved ≈ 87, the measured signal peak of the output was

$$V_{out}Peak = 1.749V \tag{61}$$

$$V_{out}RMS = \frac{1.749V}{\sqrt{2}} = 1.236V_{RMS} \tag{62}$$

Whereas the input rms is roughly $V_{in}RMS = 0.014V$ this leads to a input to output ratio of

$$\frac{V_{out}}{V_{in}} = \frac{1.236V}{0.014} \approx 87.45 \tag{63}$$

As for power, the output current becomes $\frac{1.236}{16\Omega} = 77.25mA_{RMS}$ which results in $1.749V \cdot 77.25mA = 95.53mW$ of power being drawn, this is also not close our target of 200.