AARHUS UNIVERSITY

EIC

Integrerede kredsløb

IC Project - class AB Amplifier

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Afleveringsdato: XX/12/2025

1 introduction

The purpose of this project is to design and implement a Class AB audio power Amplifier, with some general requirements.
From the provided requirements of the project, the below states specifications are:

- **Output power** - This specification is a free choice and will be expanded later
- **Input Resistance** - $>= 10k\Omega$
- **Output Resistance** - $< 5\Omega$
- **Bandwidth** - bandwidth is specified to be in the human hearing range 20Hz - 20KHz
- **Design Structure** - must be based on a three stage topology, differential pre-amp, voltage amp stage and power amp stage.

From these given, overall requirements, our derived specifications are:

- **Output power** - $P_{out} = 200mW$
- **load size** - Giver the output power, the chosen load size is $R_{load} = 16\Omega$
- **Supply contrains** - given power requirements and load size, the supply rails of the Amplifier system is $\pm 15V$

From our on own requirements, it is possible to derive some other specifications about the system. The output voltage/current RMS

$$V_{outRMS} = \sqrt{P_{out} \cdot R_{load}} \tag{1}$$

$$I_{outRMS} = \sqrt{\frac{P_{out}}{R_{load}}} \tag{2}$$

We assume an input signal of $V_{inRMS} = 20mV$, this gives an overall gain of

$$\frac{V_{out}}{V_{in}} \approx 126 \tag{3}$$

To limit the Amplifier to the human hearing range, an lowpass filter is added to limit frequency content above 20KHz

$$f_C = 20KHz \tag{4}$$

$$C = 470\mu F \tag{5}$$

$$X_C = \frac{1}{2\pi f \cdot C} = 0.017\Omega \tag{6}$$

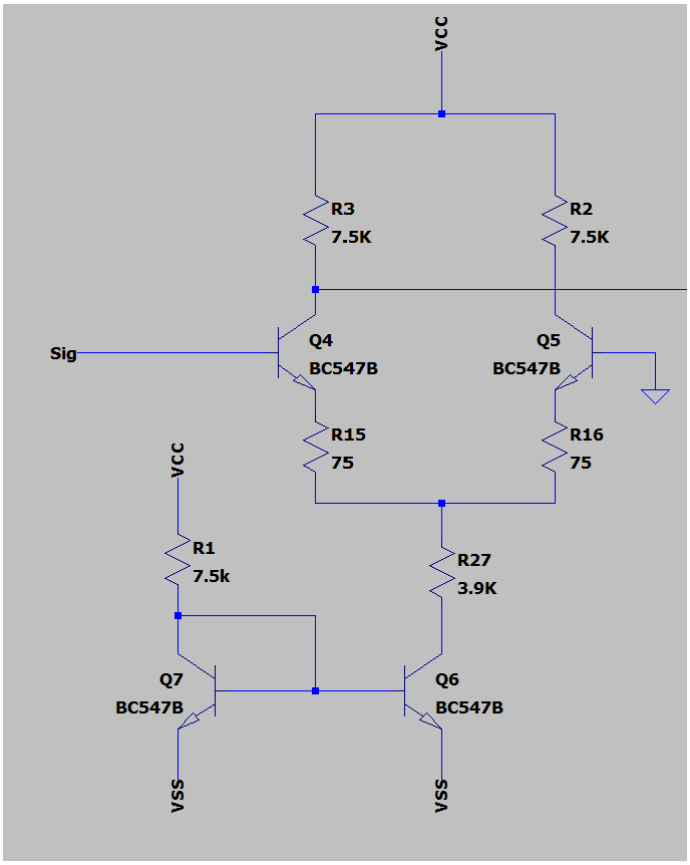
2 Input stage

The first part of the amplifier is the input stage, this specific implementation is build around a pair of NPN transistors. This particular implementation includes a tail current source, more specifcally a current mirror build as a sink.

2.1 topology

2.1.1 differential pair

Q4 and Q5 is an NPN differential pair, with R3 and R2 as collector loads and R15 and R16 as emitter degeneration resistors. This create a single-ended output differential amplifier. The emitter resistances are included to negate the temperature dependence of BJT's and to make the transistor have a more linear behavior. This however changes how the transistors transconductance is calculated from $gm = \frac{I_C}{V_T}$ to $gm \approx \frac{1}{R_E}$, if and only if $gmR_E \gg 1$.



DC analysis

It is assumed that the BC547 has an beta factor of $\beta = 325$ and we aim for a diff amp gain of roughly $A_{diff} \approx 42$. The current sink in bottom tries to draw 4mA of current, thus $I_{Ecm} = 2mA$ must run in each branch of the Amplifier. The collector resistance then becomes

$$V_{Ccm} = V_{CC} - R_{Ccm} \cdot I_{Ecm}\alpha \Rightarrow R_{Ccm} = \frac{V_{CC} - V_{Ccm}}{I_{Ecm}\alpha} = 8.175k\Omega \tag{7}$$

AC analysis

For AC analysis, the intrinsic emitter resistance is $r_e = \frac{V_T}{2mA} = 12.5\Omega$ and the external emitter resistance is $R_E = 110\Omega$ this yields a total emitter resistance of $r_{etot} = 12.5\Omega + 75\Omega = 87.5\Omega$. Thus changes to temperature only affects the term with V_T, which is $\approx \pm 2mV/C$

The goal here is to relate the differential input voltage V_d to the output voltage V_o, by elimintating the internal transistor current i_b, this will yield the gain. Since the desired gain for this Amplifier is chosen, we can use this to find the emitter resistance, which stated earlier is $R_E = 75\Omega$.

Since the other input of the differential amplifier is grounded, the differential voltage for Q4 becomes:

$$\frac{v_d}{2} = i_b r_\pi + i_e R_E \tag{8}$$

$$r_\pi = \beta r_e \tag{9}$$

$$i_e = (\beta + 1) i_b \tag{10}$$

$$\Downarrow v_d = 2 i_b (\beta r_e + (\beta + 1) R_E) \tag{11}$$

And the common mode voltage then becomes:

$$v_{o1cm} = -\beta \cdot i_{bcm} \cdot R_{Ccm} \tag{12}$$

These two defines the differential gain:

$$A_{diff} = \frac{v_{o1cm}}{v_d} = -\frac{\beta R_C}{2(\beta r_e + (\beta + 1) R_E)} \tag{13}$$

Since the gain has already been chosen in the design stage, as mentioned ealier, $A_{diff} \approx 42$. The emitter resistance can be calculated, by solving for R_E:

$$A_{diff} \rightarrow R_E \approx 75\Omega \tag{14}$$

It should be noted that the expression for the differential gain gets rather lengthy when expanded, thus for gains much larger than $\beta \gg 1$, the 1 term in $(\beta + 1)$, can safely be ignored. This factors out β in both numerator and denominator:

$$2(\beta r_e + (\beta + 1) R_E) \Rightarrow\approx \beta (r_e + R_E) \tag{15}$$

$$A_{diff} \approx -\frac{R_C}{2(r_e + R_E)} \tag{16}$$

2.2 Current Sink

The pupose of the current mirror is to supply, or in this case "sink" the required current for the differential amplifier. This means that it should be specified to draw the sum of the currents leaving both branches of the diff amp. Thus the equations becomes:

$$I_{CQ6} = I_{EEcm} = 4mA \tag{17}$$

$$\tag{18}$$

Because it is a BC547 again, the same $\beta = 325$ is assumed, this means that current entering the base of Q6.

$$I_{BQ6} = \frac{I_{CQ6}}{\beta} \approx 12\mu A \tag{19}$$

$$\tag{20}$$

Since the current mirror is comprised to two NPN transistors, the current drawn should be the sum of the collector current I_{CQ5} and 2 base currents.

$$I_{RCQ5} = 2 I_{BQ6} + I_{CQ5} = 4.025mA \tag{21}$$

Therefore the resistance to define the reference current becomes:

$$R_{ref} = \frac{V_{CC} - V_{EE}}{I_{RCQ5}} \approx 7.5k\Omega \tag{22}$$

3 Voltage Amplification Stage

Following the differential amplifier is a Voltage amplification stage. The purpose of this circuit is to gain the signal.

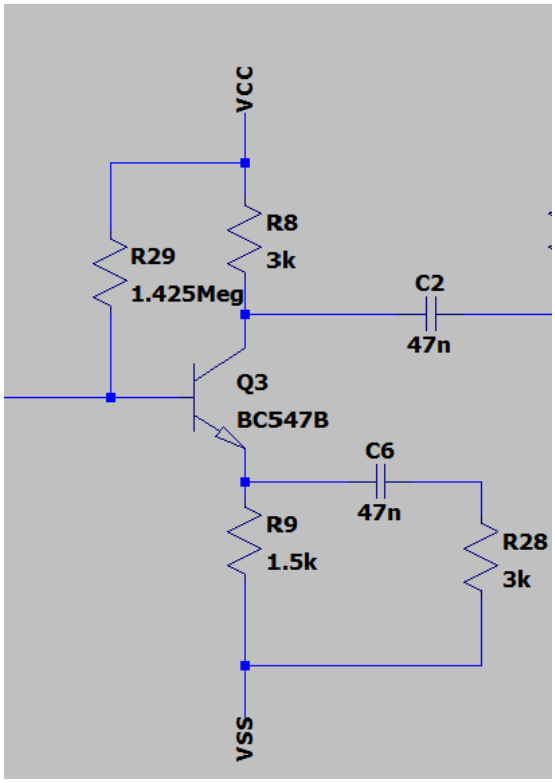


Figure 1: voltage amplification stage

The topology is a common-emitter amplifier.R10 and R11 is setting the bias point of the stage The design goal of this stage is a gain of 3. And to realize this goal a few other contraints are chosen to make it easier, such as the emitter current should be $I_E = 5mA$ and $V_{CE} = 7.5V$, to ensure in the active region.

From these contrains the ratio of the emitter and collector resistor can be determined. Also note that this the current design is for DC, thus for the AC gain an additional impedance can be coupled in to reduce the emitter resistance in AC and increase the gain.

$$i_B = \frac{v_{in}}{R_{IN}} v_o = -R_C i_b \beta \tag{23}$$

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$$v_o = -R_C \frac{v_{in}}{R_{IN}} \beta \Rightarrow -\alpha \frac{R_C}{R_E} \tag{24}$$

Setting $R_C = 3k\Omega$, means that, at AC, $R_E = 1k\Omega$

To achieve the current at DC, the emitter resistance can be calculated:

$$R_{Edc} = \frac{V_{CC} - R_C I_E \alpha - VCE - V_{EE}}{I_E} \approx 1.5k\Omega \tag{25}$$

To compensate for this in AC, an impedance consisting of a resistance and a capacitor is set in parallel with the emitter resistance. This essentially shapes the gain when an AC input is given.

$$A_{Ndc} = \frac{R8}{R9} = 2A_{Nac} = \frac{R8}{R9||R28} = 3 \tag{26}$$

This happends when when the corner frequency of:

$$f_c = \frac{1}{2\pi R28C6} = \frac{1}{2\pi \cdot 3k\Omega \cdot 47nF} \approx 1.13kHz \tag{27}$$

is exceeded.

Other parameters for the stage:

$$V_C = V_{CC} - R_C I_E \alpha = 0.046V V_E = I_E R_E + V_{EE} = -7.5V V_B = V_E + V_{BE} = -6.8V I_B = \frac{I_E}{(\beta + 1)} \approx 15.3\mu A \tag{28}$$

Biasing the stage then comes from a collector base resistor

$$R_C B = \frac{15V - (-6.8V)}{15.3\mu A} = 1.425M\Omega \tag{29}$$

4 Unity gain Buffer

To prevent loading of the voltage amplification stage into the output stage, a unity gain buffer is implemented to increase the perceived impedance, the output of the voltage amplification stage sees. This is implemented as a common collector amplifier with a gain of ≈ 1.

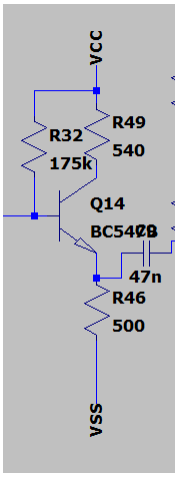

Figure 2: common collector unity gain buffer

To ensure that the buffer has low output impedance, so it does not affect the circuitry that comes after, a decently sized standing current is necessary. To drive the stage a ratherl large emitter current of 28mA is chosen.

$$V_E = V_{SS} + I_E R46 = -1V V_B = V_B + 0.7V = -0.3V I_B = \frac{I_E}{\beta + 1} \approx 85\mu A \tag{30}$$

The biasing resistor then becomes:

$$R32 = \frac{V_{SS} - V_B}{I_B} \approx 178k\omega \tag{31}$$

The collector current then becomes:

$$I_C = \frac{\beta}{\beta + 1} I_E \approx 27.9mA \tag{32}$$

and to sanity check if the current is possible the voltage across the collector and emitter must be above 0.3V

$$V_C = Vcc - I_C R49 = -0.074V V_{CE} = V_C - V_E = 0.926V \tag{33}$$

This shows that the unity gain buffer can drive this configuration.
The small signal parameters becomes:

$$r_e \approx \frac{V_T}{I_E} = \frac{25mV}{28mA} = 0.893\Omega r_\pi = \beta r_e \approx 290\Omega \tag{34}$$

Output impedance, when looking into the emitter. The sources becomes AC ground, this means that the output impedance becomes

$$R_{out} \approx r_e || 500\Omega \approx r_e \tag{35}$$

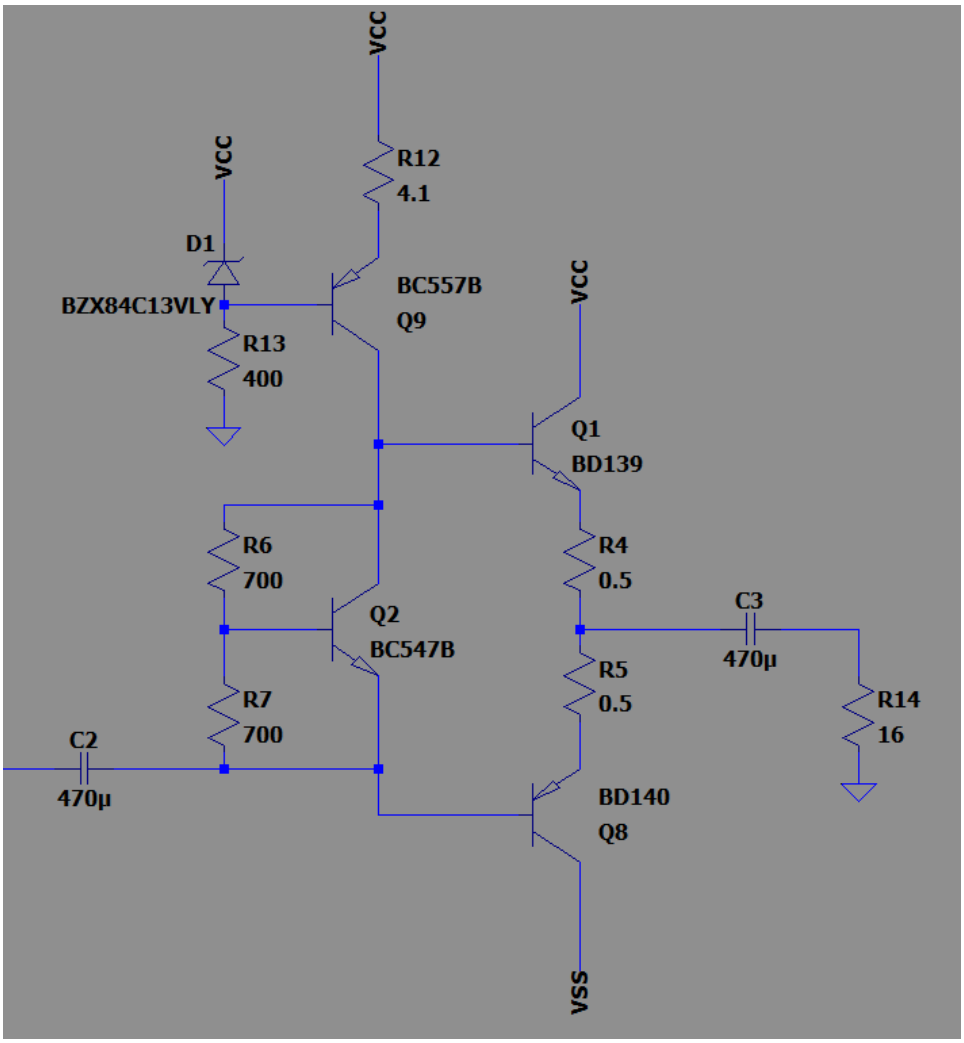

Figure 3: Output stage

5 Output Stage

The output stage consists mainly of circuitry to handle the final power amplification of the amplification, the purpose is to gain the currents and not the voltage signal. Because this is a Class AB, this means that two output transistors are driving each half of the signal cycle, however to change this from class B to AB, it requires transistor biasing, so that cross distortion is avoided.