AARHUS UNIVERSITY

EIC

Integrerede kredsløb

IC Project - class AB Amplifier

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1 introduction

The purpose of this project is to design and implement a Class AB audio power Amplifier, with some general requirements.
From the provided requirements of the project, the below states specifications are:

- **Output power** - This specification is a free choice and will be expanded later

- **Input Resistance** - $>= 10k\Omega$

- **Output Resistance** - $< 5\Omega$

- **Bandwidth** - bandwidth is specified to be in the human hearing range 20Hz - 20KHz

- **Design Structure** - must be based on a three stage topology, differential pre-amp, voltage amp stage and power amp stage.

From these given, overall requirements, our derived specifications are:

- **Output power** - $P_{out} = 200mW$

- **load size** - Giver the output power, the chosen load size is $R_{load} = 16\Omega$

- **Supply contrains** - given power requirements and load size, the supply rails of the Amplifier system is $\pm 15V$

From our on own requirements, it is possible to derive some other specifications about the system. The output voltage/current RMS

$$V_{outRMS} = \sqrt{P_{out} \cdot R_{load}} \tag{1}$$

$$I_{outRMS} = \sqrt{\frac{P_{out}}{R_{load}}} \tag{2}$$

We assume an input signal of $V_{inRMS} = 20mV$, this gives an overall gain of

$$\frac{V_{out}}{V_{in}} \approx 126 \tag{3}$$

To limit the Amplifier to the human hearing range, an lowpass filter is added to limit frequency content above 20KHz

$$f_C = 20KHz \tag{4}$$

$$C = 470\mu F \tag{5}$$

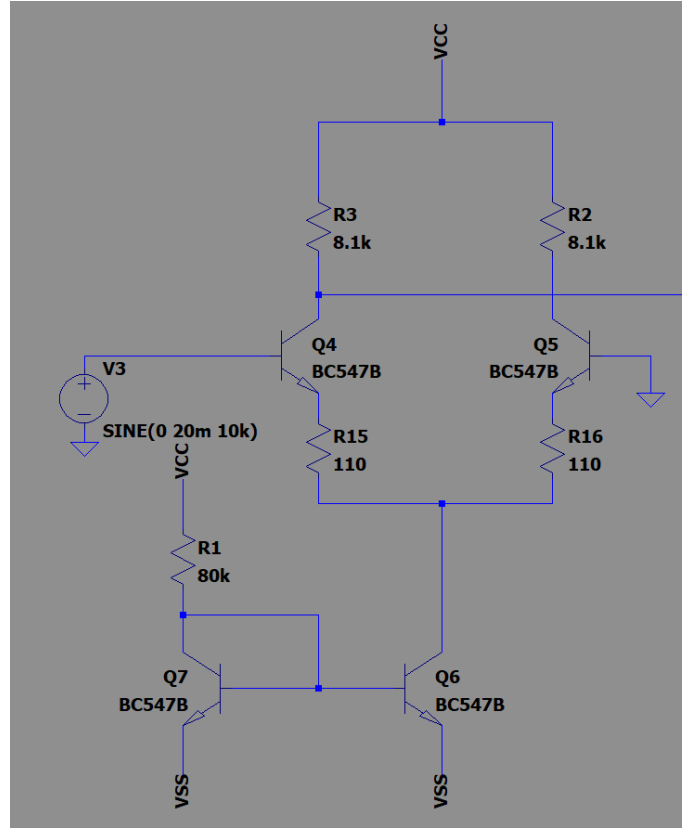$$X_C = \frac{1}{2\pi f \cdot C} = 0.017\Omega \tag{6}$$

2 Input stage

The first part of the amplifier is the input stage, this specific implementation is build around a pair of NPN transistors. This particular implementation includes a tail current source, more specifcally a current mirror build as a sink.

2.1 topology

2.1.1 differential pair

Q4 and Q5 is an NPN differential pair, with R3 and R2 as collector loads and R15 and R16 as emitter degeneration resistors. This create a single-ended output differential amplifier. The emitter resistances are included to negate the temperature dependence of BJT's and to make the transistor have a more linear behavior. This however changes how the transistors transconductance is calculated from $gm = \frac{I_C}{V_T}$ to $gm \approx \frac{1}{R_E}$, if and only if $gmR_E \gg 1$.

DC analysis
It is assumed that the BC547 has an beta factor of $\beta = 325$ and we aim for a diff amp gain of roughly $A_{diff} \approx 42$. The current sink in bottom tries to draw 4mA of current, thus $I_{Ecm} = 2mA$ must run in each branch of the Amplifier. The collector resistance then becomes

$$V_{Ccm} = V_{CC} - R_{Ccm} \cdot I_{Ecm}\alpha \Rightarrow R_{Ccm} = \frac{V_{CC} - V_{Ccm}}{I_{Ecm}\alpha} = 8.175k\Omega \tag{7}$$

AC analysis For AC analysis, the intrinsic emitter resistance is $r_e = \frac{V_T}{2mA} = 12.5\Omega$ and the external emitter resistance is $R_E = 110\Omega$ this yields a total emitter resistance of $r_{etot} = 12.5\Omega + 110\Omega = 122.5\Omega$. Thus changes to temperature only affects the term with V_T, which is $\approx \pm 2mV/C$

The goal here is to relate the differential input voltage V_d to the output voltage V_o, by elimintating the internal transistor current i_b, this will yield the gain. Since the desired gain for this Amplifier is chosen, we can use this to find the emitter resistance, which stated earlier is $R_E = 110\Omega$.

Since the other input of the differential amplifier is grounded, the differential voltage for Q4 becomes:

$$\frac{v_d}{2} = i_b r_\pi + i_e R_E \tag{8}$$

$$r_\pi = \beta r_e \tag{9}$$

$$i_e = (\beta + 1)i_b \tag{10}$$

$$\Downarrow v_d = 2i_b(\beta r_e + (\beta + 1)R_E) \tag{11}$$

And the common mode voltage then becomes:

$$v_{o1cm} = -\beta \cdot i_{bcm} \cdot R_{Ccm} \tag{12}$$

These two defines the differential gain:

$$A_{diff} = \frac{v_{o1cm}}{v_d} = -\frac{\beta R_C}{2(\beta r_e + (\beta + 1)R_E)} \tag{13}$$

Since the gain has already been chosen in the design stage, as mentioned ealier, $A_{diff} \approx 42$. The emitter resistance can be calculated, by solving for R_E:

$$A_{diff} \rightarrow R_E \approx 109.524\Omega \tag{14}$$

It should be noted that the expression for the differential gain gets rather lengthy when expanded, thus for gains much larger than $\beta \gg 1$, the 1 term in $(\beta + 1)$, can safely be ignored. This factors out β in both numerator and denominator:

$$2(\beta r_e + (\beta + 1)R_E) \Rightarrow \approx \beta(r_e + R_E) \tag{15}$$

$$A_{diff} \approx -\frac{R_C}{2(r_e + R_E)} \tag{16}$$

2.2   Current Sink

The pupose of the current mirror is to supply, or in this case "sink" the required current for the differential Amplifier, this means that it should be specified to draw the sum of the currents leaving both branches of the diff amp. thus the equations becomes:

$$I_{CQ6} = I_{EEcm} = 4mA \tag{17}$$

$$\tag{18}$$

Because it is a BC547 again, the same $\beta = 325$ is assumed, this means that current entering the base of Q6.

$$I_{BQ6} = \frac{I_{CQ6}}{\beta} \approx 12\mu A \tag{19}$$

$$\tag{20}$$

Since the current mirror is comprised to two NPN transistors, the current drawn should be the sum of the collector current I_{CQ5} and 2 base currents.
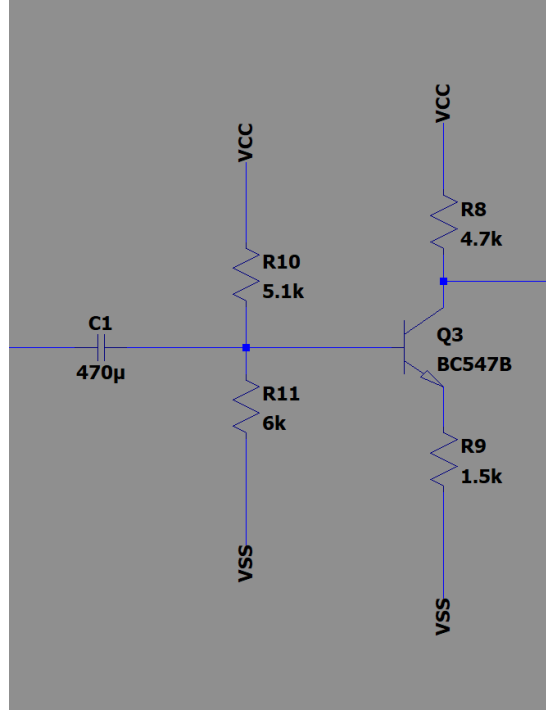
$$I_{RCQ5} = 2I_{BQ6} + I_{CQ5} = 4.025mA \tag{21}$$

Therefore the resistance to define the reference current becomes:

$$R_{ref} = \frac{V_{CC} - V_{EE}}{I_{RCQ5}} \approx 7.5k\Omega \tag{22}$$

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3 Voltage Amplification Stage

Following the differential amplifier is a Voltage amplification stage. The purpose of this circuit is to gain the signal.

The topology is a common-emitter amplifier.R10 and R11 is setting the bias point of the stage

$$V_{bQ3} = V_{SS} + \frac{R_{11}}{R_{10} + R_{11}}(V_{CC} - V_{SS}) \approx 1.22V \tag{23}$$

The Emitter of Q3 will then sit a diode drop below:

$$V_{Eq3} = V_{bQ3} - 0.7V \tag{24}$$

And the emitter current becomes:

$$I_{Eq3} = \frac{V_{Eq3} - V_{SS}}{R_9} = 10.4mA \tag{25}$$

Aiming for a "symmetric swing" around the quiescent collector voltage, meaning that we place the collector voltage at halfway between out supply rail and a lower limits, which is set by out NPN transistor. This lower is critical, cause it ensures that the transistor does not hit saturation, so V_{CE} at the lowest potential should still keep the transistor in the active region. We can then set it as:

$$V_{Cq} = \frac{V_{CC+0.82V}}{2} = 7.92V \tag{26}$$

the collector resistances then becomes:

$$R_C = \frac{V_{CC} - V_{Cq}}{I_C} \tag{27}$$