NURSULTAN KABYLKAS

RESEARCHER & DESIGNER

PROFILE

Looking for an engineering/research internship position to support projects across Nvidia using my academic skills and experience.

CONTACT

Mobile	+1 (831) 435 8367
Email	nkabylka@ucsc.edu

LINKS

Website	kabylkas.github.io
Blog	kabylkas.github.io/blog

PERSONAL

Birthday	Jan 19, 1990
Relationship	Married
Languages	English, Russian, Kazakh, Turkish

WORK

2019 — **Verification Research Internship**
Esperanto Technologies, Mountain View, CA, USA
(1) Inserted "fuzzing" logic into the RTL implementation of an out-of-order core for verification purposes (my research). (2) Also made an analysis of effectiveness of different random instruction generators.

2018 — **Performance Modeling Internship**
Esperanto Technologies, Mountain View, CA, USA
Maintained and added features to a thousand-core cycle-accurate C++ architectural simulator. Studied trade-offs and explored design space.

2016-__ — **Research Assistant**
MicroArchitecture Santa Cruz (MASC) Group, Santa Cruz, CA, USA
Research topic: currently trying to increase verification coverage without writing/generating additional verification code.

EDUCATION

2016-__ — **PhD Student, Computer Engineering**
University of California Santa Cruz, Santa Cruz, CA, USA
Related courses: Computer Architecture, Digital VLSI design, VLSI SoC Design, Machine Learning.

2008-13 — **Bachelor of Science, Computer Engineering Tech**
Rochester Institute of Technology, Rochester, NY, USA
GPA: 3.74/4.00 (Major GPA: 3.81/4.00)
Related courses: Microcontrollers, Embedded System Design, Principles of Design Automation, Operating Systems, C++ Programming, Java Programming, Circuit Theory, Advanced Electronics.

PROGRAMMING

- C++
- Python
- VHDL
- Verilog
- Tensorflow
- Reading Assembly (RISC-V, MIPS, etc.)

TOOLS

- Xilinx *Vivado* Design Flow
- Magic (Open-source VLSI layout tool)
- Altera *Quartus II* Design Flow
- XCircuit/Netgen/NgSpice
- Synopsys VCS
- Verilator

FUN PROJECTS

1) ECC for OpenRAM
OpenRAM is an open-source memory compiler. I am implementing the Error Correcting Codes.

2) Some course RTL projects: A Simple Processor, Direct Memory Access Controller (DMAC), Hardware Accelerator for Trigonometric Calculations
These were implemented in VHDL using Altera's Design Flow and ran on Cyclone II FPGA.

3) Rap Machine
Machine Learning/Image Recognition. Implementation of Machine Learning seq-to-seq model to generate rap lyrics based on the provided image.