(4) $t = \bar{c}\bar{d} + c\bar{d} =$

$= \underline{\bar{d}}$

ab/cd	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	x	x	x	x
10	1	0	x	x

zatem będzie to wyprowadzone w Verilogu

```
module zad7 ( input [3:0] i , output [3:0] o);
    logic a,b,c,d;
    assign a = i[3];
    assign b = i[2];
    assign c = i[1];
    assign d = i[0];
    assign o[3] = !a & !b & !c;
    assign o[2] = (b & !c) | (!a & !b & c);
    assign o[1] = c;
    assign o[0] = !d;
endmodule
```