4:1 Multiplexer

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity multiplexer_4_1 is
     port(
          din : in STD_LOGIC_VECTOR(3 downto 0);
          sel : in STD_LOGIC_VECTOR(1 downto 0);
          dout : out STD_LOGIC
          );
end multiplexer_4_1;

architecture multiplexer4_1_arc of multiplexer_4_1 is
begin

    with sel select
    dout <= din(0) when "00",
            din(1) when "01",
            din(2) when "10",
            din(3) when others;

end multiplexer4_1_arc;
```