Binary to Gray

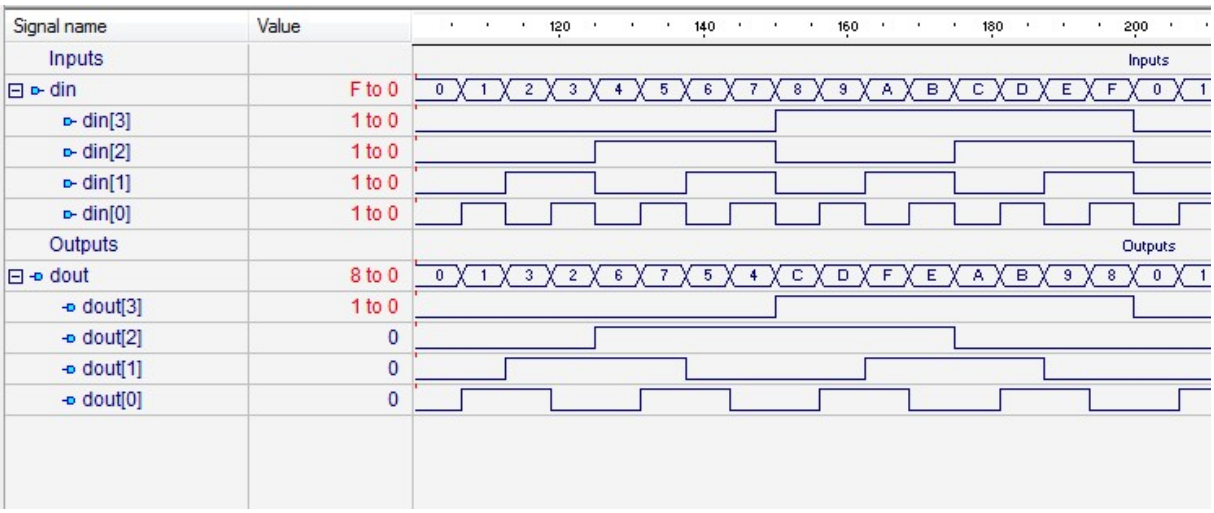
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity binary_to_gray is
    port(
        din : in STD_LOGIC_VECTOR(3 downto 0);
        dout : out STD_LOGIC_VECTOR(3 downto 0)
        );
end binary_to_gray;

architecture binary_to_gray_arc of binary_to_gray is
begin

   dout(3) <= din(3);
   dout(2) <= din(3) xor din(2);
   dout(1) <= din(2) xor din(1);
   dout(0) <= din(1) xor din(0);

end binary_to_gray_arc;
```



Gray to Binary

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Gray_to_Binary is
    port(
        din : in STD_LOGIC_VECTOR(3 downto 0);
        dout : out STD_LOGIC_VECTOR(3 downto 0)
        );
end Gray_to_Binary;

architecture Gray_to_Binary_arc of Gray_to_Binary is
begin

   dout(3) <= din(3);
   dout(2) <= din(3) xor din(2);
   dout(1) <= din(3) xor din(2) xor din(1);
   dout(0) <= din(3) xor din(2) xor din(1) xor din(0);

end Gray_to_Binary_arc;
```