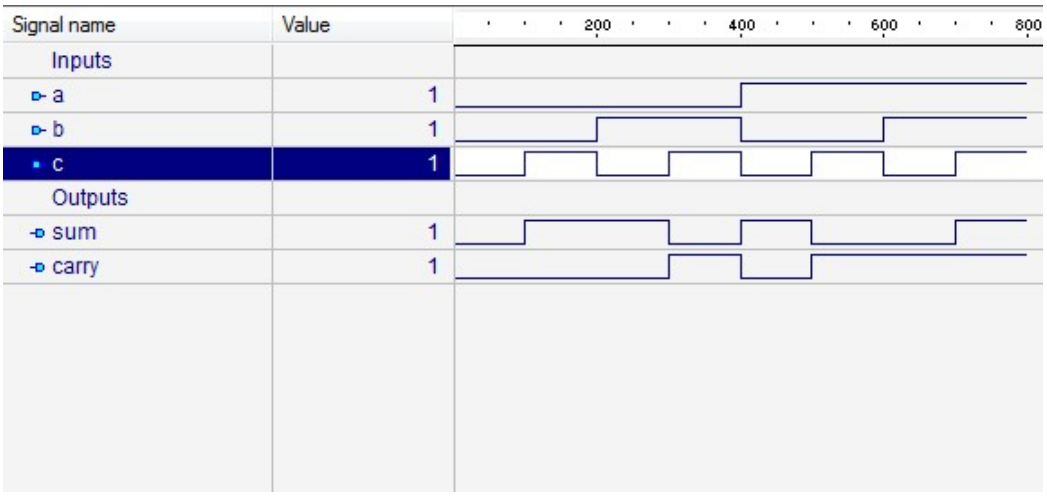
FULL ADDER

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Full_Adder_Design is
     port(
          a : in STD_LOGIC;
          b : in STD_LOGIC;
          c : in STD_LOGIC;
          sum : out STD_LOGIC;
          carry : out STD_LOGIC
          );
end Full_Adder_Design;

architecture Full_Adder_Design_arc of Full_Adder_Design is
begin

    sum <= a xor b xor c;
    carry <= (a and b) or
             (b and c) or
             (c and a);
end Full_Adder_Design_arc;
```



FULL SUBTRACTOR

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity full_subtractor is
     port(
          a : in STD_LOGIC;
          b : in STD_LOGIC;
          c : in STD_LOGIC;
          difference : out STD_LOGIC;
          borrow : out STD_LOGIC
          );
end full_subtractor;

architecture full_subtractor_arc of full_subtractor is
begin

    difference <= a xor b xor c;
    borrow <= ((not a) and b) or
              (b and c) or
              (c and (not a));

end full_subtractor_arc;
```