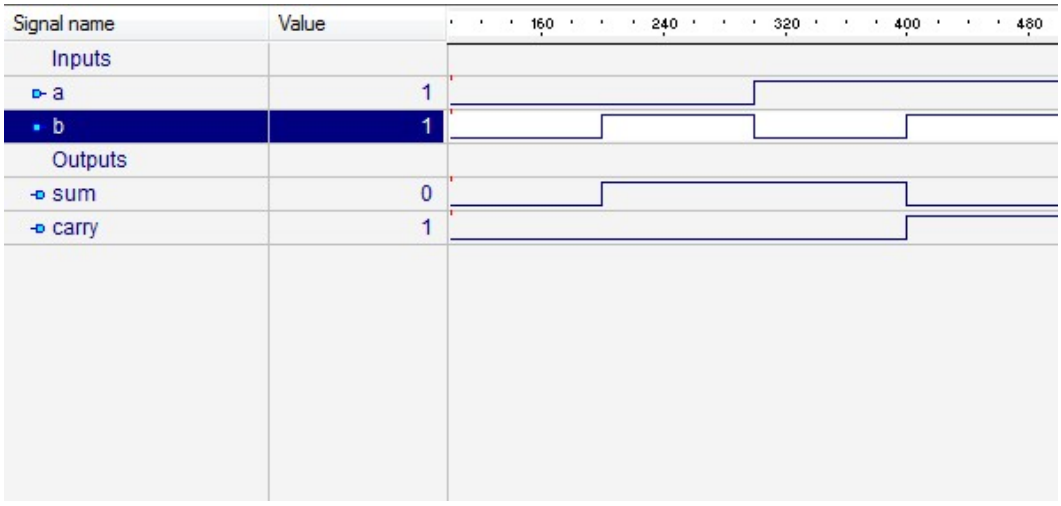
HALF ADDER

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity Half_Adder is
     port(
          a : in STD_LOGIC;
          b : in STD_LOGIC;
          sum : out STD_LOGIC;
          carry : out STD_LOGIC
          );
end Half_Adder;

architecture Half_Adder_arc of Half_Adder is
begin

    sum <= a xor b;
    carry <= a and b;
end Half_Adder_arc;
```



HALF SUBTRACTOR

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity half_subtractor is
    port(
        a : in STD_LOGIC;
        b : in STD_LOGIC;
        diff : out STD_LOGIC;
        borrow : out STD_LOGIC
        );
end half_subtractor;

architecture half_subtractor_arc of half_subtractor is
begin

   diff <= a xor b;
   borrow <= (not a) and b;

end half_subtractor_arc;
```