Johnny Li

COP4600

HW 3.1

2. It is an accident that the base and limit registers contain the same value. Since the program is just loaded at address 16,384, the base register would also be 16,384, could have been loaded anywhere. Since the program contains 16,384 bytes, the limit register would be 16,384, could have been any length.

3. Reading 32-bit, or 4 bytes = 4 nsec -> 1 byte = 1 nsec 4 GB = 4.29\*109 bytes

Writing = 2 nsec -> 2 nsec/ byte compacted -> 500,000,000 bytes/sec

Thus, 4.29\*109 bytes/500,000,000 bytes/sec = 859 msec

4. First fit: 20 MB, 10 MB, 18 MB

Best fit: 12 MB, 10 MB, 9MB

Worst fit: 20 MB, 18 MB, 15 MB

Next fit: 20 MB, 18MB, 9 MB

6. 4-KB page size: (4, 3616), (8, 0), (14,2656)

8-KB page size: (2, 3616), (4, 0), and (7, 2656)

8. They inserted an MMU between the processor and the bus. All the physical addresses had to go into the MMU as virtual addresses which then mapped them onto physical addresses, output to the bus

11. a) To ensure a TLB miss for every access to an element of X, M has to be at least 4096, where any value of N will do.

b) To ensure a TLB miss for every access to an element of X, M has to be at least 4,096. However, now N has to be greater than 64K to thrash the TLB rather than be any value as in part a.

15. Machine = 48-bit virtual addresses and 32-bit physical addresses

a) pages = 4 KBOne entry for per page -> 2^(24) entries

Page number field = 48−12 = 36 bits

b) There is 100% hit in the TLB for instruction address. A 4-KB page contains 1,024 integers, thus there will be one TLB miss and an extra memory access.

22. Process with 1024 pages with 5 nsec to read.

TLB holds 32 pairs with 1 nsec to lookup.

Time = 1h+5(1−h) -> 2 nsec = 1h+5(1-h) -> h= 0.75

23. For associated memory device to implemented in hardware there must be a set of comparators for each bit in the register for the key to be searched for. More register would mean more comparators which would get expensive in a linear fashion.

24. A machine has 48-bit virtual addresses and 32-bit physical addresses. Pages are 8 KB Number of virtual pages = 2^(48)/2^(13) = 2^(35)

27. a) The standard replacement algorithms (LRU, FIFO, clock) not be effective in handling this workload for a page allocation that is less than the sequence length because every reference will page fault unless the number of page frames is the sequence length.

b) If this program were allocated 500 page frames a better page replacement method could be a page map from 0–498 to fixed frames and vary only one frame.

29. Consider the page sequence of Fig. 3-15(b). Suppose that the R bits for the pages B through A are 11011011, respectively, then the page that second chance would remove would be the first page with a 0 bit.

31. A simple example of a page reference sequence where the first page selected for replacement will be different for the clock and LRU page replacement algorithms, assuming that a process is allocated 3=three frames, and the reference string contains page numbers from the set 0, 1, 2, 3 would:

0, 1, 2, 1, 2, 0, 3

In LRU, 3 replaces 1 and in clock, 0 replaces 1.

33. a) If a clock interrupt occurs at tick 10:

For every 10 tick, clear all set R bits and change the time value.

Page Time stamp V R M

0 6 1 0 0

1 10 1 0 0

2 10 1 0 1

b) Remove page 3 (R= 0 and M= 0) and load page 4.

Page Time stamp V R M

0 6 1 0 1

1 9 1 1 0

2 9 1 1 1

3 7 0 0 0

4 10 1 1 0

35. a) Load a 64-KB program with a seek time is 5 msec, whose rotation time is 5 msec, and whose tracks hold 1 MB. A 2-KB page size.

Transfer time ~0.0098 msec + 10 msec = 10.0098 msec \* 32 pages = 320.21 msec

b) A 4-KB page size.

Transfer time ~0.0098 msec \*2 (double) + 10 msec = 10.02 msec \* 16 pages = 160.3 msec

37. a) The conditions that the page table update for process B be delayed even though the handling of process A’s page fault will bring the shared page into memory would be if process B never access the shared page or when the page has been swapped out.

b) The potential cost of delaying the page table update is that bad page fault handling leads to more page faults.