Lab 7

Now we will implement the Jump and branch instructions

imm[31:12]				rd	0110111	LUI
imm[31:12]				rd	0010111	AUIPC
imm[20|10:1|11|19:12]				rd	1101111	JAL
imm[11:0]		rs1	000	rd	1100111	JALR
imm[12|10:5]	rs2	rs1	000	imm[4:1|11]	1100011	BEQ
imm[12|10:5]	rs2	rs1	001	imm[4:1|11]	1100011	BNE
imm[12|10:5]	rs2	rs1	100	imm[4:1|11]	1100011	BLT
imm[12|10:5]	rs2	rs1	101	imm[4:1|11]	1100011	BGE
imm[12|10:5]	rs2	rs1	110	imm[4:1|11]	1100011	BLTU
imm[12|10:5]	rs2	rs1	111	imm[4:1|11]	1100011	BGEU

Branch is known during decode stage. At this point the next instruction has been fetched. The pipeline must flush that fetched instruction and then stall till the branch is resolved (next PC is known).

The branch is resolved (next PC is known) - at the end of Execute stage. Then unstall and start fetching from branch target.

Offset is signed, must be sign extended and shifted left by 1 bit to get half word aligned target address.

Deliverables -
Demo - 50 marks
Code submission - 50 marks