Chittagong University of Engineering and Technology

Department of Electrical and Electrical Engineering

EEE 476: VLSI Technology Sessional

Experiment No. # 1
Experiment Name: Draw the Schematic of a 2 - input NAND Gate, Create a Symbol, Perform Simulation and Plot the Output Wave Forms

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Section:
Date of Experiment:
Date of Report Submission:

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ABSTRACT

This experiment introduces **Cadence Virtuoso Software** which provides an environment to simulate our Verilog codes and test whether it works as it has to. Using this we designed the schematic of a 2-input NAND gate, designed its symbol and determined its rise time, fall time using bit and pulse for four different conditions of NAND gate.We also observed the transient response of the input and output ports. A unique directory was created for the circuit design project.

KEYWORDS

2-input NAND Gate, Rise time, Fall time, Propagation delay

OBJECTIVES

1. To login in to the Cadence Server shell and start the Cadence virtuoso software
2. To create a working library
3. To draw the schematic of a 2-input NAND gate in Cadence Virtuoso Schematic Editor
4. To create a symbol view of the NAND gate from the schematic
5. To simulate the NAND gate using MMSIM Spectre
6. To determine the rise time and fall time of the output waveforms.

INTRODUCTION

This experiment introduces how to use Cadence Virtuoso Software to design a 2-input NAND Gate. It teaches us to create a library and draw the required schematic and simulate the circuit.

THEORY

A NAND gate is a universal gate capable observing the behavior of gates like OR, AND and NOT. A CMOS NAND gate consists of two series nMOS transistors and two parallel pMOS transistors.

A 2-input CMOS NAND gate consists of two series nMOS transistors and two parallel pMOS transistors.

TRUTH TABLE

A	B	Pull Down Network	Pull up Network	Output (Y)
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

PROPAGATION DELAY

For P*mos*=240 nm , N*mos*=240 nm :

A	B	t*pdr*	t*pdf*
0	0	5.96E-12	9.208E-12
0	1	8.201E-12	6.254E-12
1	0	11.97E-12	8.07E-12

Propagation delay rise time t*pdr* -
Worst case 0 0
Best case 1 0
Propagation delay fall time t*pdf* -
Worst case 0 1
Best case 0 0
Rise Time : 6.273E-12 ; **Fall Time : 6.273E-12**

PROPAGATION DELAY

For P*mos*=240 nm , N*mos*=120 nm :

A	B	t*pdr*	t*pdf*
0	0	5.224E-12	13.18E-12
0	1	7.228E-12	9.79E-12
1	0	9.259E-12	12.4E-12

Propagation delay rise time t*pdr* -
Worst case 0 0,
Best case 1 0

Propagation delay fall time t*pdf* -
Worst case 0 1
Best case 0 0
Rise Time : 6.056E-12 ; **Fall Time : 6.056E-12**

SIMULATION

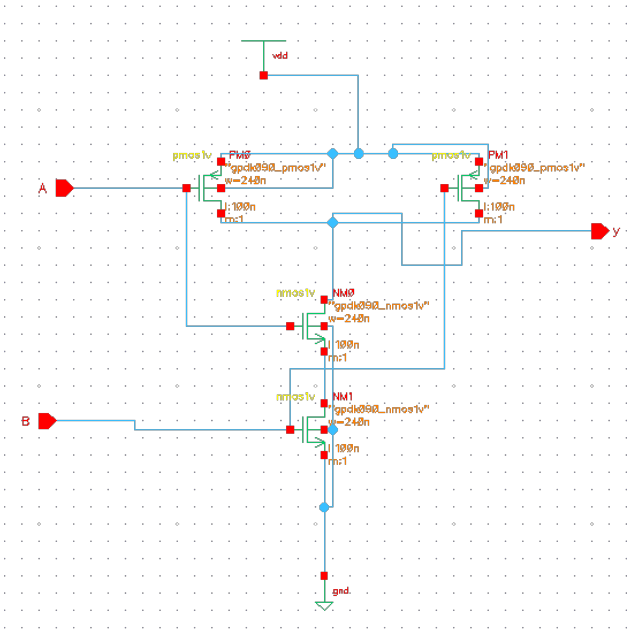

Figure 01 : Schematic Drawing for P*mos*=240 nm , N*mos*=240 nm

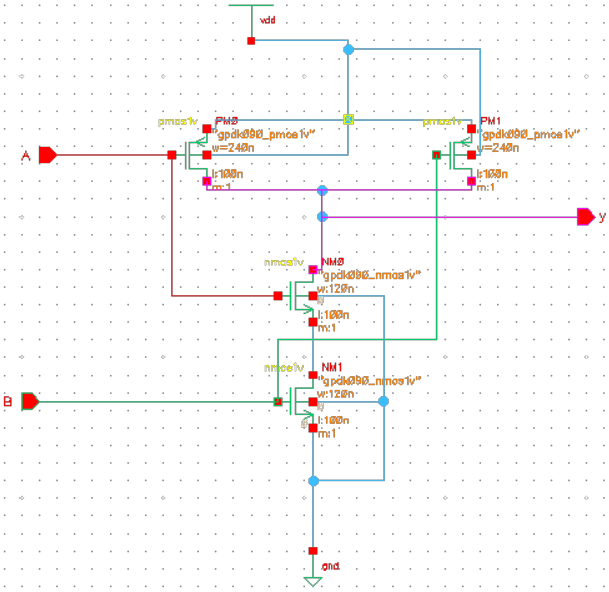

Figure 02 : Schematic Drawing for Pmos=240 nm , Nmos=120 nm

PARAMETERS

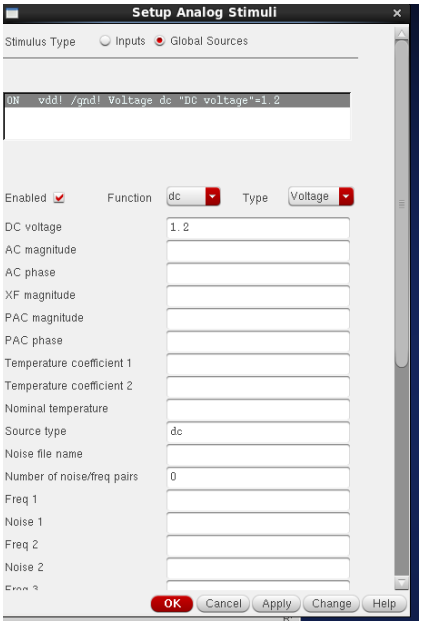

Figure 03 : Parameter selection for global source

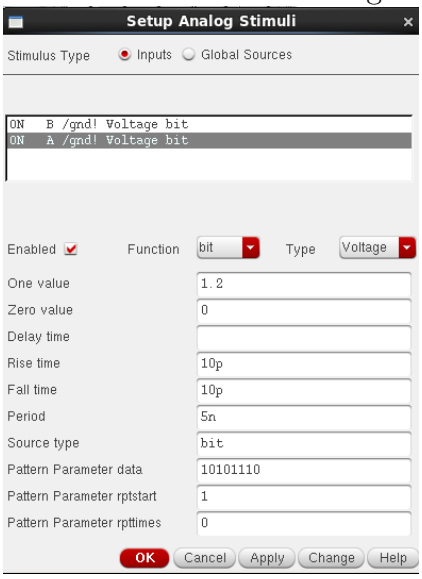

Figure 04 : Bit pattern for input pin A

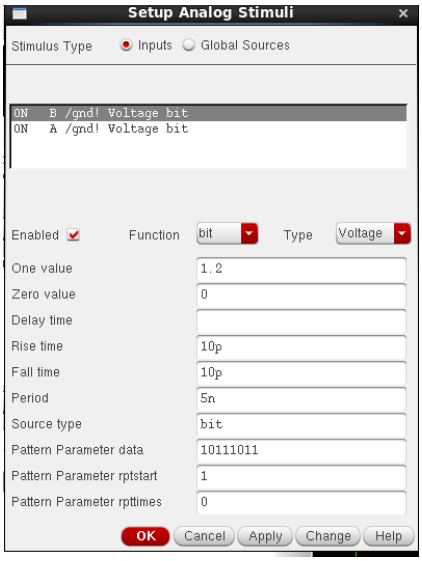

Figure 05 : Bit pattern for input pin B

SIMULATION RESULT

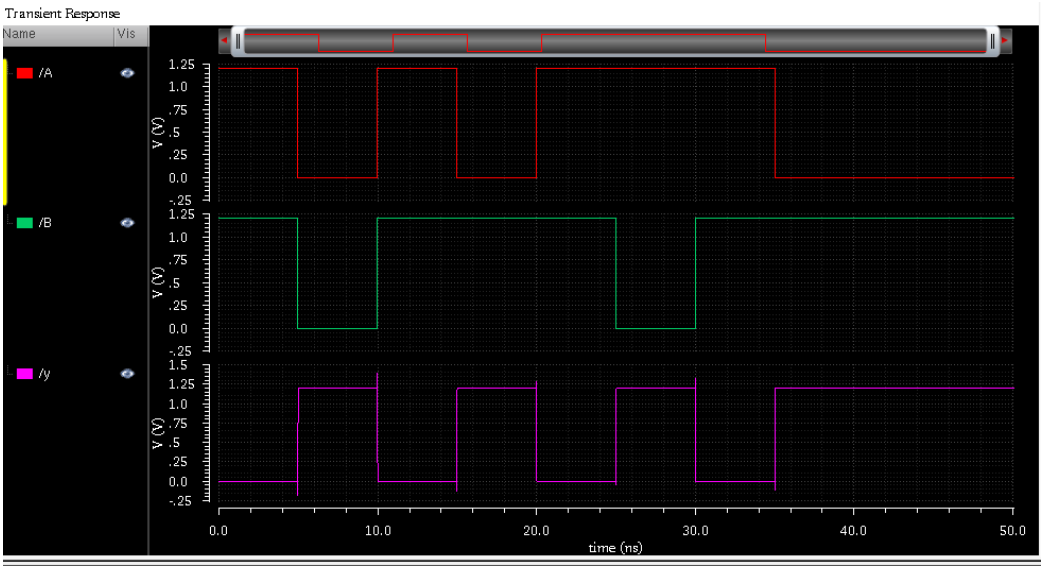

Figure 06 : Output wave forms for Pmos=240 nm , Nmos=240 nm

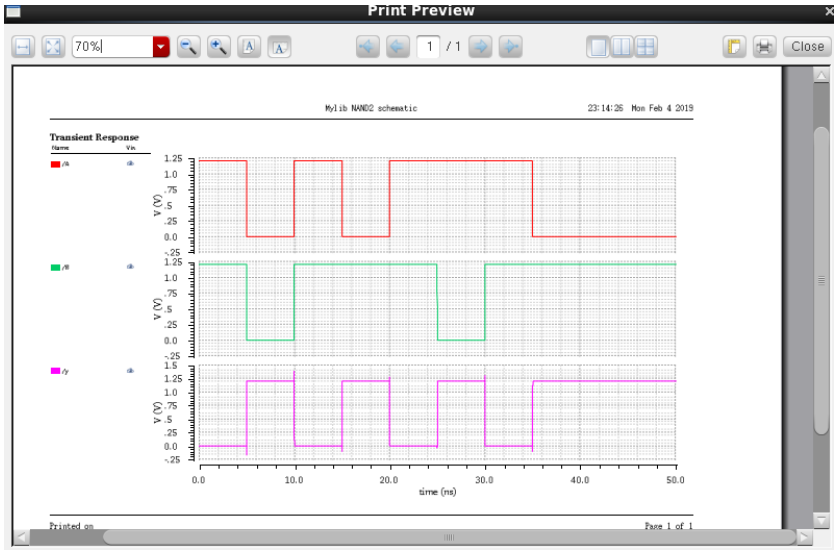

Figure 07 : Output wave forms for Pmos=240 nm , Nmos=240 nm (in Graph)

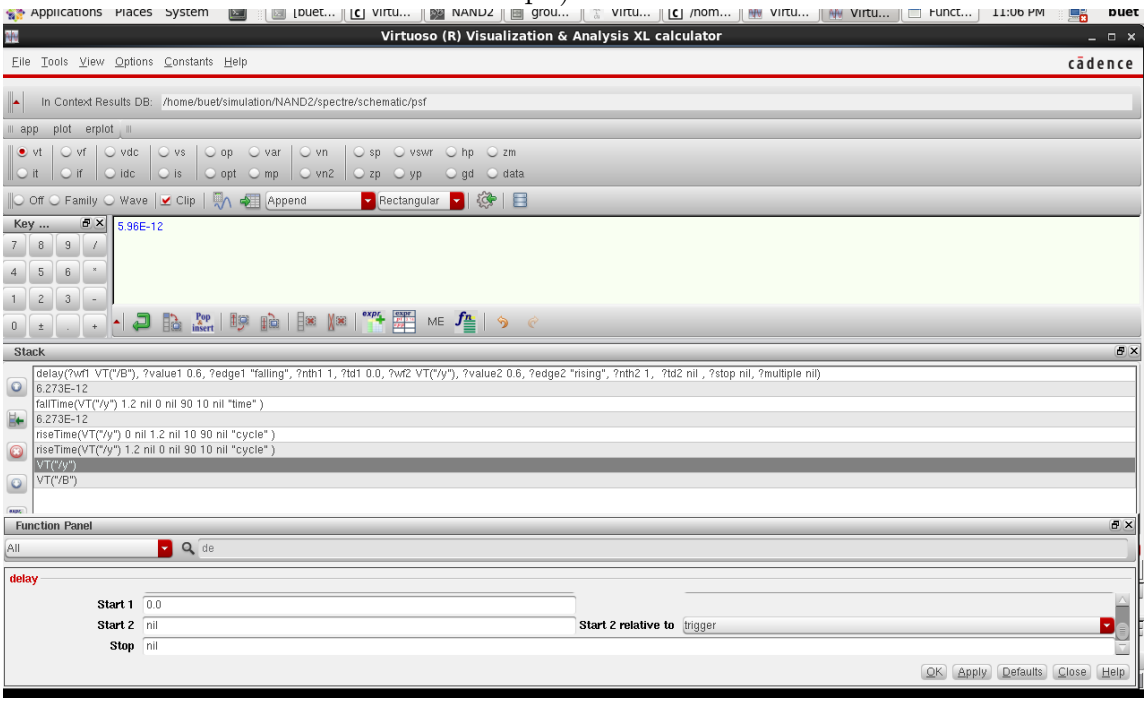

Figure 08 : Propagation delay rise time

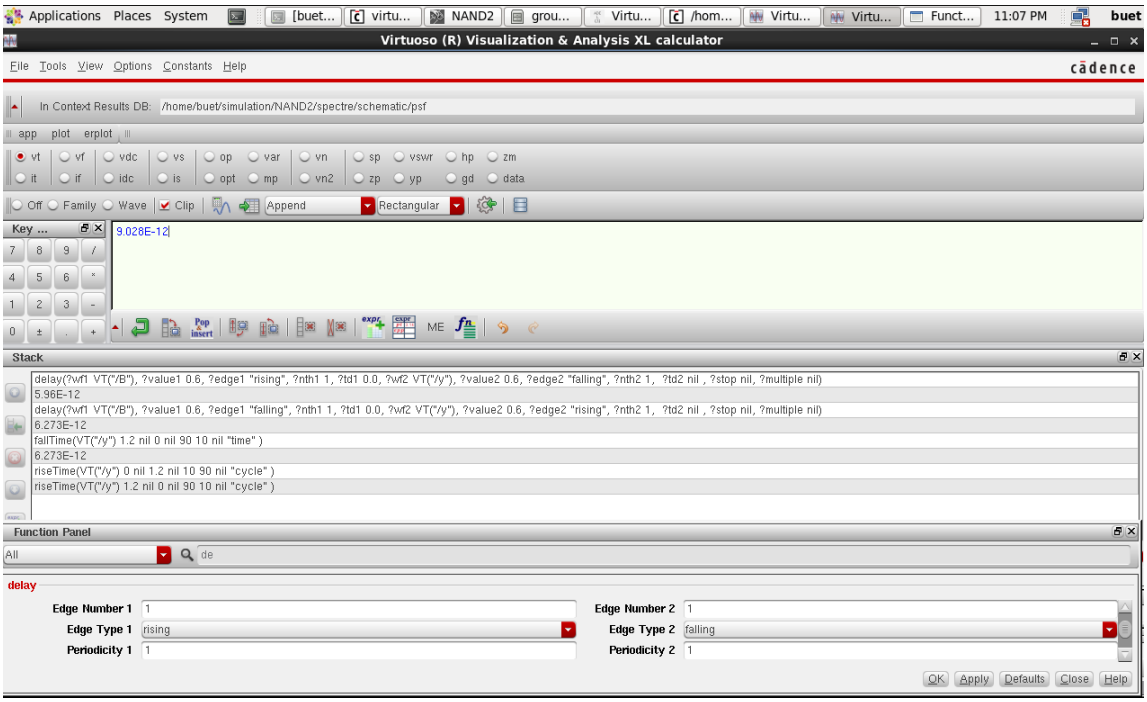

Figure 09 : Propagation delay fall time

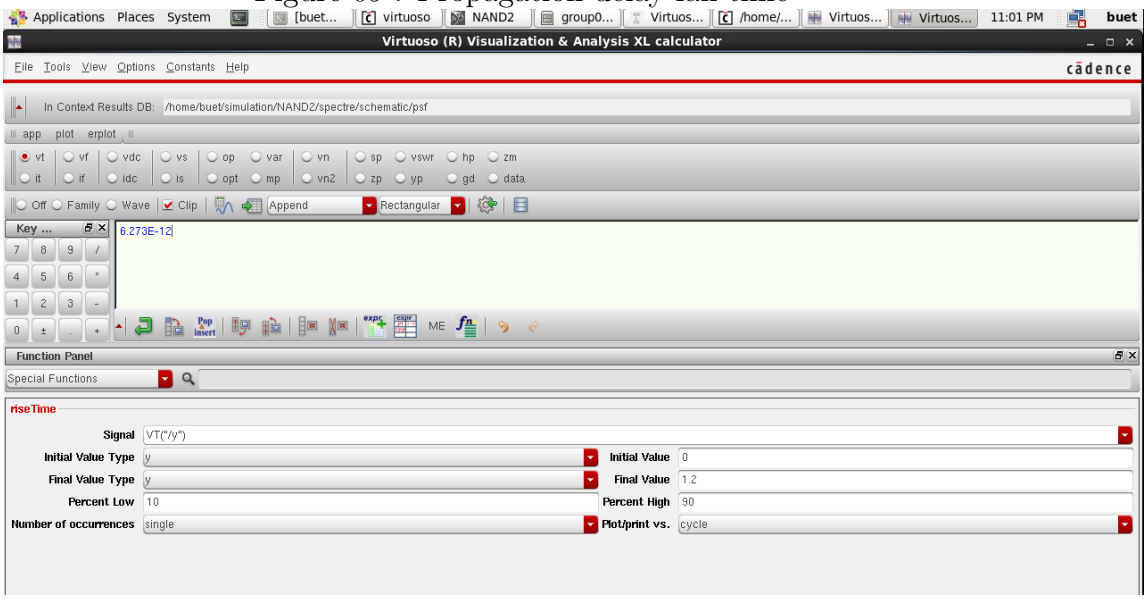

Figure 10 : Rise time

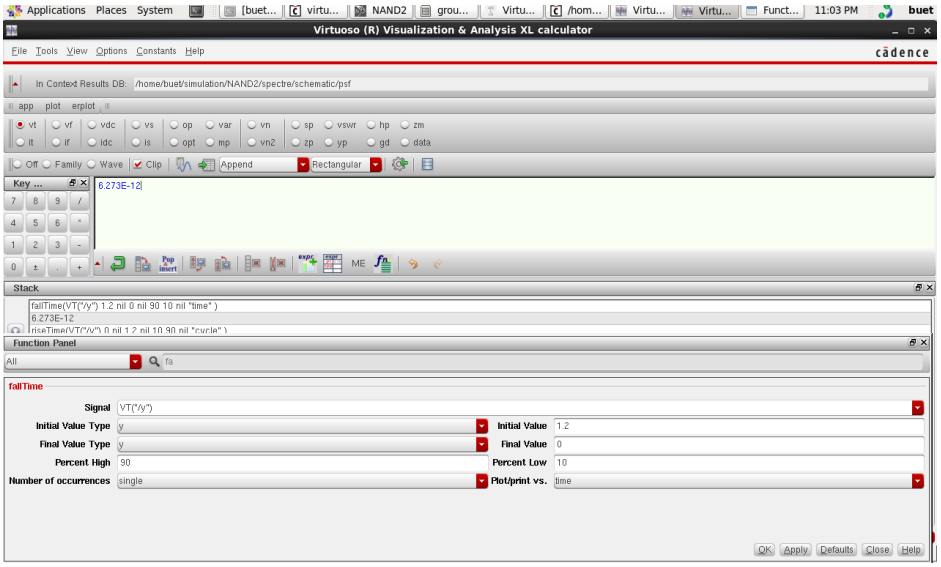

Figure 11 : Fall time

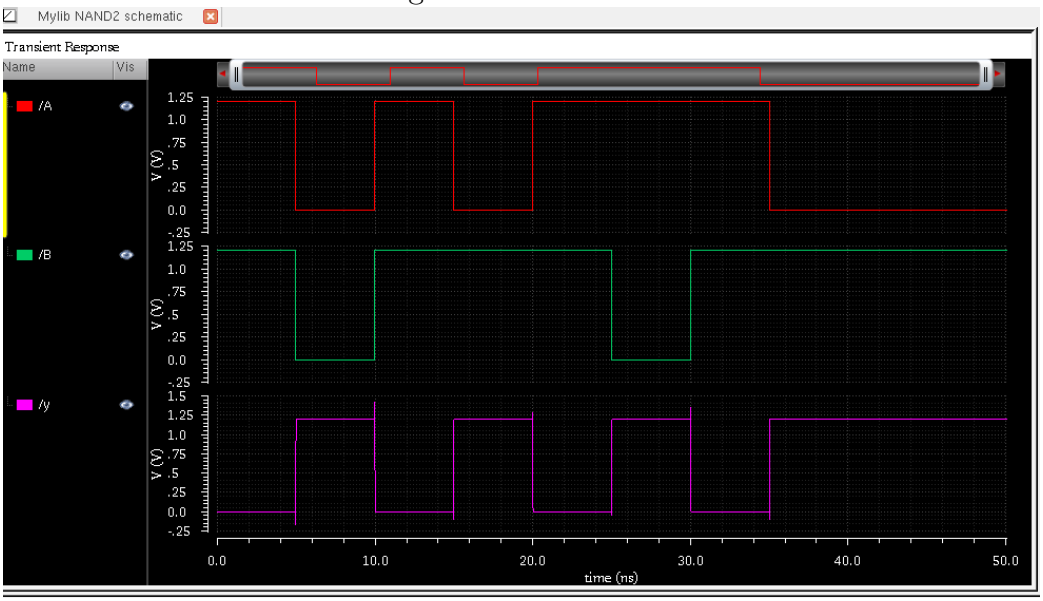

Figure 12 : Output wave forms for Pmos=240 nm , Nmos=120 nm

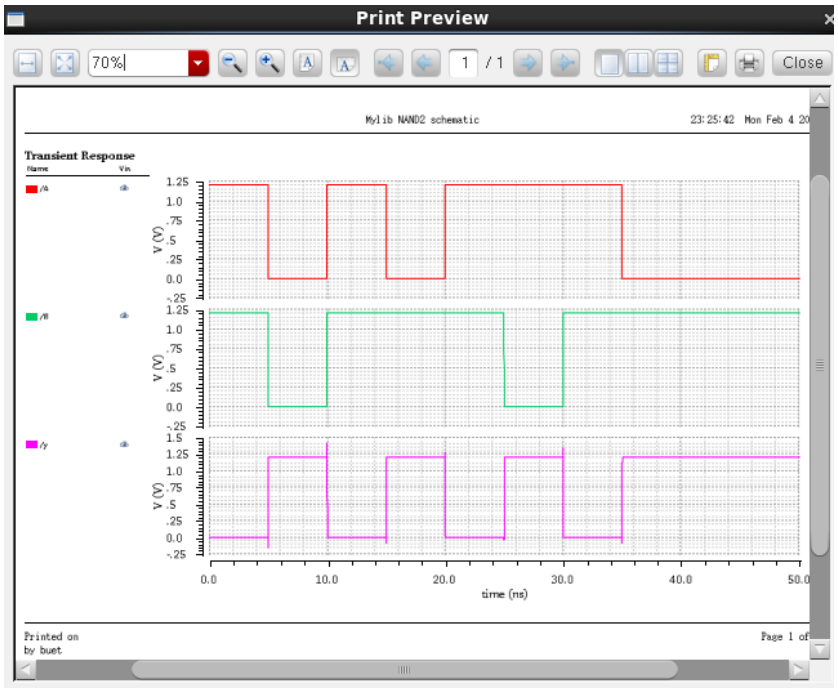

Figure 13 : Output wave forms for Pmos=240 nm , Nmos=120 nm (in Graph)

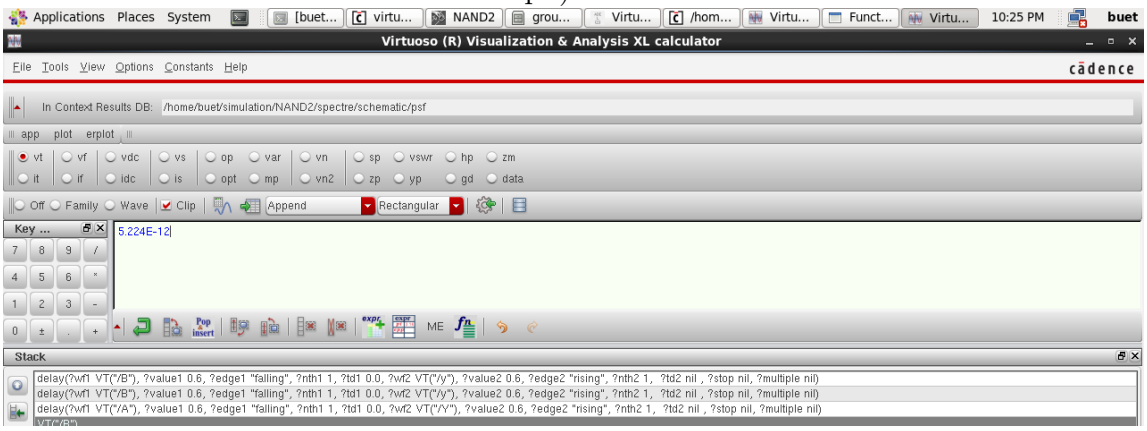

Figure 14 : Propagation delay rise time (worst case)

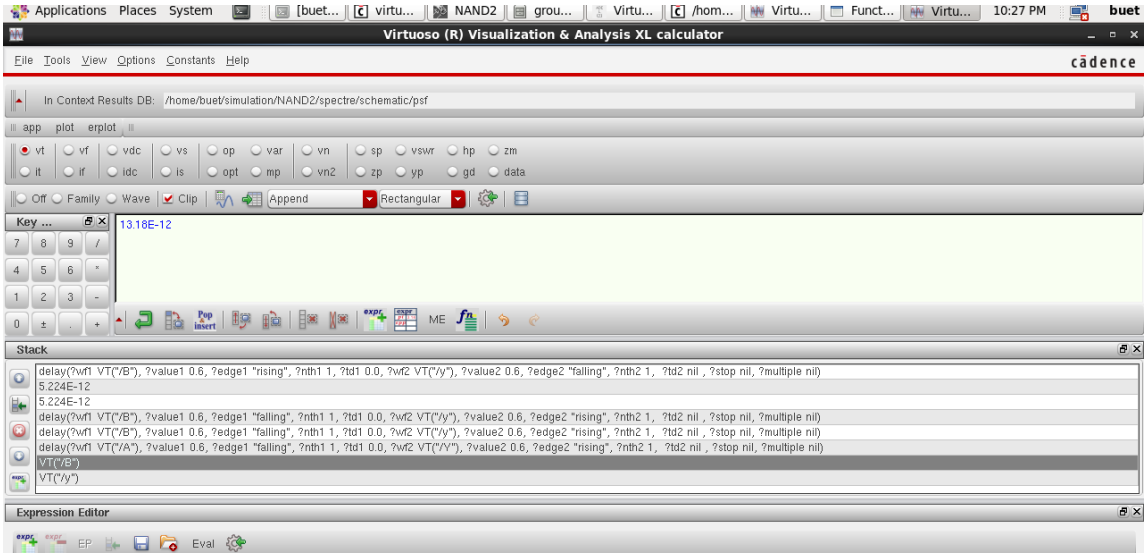

Figure 15 : Propagation delay fall time

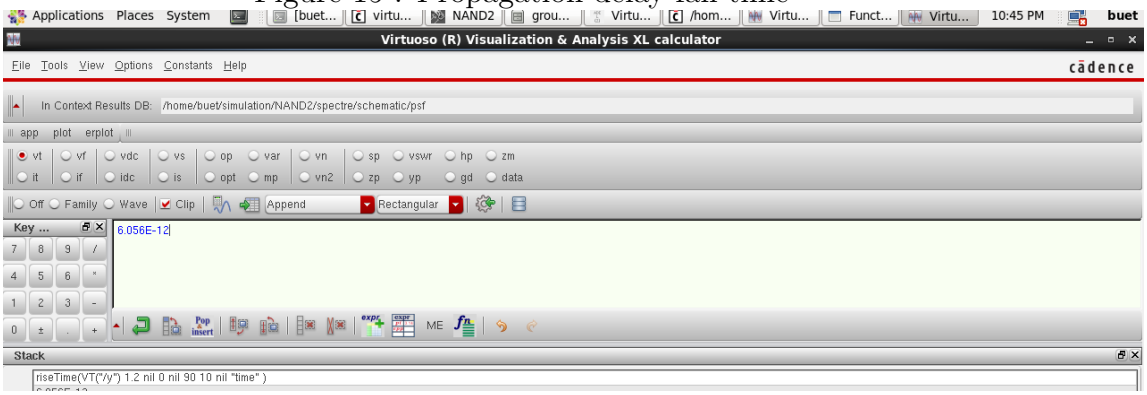

Figure 16 : Rise time

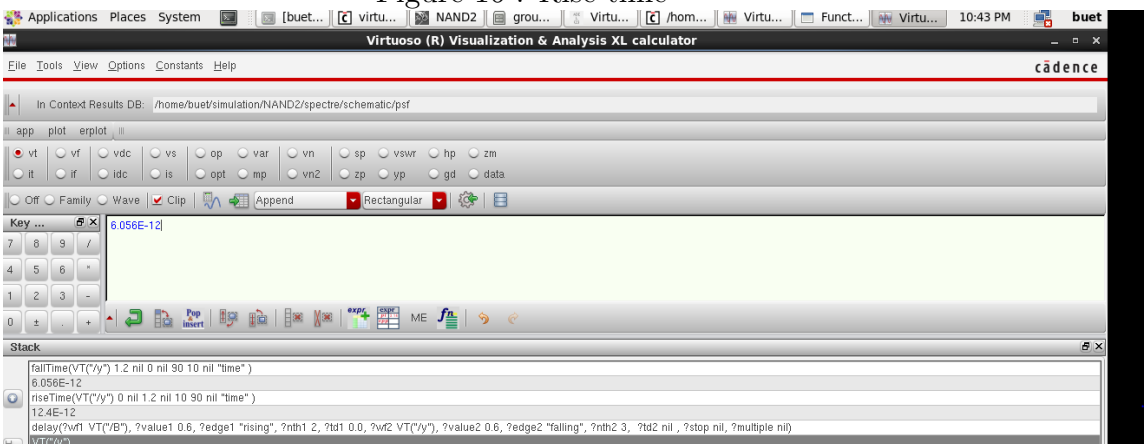

Figure 17 : Fall time

TOOLS USED

1. Cadence Virtuoso.
2. Virtual Box.

CONCLUSION

In this experiment we got familiar with Cadence Software. We designed the schematic for a 2-input NAND gate and determined the necessary parameters and waveforms. We prepared a truth table and compared the simulated result with the table.

REFERENCES

1. Lab Manual.
2. Cadence Tutorial.
3. https://www.google.com/