TE (Comp) VI 18/5/13

Advanced µp

VT-F.H.Exam. May-13-14

Con. 7352–13. **GS–9933**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Draw **neat** labelled **diagram** wherever **necessary**.
(4) Answers to **each** new questions to be started on a **fresh page**.

1. (a) Draw the block diagram of 80386 DX processor and explain each block in brief. **10**
(b) Differentiate segmentation in real mode and in protected mode. **5**
(c) Discuss the register set of 80386 processor. **5**

2. (a) What are the different types of instruction Hazards ? Explain in detail. **10**
(b) Draw and explain Pentium processor architecture. **10**

3. (a) Explain dynamic branch prediction logic of Pentium processor. **10**
(b) Explain different stages of Integer pipeline and floating point pipeline of Pentium processor. **10**

4. (a) Compare Super SPARC and Ultra SPARC processor. Draw and explain in brief the architecture of Super SPARC. **10**
(b) Explain the Itanium processor with respect to instruction format, core pipeline stages and the functionality. **10**

5. (a) Explain the Cache Organization of Pentium processor. **10**
(b) Draw and explain the state diagram of MESI transitions that occur within the Pentium's data Cache memory. **10**

6. (a) Explain EFLAGS bits of Pentium. **10**
(b) State the features of PCI bus. Draw a work station based on PCI bus and explain. **10**

7. Write a short note on (any **two**) :– **20**
(a) Layered architecture of SCSI
(b) USB
(c) VESA.

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