10/12/13 S.E. Sem - III CBSJ (I.T)
Analog and Digital Circuits

Lax5-D:\Data-96

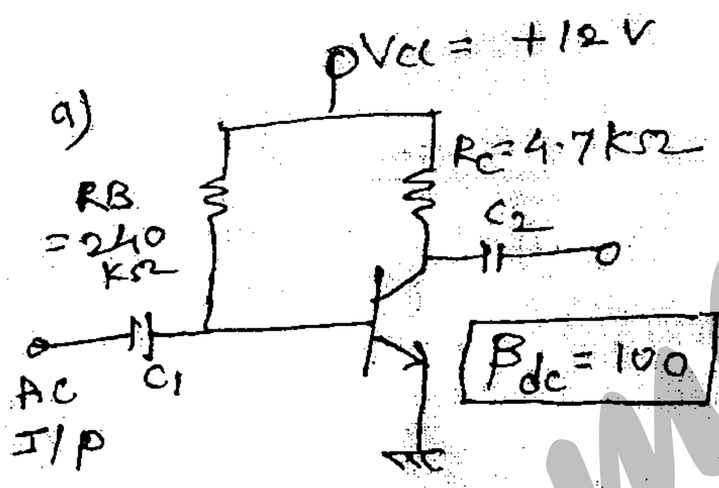
Con. 9817-13. **GX-12167**

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** questions out of **remaining** questions.
(3) Assume **suitable** data if **necessary.**

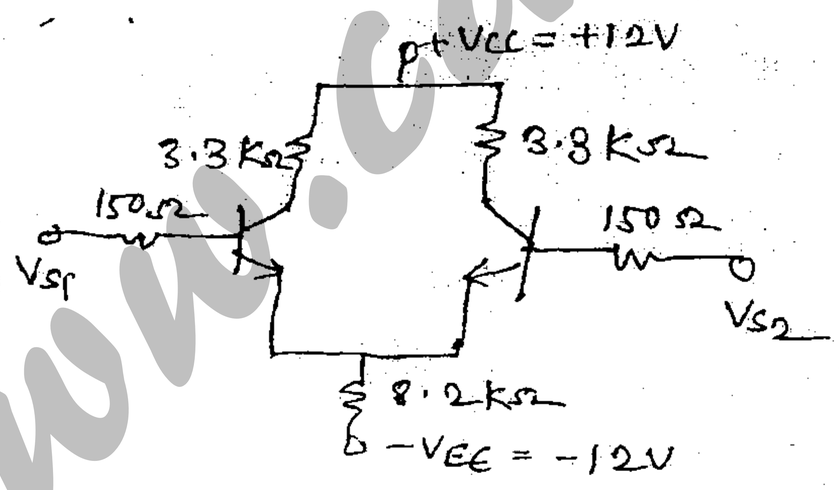
1. Solve any **four** :– **20**
   (a) Find out relations between α, β and γ as current amplification factors for CE, CB, CC configurations.
   (b) State ideal and practical characteristics of Op-Amp.
   (c) Convert following decimal mumber to Binary, Octal, Herl-equivalent and gray code.
   (i) $(306 \cdot 8)_{10}$ (ii) $(147 \cdot 8)_{10}$
   (d) Add $(57)_{10}$ and $(26)_{10}$ in BCD.
   (e) Convert S-R filp-flop to D-flip-flop.
   (f) Explain parallel input, serial output shift register.

2. (a) Determine the following for the fixed bias **8**



   (i) I_{BQ} and I_{CQ}
   (ii) V_{CEQ}
   (iii) V_B and V_C
   (iv) V_{BC}

   (b) For the differential amplifier as shown below calculate :– **8**



   (i) Operating points
   (ii) Voltage gain
   (iii) Input Impedance
   (iv) Output impedance

   (c) Design a circuit to $V_0 = 15(V_1 - V_2)$ where V_1 and V_2 are input voltages to Op-Amp. **4**

3. (a) What are different methods used to improve CMRR in differential amplifier? **8**
   (b) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 5 KHz. **8**
   (c) Explain Instrumentation amplifier using 3 Op-Amps. **4**

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4. (a) Design an astable multivibrator for an output frequency of 1KHz and duty cycle 40 %. **6**

   (b) Minimize the following expression using K-map and realize using the gates. **6**

   $$Y = \sum m(1, 2, 9, 10, 11, 15, 15)$$

   (c) Design 2 - Bit magnitude comparator using basic gates. **8**

5. (a) Implement the following function using 8 : 1 MUX **6**

   $$f(A, B, C, D) = \sum m(2, 4, 5, 7, 10, 15)$$

   (b) Implement full adder using demultiplexer. **6**

   (c) Design the divide by 7 (mod-7) asynchronous up-counter using J-K flip-flop. Also state difference between synchronous and asynchronous counter. **8**

6. (a) Explain universal shif register and its applications. **6**

   (b) Explain VHDL. **4**

   (c) What is Zener shunt regulator? Explain and derive stability factor. **4**

   (d) Realize following using only NAND gates. **6**

   $$Y = (AB + BC)\,C.$$
