Team Members

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Aim

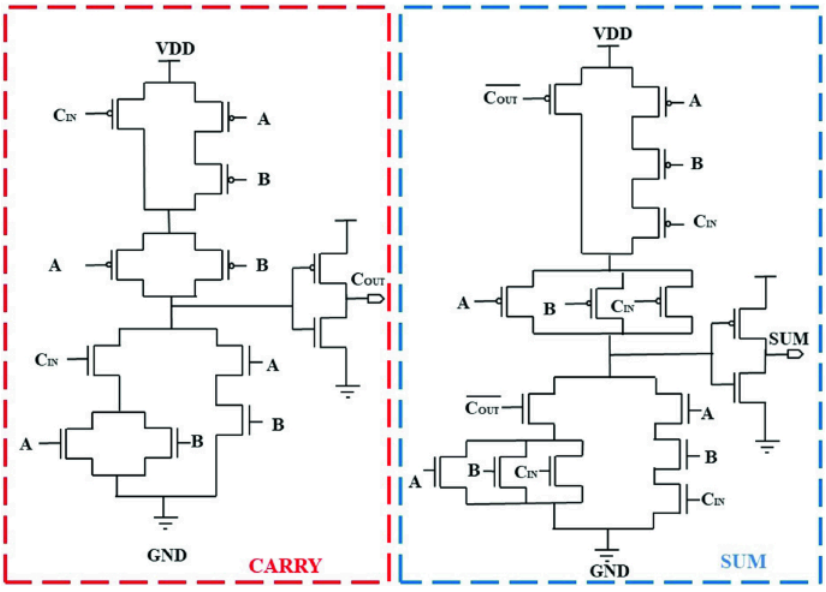
Design a 16-bit scalable, area-efficient, and low-power Ladner Fischer adder using static CMOS Technology. Evaluate the performance – including delay, power, and area through simulation. Compare the result with 16-bit RCA and use the above adder to implement a 16x16-bit multiplier.

Specifications

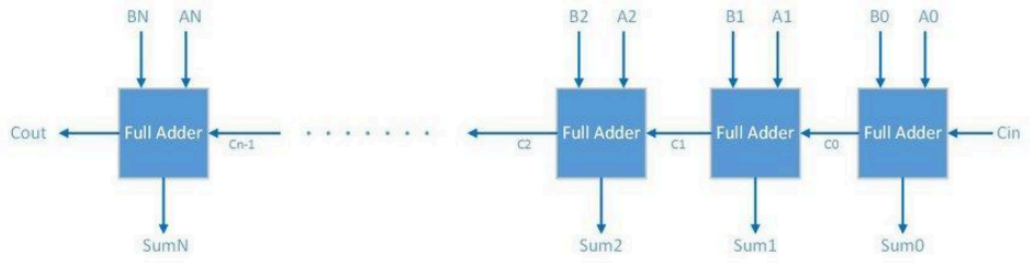
Sizing	5 : 1
Load capacitance	200 fF
Intermediate capacitance	10 fF

Ripple Carry Adder (RCA)

The Ripple carry adder is the most basic adder circuit. It is designed by cascading N full adder blocks such that the C_{out} of one stage is fed to the C_{in} of the next stage. 28T circuit was used for the full adder blocks. 16 full adder blocks were used to design the 16-bit RCA.



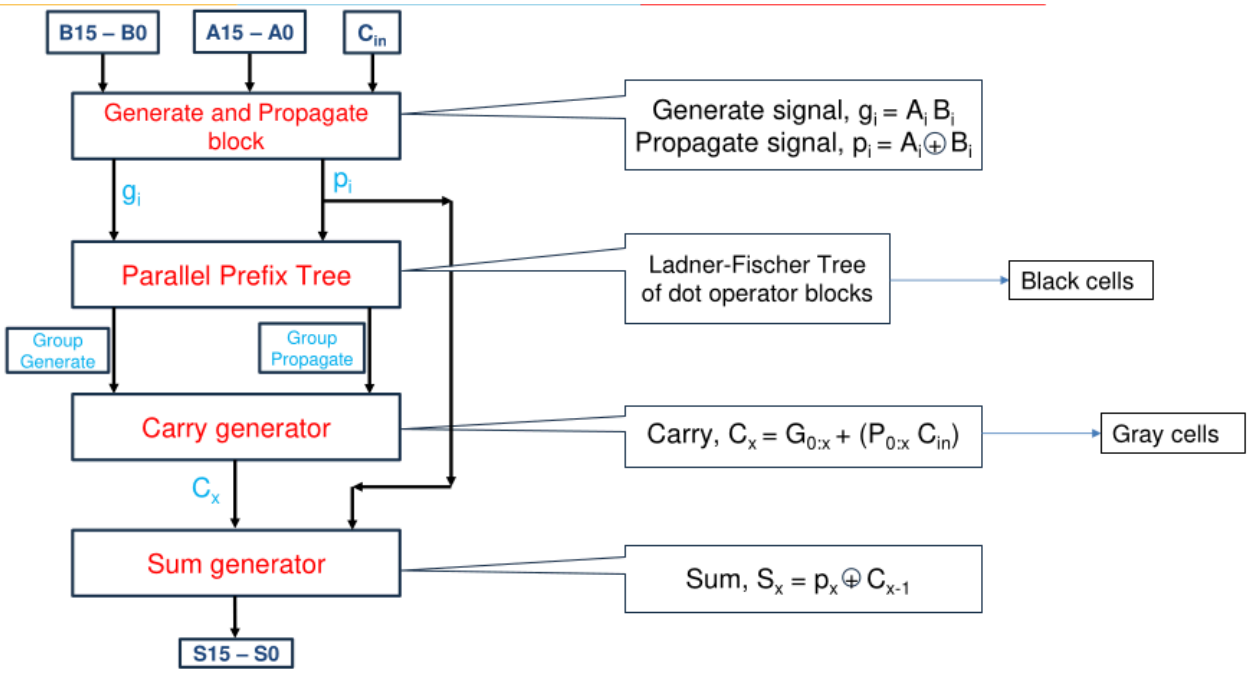
28T full adder



Block diagram of an N-bit RCA

Ladner-Fischer Adder

The Ladner-Fischer adder (LFA) comes under the category of Parallel Prefix Adders (PPA). The designed Ladner-Fischer adder comprises 4 stages, as shown in the block diagram below. Each of them has been briefly explained in the sections below.



Block diagram of the implemented 16-bit LFA

Preprocessing stage

This stage takes the operands $\mathbf{a_i}$ & $\mathbf{b_i}$ and produces the generate($\mathbf{g_i}$) and propagate($\mathbf{p_i}$) signals as outputs. These are given to the prefix tree as inputs. The concept of these signals comes from the truth table of a full adder.

Propagate signal turns 1 if the full adder is propagating a previous stage carry (C_{in}) through its C_{out}. The generated signal turns 1 if the full adder is creating a carry out.

$$p_i = A_i \oplus B_i$$

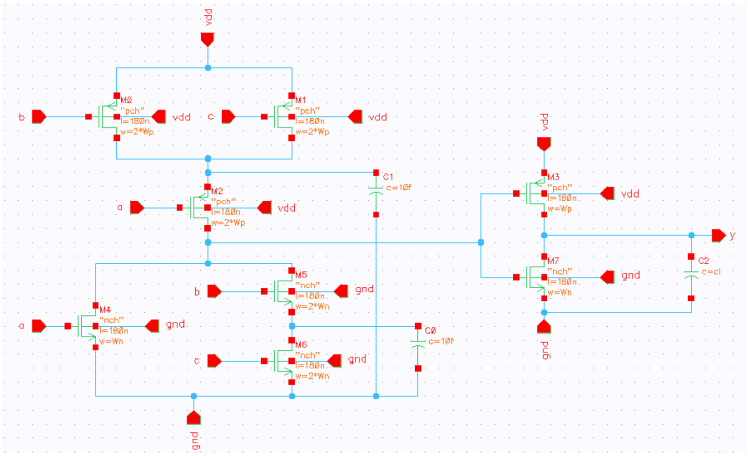
$$g_i = A_i \,.\, B_i$$

Prefix tree

The prefix tree is responsible for evaluating the group generate and group propagate signals used in the subsequent stage for generating the carry. The prefix tree comprises several dot operator blocks, consisting of AND gates and (A+BC) gates. The dot operators are arranged in a tree-like structure. The AND gates are used for the group propagate logic while the (A+BC) gate is used for the group generate.

A+BC gate

The A+BC operation is often used in this design, so a transistor-level implementation of this gate was created instead of cascading an AND gate & an OR gate.

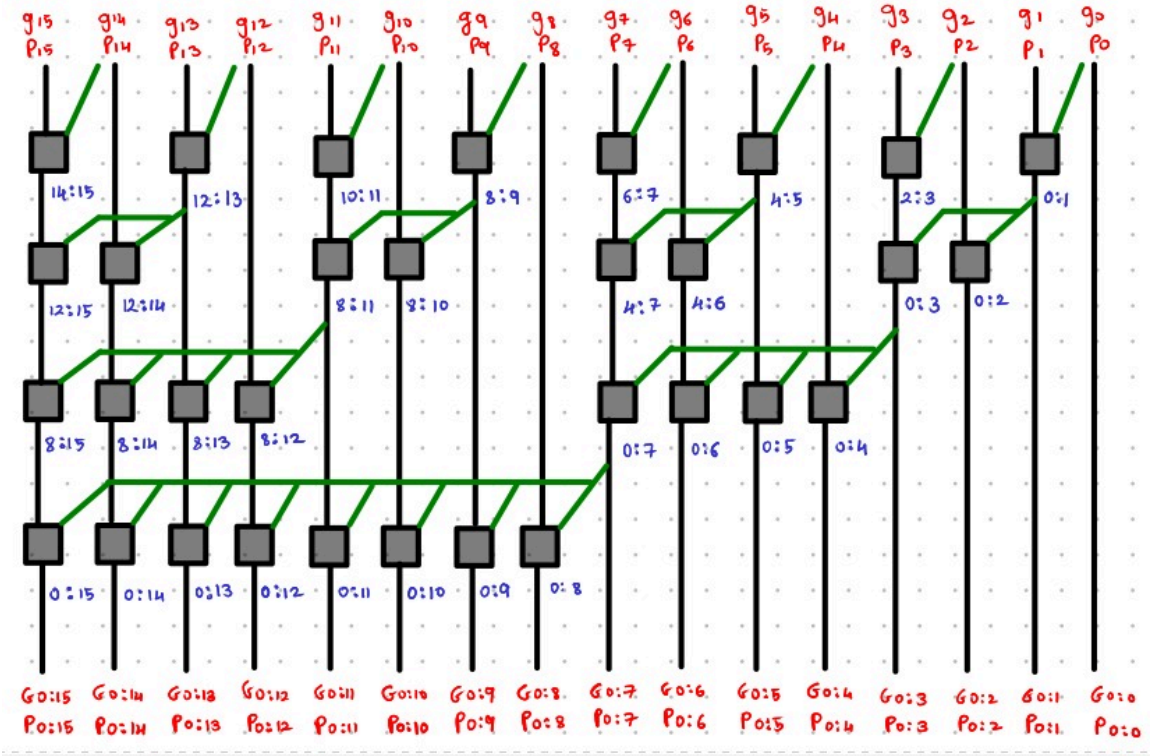


A+BC gate

These two gates are put together to form what is called a Dot operator block or **Black cell**. Their main function is to combine two different ranges of group generates and propagates.

$$(G_{i:j} , P_{i:j}) \cdot (G_{m:n} , P_{m:n}) = (G_{i:n} , P_{i:n})$$
$$i < m \leq (j+1)$$

The carry C_i can be generated only if group generate and propagate is spanning the full range from 0 (LSB) to bit ‘i’. The Ladner-Fischer prefix tree is shown in the figure below. Each black box denotes a black cell.



Ladner-Fischer prefix tree

Carry generation stage

The carry generation stage generates C_x based on the inputs C_{in}, $G_{0:x}$ and $P_{0:x}$. The carry expression is given by:

$$C_x = G_{0:x} + P_{0:x} \,.\, C_{in}$$

This expression is of the form (A+BC). In PPA architecture, it is called a **Grey cell**. Thus it has been realized using 16 such (A+BC) gates to get 16 carries (15 intermediate carries and 1 C_{out}).

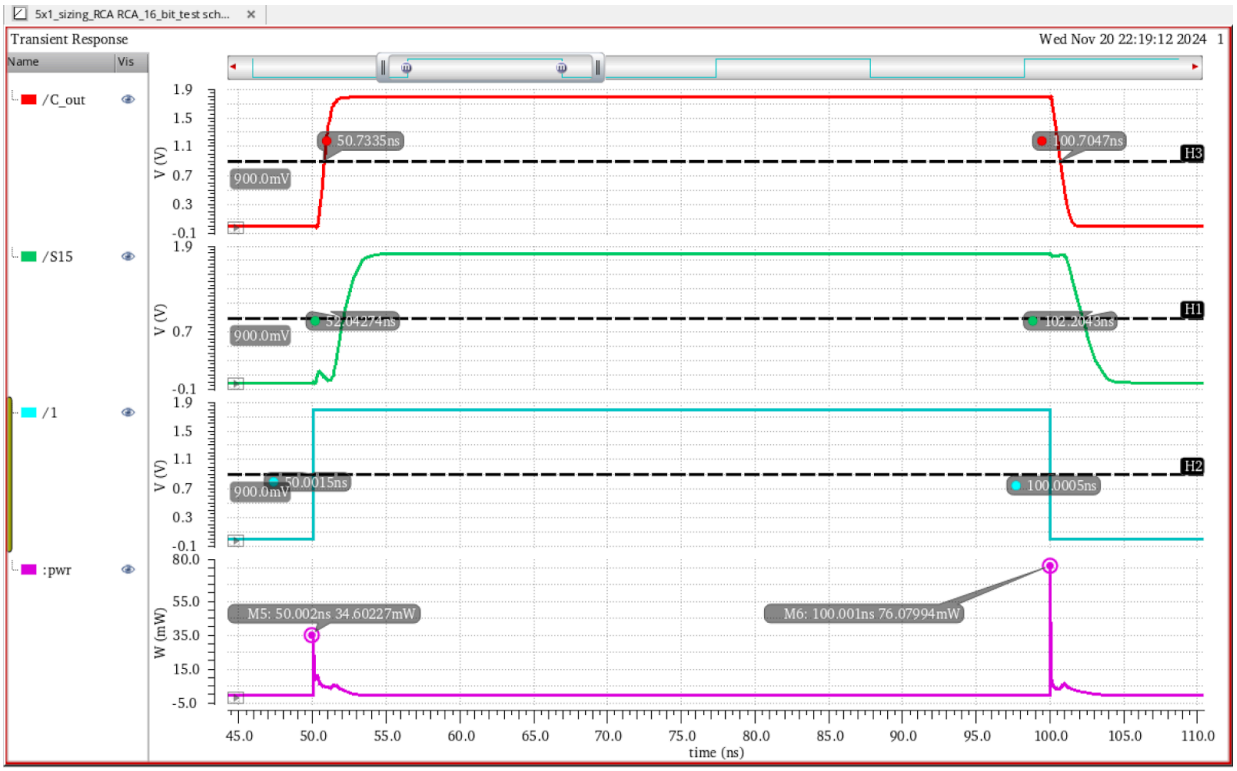
Sum generation stage

The final sum is generated using a set of XOR gates using propagate and carry signals. The 16-bit adder thus consists of 16 XOR gates.

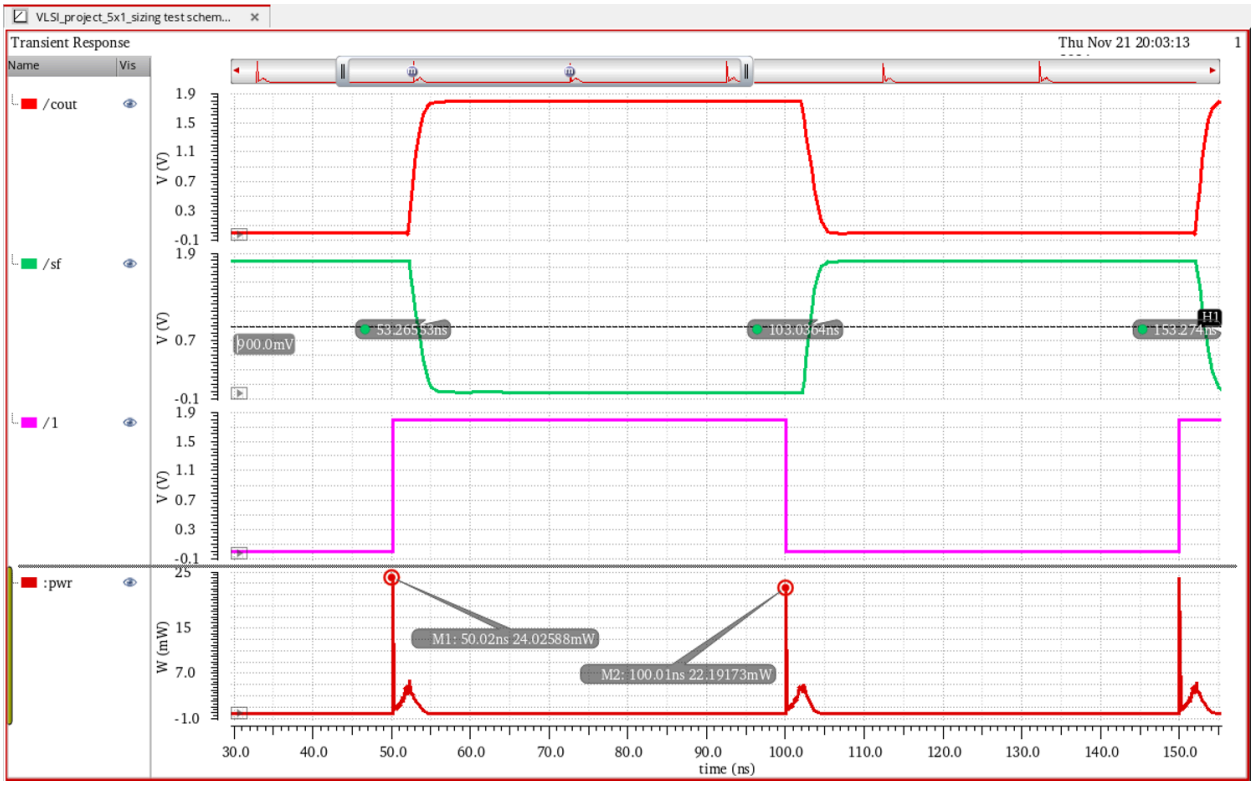
$$S_i = A_i \oplus B_i \oplus C_{i-1} = p_i \oplus C_{i-1}$$

Results and comparative analysis of the adders

The comparative analysis of the 16-bit RCA and LFA was done based on delay, power dissipation and area consumed (Number of transistors). To have consistency in the results, both adders were tested for delay and power at the same input frequency of 10 MHz.
The delay waveforms for both the adders are shown below.



Waveforms of 16-bit RCA



Waveforms of 16-bit LFA for worst-case delay

The observations are tabulated below.

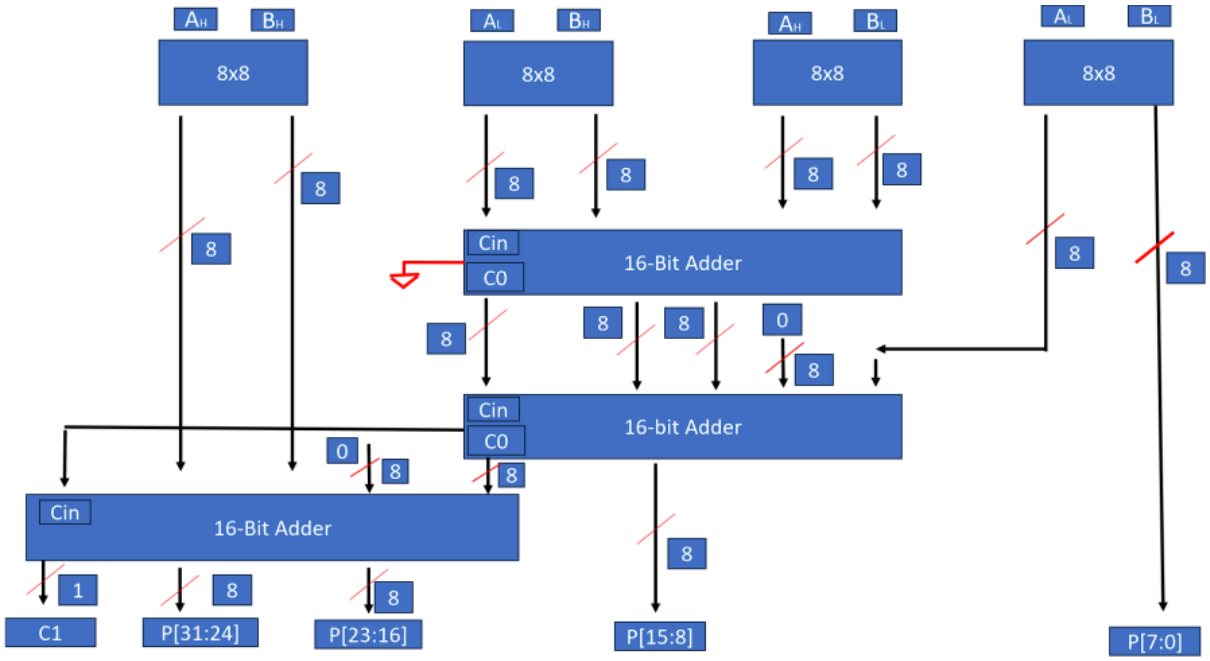
Adder	Load	Peak power	Average power	Delay	No. of transistors
16-bit RCA	200f F	76.08 mW	270.5 µW	15.745 ns	448
16-bit LFA	200f F	40.195 mW	205 µW	3.15 ns	1056

The Ladner-Fischer adder, by nature, performs much better than the conventional RCA. The delay in the 16-bit LFA has decreased by **79.9%** compared to the RCA. Additionally, average power consumption in LFA has been reduced by **24.2%**. However, this gain in performance comes at the cost of area. The LFA uses **2.35 times** more transistors than the RCA to achieve its performance.

16-bit Multiplier

Architecture

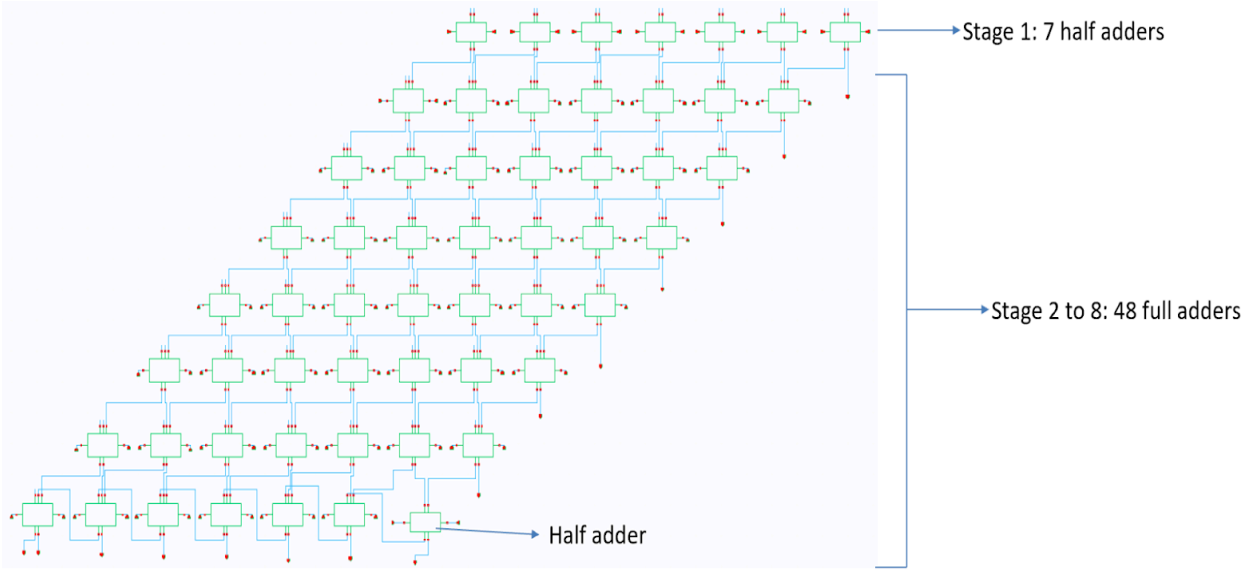
The 16-bit multiplier was implemented using four 8x8 array multipliers along with three 16-bit Ladner Fischer adders. The block diagram for the same is shown below.



Block diagram for 16-bit multiplier

The 8x8 multiplier block architecture

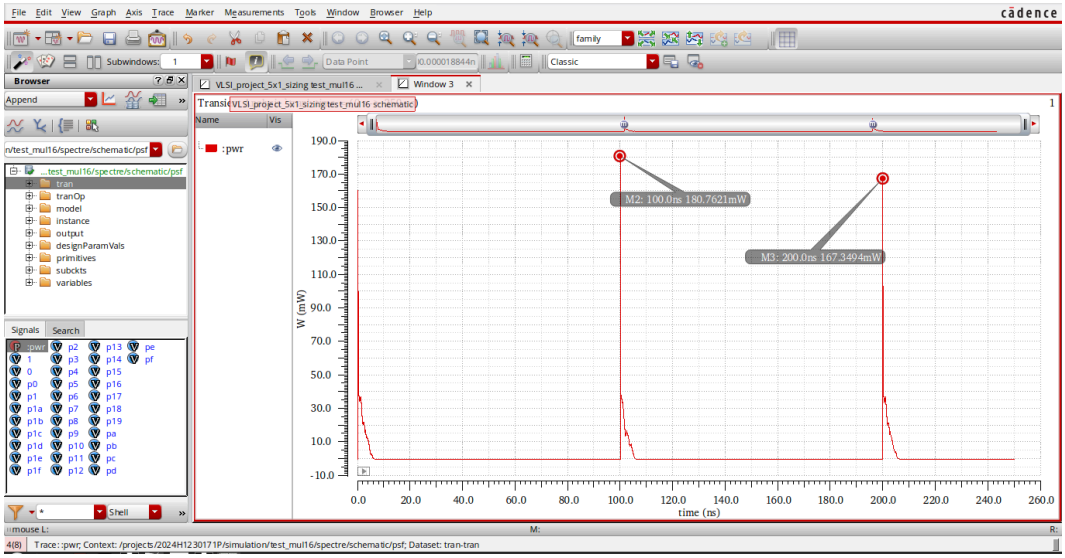
An array of 64 AND gates do the multiplication of the bits. The partial products thus obtained are added by using a Carry Save Adder (CSA) architecture. This helps in adding multiple operands (8 partial products) with good performance without using up a lot of area. A total of 48 full adders and 8 half adders were used.



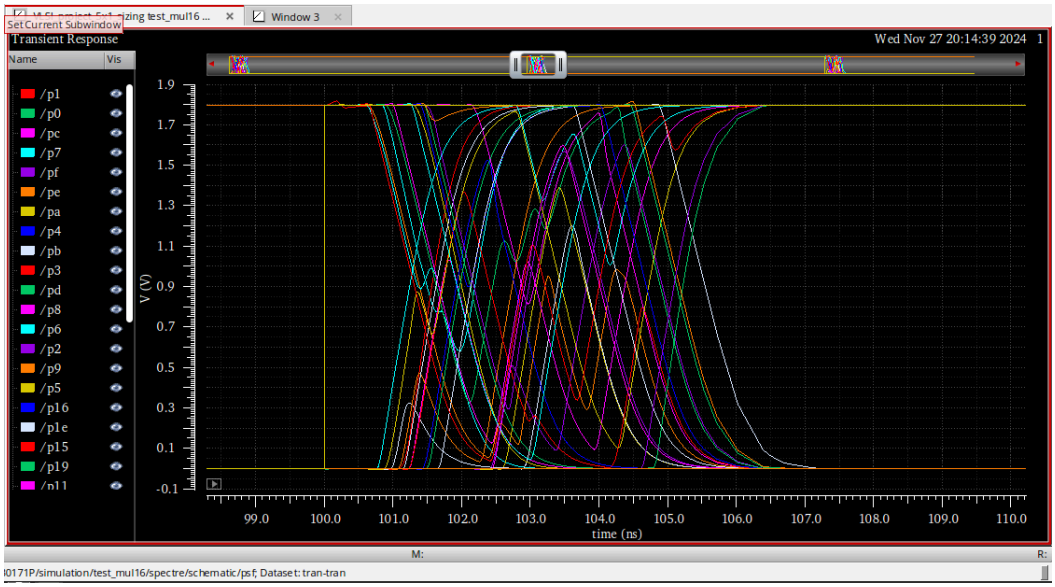
Matrix of half and full adders for partial product addition in the 8x8 multiplier

Results

The designed multiplier was tested for multiple input combinations and the results of the transient analysis are shown below.



Dynamic power plot for the 16-bit multiplier



Output signal waveforms during Transient analysis for a random input

Peak dynamic power	180.7621 mW
Average dynamic power	1.188 mW

References

[1] Richard E. Ladner and Michael J. Fischer. 1980. Parallel Prefix Computation. J. ACM 27, 4 (Oct. 1980), 831–838.

[2] Behrooz Parhami (2010), Computer Arithmetic Algorithms and Hardware Designs, Second Edition, Oxford University Press.