

## 1. Description

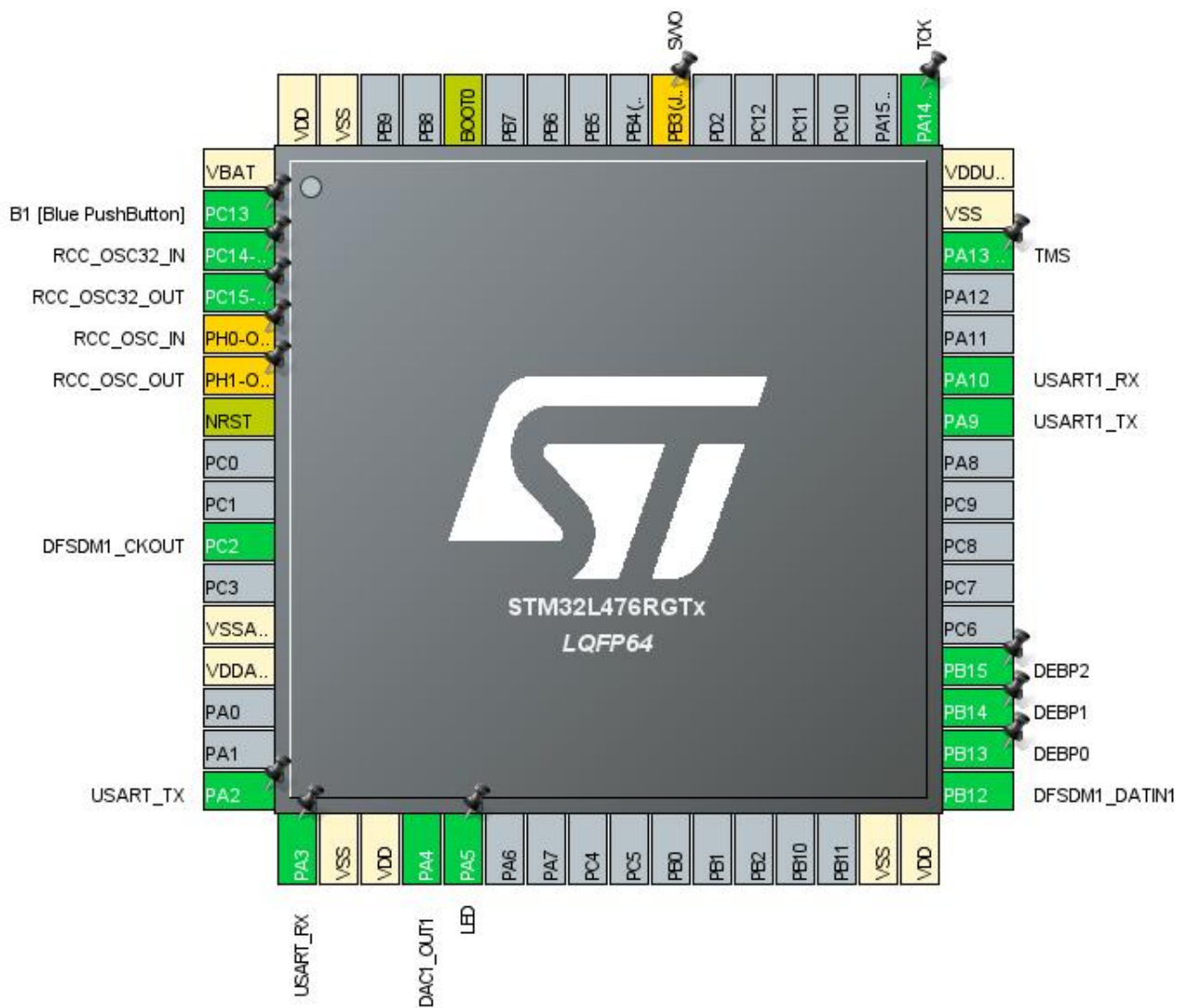
### 1.1. Project

|                 |                   |
|-----------------|-------------------|
| Project Name    | l476_pdm32k       |
| Board Name      | NUCLEO-L476RG     |
| Generated with: | STM32CubeMX 5.2.0 |
| Date            | 10/08/2019        |

### 1.2. MCU

|                |               |
|----------------|---------------|
| MCU Series     | STM32L4       |
| MCU Line       | STM32L4x6     |
| MCU name       | STM32L476RGTx |
| MCU Package    | LQFP64        |
| MCU Pin number | 64            |

## 2. Pinout Configuration



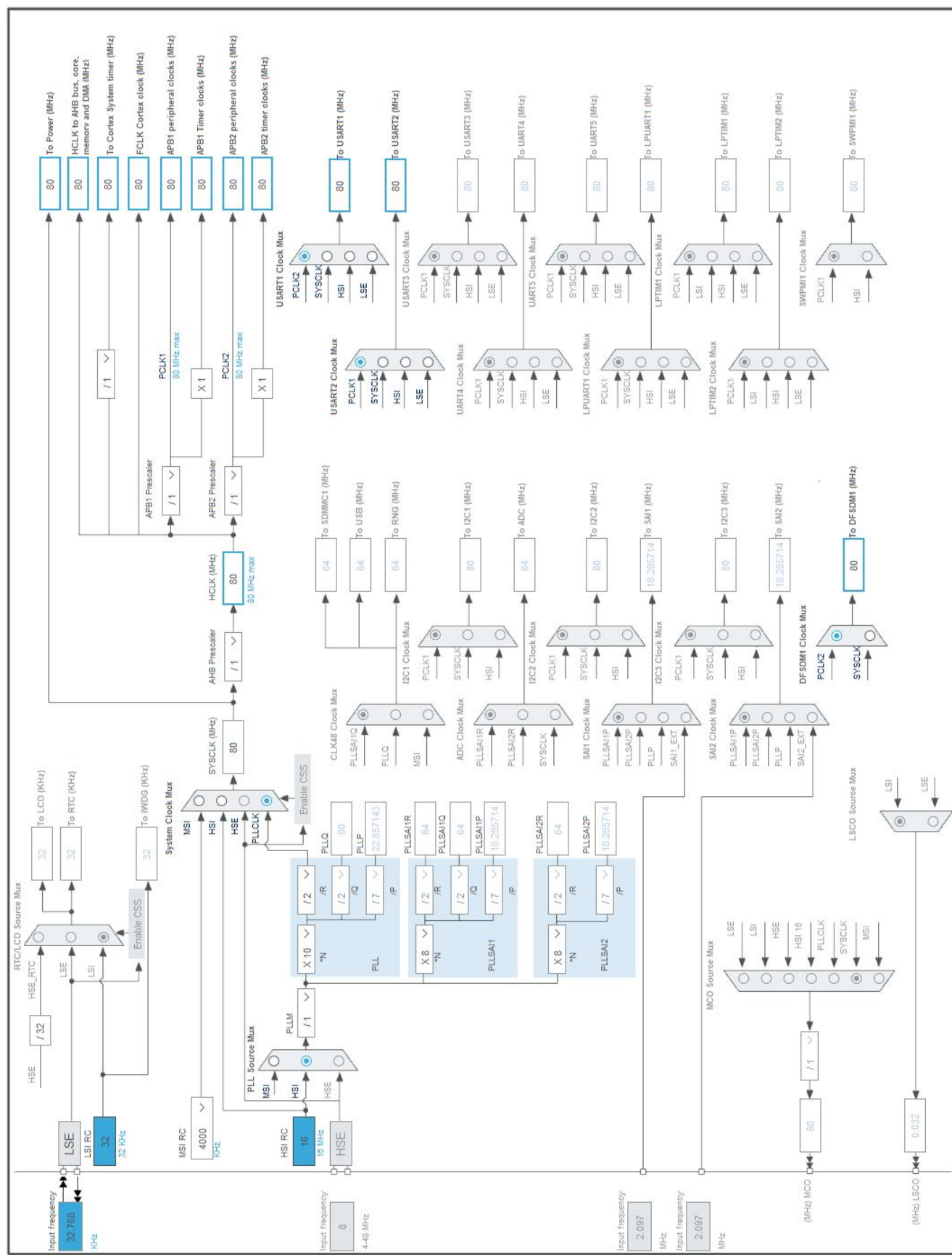
### 3. Pins Configuration

| Pin Number<br>LQFP64 | Pin Name<br>(function after<br>reset) | Pin Type | Alternate<br>Function(s) | Label                |
|----------------------|---------------------------------------|----------|--------------------------|----------------------|
| 1                    | VBAT                                  | Power    |                          |                      |
| 2                    | PC13                                  | I/O      | GPIO_EXTI13              | B1 [Blue PushButton] |
| 3                    | PC14-OSC32_IN (PC14)                  | I/O      | RCC_OSC32_IN             |                      |
| 4                    | PC15-OSC32_OUT (PC15)                 | I/O      | RCC_OSC32_OUT            |                      |
| 5                    | PH0-OSC_IN (PH0) *                    | I/O      | RCC_OSC_IN               |                      |
| 6                    | PH1-OSC_OUT (PH1) *                   | I/O      | RCC_OSC_OUT              |                      |
| 7                    | NRST                                  | Reset    |                          |                      |
| 10                   | PC2                                   | I/O      | DFSDM1_CKOUT             |                      |
| 12                   | VSSA/VREF-                            | Power    |                          |                      |
| 13                   | VDDA/VREF+                            | Power    |                          |                      |
| 16                   | PA2                                   | I/O      | USART2_TX                | USART_TX             |
| 17                   | PA3                                   | I/O      | USART2_RX                | USART_RX             |
| 18                   | VSS                                   | Power    |                          |                      |
| 19                   | VDD                                   | Power    |                          |                      |
| 20                   | PA4                                   | I/O      | DAC1_OUT1                |                      |
| 21                   | PA5 **                                | I/O      | GPIO_Output              | LED                  |
| 31                   | VSS                                   | Power    |                          |                      |
| 32                   | VDD                                   | Power    |                          |                      |
| 33                   | PB12                                  | I/O      | DFSDM1_DATIN1            |                      |
| 34                   | PB13 **                               | I/O      | GPIO_Output              | DEBP0                |
| 35                   | PB14 **                               | I/O      | GPIO_Output              | DEBP1                |
| 36                   | PB15                                  | I/O      | GPIO_EXTI15              | DEBP2                |
| 42                   | PA9                                   | I/O      | USART1_TX                |                      |
| 43                   | PA10                                  | I/O      | USART1_RX                |                      |
| 46                   | PA13 (JTMS-SWDIO)                     | I/O      | SYS_JTMS-SWDIO           | TMS                  |
| 47                   | VSS                                   | Power    |                          |                      |
| 48                   | VDDUSB                                | Power    |                          |                      |
| 49                   | PA14 (JTCK-SWCLK)                     | I/O      | SYS_JTCK-SWCLK           | TCK                  |
| 55                   | PB3 (JTDO-TRACESWO) *                 | I/O      | SYS_JTDO-SWO             | SWO                  |
| 60                   | BOOT0                                 | Boot     |                          |                      |
| 63                   | VSS                                   | Power    |                          |                      |
| 64                   | VDD                                   | Power    |                          |                      |

\*\* The pin is affected with an I/O function

\* The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

| Name                              | Value                               |
|-----------------------------------|-------------------------------------|
| Project Name                      | I476_pdm32k                         |
| Project Folder                    | D:\CubeIDE_WORK\project\I476_pdm32k |
| Toolchain / IDE                   | STM32CubeIDE                        |
| Firmware Package Name and Version | STM32Cube FW_L4 V1.14.0             |

### 5.2. Code Generation Settings

| Name  | Value                                 |
|---|---------------------------------------|
| STM32Cube Firmware Library Package                              | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files   | No                                    |
| Backup previously generated files when re-generating            | No                                    |
| Delete previously generated files when not re-generated         | Yes                                   |
| Set all free pins as analog (to optimize the power consumption) | No                                    |

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

|           |               |
|-----------|---------------|
| Series    | STM32L4       |
| Line      | STM32L4x6     |
| MCU       | STM32L476RGTx |
| Datasheet | 025976_Rev4   |

### 6.2. Parameter Selection

|             |     |
|-------------|-----|
| Temperature | 25  |
| Vdd         | 3.0 |

## 7. IPs and Middleware Configuration

### 7.1. DAC1

**OUT1 mode: Connected to external pin only**

#### 7.1.1. Parameter Settings:

##### DAC Out1 Settings:

|                      |                                    |
|----------------------|------------------------------------|
| Output Buffer        | Enable                             |
| Trigger              | <b>Timer 2 Trigger Out event *</b> |
| Wave generation mode | Disabled                           |
| User Trimming        | Factory trimming                   |
| Sample And Hold      | Sampleandhold Disable              |

### 7.2. DFSDM1

**mode: PDM/SPI Input from ch1 and Internal Clock**

**mode: PDM/SPI input from ch1 and internal clock**

**mode: CKOUT**

#### 7.2.1. Filter 0:

##### regular channel selection:

|                                     |                    |
|-------------------------------------|--------------------|
| regular channel selection           | <b>Channel 0 *</b> |
| Continuous Mode                     | Continuous Mode    |
| Trigger to start regular conversion | Software trigger   |
| Fast Mode                           | <b>Enable *</b>    |
| Dma Mode                            | <b>Enable *</b>    |

##### injected channel selection:

|                              |         |
|------------------------------|---------|
| Channel0 as injected channel | Disable |
| Channel1 as injected channel | Disable |
| Channel2 as injected channel | Disable |
| Channel3 as injected channel | Disable |
| Channel4 as injected channel | Disable |
| Channel5 as injected channel | Disable |
| Channel6 as injected channel | Disable |
| Channel7 as injected channel | Disable |

##### Filter parameters:

|            |                             |
|------------|-----------------------------|
| Sinc Order | <b>Sinc 4 filter type *</b> |
| Fosr       | <b>64 *</b>                 |



losr

1

### 7.2.2. Filter 1:

#### regular channel selection:

regular channel selection

Continuous Mode

Trigger to start regular conversion

Fast Mode

Dma Mode

#### Channel 1 \*

Continuous Mode

Software trigger

**Enable \***

**Enable \***

#### injected channel selection:

Channel0 as injected channel

Disable

Channel1 as injected channel

Disable

Channel2 as injected channel

Disable

Channel3 as injected channel

Disable

Channel4 as injected channel

Disable

Channel5 as injected channel

Disable

Channel6 as injected channel

Disable

Channel7 as injected channel

Disable

#### Filter parameters:

Sinc Order

**Sinc 4 filter type \***

Fosr

**64 \***

losr

1

### 7.2.3. Filter 2:

#### regular channel selection:

regular channel selection

- None -

#### injected channel selection:

Channel0 as injected channel

Disable

Channel1 as injected channel

Disable

Channel2 as injected channel

Disable

Channel3 as injected channel

Disable

Channel4 as injected channel

Disable

Channel5 as injected channel

Disable

Channel6 as injected channel

Disable

Channel7 as injected channel

Disable

#### 7.2.4. Filter 3:

##### regular channel selection:

regular channel selection - None -

##### injected channel selection:

|                              |         |
|------------------------------|---------|
| Channel0 as injected channel | Disable |
| Channel1 as injected channel | Disable |
| Channel2 as injected channel | Disable |
| Channel3 as injected channel | Disable |
| Channel4 as injected channel | Disable |
| Channel5 as injected channel | Disable |
| Channel6 as injected channel | Disable |
| Channel7 as injected channel | Disable |

#### 7.2.5. Output Clock:

##### Output Clock parameters:

|           |   |
|-----------|---|
| Selection | Source for output clock is system clock |
| Divider   | 39 *                                    |

#### 7.2.6. Channel 0:

##### Channel 0 parameters:

|                 |                      |
|-----------------|----------------------|
| Type            | SPI with rising edge |
| Spi Clock       | Internal SPI clock   |
| Offset          | 0                    |
| Right Bit Shift | 0x00 *               |

##### Analog watchdog parameters:

|              |                      |
|--------------|----------------------|
| Filter Order | FastSinc filter type |
| Oversampling | 1                    |

#### 7.2.7. Channel 1:

##### Analog watchdog parameters:

|              |                      |
|--------------|----------------------|
| Filter Order | FastSinc filter type |
| Oversampling | 1                    |

##### Channel 1 parameters:

|           |                      |
|-----------|----------------------|
| Type      | SPI with rising edge |
| Spi Clock | Internal SPI clock   |

|                 |               |
|-----------------|---------------|
| Offset          | 0             |
| Right Bit Shift | <b>0x00 *</b> |

## 7.3. RCC

### Low Speed Clock (LSE) : Crystal/Ceramic Resonator

#### 7.3.1. Parameter Settings:

##### System Parameters:

|                   |                    |
|-------------------|--------------------|
| VDD voltage (V)   | 3.3                |
| Instruction Cache | Enabled            |
| Prefetch Buffer   | <b>Enabled *</b>   |
| Data Cache        | Enabled            |
| Flash Latency(WS) | 4 WS (5 CPU cycle) |

##### RCC Parameters:

|                                |          |
|--------------------------------|----------|
| HSI Calibration Value          | 16       |
| MSI Calibration Value          | 0        |
| MSI Auto Calibration           | Disabled |
| HSE Startup Timeout Value (ms) | 100      |
| LSE Startup Timeout Value (ms) | 5000     |

##### Power Parameters:

|                               |                                 |
|-------------------------------|---------------------------------|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 1 |
|-------------------------------|---------------------------------|

## 7.4. SYS

### Debug: Serial Wire

### Timebase Source: TIM17

## 7.5. TIM2

### Clock Source : Internal Clock

#### 7.5.1. Parameter Settings:

##### Counter Settings:

|   |             |
|---|-------------|
| Prescaler (PSC - 16 bits value)                       | 0           |
| Counter Mode  | Up          |
| Counter Period (AutoReload Register - 32 bits value ) | 0           |
| Internal Clock Division (CKD)                         | No Division |
| auto-reload preload                                   | Disable     |

### Trigger Output (TRGO) Parameters:

|                              |  |
|------------------------------|--|
| Master/Slave Mode (MSM bit)  | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR)               |

## 7.6. USART1

### Mode: Asynchronous

#### 7.6.1. Parameter Settings:

##### Basic Parameters:

|             |                           |
|-------------|---------------------------|
| Baud Rate   | 921600 *                  |
| Word Length | 8 Bits (including Parity) |
| Parity      | None                      |
| Stop Bits   | 1                         |

##### Advanced Parameters:

|                |                      |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling  | 16 Samples           |
| Single Sample  | Disable              |

##### Advanced Features:

|                               |         |
|-------------------------------|---------|
| Auto Baudrate                 | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion                | Disable |
| TX and RX Pins Swapping       | Disable |
| Overrun                       | Enable  |
| DMA on RX Error               | Enable  |
| MSB First                     | Disable |

## 7.7. USART2

### Mode: Asynchronous

#### 7.7.1. Parameter Settings:

##### Basic Parameters:

|             |                           |
|-------------|---------------------------|
| Baud Rate   | 115200                    |
| Word Length | 8 Bits (including Parity) |
| Parity      | None                      |
| Stop Bits   | 1                         |

##### Advanced Parameters:

|                |                      |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling  | 16 Samples           |
| Single Sample  | Disable              |

#### Advanced Features:

|                               |         |
|-------------------------------|---------|
| Auto Baudrate                 | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion                | Disable |
| TX and RX Pins Swapping       | Disable |
| Overrun                       | Enable  |
| DMA on RX Error               | Enable  |
| MSB First                     | Disable |

## 7.8. FREERTOS

### Interface: CMSIS\_V1

#### 7.8.1. Config parameters:

##### API:

|              |          |
|--------------|----------|
| FreeRTOS API | CMSIS v1 |
|--------------|----------|

##### Versions:

|                    |        |
|--------------------|--------|
| FreeRTOS version   | 10.0.1 |
| CMSIS-RTOS version | 1.02   |

##### Kernel settings:

|                                   |                 |
|-----------------------------------|-----------------|
| USE_PREEMPTION                    | Enabled         |
| CPU_CLOCK_HZ                      | SystemCoreClock |
| TICK_RATE_HZ                      | 1000            |
| MAX_PRIORITIES                    | 7               |
| MINIMAL_STACK_SIZE                | 128             |
| MAX_TASK_NAME_LEN                 | 16              |
| USE_16_BIT_TICKS                  | Disabled        |
| IDLE_SHOULD_YIELD                 | Enabled         |
| USE_MUTEXES                       | Enabled         |
| USE_RECURSIVE_MUTEXES             | Disabled        |
| USE_COUNTING_SEMAPHORES           | Disabled        |
| QUEUE_REGISTRY_SIZE               | 8               |
| USE_APPLICATION_TASK_TAG          | Disabled        |
| ENABLE_BACKWARD_COMPATIBILITY     | Enabled         |
| USE_PORT_OPTIMISED_TASK_SELECTION | Enabled         |
| USE_TICKLESS_IDLE                 | Disabled        |
| USE_TASK_NOTIFICATIONS            | Enabled         |

RECORD\_STACK\_HIGH\_ADDRESS Disabled

#### Memory management settings:

Memory Allocation Dynamic

TOTAL\_HEAP\_SIZE **4096 \***

Memory Management scheme heap\_4

#### Hook function related definitions:

USE\_IDLE\_HOOK Disabled

USE\_TICK\_HOOK Disabled

USE\_MALLOC\_FAILED\_HOOK Disabled

USE\_DAEMON\_TASK\_STARTUP\_HOOK Disabled

CHECK\_FOR\_STACK\_OVERFLOW Disabled

#### Run time and task stats gathering related definitions:

GENERATE\_RUN\_TIME\_STATS Disabled

USE\_TRACE\_FACILITY Disabled

USE\_STATS\_FORMATTING\_FUNCTIONS Disabled

#### Co-routine related definitions:

USE\_CO\_ROUTINES Disabled

MAX\_CO\_ROUTINE\_PRIORITIES 2

#### Software timer definitions:

USE\_TIMERS Disabled

#### Interrupt nesting behaviour configuration:

LIBRARY\_LOWEST\_INTERRUPT\_PRIORITY 15

LIBRARY\_MAX\_SYSCALL\_INTERRUPT\_PRIORITY 5

## 7.8.2. Include parameters:

#### Include definitions:

vTaskPrioritySet Enabled

uxTaskPriorityGet Enabled

vTaskDelete Enabled

vTaskCleanUpResources Disabled

vTaskSuspend Enabled

vTaskDelayUntil Disabled

vTaskDelay Enabled

xTaskGetSchedulerState Enabled

xTaskResumeFromISR Enabled

xQueueGetMutexHolder Disabled

xSemaphoreGetMutexHolder Disabled

pcTaskGetTaskName Disabled

uxTaskGetStackHighWaterMark Disabled

xTaskGetCurrentTaskHandle Disabled

|                          |          |
|--------------------------|----------|
| eTaskGetState            | Disabled |
| xEventGroupSetBitFromISR | Disabled |
| xTimerPendFunctionCall   | Disabled |
| xTaskAbortDelay          | Disabled |
| xTaskGetHandle           | Disabled |

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

| IP                    | Pin                   | Signal         | GPIO mode  | GPIO pull/up pull down      | Max Speed   | User Label           |
|-----------------------|-----------------------|----------------|--|-----------------------------|-------------|----------------------|
| DAC1                  | PA4                   | DAC1_OUT1      | Analog mode  | No pull-up and no pull-down | n/a         |                      |
| DFSDM1                | PC2                   | DFSDM1_CKOUT   | Alternate Function Push Pull                                       | No pull-up and no pull-down | Low         |                      |
|                       | PB12                  | DFSDM1_DATIN1  | Alternate Function Push Pull                                       | No pull-up and no pull-down | Low         |                      |
| RCC                   | PC14-OSC32_IN (PC14)  | RCC_OSC32_IN   | n/a  | n/a                         | n/a         |                      |
|                       | PC15-OSC32_OUT (PC15) | RCC_OSC32_OUT  | n/a  | n/a                         | n/a         |                      |
| SYS                   | PA13 (JTMS-SWDIO)     | SYS_JTMS-SWDIO | n/a  | n/a                         | n/a         | TMS                  |
|                       | PA14 (JTCK-SWCLK)     | SYS_JTCK-SWCLK | n/a  | n/a                         | n/a         | TCK                  |
| USART1                | PA9                   | USART1_TX      | Alternate Function Push Pull                                       | No pull-up and no pull-down | Very High * |                      |
|                       | PA10                  | USART1_RX      | Alternate Function Push Pull                                       | No pull-up and no pull-down | Very High * |                      |
| USART2                | PA2                   | USART2_TX      | Alternate Function Push Pull                                       | No pull-up and no pull-down | Very High * | USART_TX             |
|                       | PA3                   | USART2_RX      | Alternate Function Push Pull                                       | No pull-up and no pull-down | Very High * | USART_RX             |
| Single Mapped Signals | PH0-OSC_IN (PH0)      | RCC_OSC_IN     | n/a  | n/a                         | n/a         |                      |
|                       | PH1-OSC_OUT (PH1)     | RCC_OSC_OUT    | n/a  | n/a                         | n/a         |                      |
|                       | PB3 (JTDO-TRACESWO)   | SYS_JTDO-SWO   | n/a  | n/a                         | n/a         | SWO                  |
| GPIO                  | PC13                  | GPIO_EXTI13    | <b>External Interrupt Mode with Falling edge trigger detection</b> | No pull-up and no pull-down | n/a         | B1 [Blue PushButton] |
|                       | PA5                   | GPIO_Output    | Output Push Pull   | No pull-up and no pull-down | Low         | LED                  |
|                       | PB13                  | GPIO_Output    | Output Push Pull   | No pull-up and no pull-down | Low         | DEBP0                |



| IP | Pin  | Signal      | GPIO mode  | GPIO pull/up pull down      | Max Speed | User Label |
|----|------|-------------|--|-----------------------------|-----------|------------|
|    | PB14 | GPIO_Output | Output Push Pull   | No pull-up and no pull-down | Low       | DEBP1      |
|    | PB15 | GPIO_EXTI15 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a       | DEBP2      |

## 8.2. DMA configuration

| DMA request | Stream        | Direction            | Priority |
|-------------|---------------|----------------------|----------|
| USART1_TX   | DMA2_Channel6 | Memory To Peripheral | Low      |
| DAC_CH1     | DMA1_Channel3 | Memory To Peripheral | Low      |
| DFSDM1_FLT0 | DMA1_Channel4 | Peripheral To Memory | Low      |
| DFSDM1_FLT1 | DMA1_Channel5 | Peripheral To Memory | Low      |

### USART1\_TX: DMA2\_Channel6 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### DAC\_CH1: DMA1\_Channel3 DMA request Settings:

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Half Word  
Memory Data Width: Half Word

### DFSDM1\_FLT0: DMA1\_Channel4 DMA request Settings:

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Word  
Memory Data Width: Word

### DFSDM1\_FLT1: DMA1\_Channel5 DMA request Settings:

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Word

Memory Data Width: Word

### 8.3. NVIC configuration

| Interrupt Table  | Enable | Preenmption Priority | SubPriority |
|--|--------|----------------------|-------------|
| Non maskable interrupt   | true   | 0                    | 0           |
| Hard fault interrupt   | true   | 0                    | 0           |
| Memory management fault  | true   | 0                    | 0           |
| Prefetch fault, memory access fault  | true   | 0                    | 0           |
| Undefined instruction or illegal state                                     | true   | 0                    | 0           |
| System service call via SWI instruction                                    | true   | 0                    | 0           |
| Debug monitor  | true   | 0                    | 0           |
| Pendable request for system service  | true   | 15                   | 0           |
| System tick timer  | true   | 15                   | 0           |
| DMA1 channel3 global interrupt   | true   | 5                    | 0           |
| DMA1 channel4 global interrupt   | true   | 5                    | 0           |
| DMA1 channel5 global interrupt   | true   | 5                    | 0           |
| TIM1 trigger and commutation interrupts and TIM17 global interrupt         | true   | 0                    | 0           |
| USART1 global interrupt  | true   | 5                    | 0           |
| TIM6 global interrupt, DAC channel1 and channel2 underrun error interrupts | true   | 5                    | 0           |
| DFSDM1 filter0 global interrupt  | true   | 5                    | 0           |
| DFSDM1 filter1 global interrupt  | true   | 5                    | 0           |
| DMA2 channel6 global interrupt   | true   | 5                    | 0           |
| PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38       | unused |                      |             |
| Flash global interrupt   | unused |                      |             |
| RCC global interrupt   | unused |                      |             |
| TIM2 global interrupt  | unused |                      |             |
| USART2 global interrupt  | unused |                      |             |
| EXTI line[15:10] interrupts  | unused |                      |             |
| FPU global interrupt   | unused |                      |             |

\* User modified value

## ***9. Software Pack Report***