WESTERN NEW ENGLAND UNIVERSITY | WNE

Department of Electrical and Computer Engineering

CPE 462/562 VHDL: Simulation & Synthesis

Midterm Project: 4-bit ALU Design and Implementation

Katelyn Charbonneau
Email: kc325844@wne.edu
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Tasks	**Grades**
Task 1. Design, test, and verify 4-bit ALU (50')	
Task 2. Program DE2-115 and demonstrate 4-bit ALU (10')	
Task 3. Display INPUT and OUTPUT decimal equivalent values on SSDs (20')	
Report (20')	
Bonus (10')	
Total (100/110):	

1 Objective

The objectives of the project are to be familiar with behavioral architecture; be able to write a behavioral VHDL code to design a 4-bit arithmetic logic unit (ALU), write a testbench to verify the design, and implement the ALU on FPGA.

2 Design Procedure

While testing of this design was done using a 4-bit bus width, their sizes are really defined as generics. Thus, there is a variable bus size. As part of this project, a ripple carry adder (RCA) is needed. A fixed 4-bit width RCA design was available and was edited to also allow for a variable bus width. This design was tested using a 6-bit width; sample results are in Section 3. A block diagram for this is shown in

3 Simulation Results

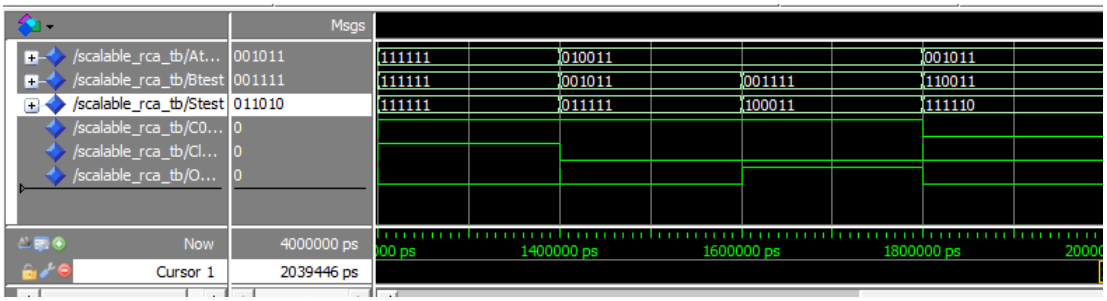

Figure 1: A few example operations on the RCA design using 6 bits

4 Demonstration on FPGA

pictures of on board demo and discussions...

5 Conlusion

your conclusion goes here...