WESTERN NEW ENGLAND UNIVERSITY | WNE

Department of Electrical and Computer Engineering

CPE 462/562 VHDL: Simulation & Synthesis

Midterm Project: 4-bit ALU Design and Implementation

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Tasks	**Grades**
Task 1. Design, test, and verify 4-bit ALU (50')	
Task 2. Program DE2-115 and demonstrate 4-bit ALU (10')	
Task 3. Display INPUT and OUTPUT decimal equivalent values on SSDs (20')	
Report (20')	
Bonus (10')	
Total (100/110):	

1 Objective

The objectives of the project are to be familiar with behavioral architecture; be able to write a behavioral VHDL code to design a 4-bit arithmetic logic unit (ALU), write a testbench to verify the design, and implement the ALU on FPGA.

2 Design Procedure

While testing of this design was done using a 4-bit bus width, their sizes are really defined as generics. Thus, there is a variable bus size. As part of this project, a ripple carry adder (RCA) is needed. A fixed 4-bit width RCA design was available and was edited to also allow for a variable bus width. This design was tested using a 6-bit width; sample results are in Section 3. A block diagram for this is shown in Figure 1.

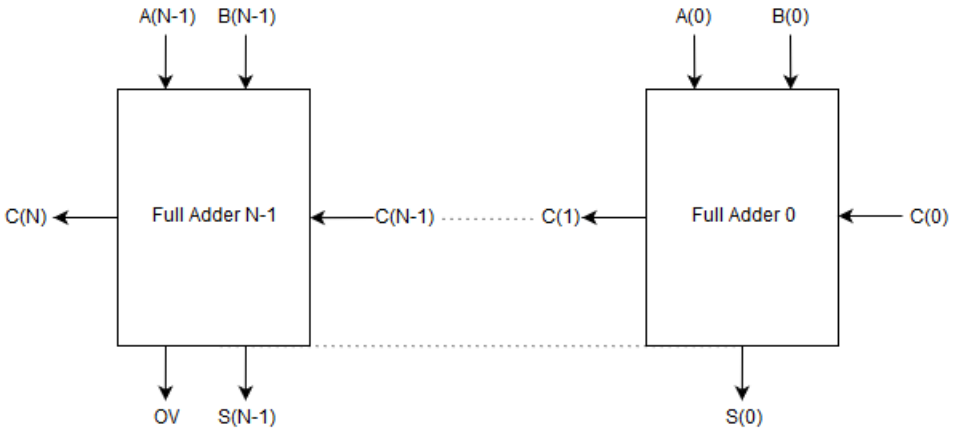

Figure 1: The RCA used to perform arithmetic calculations

Where N is the bus width, A, B, and S (sum) are vectors of length N-1, C (carry) is a vector of length N, and OV is defined as C(N) $\oplus$ C(N-1).

The operations that the ALU can perform, as listed in the project requirements, are listed below:

F_BUS	**C_BUS**	**CBout**	OVERFLOW
000	A_BUS	PASS	0
001	A_BUS + B_BUS + CBin	CBout	Overflow
010	A_BUS - B_BUS - CBin	CBout	Overflow
011	A_BUS OR B_BUS	PASS	0
100	A_BUS XOR B_BUS	PASS	0
101	A_SRA 3	PASS	0
110	A_BUS SLL 3	A_BUS(N-1)	Overflow
111	A_BUS ROR -3	PASS	0

Table 1: ALU Operations

The RCA is used in cases 1 and 2 - addition and subtraction. All other cases are handled by simple pre-defined operations within VHDL. Note that there is overflow for case 6 if the value of A_Bus(N-1) changes after shifting.

3 Simulation Results

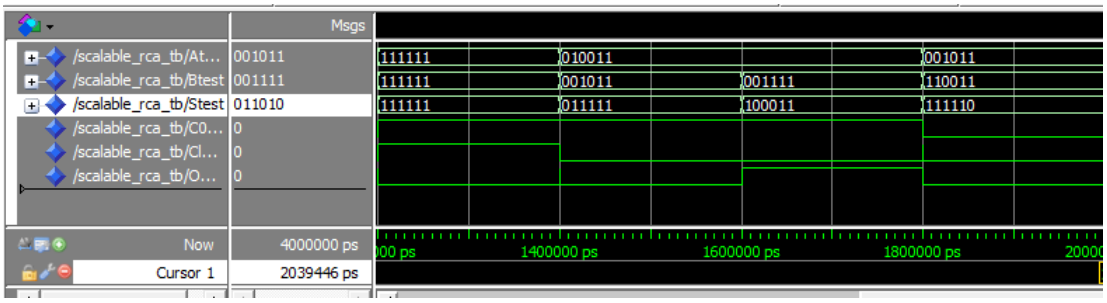

Figure 2: A few example operations on the RCA design using 6 bits

4 Demonstration on FPGA

pictures of on board demo and discussions...

5 Conlusion

your conclusion goes here...