Multilevel inverters:-

* VSI -inverters (2-level inverters) produce o/p with 0 (or) $\pm V_{DC}$ => 2-levels.

→ For minimum ripple content we require
  (1) High switching freq.
  (2) various PWM-strategies.

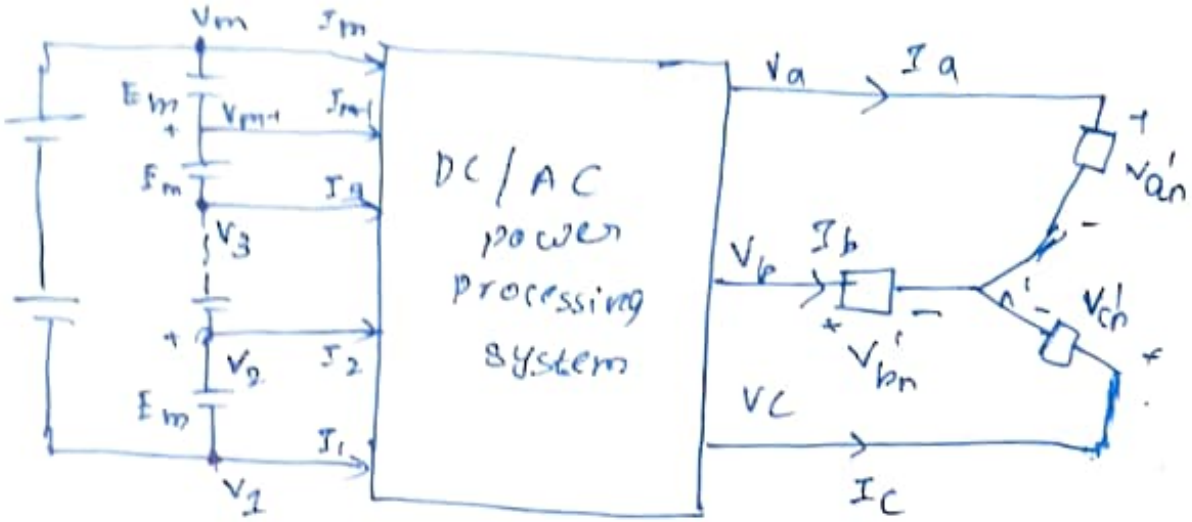
∴ But for high power, high voltage applications 2-level inverters have some limitation.
  → They have high switching losses
  → constraint on device ratings.

∴ In multilevel inverters the device voltage stresses are controlled i.e we can increase no. of voltage levels in inverter without requiring higher ratings on individual devices

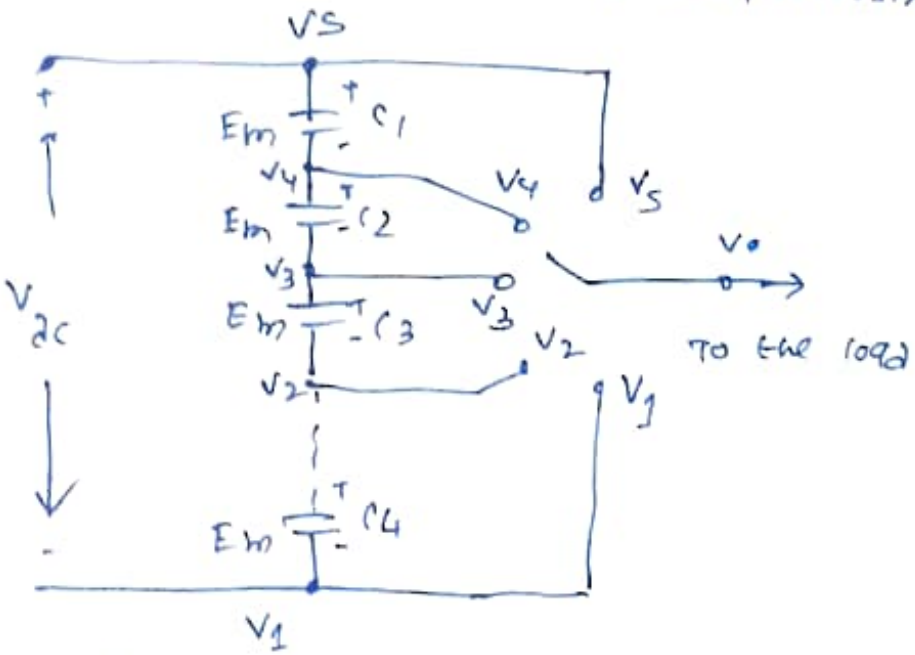
→ So low harmonics as no. of levels ↑
o/p harmonics ↓

$$THD = \sqrt{\frac{1}{g^2} - 1}$$

Multilevel concept:-



(a) 3 ϕ · multilevel power processing system



(b) schematic of single pole of multilevel inverter by a switch.

→ above are general topologies of MLI

→ Nodes can be connected to Load.

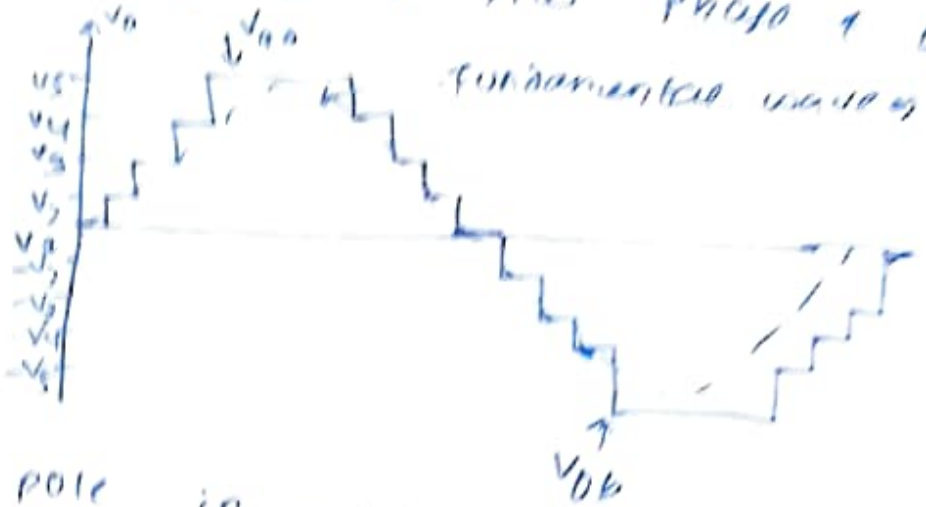
Each cap. voltage = E_m (say my)

P_m	V_{dc} / $m-1$

m: no. of levels
l: no. of nodes to which inverter is accessible

∴ m level inverter, needs (m-1) capacitors

o/p voltage V_o = "V" blw phase & GND pole



fundamental waveform

A pole in MLI => single-pole, multiple-throw switch.

I/P dc voltages => $V_1, V_2, \ldots$

I/P dc currents => $I_1, I_2, \ldots$

V_a, V_b, V_c => rms value line-voltages

I_a, I_b, I_c => rms line load currents.

By connecting to any node we can access the voltage level.

=> The actual realization of switch requires bidirectional switching devices of each node.

Topology of MLI must have

(1) less switching devices as far as possible.

(2) capable of withstanding very high i/p voltage for high power applications

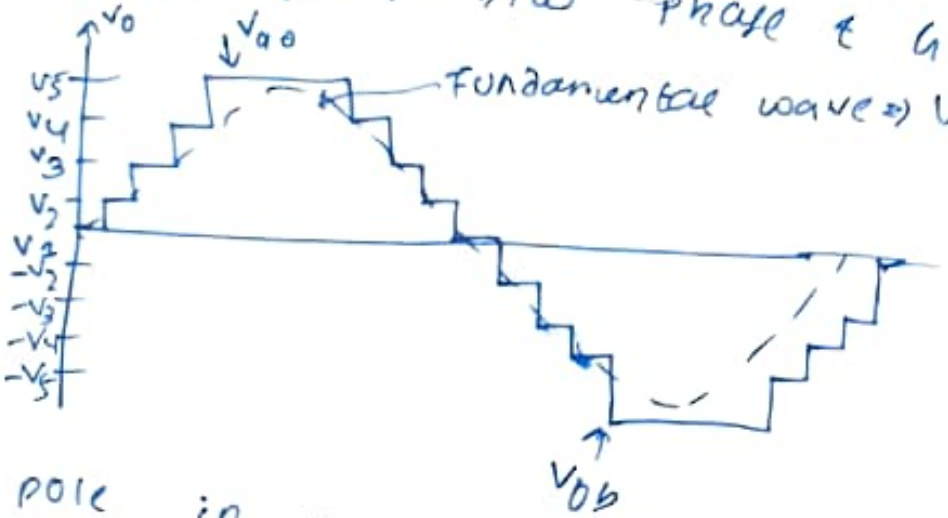
(3) have least switching freq. for each switching device

$$E_m = \frac{V_{dc}}{m-1}$$

m = no. of levels.
↳ No. of nodes to which inverter is accessible.

∴ m-level inverter needs (m-1) capacitors.

O/P voltage V_o = "V" b/w phase & GND pole



A pole in MLI ⇒ single-pole, multiple-throw switch.

I/P d.c voltage ⇒ $V_1, V_2, \ldots$

I/P d.c Currents ⇒ $I_1, I_2, \ldots$

V_a, V_b, V_c ⇒ rms value Line-voltages

I_a, I_b, I_c ⇒ rms line load currents.

By connecting to any node we can access the voltage level.

→ The actual realizth of switch requires bidirectional switching devices of each node.

Topology of MLI must have

(1) Less switching devices as far as possible.

(2) Capable of withstanding very high i/p voltage for high-power applications

(3) have lower switching freq. for each switching device

Types of MLI:-

→ The general structure of MLI is to get near sinusoidal voltage from several levels of dc-voltages

↓

obtained by capacitor voltage sources

No. of voltage levels ↑ ⇒ no. of steps ↑ se o/p

Staircase waveform.

↓

reduces THD at o/p wave approaching zero as m ↑ se

o/p V- at +ve-half cycle = $V_{ao} = \sum_{n=1}^{m} E_n SF_n$

SF_n = switching or control fn of n^{th} node

↓

0 or 1

Generally $E_1, E_2, \ldots E$ capacitor trimmed voltages) are all same E_m.

$V_{ao(peak)} = (m-1)E_m = V_{dc}$ → peak o/p voltage

→ To generate +ve & -ve values, there is another switch for -ve-values.

V_{ob} => -ve half

$$V_{ab} = V_{ao} + V_{ob} = V_{ao} - V_{bo}$$

1) Diode-clamped MLI → Diodes for clamping voltage.

2) Flying capacitor MLI → capacitor for clamping

3) Cascade MLI → Uses seperate H-bridge

↓

Most superior o/p waveform

each H-bridge needs seperate D.C voltage source

↓

Does not require any voltage-clamping diodes or voltage-balancing capacitors.

Diode-clamped MLI :-

DC MLI ⇒ m-level inverter needs (m-1) capacitors on dc-bus and produces m-levels on phase voltage.

m-level inverter leg → (m-1) capacitors

2(m-1) switching devices

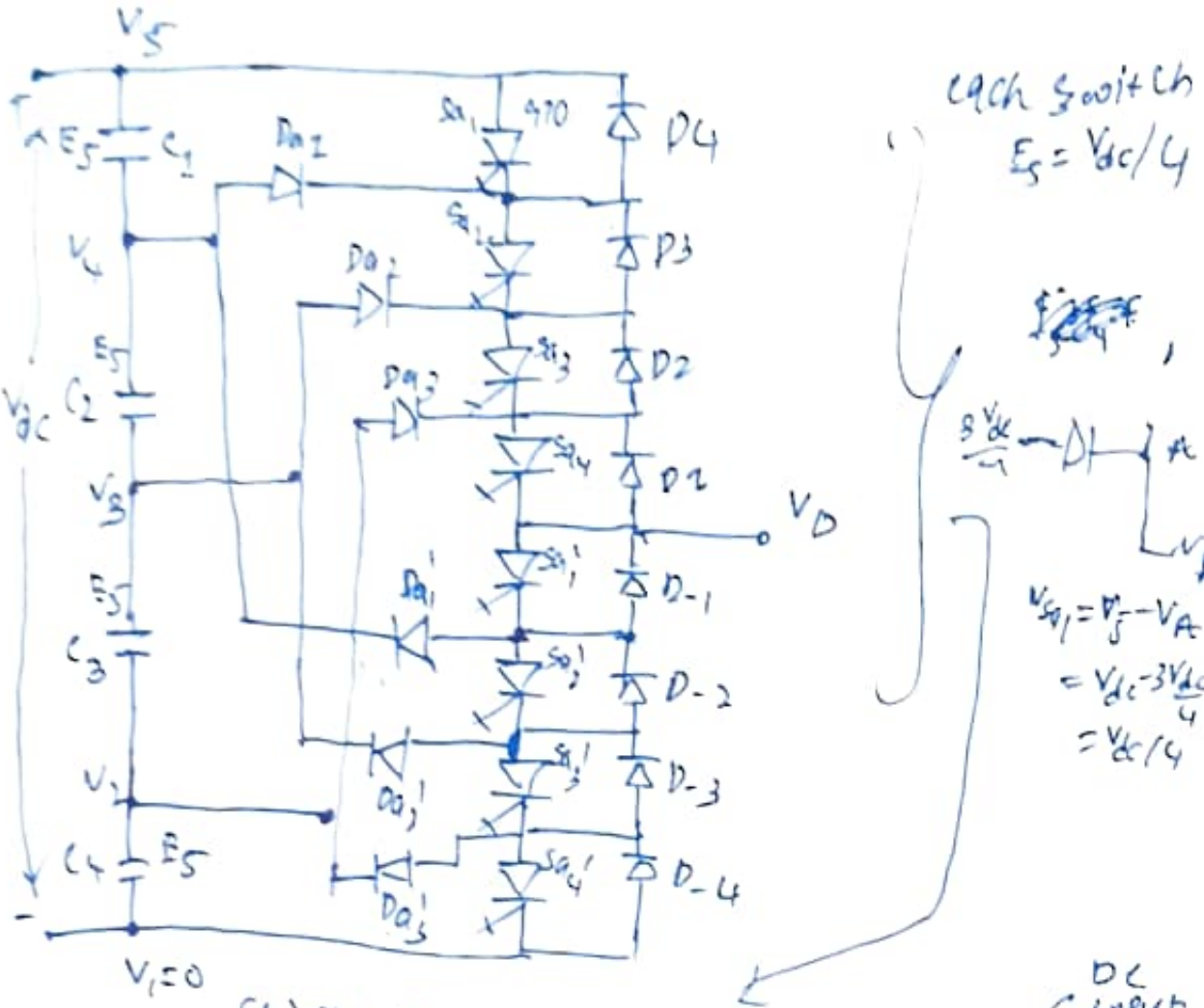
(m-1)(m-2) clamping diodes.

⇒ Sa_1, Sa_2, Sa_3, Sa_4, Sa_1', Sa_2', Sa_3', Sa_4'

switches

→ 4 capacitors ⇒ C_1, C_2, C_3 & C_4

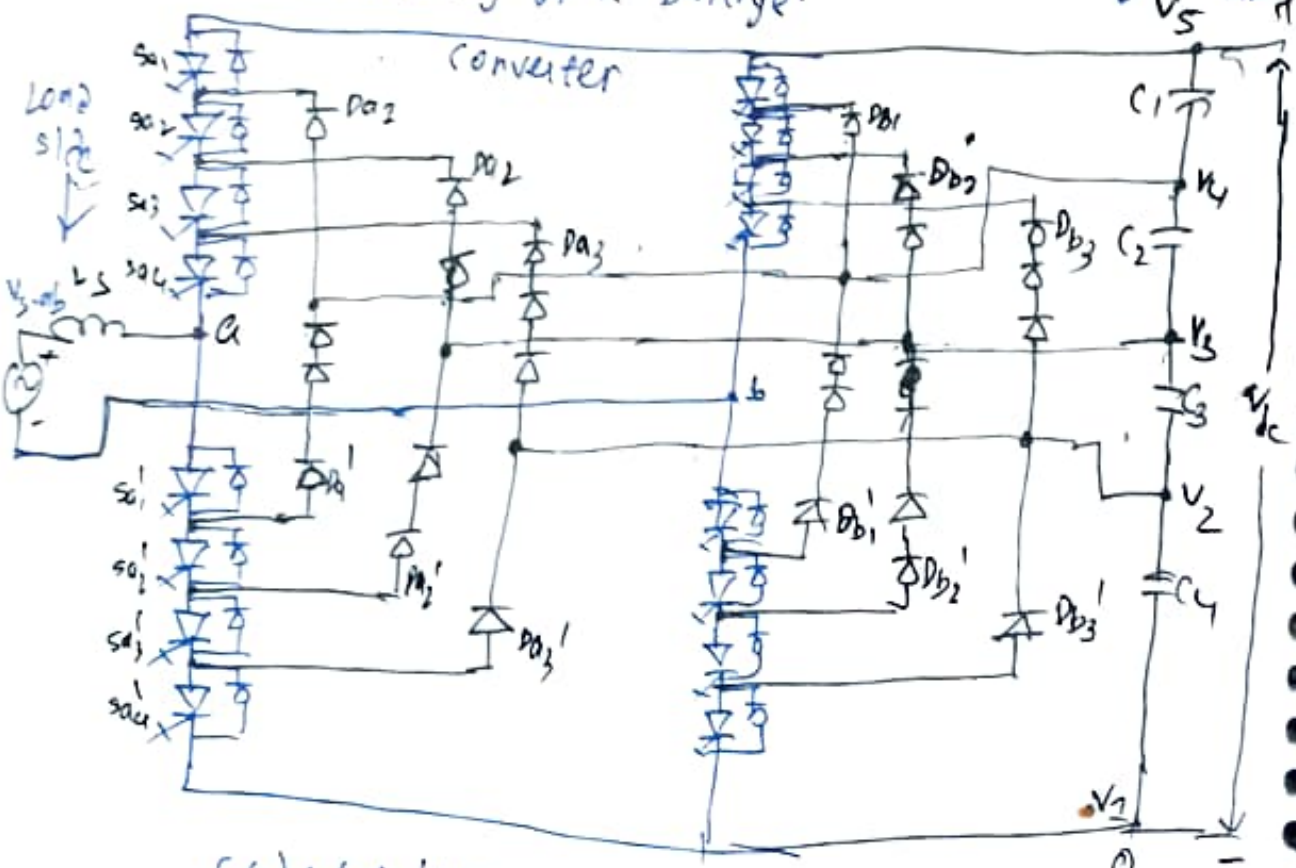
→ $V_{dc}/4$ → ~~[illegible]~~ m = 5 levels.



each switch
$E_5 = V_{dc}/4$

$V_{Sa_1} = V_5 - V_A$
$= V_{dc} - 3V_{dc}/4$
$= V_{dc}/4$

(a) one leg of a bridge.



(b) 1 ϕ- bridge.

principle of operation:-

→ consider one leg 5-level inverter

→ dc rail 0 is ref pt of o/p phase voltage.

1. For o/p voltage level $V_{ao} = V_{dc}$ (Turn on upper-half switches Sa_1 through Sa_4)

2. For an o/p voltage level $V_{ao} = 3V_{dc}/4$ (Turn on 3-upper switches Sa_2 through Sa_5 and one lower switch Sa_1').

⁂ ↓

Now Sa_2, Sa_3, Sa_4 alone give $3V_{dc}/4$ but its not stage by itself because:-

1. as we need defined return path for load current.

2. A defined blocking condition for rest of stack so that no single IGBT is asked to block more voltage than it's rated for.

Sa_1' act like to solidify o/p node & give low-impedance path that keeps node from floating.

→ Need for clamping??

↓

Da_1, Da_2, ... ⇒ diode-clamp

when certain switches are OFF, the diodes connect intermediate switch node to correct capacitor level.

that clamps the voltage on the node so no single OFF device is forced to hold more than $V_{dc}/4$

Eg:-

If sa_2 is OFF but sa_2 is ON node b/w them would float. somewhere b/w V_5 & V_4 that could place more than one capacitor's worth of voltage across sa_1 or sa_2.

clamp diode fix that floating node to exactly $V_4 = 3V_{dc}/4$

each switch just sees $\frac{1}{4} V_{dc}/4$

3. For $V_{10} = V_{dc}/2$

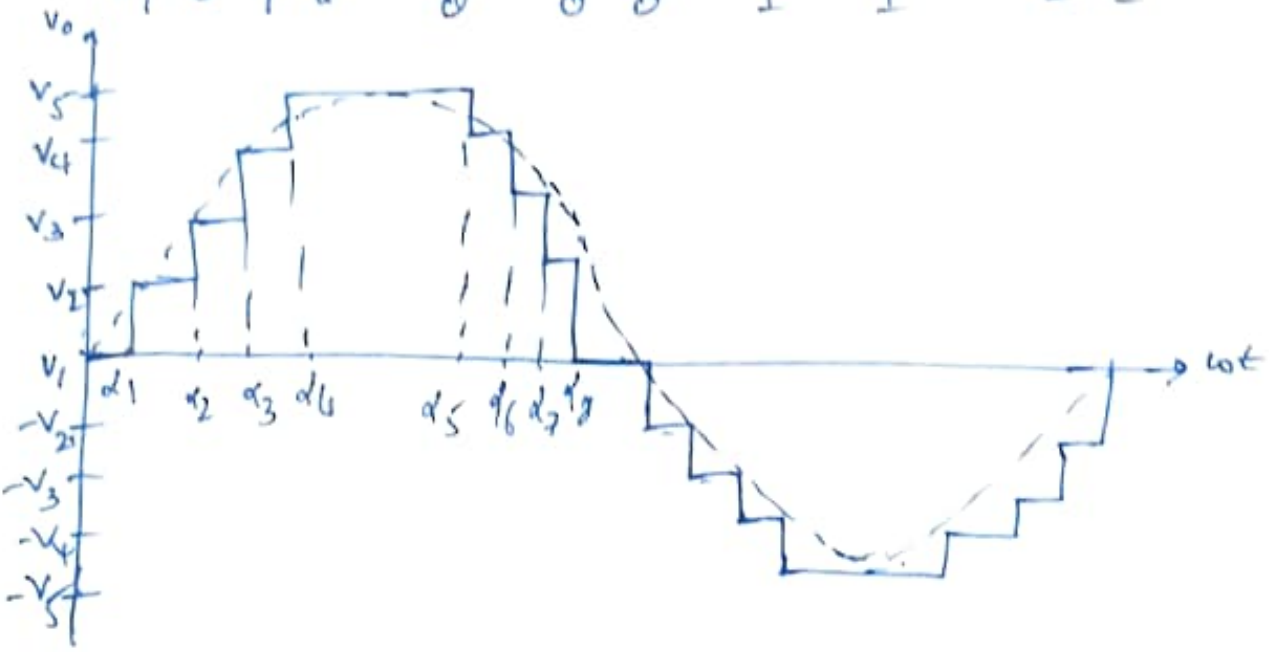
⇒ sa_3, sa_4 - ON & sa_1' & sa_2' OFF

4. $V_{a0} = V_{dc}/4$ ⇒ sa_4 → ON

sa_1', & sa_3' → ON

5. For $V_{ao} = 0$ ⇒ Sa_1' to Sa_4' → on.

V_{ao}	Sa_1	Sa_2	Sa_3	Sa_4	Sa_1'	Sa_2'	Sa_3'	Sa_4'
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1



1. High-voltage rating for blocking diodes:

→ each switching device requires only $\frac{V_{dc}}{m-1}$ block voltage capacity

→ clamping diode needs different reverse voltage blocking rating

⇓

when Sa_1' through Sa_4' are turned on diode D_{a_1} needs to block 3 capacitor voltage or $3V_{dc}/4$; diodes D_{a_2} & D_{a_3} need to block

$2V_{dc}/4$ & D_{a3} needs to block $V_{dc}/4$

→ each clamping diode gets uneven distribution.

$$V_D = \frac{m-1-k}{m-1} V_{dc}$$

↓ blocking voltage of each diode.

m = no. of levels
k = 1 to (m-2)
V_{dc} ⇒ total dc-link voltage.

→ If blocking voltage rating of each diode is same as that of switching device.

No. of diodes for each phase

$$N_D = (m-1) \times (m-2)$$

For $m = 5$

$N_D = (5-1) \times (5-2) = 12$

So for m is large it becomes impractical as we need so many diodes.

↓ limits no. of levels.

2. Unequal switching device rating

↓

S_{a1} conducts only during $V_{a0} = V_{dc}$ whereas S_{a4} conducts over entire cycle except during $V_{a0} = 0$

↓

Different current ratings for switching devices

So upper switches may be oversized & lower switches may be undersized

So $2 \times (m-2)$ upper devices oversize

3. Capacitor voltage unbalance.

↓

voltage levels at capacitor terminals are different, current supplied is also different.

→ When operating at unity power factor, the discharging time for inverter operation (or charging time for rectifier operation) for each capacitor is different.

↓

Such capacitor charging profile repeats every half-cycle & result in unbalanced capacitor voltages $\Rightarrow$ diff. levels.

∴ The voltage imbalance in MLI is resolved by using approaches such as replacing capacitors by controlled constant dc-voltage source, PWM voltage regulators or batteries.

Adv. Of MLI :-

1. No. of levels high enough - THD is low
   - avoid need for filters
2. Inverter efficiency is high because all devices switched at fundamental freq.

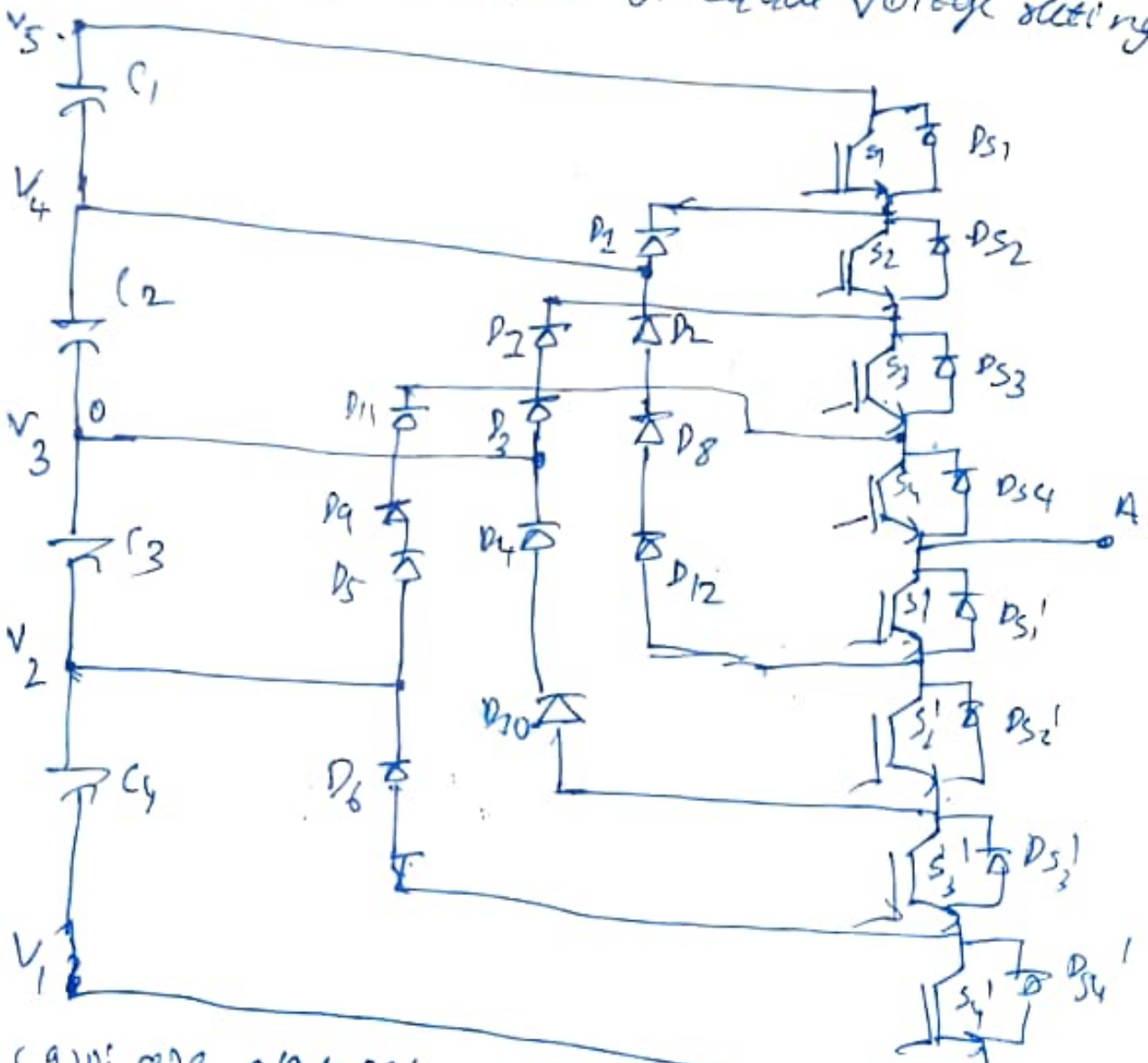
3. simple control method.

disadv. of MLI

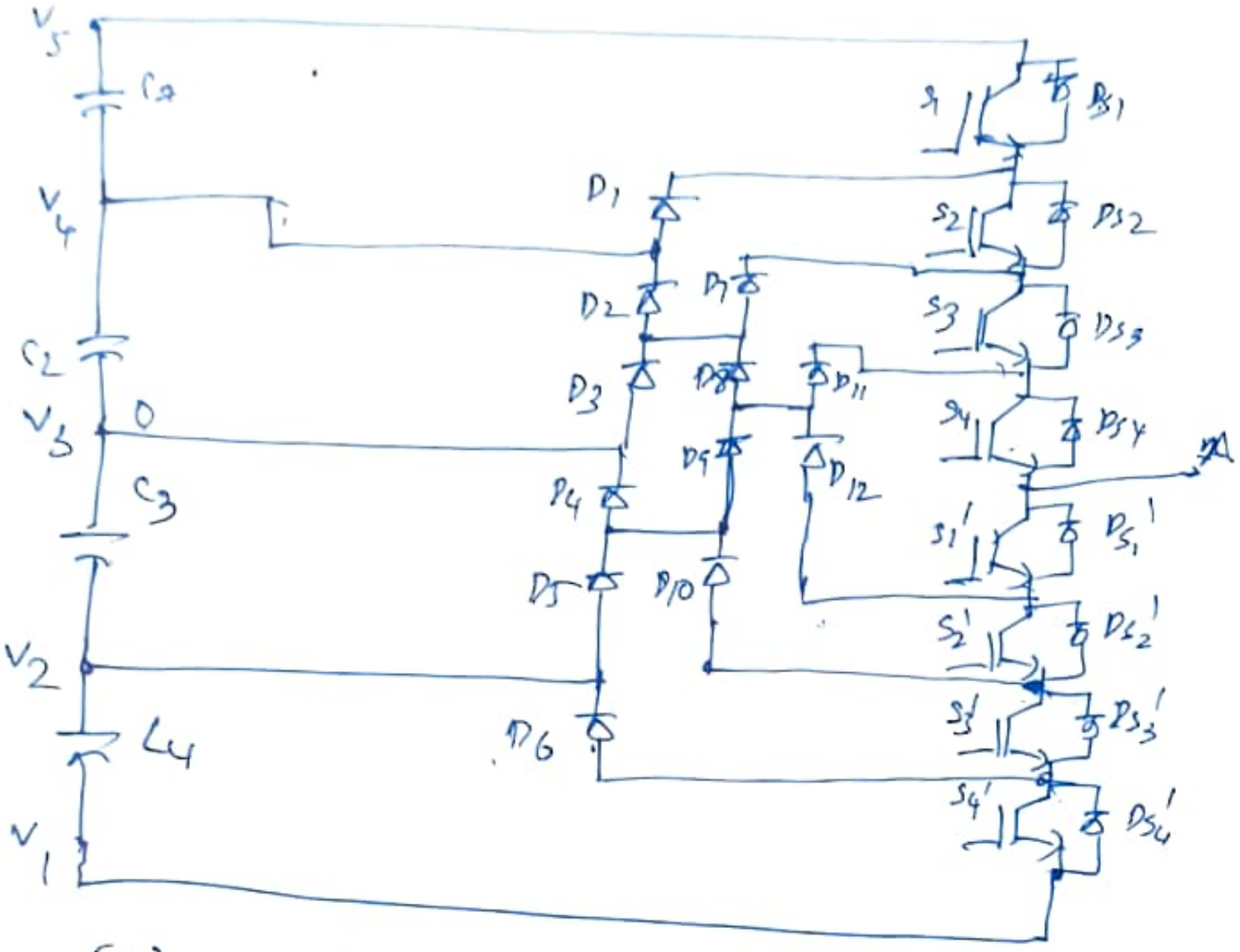
1. excessive clamping diodes for high levels
2. Difficult to control real power flow of individual converter in MLI.

Improved Diode-clamped MLI:-

8-switches & 12 diodes of equal voltage rating



(a) Diode clamped MLI with diodes in series.



(b) Modified Diode-clamped inverter with distributed clamping diodes.

→ Five level inverter requires

$m - 1 = 4$ caps

$2(m-1) = 8$ switches

$(m-1)(m-2) = 12$ clamping diodes

→ modified diode-clamped inverter is 3-level switching cells.

for m-level inverter there are (m-1) switching cells

$m = 5 \rightarrow 4$ cells.

In cell 1 → S_2, S_3 & S_4 are always ON
↳ S_1 & S_1' are switched alternatively to produce o/p voltage $V_{dc}/4$ & 'V_{dc}'/4

In cell 2 => S_3 & S_4 & S_1' are always ON
↳ S_2 & S_2' are switched alternatively ON to produce o/p voltage $V_{dc}/4$ & 0 ..

In cell-3 => S_4, S_1' & S_2' are ON always
↳ S_3 & S_3' switched alternatively to produce o/p voltage 0 & $-V_{dc}/4$.

In cell-4 => S_1', S_2' & S_3' are always ON
↳ S_4 & S_4' are switched alternatively to produce $-V_{dc}/4$ & $-V_{dc}/2$.

→ Each switching cell works as normal 2-level inverter, except each forward & freewheeling path in cell involves (m-1) devices instead of only one.

Eg:-

cell-2 =>

Forward path of up-arm

↓

D_1, S_2, S_3 & S_4

Freewheeling path of up-arm involves S_1'; D_{12}, D_8, & P_2 connecting inverter o/p to $V_{dc/4}$ level for either +ve or -ve current flow.

→ Forward path of down-arm

↓

S_1', S_2', D_{10} & D_4

→ Freewheeling path of down-arm involves

↓

D_3, D_7, S_3 & S_4. connecting inverter o/p to zero level for either +ve or -ve current flow

1. At any moment there must be (m-1) neighboring switches that are on.

2. For each two neighbouring switches, the outer switch can only be turned on when inner switch is on.

3. For each two neighbouring switches, inner switch can only be turned off when outer switch is off.

Flying Capacitor MLI:-

→ Each phase leg has identical structure.

→ Assume each capacitor has same voltage rating, the series connection of capacitors indicates the voltage b/w clamping points.

→ 3-inner loop balancing caps. (C_{a1}, C_{a2} & C_{a3}) for phase-leg a are independent from those of phase-leg b.

All phase legs share same DC-link capacitors C_1 through C_4.

→ voltage level for flying capacitors converter is similar to that of DCMLI

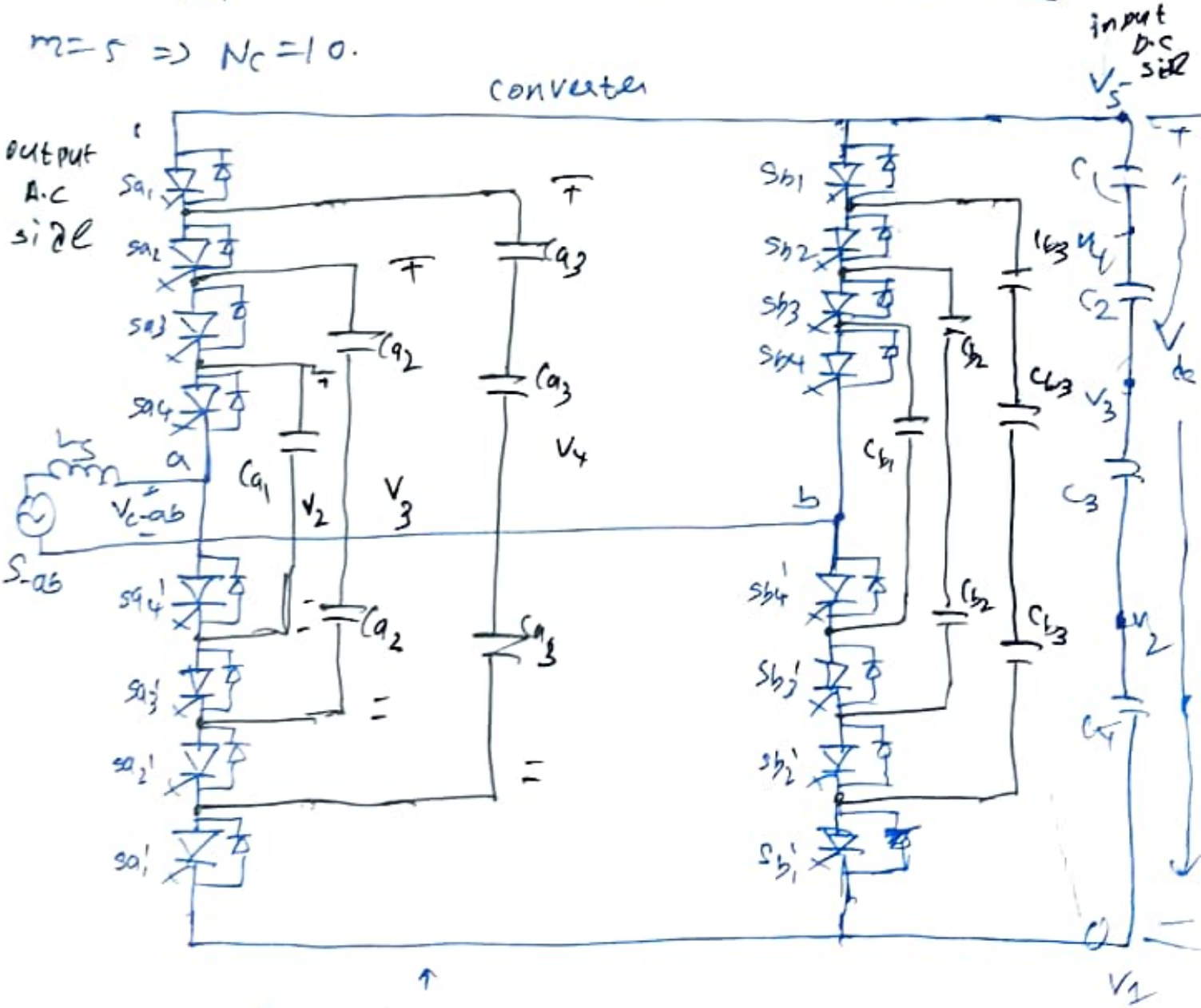
m-level converter → V_{ao}

line voltage V_{ab} → (2m-1) levels

DC-bus needs → (m-1) capacitor for m-level conv.

$$N_c = \sum_{j=1}^{m} (m-j) \rightarrow \text{No. of capacitors per phase}$$

$m=5 \Rightarrow N_c = 10.$



(a) FC MLI 1 Ø- inverter.

Operation:-

1. For an o/p $V_{ao} = V_{dc}$ · turn on all upper-half S_{a1} to S_{a4}
2. For an o/p $V_{ao} = 3V_{dc}/4$ there are 4-combinations:
   a. $V_{ao} = V_{dc} - \frac{V_{dc}}{4}$ · by turn on S_{a1}, S_{a2}, S_{a3} & S_{a4}'

(Each individual flying capacitor is regulated around $V_{dc}/4$ (step size).

↓

this way each time you route through a bank (by turning lower device of that cell ON), you introduce one step of $\frac{V_{dc}}{4}$ drop in path from V_f down to node a.

↓

Standard for n-level-FC Inv

→ Polarity of F.C is oriented so that when you traverse from top rail V_f through a cell's power path, the capacitor's stored voltage opposes the bus (i.e, it subtracts a step). That is why we drop $\frac{V_{dc}}{4}$ per lower device in conduction path & count drops

to get V_{a0}

$V_{a0} = V_{dc} - n \cdot \frac{V_{dc}}{4} = (4-n)\frac{V_{dc}}{4}$

b. $V_{a0} = \frac{3V_{dc}}{4} \Rightarrow$ ON Sa_2, Sa_3, Sa_4 & Sa_1'

c. $V_{a0} = V_{dc} - \frac{3V_{dc}}{4} + \frac{V_{dc}}{2} \Rightarrow$ ON
Sa_1, Sa_3, Sa_4 & Sa_2'

$\Rightarrow V_S$ goes to Sa_1 through $Ca_3 \Rightarrow$ 3-caps & Sa_2' & caps thru to Sa_3, Sa_4

So KVL $\Rightarrow V_{a0} = V_{dc} - 3 \times (V_{Ca_3}) + 2 \times (V_{Ca_2})$

$V_{Ca_3} = V_{a(3)} = \frac{V_{dc}}{4}$

d. $V_{a0} = V_{dc} - \frac{V_{dc}}{2} + \frac{V_{dc}}{4} \Rightarrow$ ON $\Rightarrow Sa_1, Sa_2, Sa_4$ & Sa_3'

NOTE: UP to down for F.C $\Rightarrow$ subtract voltage traversing

down to up for FC $\Rightarrow$ add voltage traversing

$V_{a0} = V_{dc} - 2 \times (V_{Ca_2}) + 1 \times V_{Ca_1} = V_{dc} - 2 \times \frac{V_{dc}}{4} + \frac{V_{dc}}{4}$
$= V_{dc} - \frac{V_{dc}}{2} + \frac{V_{dc}}{4}$

3. For $V_{a0} = \frac{V_{dc}}{2} \Rightarrow$ 6-combination.

a. $V_{a0} = V_{dc} - \frac{V_{dc}}{2} \Rightarrow Sa_1, Sa_2, Sa_3'$ & Sa_4'

b. $V_{a0} = \frac{V_{dc}}{2} \Rightarrow$ ON Sa_3, Sa_4, Sa_1' & Sa_2'

NOTE:-

The FC-caps get $\frac{V_{dc}}{4}$ supposed drop equal we need to configure them to do so

1) start-up precharge: you use controlled sequence through switches to connect a given bank briefly to appropriate dc-link node(s), or you use auxiliary pre-charge path. (resistors or small converters). This brings C_{a1} to $\frac{V_{dc}}{4}$, the C_{a2} series pair to $V_{dc}/2$ & C_{a3} to $3\frac{V_{dc}}{4}$ before normal normal pwm begins.

2) Balancing during operation: Duty pwm, flying caps naturally charge or discharge depending on load current direction & which redundant state you pick at a given o/p-level.

→ phase-shifted carrier pwm already provides natural balancing.

---

c. $V_{a0} = V_{dc} - 3\frac{V_{dc}}{4} + \frac{V_{dc}}{2} - \frac{V_{dc}}{4}$

$\Downarrow$

ON S_{a1}, S_{a3}, S'_{a2} & S'_{a4}

$V_{a0} = V_{dc} - 3 \times V_{ra3} + 2 \times V_{ra2} - V_{ra1}$

2. $V_{a0} = V_{dc} - 3\frac{V_{dc}}{4} + \frac{V_{dc}}{4}$ => ON sa_1, sa_4, sa_1' & sa_3'

e. $V_{a0} = 3 \cdot \frac{V_{dc}}{4} - \frac{V_{dc}}{2} + \frac{V_{dc}}{4}$ => ON sa_2, sa_4, sa_1' & sa_3

f. $V_{a0} = 3\frac{V_{dc}}{4} - \frac{V_{dc}}{4}$ => ON sa_2, sa_3, sa_1' & sa_4'

4. $V_{a0} = \frac{V_{dc}}{4}$ => 4 - combinations

a. $V_{a0} = V_{dc} - 3\frac{V_{dc}}{4}$ => ON sa_1, sa_2', sa_3' & sa_4'

b. $V_{a0} = \frac{V_{dc}}{4}$ => ON sa_4, sa_1', sa_2' & sa_3'

c. $V_{a0} = \frac{V_{dc}}{2} - \frac{V_{dc}}{4}$ => ON sa_3, sa_1', sa_2' & sa_4'

d. $V_{a0} = 3\frac{V_{dc}}{4} - \frac{V_{dc}}{2}$ => ON sa_2, sa_1', sa_3' & sa_4'.

5. $V_{a0} = 0$ => ON all lower switches sa_1' to sa_4'

V_{ao}	Sa_1	Sa_2	Sa_3	Sa_4	Sa_4'	Sa_3'	Sa_2'	Sa_1'
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = \frac{3V_{dc}}{4}$	1	1	1	0	1	0	0	0
$V_3 = \frac{V_{dc}}{2}$	1	1	0	0	1	1	0	0
$V_2 = \frac{V_{dc}}{4}$	1	0	0	0	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

Features of MLI:-

1. Large No. of caps: The inverter requires a large no. of storage capacitors. Assuming that the voltage rating of each caps is same as that of switching device. m-level convel converter requires a total of $(m-1) \times \frac{(m-2)}{2}$ auxiliary caps per phase leg in addition to $(m-1)$ dc bus caps.

For m-level diode-clamp inverter only requires $(m-1)$ caps. of same voltage rating. ($m=5$, $N_c = 4 \times \frac{3}{2} + 4 = 10$ compared to $N_c = 4$ for diode clamped).

2. Balancing capacitor voltages: unlike DCMLI, FCMLI has redundancy at its inner voltage levels.

⇒ A voltage level is redundant if two or more valid switch combinations can synthesize it. The availability of voltage redundancies allows controlling individual cap. voltages. In producing same O/P voltage, the inverter can involve different combinations of capacitors, allowing preferential charging or discharging individual caps.

⇓

flexibility allows to manipulate cap. voltages & keep them proper value.

→ For mid-level voltages (i.e $3\frac{V_{dc}}{4}$, $\frac{V_{dc}}{2}$ & $\frac{V_{dc}}{4}$) the ~~other~~ can employ various switching combinations in one or several o/p cycles to balance charging & discharging of capacitors. Thus, by proper selection of switch combination, it becomes very complicated. But real power conversions is possible but switching freq. needs to be higher than fundamental freq.

adv of FC-MLIL

1. Large amounts of storage capacitors can provide ride-through capabilities during power outages.
2. These inverters provide switch combination redundancy for balancing different voltage levels
3. Like DC-MLI with more levels, harmonic content is low enough to avoid need for filters.
4. Both real & reactive power flow can be controlled.

Dis adv

1. Excessive storage caps required for higher level inverters. Hard to package bulky caps & expensive.
2. The inverter control can be very complicated & switching freq. & switching losses are high for real power transmission.

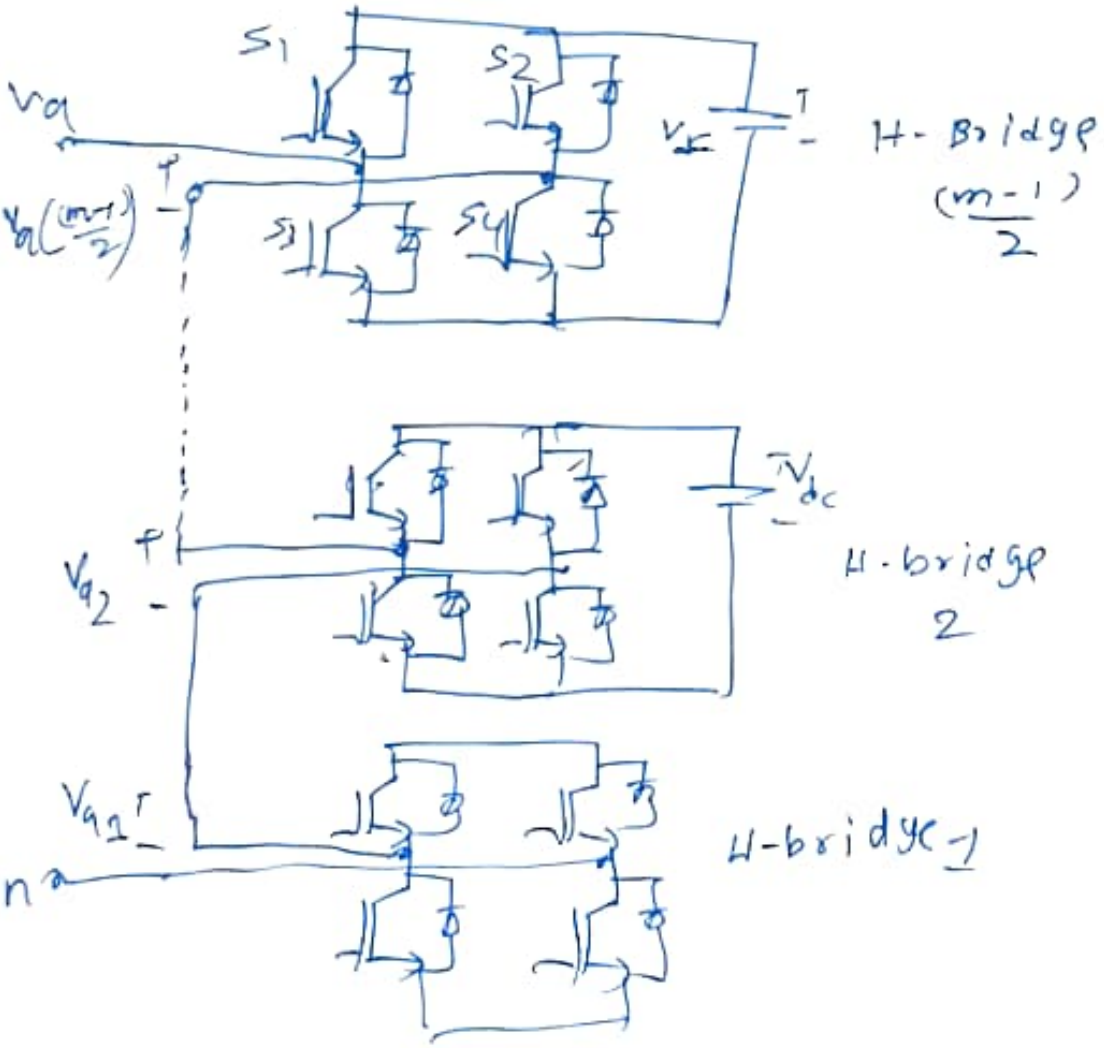
CASCADED MLI:-

series of H-bridge (2Φ, full bridge) inverter units.

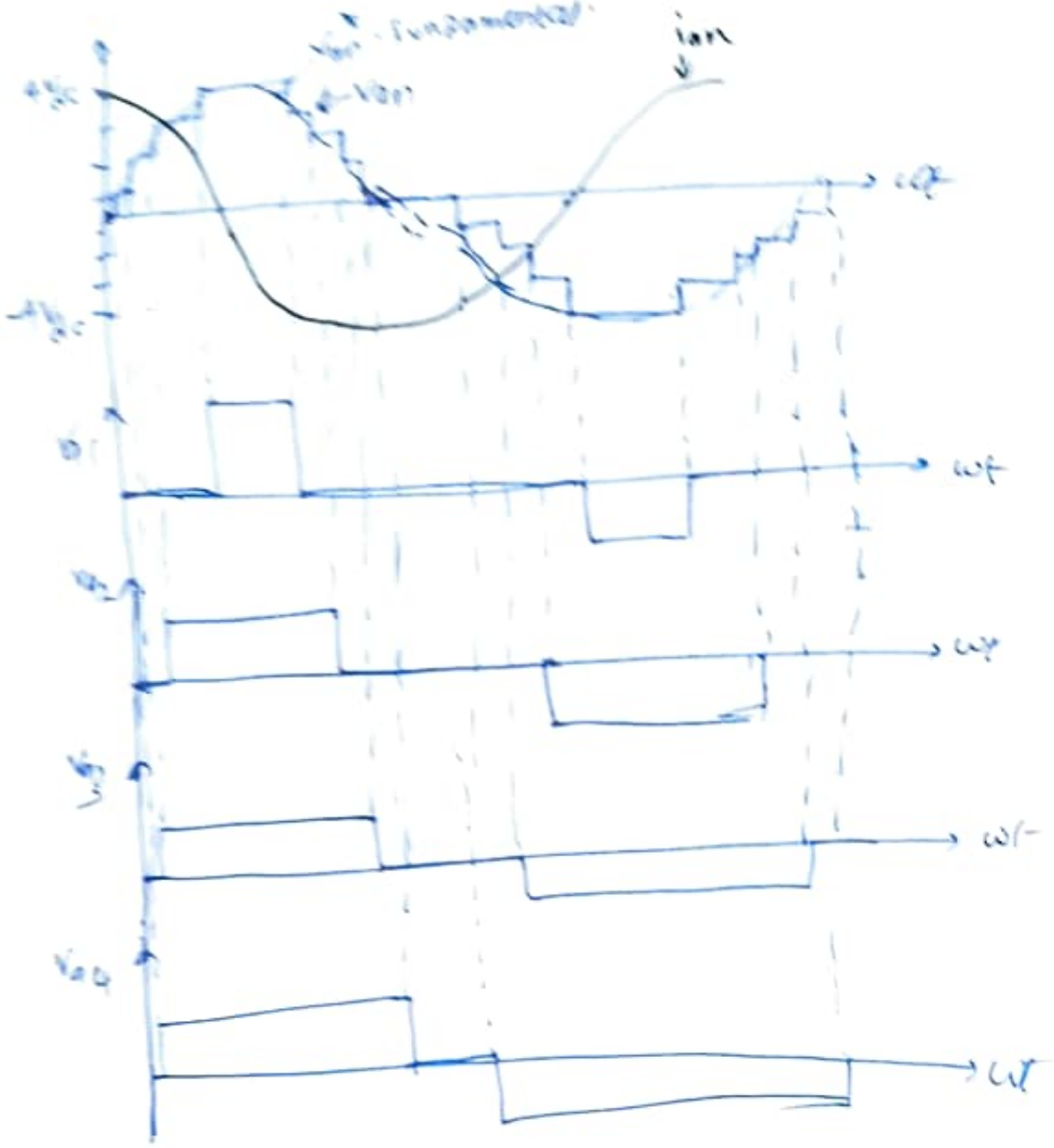
⇓

generation of this MLI is to synthesize desired voltage from several separate dc-sources which may be batteries, fuel cells, solar cells.

→ do not require voltage-clamping diodes or voltage-balancing capacitors.



circuit diagram.



(a) O/p waveform of 9-level phase voltage.

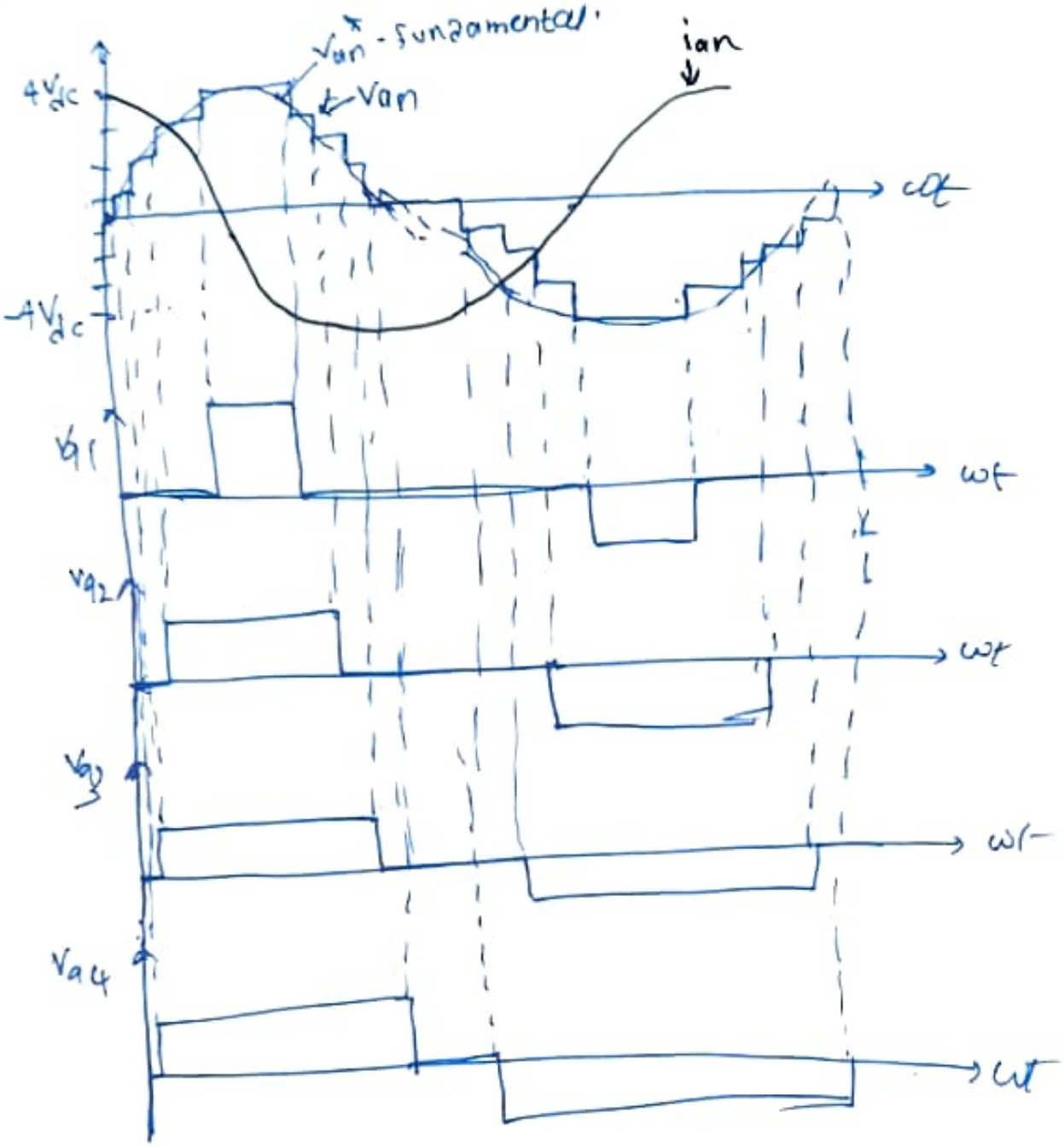
→ All individual o/p's are summed

$$V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4}$$

Each inverter level can generate 3 different voltage o/p's,

↳ (+V_{dc}, 0, -V_{dc})

4-switches S_1, S_2, S_3 & S_4.



(b) o/p waveform of 9-level phase voltage.

→ All individual o/p's are summed

$$V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4}$$

Each inverter level can generate 3 different voltage o/p's,

↳ ($+V_{dc}$, 0, $-V_{dc}$)

4 switches S_1, S_2, S_3 & S_4.

* Turing on S_1 & S_4 $\Rightarrow$ $V_{ab} = +V_{dc}$
* Turing on S_2 & S_3 $\Rightarrow$ $V_{ab} = -V_{dc}$
* Turing off all switchs $\Rightarrow$ $V_{ab} = 0$

Each level ac-o/p voltage is same way obtained.

N_s = no. of dc sources

o/p-phase voltage level $\Rightarrow$ $\boxed{m = N_s + 1}$

→ For a 5-level cascaded inverter needs 4-SDCs & 4-full bridge

o/p voltage of inverter is almost sine & has THD less than 5%

↓

each H-bridge switching only at fundamental freq.

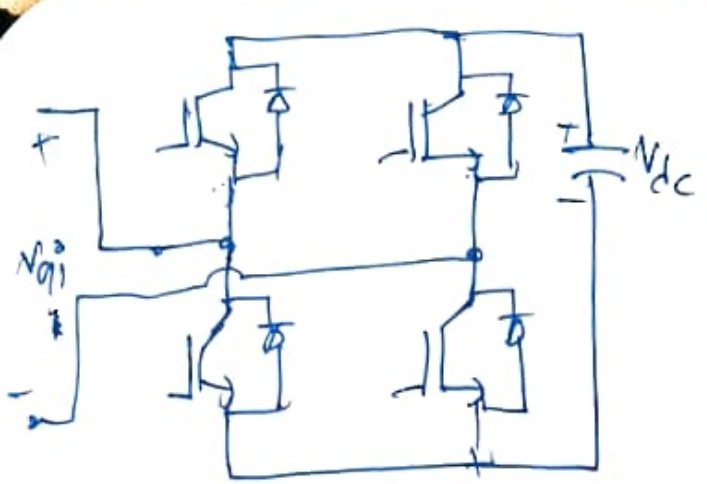
→ phase current i_a is sinusoidal and leads or lags phase voltage V_{an} by 90°

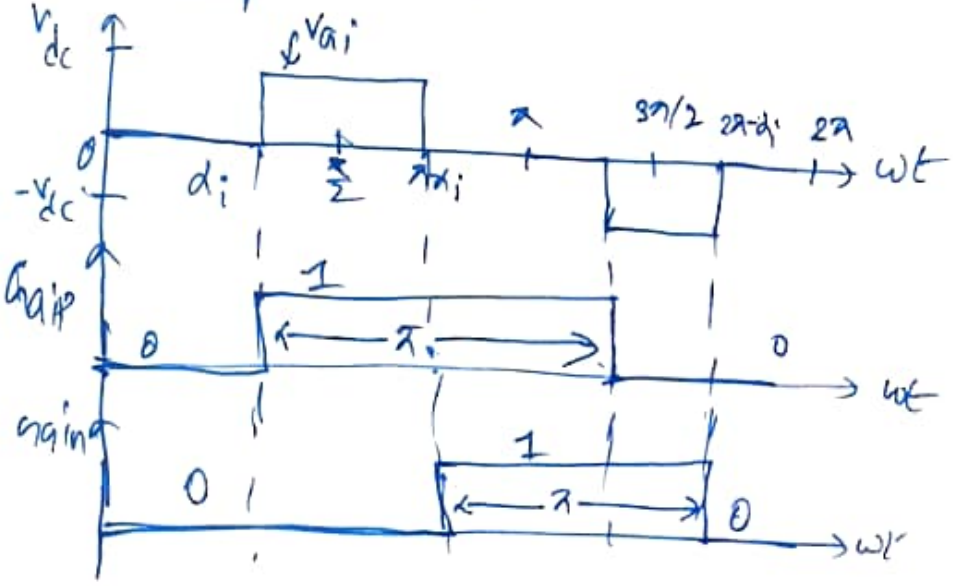
∴ avg. charge to each ac-cap is zero over one-cycle. so all SDCs-caps can be balanced (voltage).

→ Each H-bridge generates quasi-square wave of an H-bridge

→ Each switching device conducts for 180° ($\frac{1}{2}$-cycle)

All ↓ switching device current stress equal.





Gaip, Gain is 1 if upper switch is on & 0 if lower switch is on.

(b) switching time.

Features of cascaded inverters:-

1) For real power conversion ac to dc and then dc to ac, the cascaded inverters need seperate dc-sources. The structure of seperate dc-sources is well suited for various renewable energy sources such as fuel cell, photovoltaic and bio mass

2) connecting dc source b/w 2 converters in back-to-back fashion is not possible because a short ckt is introduced if 2-converters are not switching synchronously.

adv:-

→ Compared to diod-clamped & flying capacitor inv, it requires least no. of components to achieve same no. of voltage levels

→ optimized circuit layout & packaging are possible because each level has the same structure & no extra clamping diody Voltage-balancing caps.

→ soft-switching techniques can be used to reduce switching losses & device stress.

dis-adv:-

→ It needs seperate dc sources for real power conversions, thereby limiting its applications.

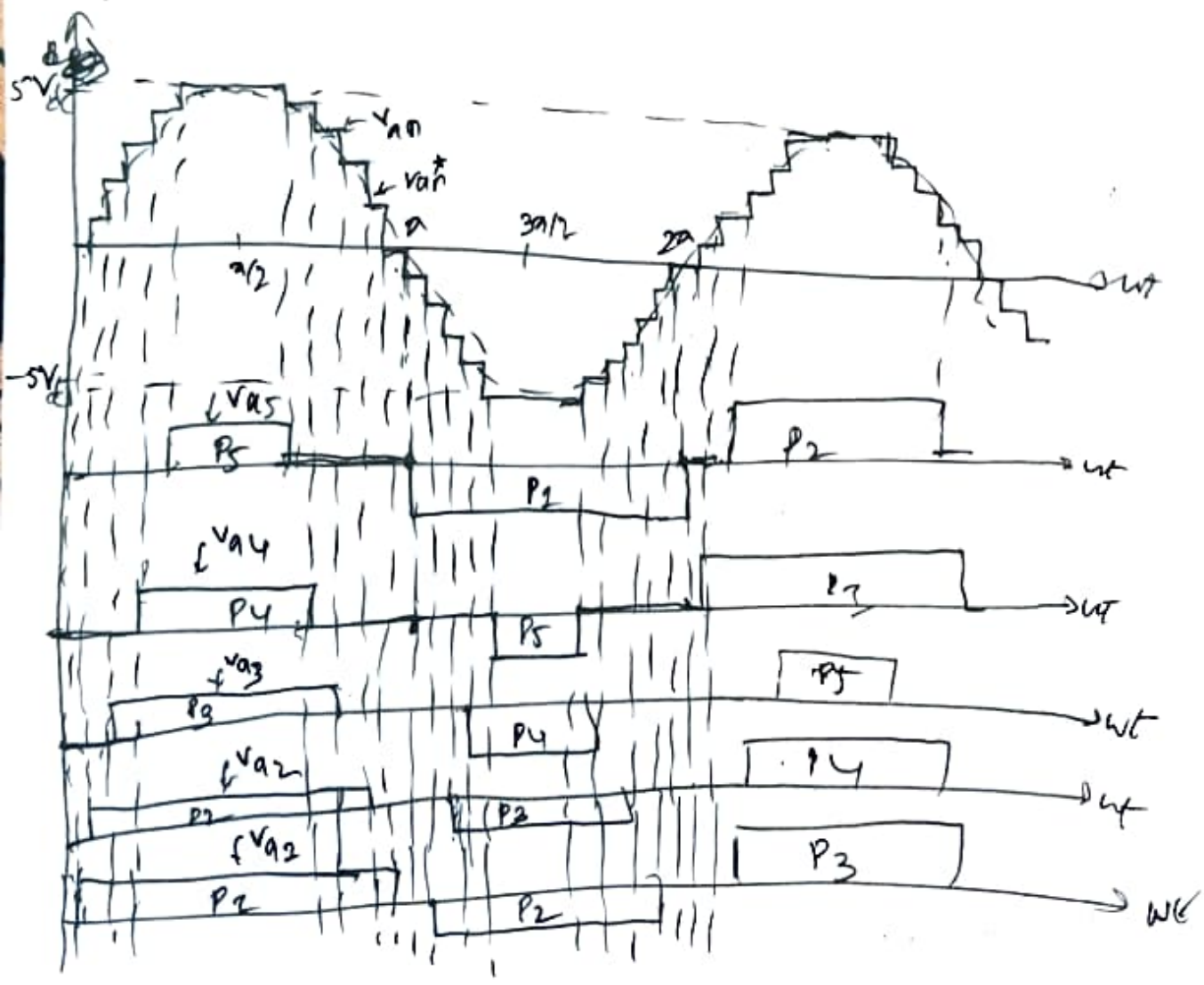
Q) Finding switching angles to eliminate specific harmonics

Phase voltage waveform for cascaded inverter for m=6 (including 0-level) is given

(a) Find generalized Fourier series of phase voltage.

(b) Find switching angles to eliminate 5th, 7th, 11th & 13th harmonics if peak fundamental phase voltage is 80% of its max. value.

(c) Find fundamental component B1, THD, & distortion factor (DF).



m-level cascaded inverter (including 0-level)

a) 1. $V_{an} = V_{a1} + V_{a2} + V_{a3} + \ldots + V_{am-1}$ ← o/p voltage.

due to quarter-wave symmetry along x-axis a_0 & a_n are zero.

$$b_n = \frac{4V_{dc}}{\pi}\left[\int_{d_1}^{\pi/2} \sin(n\omega t)\, d(\omega t) + \int_{d_2}^{\pi/2} \sin(n\omega t)\, d(\omega t) + \ldots + \int_{d_{m-1}}^{\pi/2} \sin(n\omega t)\, d(\omega t)\right]$$

$$= \frac{4V_{dc}}{n\pi} \sum_{j=1}^{m-1} \cos(n d_j)$$

$$V_{an}(\omega t) = \frac{4V_{dc}}{n\pi}\left[\sum_{j=1}^{m-1} \cos(n d_j)\right] \sin(n\omega t)$$

b. If peak o/p phase voltage $V_{an(peak)}$ must equal carrier phase voltage,

$$V_{cr(peak)} = (m-1)V_{dc}$$

$$M = \text{modulation index} = \frac{V_{cr(peak)}}{V_{an(peak)}} = \frac{V_{cr(peak)}}{(m-1)V_{dc}}$$

conduction angles $d_1, d_2, \ldots, d_{m-1}$ can be chosen to minimize THD of phase voltage.

Given $M = 0.8$

(peak fundamental voltage is 80% of max-value).

we need to eliminate 5th, 7th, 11th & 13th harmonics

Fourier series

$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) = 0$

$\cos(7\alpha_1) + \cos(7\alpha_2) + \ldots + \cos(7\alpha_5) = 0$

$\cos(11\alpha_1) + \cos(11\alpha_2) + \ldots + \cos(11\alpha_5) = 0$

$\cos(13\alpha_1) + \cos(13\alpha_2) + \ldots + \cos(13\alpha_5) = 0$

$\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) = (m-1)M$

$= 5 \times 0.8 = 4$

By solving by Newton-Raphson method we get

$\alpha_1 = 6.57°$, $\alpha_2 = 18.94$, $\alpha_3 = 27.18°$

$\alpha_4 = 45.15°$ & $\alpha_5 = 62.4°$

C. $B_1 = 5.093$ y. , THD = 5.078 y. & DF = 0.08%

MLI-applications:-

∴ utility systems for controlled source of reactive power.

→ In steady-state opetn, an inverter can produce controlled reactive current & act as static var-ampere reactive (VAR) compensator (STATCOM)

→ These inverters can reduce physical size of compensator.

→ High-voltage inverter makes possible direct connection to high-voltage (e.g. 13kV) distribution system, eliminating distribution T/F and reducing system cost.

→ Harmonic content of inverter can be reduced with control methods & η can be improved.

Most common applications are

(1) Reactive power compensation

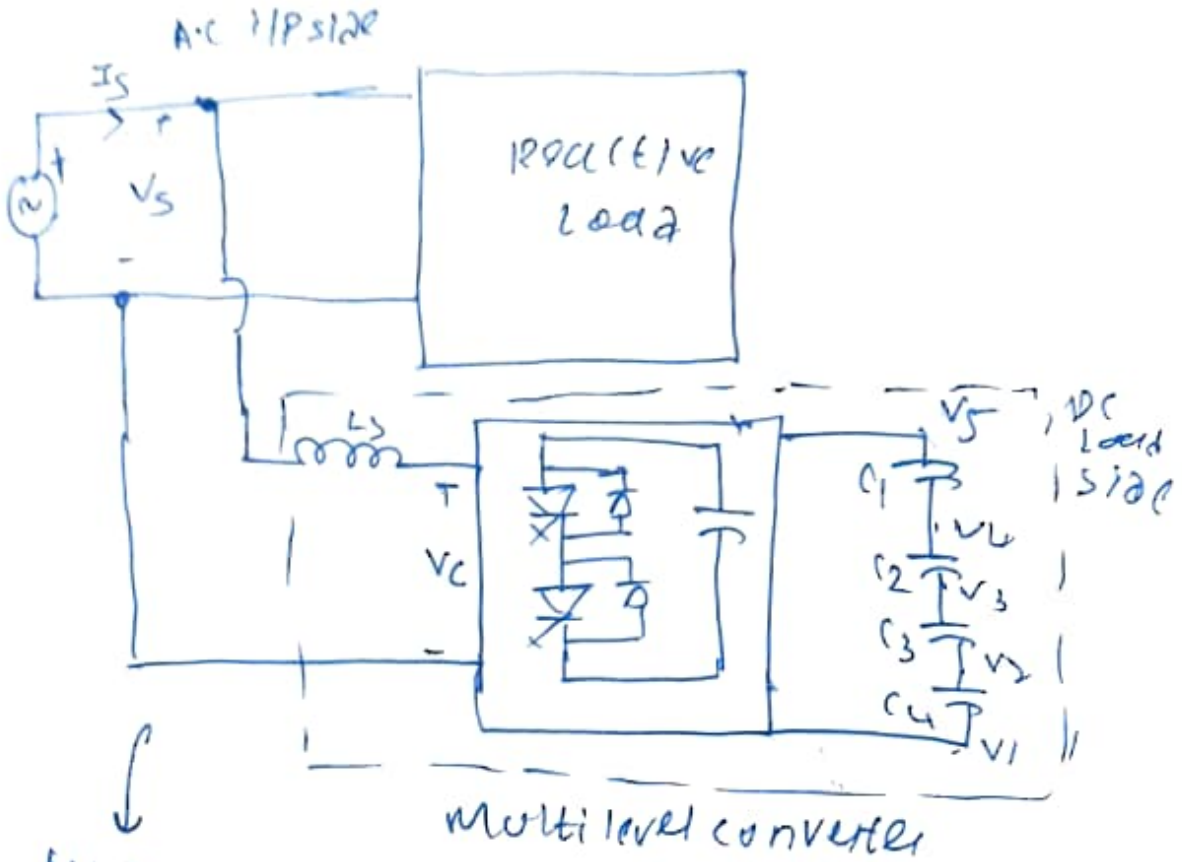
(2) back-to-back intertie

(3) Variable speed drives.

Reactive power compensation:-

→ Inverter converts dc voltage to an ac voltage with 180° phase shift (DC-AC converter). a controlled rectifier.

→ With purely capacitive load, the inverter operating as a dc-ac converter can draw reactive current from ac-supply.



.MLI - connected to a power system for reactive power compensation

Load side → connected to ac-supply

dc side → open (not connected to any de-voltage)

For control of reactive power flow, the inverter gate control is phase shifted by 180° & dc-side capacitors act as load

→ when MLI draws purely reactive power, phase voltage & current are 90°. a perfect capacitor charge & discharge can be balanced.

↓

Static - VAR generator (SVG)

All 3-types MLI can be used for reactive power

compensation without having high voltage unbalance problem

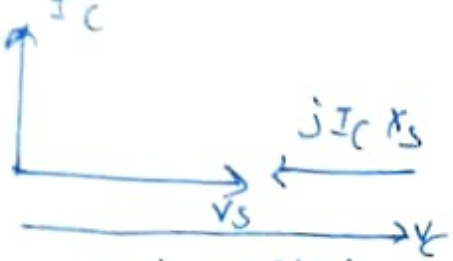
→ when MLI draws pure reactive power.

V_S (source voltage vector), V_c (converter voltage)

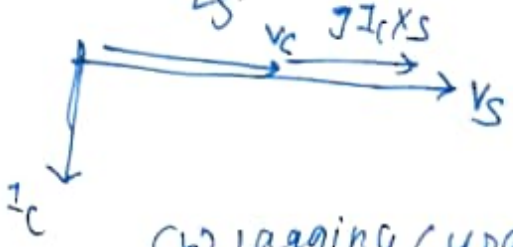
$V_S = V_c + j \cdot I_c \cdot X_S$

I_c → converter current vector.

X_S → reactance of inductor L_S



(a) Leading current



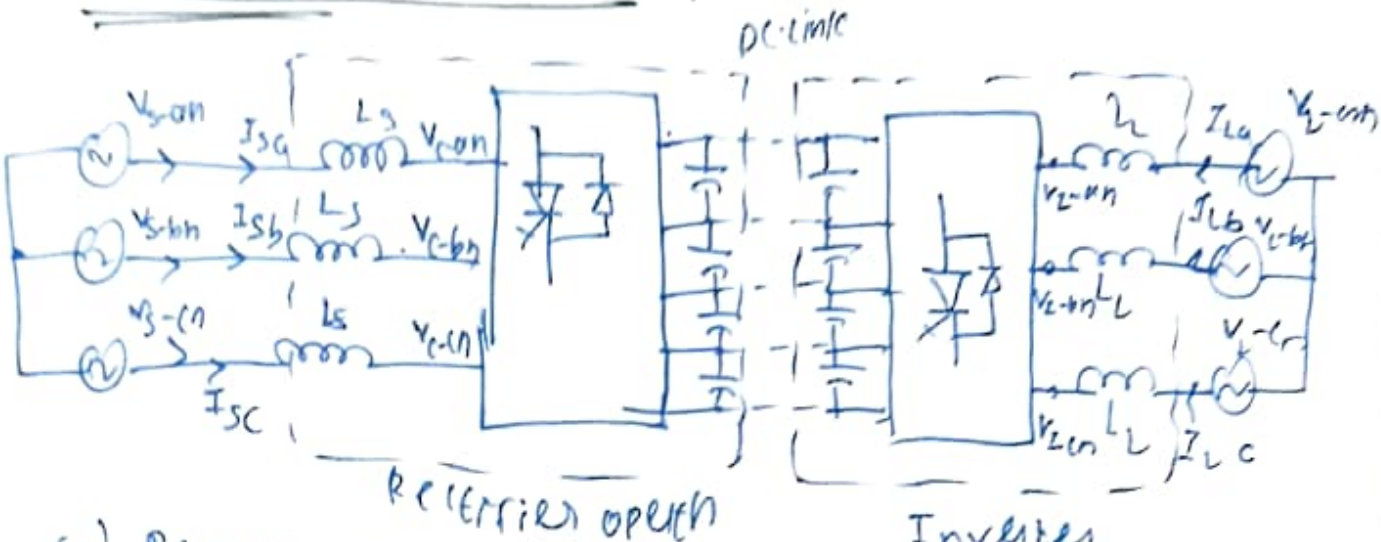
(b) Lagging current

Polarity & magnitude of reactive current is controlled by magnitude of V_c (converter voltage) → fn of dc-bus voltage & voltage modulation index.

$$B_n = \frac{4V_{dc}}{n\pi}\left[\sum_{j=1}^{\frac{m-1}{2}} \cos(n\alpha_j)\right]$$

$$V_{an}(\omega t) = \frac{4V_{dc}}{n\pi}\left[\sum_{j=1}^{\frac{m-1}{2}} \cos(n\alpha_j)\right] \sin(n\omega t)$$

Back-to-Back interlie:



(a) Back to Back interlie with 2-DCMLI

LH-side converter → rectifier for utility

RH-side converter → inverter to supply AC load

∴ Each switch remains on once per fundamental cycle.

↓

voltage across each-cap remains balanced & unbalanced capacitor voltages on each side tend to compensate each other.

↓

such DC-cap link is back to back tie it maintains staircase voltage.

→ connects 2-asynchronous systems can be regarded as

(1) freq changer

(2) phase shifter

(3) power flow controller

↓

bidirectionally controlled.

I_{source} → can be leading or lagging or in phase w.r.t V_{source}.

$V_{converter}$ → phase shifted from V_{source} with power angle − δ

If V_{source} is constant, then current or power flow can be controlled by $V_{converter}$

for δ = 0 → I_{source} is either 90° leading or lagging. Only reactive power is generated.

Adjustable (ASD) Speed drive:-

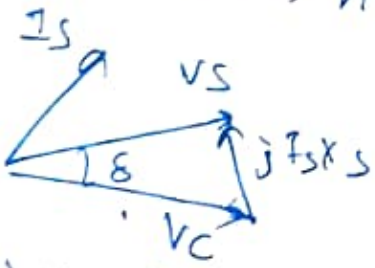
Back-to-Back interface applied to utility compatible ASD.

↓

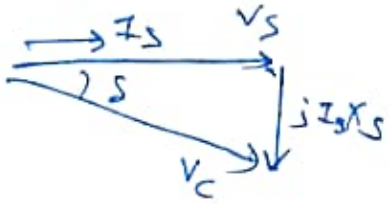
i/p = const. freq. A.C source from utility

o/p = variable freq. A.C load.

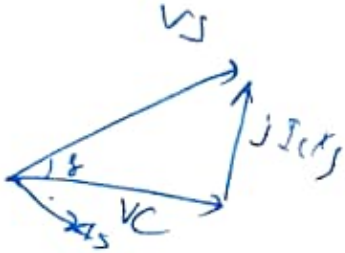
Ideally we need → unity pf
- → negligible harmonics
- → NO EMI.
- → high η.



(a) leading p.f



(b) unity p.f

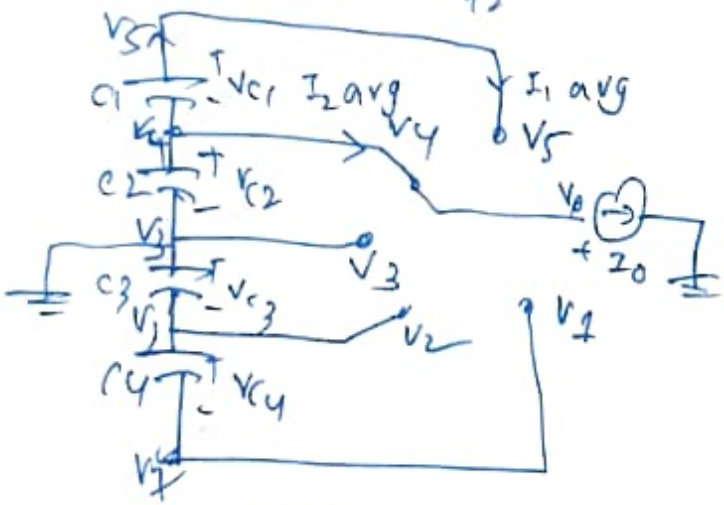


(c) Lagging p.f

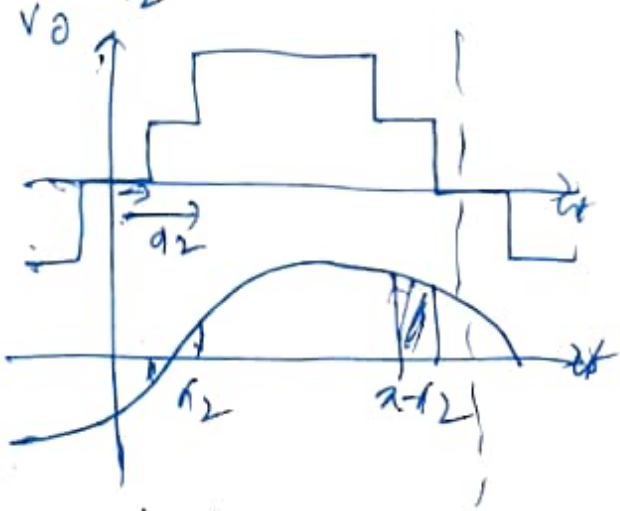
ASD needs to operate at different freq, the dc-link capacitor needs to be well sized to avoid a large voltage swing under dynamic conditions.

DC-Link capacitor voltage balancing :-

→ $I_{1(avg)} = \frac{1}{2\pi} \int_{\alpha_2}^{\pi-\alpha_2} i_0 \, d(\omega t) = \frac{1}{2\pi} \int_{\alpha_2}^{\pi-\alpha_2} I_m \sin(\omega t - \phi) \, d(\omega t)$



(a) 3-level half-bridge inverter.



(b) Distribution of load current

$$I_{1(avg)} = \frac{I_m}{\pi} \cos\phi \cdot (\cos\alpha_2)$$

$$i_0 = I_m \sin(\omega t - \phi)$$

Voltage balancing of capacitors using as energy tank is important for MLI to work satisfactorily.

$$I_{2(avg)} = \frac{1}{2\pi}\int_{\alpha_1}^{\alpha_2} i_0\, d(\omega t) = \frac{1}{2\pi}\int_{\alpha_1}^{\gamma_2} I_m \sin(\omega t - \phi)\, d(\omega t)$$

$$= \frac{I_m}{\pi}\cos\phi\,[\cos\alpha_1 - \cos\alpha_2]$$

$I_{3\,avg} = 0$, $I_{4\,avg} = -I_{2(avg)}$ & $I_{5\,avg} = -I_{1\,avg}$

By symmetry

each capacitor voltage should be regulated so that each capacitor supplies avg. current per cycle as follows.

$$I_{C_1\,avg} = I_{1\,avg} = \frac{I_m}{\pi}\cos\phi\cos\gamma_2$$

$$I_{C_2\,avg} = I_{1\,avg} + I_{2\,avg} = \frac{I_m}{\pi}\cos\phi\cos\alpha_2$$

$I_{C_1\,avg} < I_{C_2\,avg} \rightarrow$ for $\alpha_1 < \gamma_2$

This results in capacitor charge unbalancing. & more charge flows from inner capacitor C_2 or C_3 than that of outer capacitor C_1 (or C_4) thus each cap voltage should be regulated to supply the appropriate amount of avg. current, otherwise its voltage V_{C_2} or V_{C_3} goes to and level as time goes.

$$I_{Cn\,(avg)} = \frac{I_m}{\pi}\cos\phi\cos\alpha_n$$

$$\frac{\cos d_2}{\cos d_1} = \frac{I_{c2\,avg}}{I_{c1\,avg}}$$

$$\frac{\cos d_n}{\cos d_{n-1}} = \frac{I_{cn\,avg}}{I_{c(n-1)\,avg}}$$

capacitor charge unbalancing exists regardless of load condition & it depends on control strategy such as $d_1, d_2, \ldots d_n$. Applying control strategy that forces energy transfer from outer cells to inner cells can solve unbalancing problem.

Features of MLI :-

→ MLI eliminates need for step-up T/F & reduce harmonics. of o/p.

→ MLI specialty is that dc bus voltage can be rea beyond the voltage rating of individual power device by use of voltage-clamping m/w by diode.

A. MLI structure with more than 3-levels can reduce harmonic content. By use of voltage-clamping, the system

KV-rating can be extended beyon limits of individual device.

⇓

It saves up KVA-rating & reduces harmonic, ↑es efficiency without need of PWM-techniques.

so,...

1. o/p voltage & power ↑se with no. of levels. Adding a voltage level involves adding a main switching device to each phase.

2. Harmonic content ↓es as No of levels ↑ and filtering need ↓es.

3. With additional voltage levels, the voltage waveform has more free-switching angles, which can be preselected for harmonic elimination.

4. In absence of any PWM techniques, the switching losses can be avoided. Increasing o/p-voltage and power does not require an increase in rating of individual device.

5. static & dynamic voltage sharing among switching devices is built into structure through either clamping diodes or capacitors.

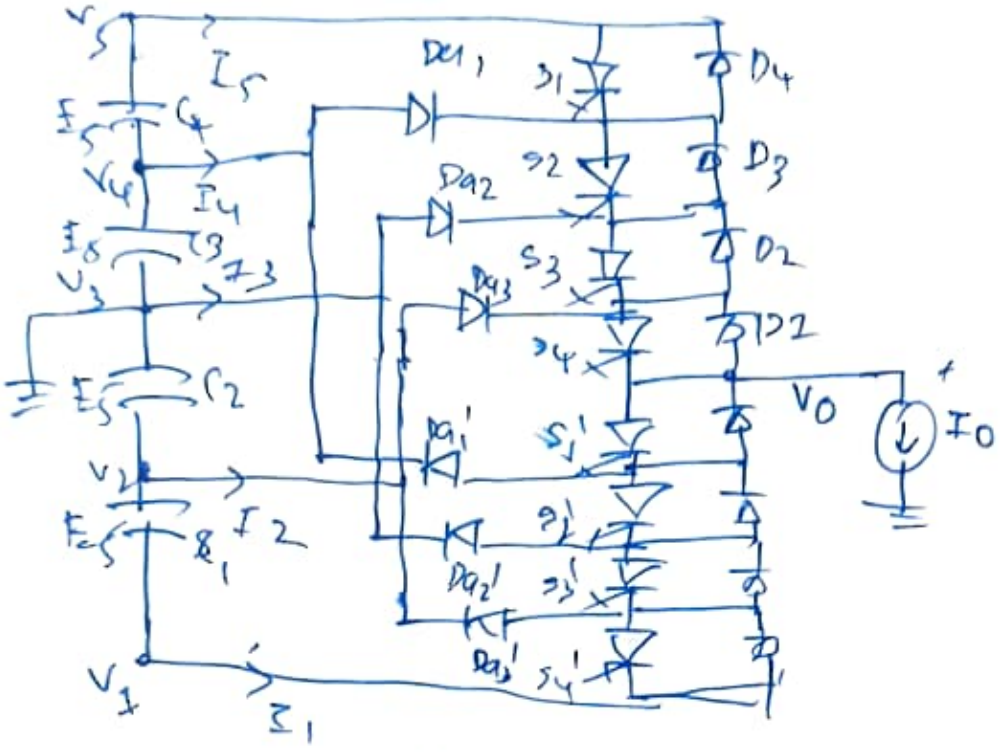
6. switching devices do not encounter voltage sharing so they can be used for large motor drives & utility grid.

7. Fundamental o/p voltage of inverter is set by dc-bus voltage V_{dc}. which can be controlled through variable dc-link.

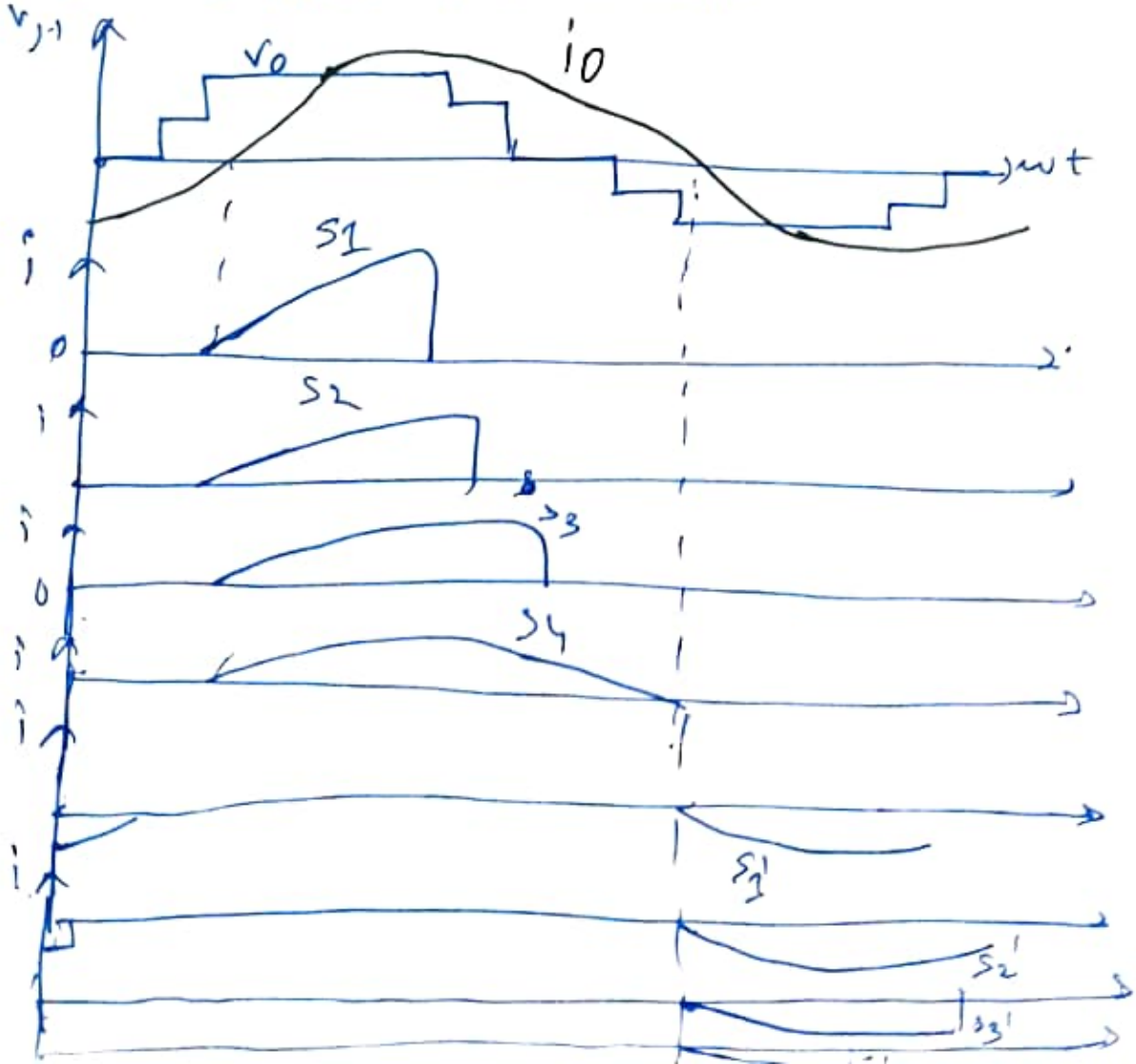
comparision of component requirements per leg of 3-MLI converter

Converter Type	Diode clamp	Flying capacitor	Cascaded inverter
1. Main switching devices	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
2. Main diodes	$(m-1)\times 2$	$(m-1)\times 2$	$(m-1)\times 2$
3. Clamping diodes	$(m-1)\times(m-2)$	0	0
4. Dc-bus capacitors	$(m-1)$	$(m-1)$	$\frac{(m-1)}{2}$
5. balancing capacitors	0	$(m-1)\times\frac{(m-2)}{2}$	0

switching device currents:-



5-level inverter circuit



Take 2-level half bridge inverter
V_o, I_o → rms load voltage & current.

→ Assuming load inductance is sufficiently large & capacitor maintain their voltage so o/p is sinusoidal

$$i_o = I_m \sin(\omega t - \phi)$$

I_m → peak value of load current
ϕ → load impedance angle.
SF_n → switching fn.

$$i_n = SF_n\, i_o \quad \text{for} \quad n = 1, 2, \ldots, m$$

inner switches S_1' & S_4' carry more current than most outer switches S_1 & S_4'.

$$I_{o(rms)}^2 = \sum_{n}^{m} I_{n(rms)}^2$$

$$I_{n(rms)} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} SF_n\, i_o^2\, d(\omega t)} \qquad n = 1, 2, \ldots m$$

$$i_{1(rms)}^2 = i_{s(rms)}^2 \quad \& \quad i_{2(rms)}^2 = i_{4(rms)}^2$$