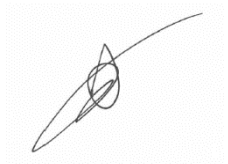
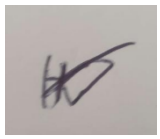
D2 Design Completion Form (semester 1)

Team Name

Team Letter(s) AG

Cohort (EL/EEE/USMC)

Team Members

Name	% Effort (sums to 100)	Description of individual contribution	Signature
Yai Sagolsem (ys6g21)	35	Sevenseg Decoder, Button Synchroniser, Die floorplanning and final integration, Final layouts and optimisation of all other layouts.	
Aimilios Angelopoulos (aa3u21)	20	Initial ALU schematics, all counter schematics, sequencer schematic integration and schematic simulations.	
Henry Knox-Johnston (hkj1g21)	17.5	Initial layouts of ALU, 32x clock divider, schematic and initial layouts of counter multiplexers.	
Vu Gia Nguyen (gnv1g21)	20	Ring Oscillator initial layout, ALU final schematic and logic optimisation, ALU initial layout, Schematic for 32x clock divider.	
Sippaphas Hirunyanitiwatna (sh2g21)	7.5	Working with Vu on ring oscillator, ALU and clock divider.	
William Ly (wl3g21)	0	No contribution to the final design, attempted schematics for ALU and button synchroniser without communicating with the rest of the team.	

Stopwatch Implemented	On Schematic	On Chip
5–digit	■	■
4–digit	☐	☐
3–digit	☐	☐
2–digit	☐	☐
none	☐	☐