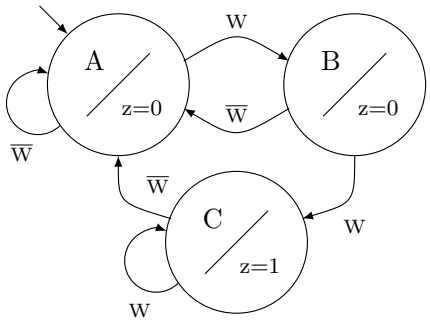
Universidade Federal do Rio Grande do Norte
Centro de Tecnologia - CT
Departamento de Engenharia Elétrica - DEE

Disciplina: ELE2715 - Circuitos Digitais
Curso: Eng. Mecatrônica

Material de suporte - MDE do tipo Moore




```
library ieee;
use ieee.std_logic_1164.all;

entity mde_b is
   port (clk, r, w: in bit;
         z        : out bit);
end mde_b;

architecture ckt of mde_b is
   type state_type is (a, b, c);
   signal y_present, y_next : state_type;
begin
   process (w,y_present)
   begin
      case y_present is
         when a =>
            if w = '0' then y_next <= a;
            else            y_next <= b; end if;
         when b =>
            if w = '0' then y_next <= a;
            else            y_next <= c; end if;
         when c =>
            if w = '0' then y_next <= a;
            else            y_next <= c; end if;
      end case;
   end process;

   process (clk,r)
   begin
      if r = '0' then
         y_present <= a;
      elsif (clk'event and clk = '1') then
         y_present <= y_next;
      end if;
   end process;
   z <= '1' when y_present = c else '0';
end ckt;
```

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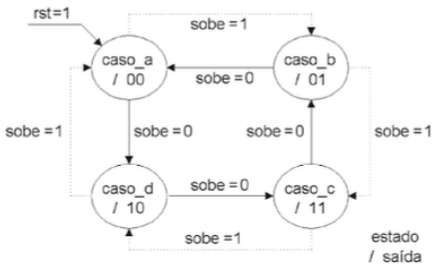
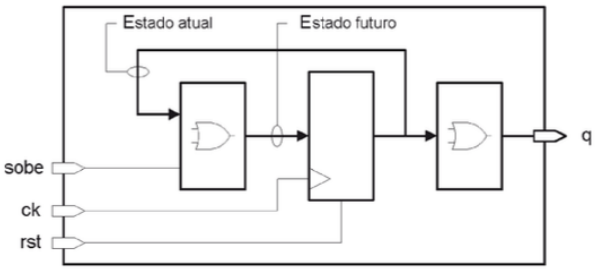
Material de suporte - MDE do tipo Moore






```
library ieee;
use ieee.std_logic_1164.all;

entity mde_d is
    port (ck, rst, sobe: in  bit;
          q            : out bit);
end mde_d;

architecture ckt of tst is
  type st is (caso_d, caso_c, caso_b, caso_a);
  signal estado : st;
begin
  with estado select
    q <= "00" when caso_a,
         "01" when caso_b,
         "11" when caso_c,
         "10" when caso_d;
  abc: process (ck, rst)
  begin
    if rst = '1' then
      estado <= caso_a;
    elsif (ck'event and ck ='1') then
      case estado is
        when caso_a =>
          if sobe = '1' then estado <= caso_b;
          else               estado <= caso_d;
          end if;
        when caso_b =>
          if sobe = '1' then estado <= caso_c;
          else               estado <= caso_a;
          end if;
        when caso_c =>
          if sobe = '1' then estado <= caso_d;
          else               estado <= caso_b;
          end if;
        when caso_d =>
          if sobe = '1' then estado <= caso_a;
          else               estado <= caso_c;
          end if;
       end case;
    end if;
  end process abc;
end ckt;
```

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Disciplina:	ELE2715 - Circuitos Digitais
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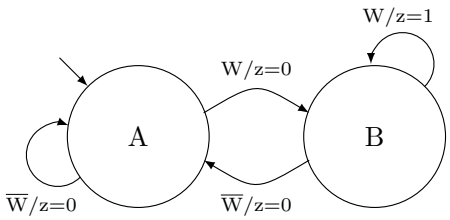
Material de suporte - MDE do tipo Mealy




```
library ieee;
use ieee.std_logic_1164.all;

entity mde_d is
    port (clk, r, w: in  bit;
          z        : out bit);
end mde_d;

architecture ckt of mde_d is
  type state_type is (a, b);
  signal y : state_type;
begin
  process (r,clk)
  begin
   if r = '0' then
     y <= a;
   elsif (clk'event and clk = '1') then
     case y is
       when a =>
         if w = '0' then y<=a;
         else            y<=b; end if;
       when b =>
         if w = '0' then y<=a;
         else            y<=b; end if;
     end case;
   end if;
  end process;

  process ( y, w )
    begin
      case y is
        when a => z <= '0';
        when b => z <= w;
      end case;
  end process;
end ckt;
```