Universidade Federal do Rio Grande do Norte
Centro de Tecnologia - CT
Departamento de Engenharia Elétrica - DEE

Disciplina:	ELE1717 - Sistemas Digitais
Curso:	Engenharia Mecatrônica

Material de suporte - Divisor de Clock

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity CLK_Div is
   port (clk_in : in  std_logic;
         clk_out: out std_logic);
end CLK_Div;

architecture ckt of CLK_Div is
signal ax : std_logic;

begin
   process(clk_in)
      variable cnt: integer range 0 to 13500000 := 0;
   begin
      if (rising_edge(clk_in)) then
         if (cnt=13500000) then
            cnt:=0;
            ax <= not ax;
         else
            cnt:=cnt+1;
         end if;
      end if;
   end process;
   clk_out<=ax;
end ckt;
```

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Material de suporte - Flip-Flop D

```
library ieee;
use ieee.std_logic_1164.all;

entity ffd is
   port (clk,d,p,c: in  std_logic;
         q        : out std_logic);
end ffd;

architecture ckt of ffd is
   signal qs: bit;
begin
   process(clk,p,c)
   begin
      if    p = ’0’ then qs <= ’1’;
      elsif c = ’0’ then qs <= ’0’;
      elsif clk=’1’ and clk’event then
         qs <= d;
      end if;
   end process;
   q <= qs;
end ckt;
```

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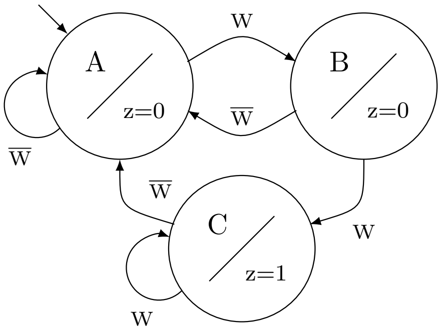
Material de suporte - MDE do tipo Moore



```
library ieee;
use ieee.std_logic_1164.all;

entity mde_b is
   port (clk, r, w: in std_logic;
         z        : out std_logic);
end mde_b;

architecture ckt of mde_b is
   type state_type is (a, b, c);
   signal y_present, y_next : state_type;
begin
   process (w,y_present)
   begin
      case y_present is
         when a =>
            if w = '0' then y_next <= a;
            else            y_next <= b; end if;
         when b =>
            if w = '0' then y_next <= a;
            else            y_next <= c; end if;
         when c =>
            if w = '0' then y_next <= a;
            else            y_next <= c; end if;
      end case;
   end process;

   process (clk,r)
   begin
      if r = '0' then
         y_present <= a;
      elsif (clk'event and clk = '1') then
         y_present <= y_next;
      end if;
   end process;
   z <= '1' when y_present = c else '0';
end ckt;
```

Disciplina: ELE1717 - Sistemas Digitais
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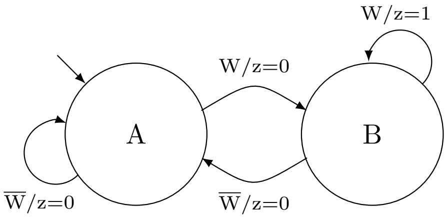
Material de suporte - MDE do tipo Mealy



```
library ieee;
use ieee.std_logic_1164.all;

entity mde_d is
    port (clk, r, w: in std_logic;
          z        : out std_logic);
end mde_d;

architecture ckt of mde_d is
  type state_type is (a, b);
  signal y : state_type;
begin
  process (r,clk)
  begin
   if r = ’0’ then
     y <= a;
   elsif (clk’event and clk = ’1’) then
     case y is
       when a =>
         if w = ’0’ then y<=a;
         else            y<=b; end if;
       when b =>
         if w = ’0’ then y<=a;
         else            y<=b; end if;
     end case;
   end if;
  end process;

  process ( y, w )
    begin
      case y is
        when a => z <= ’0’;
        when b => z <= w;
      end case;
  end process;
end ckt;
```