SEDAAF: FPGA based Single Exact Dual Approximate Adders for Approximate Processors

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Abstract—**Approximate circuits for ASICs have gained immense traction in recent years due to the benefits obtained in both energy and performance with little or no loss in output quality. Approximation in FPGAs remain a challenge due to the higher level of granularity at which logic is implemented on FPGAs. The smallest configurable blocks in FPGAs used for implementing logic consists of the look up tables (LUTs). In this paper, we exploit the inherent structures available in the FPGAs to implement SEDAAF. SEDAAF is a runtime configurable approximate adder that can perform a one-bit exact addition or two-bit approximate addition using the same hardware. SEDAAF also has a maximum bounded error, i.e. for an n-bit adder if m-bits are approximated the maximum error is $2^m - 1$. SEDAAF consumes 25% lesser power and has a 17% lesser power delay product as compared to existing designs. SEDAAF outperforms the existing state of the art designs in terms of output quality for Sobel edge detection application and can be used in approximate processors for performing both exact and approximate additions.**

I. Introduction

Approximate circuits bank on the error resilience of applications to provide benefits in terms of both energy and performance [1]–[6]. While approximate arithmetic circuits have received a lot of attention in recent years most of the works have been limited to ASIC. Due to the widespread use of adders in various applications there has been a lot of focus on approximate adders [7]–[12]. Many error tolerant applications consist of both exact and approximate sections [13]–[17]. Thus, there is a need for the hardware to configure at runtime between exact and approximate modes. In ASIC there have been some works that introduce runtime configurability by utilizing voltage and frequency as a knob for approximation [18]–[22]. There have also been works that focus on runtime configurability by crafting hybrid hardware that can perform both exact and approximate computations [23]–[28].

While a lot of approximate designs have been explored for ASICs, FPGAs have received far less attention. Approximate circuits for FPGAs are a lot more complex to design due to the higher granularity of abstraction available to the user for programming the FPGAs. There have been some recent works that have looked into the design of approximate adders and multipliers in FPGAs [29]–[31]. In [29] the authors propose approximate adders that use the look up tables (LUTs) available in the FPGAs for approximation. The work proposed various approximate adders which were implemented by exploiting the structure of the LUTs. The work also showed that approximate adders tailored for FPGAs far outperform the ASIC approximate adder designs implemented on the FPGAs. While the work has shown that approximation can be done on the FPGAs and gives benefits in terms of area, delay and power there are still several concerns thatt need to be addressed for making approximation a viable option on the FPGAs.

A full adder has two outputs, *Sum* and *Carry* [32]. In [33], authors have shown that approximate adders which need to be used in processors cannot have an error in *Carry* as it may cause an overflow. This happens because approximation in *Carry* bits, even if it is in the least significant bits (LSBs), in a multi-bit adder can affect the most significant bits (MSBs) of the outputs. The limitations of the approximate adder designs proposed in [29] are as follows: 1) All the approximate adder designs proposed have errors in the *Carry* bits thus making them unsuitable for use in processors; 2) The approximate adder designs do not allow runtime configurability between approximate and exact modes; 3) The designs also do not provide knobs to vary the amount of approximation at runtime.

In this paper we propose *SEDAAF*, an approximate adder design that addresses all the issues of the previous work. Following are the contributions of our work:

- We propose *SEDAAF*, a single exact dual approximate adder for FPGAs. *SEDAAF* can perform a single n-bit exact addition or it can be used to perform two n-bits approximate additions using the same hardware.
- *SEDAAF* allows configurability to vary the amount of approximation at runtime making it ideal for processors.
- In *SEDAAF* the maximum error is bounded because it does not introduces any approximation in the *Carry* bits. For an n-bit adder, if m-bits are approximated the maximum error is bounded by $2^m - 1$.

II. Background

We have implemented the adder designs using *Xilinx Kintex-7 FPGA KC705* board [34], [35]. In the 7-series *FPGAs*, each slice has four *LUTs* [34], [35]. *LUTs* are the basic building blocks used to implement logic functions in the *FPGA*. The two elements used for the design of *SEDAAF* are as follows:

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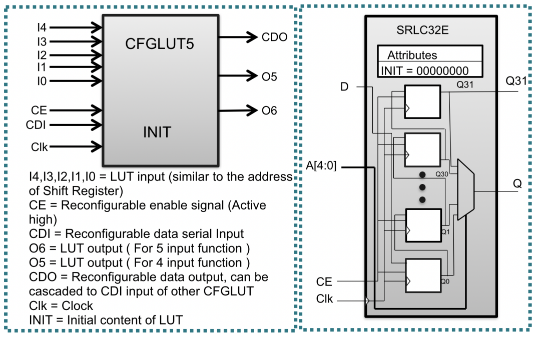


CFGLUT5
I4
I3
I2
I1
I0
CE
CDI
Clk
CDO
O5
O6
INIT
I4,I3,I2,I1,I0 = LUT input (similar to the address of Shift Register)
CE = Reconfigurable enable signal (Active high)
CDI = Reconfigurable data serial Input
O6 = LUT output (For 5 input function)
O5 = LUT output (For 4 input function)
CDO = Reconfigurable data output, can be cascaded to CDI input of other CFGLUT
Clk = Clock
INIT = Initial content of LUT
SRLC32E
Attributes
INIT = 00000000
D
Q31
A[4:0]
Q
CE
Clk

Fig. 1: CFGLUT and SRLC32E [34], [35]

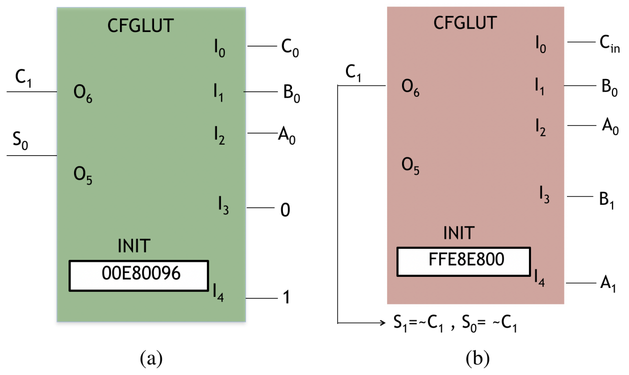


Fig. 2: (a) Exact (b) Approximate

A. *CFGLUT*

We used a 5-input dynamically reconfigurable look up table *(CFGLUT)* as shown in Fig. 1. The *CFGLUT* can be used to implement a 5-input *(I4:I0)* function or two 4-input functions. The truth table entries, also called *INIT* value, corresponding the logic to be implemented is stored in the *CFGLUT*. The output is taken either from *O6* or *O5* as shown in Fig. 1. In *CFGLUT* the *INIT* value can be changed dynamically at runtime. This is done with the help of *CE* and *CDI* pin. If *CE* is '1' the data present on the *CDI* pin is loaded into the *CFGLUT*. In 32 cycles the *INIT* value is replaced with the new *INIT* value, changing the function implemented by *CFGLUT*.

B. *SRLC32E*

SRLC32E is a variable length shift register implemented using an *LUT* as shown in Fig. 1. In *SEDAAF* we have two *SRLC32E* to store 32-bit *INIT* values for exact and approximate addition. It will be used to configure the value of *CFGLUT*. The *A* input is fixed to '11111', which configures *SRLC32E* as a 32-bit shift register. In 32 *Clk* cycles the data present in *SRLC32E* can be read out and loaded to *CFGLUT*.

III. SEDAAF

We have used 5-input *CFGLUT* in this work to allow dynamic configurability at runtime. As explained before the

TABLE I: Truth Table and INIT value for Exact Adder

A	B	Cin	S	INIT value	Cout	INIT value
1	1	1	1	9	1	E
1	1	0	0		1	
1	0	1	0		1	
1	0	0	1		0	
0	1	1	0	6	1	8
0	1	0	1		0	
0	0	1	1		0	
0	0	0	0		0	

TABLE II: Truth Table of (A1A0 + B1B0 + Cin) alongside approximation for *SEDAAF*

A1	B1	A0	B0	Cin	C1	INIT	S1=∼C1	S0=∼C1
1	1	1	1	1	1	F	0	0
1	1	1	1	0	1		0	0
1	1	1	0	1	1		0	0
1	1	1	0	0	1		0	0
1	1	0	1	1	1	F	0	0
1	1	0	1	0	1		0	0
1	1	0	0	1	1		0	0
1	1	0	0	0	1		0	0
1	0	1	1	1	1	E	0	0
1	0	1	1	0	1		0	0
1	0	1	0	1	1		0	0
1	0	1	0	0	0		1	1
1	0	0	1	1	1	8	0	0
1	0	0	1	0	0		1	1
1	0	0	0	1	0		1	1
1	0	0	0	0	0		1	1
0	1	1	1	1	1	E	0	0
0	1	1	1	0	1		0	0
0	1	1	0	1	1		0	0
0	1	1	0	0	0		1	1
0	1	0	1	1	1	8	0	0
0	1	0	1	0	0		1	1
0	1	0	0	1	0		1	1
0	1	0	0	0	0		1	1
0	0	1	1	1	0	0	1	1
0	0	1	1	0	0		1	1
0	0	1	0	1	0		1	1
0	0	1	0	0	0		1	1
0	0	0	1	1	0	0	1	1
0	0	0	1	0	0		1	1
0	0	0	0	1	0		1	1
0	0	0	0	0	0		1	1
Count					32		24	20

CFGLUT has 5 inputs and 2 outputs as shown in Fig. 1. To implement an exact adder we need to generate both *Sum* and *Carry*. Since there are two outputs available, we have implemented *Sum* and *Carry* using *CFGLUT* as shown in Fig. 2a. The I_0, I_1, I_2 are the actual inputs and remaining I_3, I_4 pins are tied to $logic-0$ and $logic-1$ respectively as shown in Fig. 2a. The 32-bit *INIT* value in hexadecimal is '$00E80096$'as shown in Table I. The '$00E8$'value corresponds to the exact *Carry* (*O6* pin) for a full adder and '0096'corresponds to the exact *Sum* (*O5* pin) for a full adder as also seen in Table I. For adding a 2-bits number i.e. $A_1A_0 + B_1B_0 + C_{in}$, we need to use 2 *CFGLUT*. This is because the number of output bits for 2-bit addition is 3 but there are only 2 output ports available in a single *CFGLUT*.

Even though a 2-bit exact adder cannot be implemented

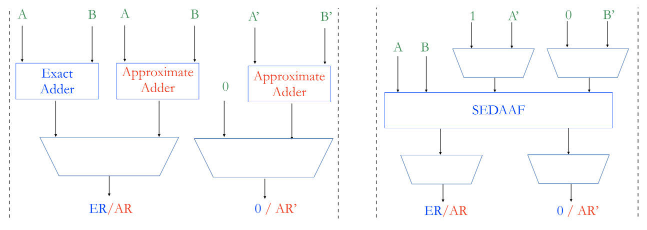


Fig. 3: (a) Baseline Design (b) *SEDAAF*

using a single *CFGLUT*, we can design a 2-bit approximate adder using one *CFGLUT*. We load the *CFGLUT* with the *INIT* value of '$FFE8E800$'. This value corresponds to the *Carry* output when $A1A0 + B1B0 + Cin$ are added as also shown in Table II. The addition will have a 3-bit output *C1, S1, S0*. The logic, 32-bit *INIT* value, for *C1* is implemented using the *CFGLUT*. *SEDAAF* introduces approximation in the *Sum* outputs *S1* and *S0*. *S1* and *S0* are equated to $\sim$*C1*. Thus, *S1* is equal to $\sim$*C1* 24 out of 32 times and *S0* is equal to $\sim$*C1* 20 out of 32 times as shown in Table. II. *S1* has a higher bit position value as compared to *S0*, and as a result *SEDAAF* introduces lesser error in *S1* as compared to *S0*. This will lead to lesser magnitude of error at the output as the most significant bit of the two will have lesser probability of error. Also, since $C1$ is not approximated the maximum error is bounded i.e. in an $n-$bit adder, if $m-$bits are approximated using *SEDAAF*, the maximum error is $2^m - 1$.

SEDAAF allows for dynamically reconfigurability between exact and approximate mode. This is enabled as follows: (i) The *INIT* value of *CFGLUT* is changed from '$00E80096$' (*INIT* value for exact) to '$FFE8E800$' (*INIT* value for approximate) using the *CDI* input of the *CFGLUT*. We already have two *SRLC32E's*, one loaded with '$FFE8E800$' and the other with '$00E80096$'. It takes 32 cycles to change the *INIT* values of *CFGLUT* to and from approximate [34], [35]. (ii) To provide the input configurability, i.e. either exact and approximate inputs, MUXes are introduced in the design of *SEDAAF*. Thus depending upon the select line of the MUXes, it will either select *A1, A0, B1, B0* and *Cin* (inputs for approximate adder) or *A0, B0* and *Cin* (inputs for exact adder) inputs as shown in Fig. 3. Thus, *SEDAAF* can be configured at runtime using *SRLC32E* and *CFGLUT*.

IV. Evaluation

We have synthesised and implemented the designs using *Xilinx Vivado 2019.1* for the *Kintex-7 KC 705 Xilinx FPGA*. We have reported the results for power consumption, delay and LUT utilization. Since runtime configurable approximate adders designs do not exist for FPGAs for a fair comparison we have implemented a number runtime configurable adders, with properties similar to *SEDAAF*, using the existing designs proposed in [29]. *SEDAAF* can perform one exact addition or two approximate additions, thus we have implemented one

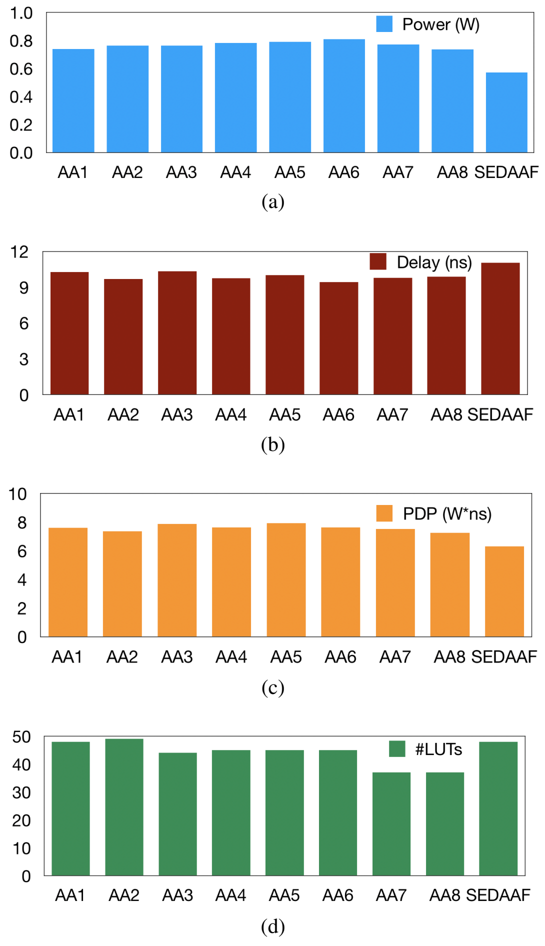
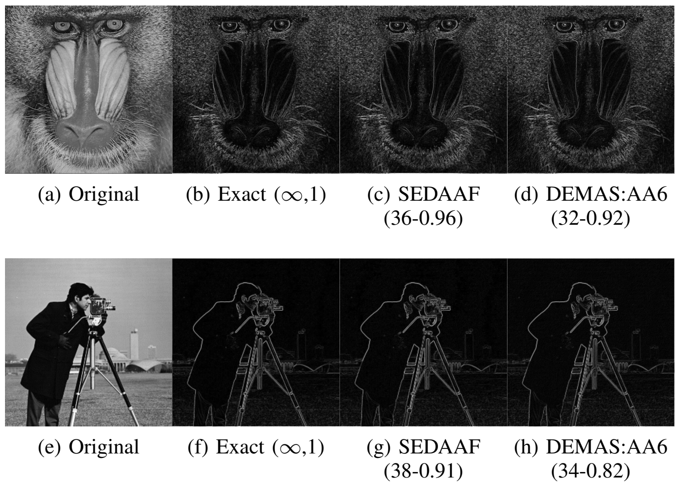


Fig. 4: 8-bit Adders (a) Power (b) Delay (c) *PDP* (d) Area

exact adder and two approximate adders (proposed in [29]). A, B are inputs for exact addition and A, B, A', B' are inputs for approximate addition[1] as shown in Fig. 3a. The ER is the exact result and AR, AR' are the approximate results in Fig. 3a. There were eight approximate adder designs proposed in [29] named *AA1* to *AA8*. We have named the baseline designs same as the name of the approximate adder used in the design. We have compared *SEDAAF* against all the designs. The corresponding design for *SEDAAF* is shown in Fig. 3b. The power, delay, power delay product (*PDP*), and area (number of LUTs) results for 8-bit approximate adders are shown in Fig. 4. On average as compared to the existing designs we obtain 25% reduction in power and 17% reduction in *PDP*. *SEDAAF* has a slight increase in area and delay overhead of 9% and 12% respectively due to the additional configuration logic. Even though we have done the comparisons with the designs proposed in [29], *SEDAAF* is the one suitable for use in processors. In this work, we have limited our analysis to 8-bit adders but it can be easily extended to 16-bit, 32-bit and 64-bit adders.

[1]Carry input is also available but has been ommited in the figure for simplicity


(a) Original (b) Exact (∞,1) (c) SEDAAF (36-0.96) (d) DEMAS:AA6 (32-0.92)

(e) Original (f) Exact (∞,1) (g) SEDAAF (38-0.91) (h) DEMAS:AA6 (34-0.82)

Fig. 5: Sobel Edge Detection Output for 4-bit approximation (PSNR-SSIM): SEDAAF and DEMAS (Best Design)

We applied *SEDAAF* for *Sobel Edge Detection* and compared it against the best design proposed in [29]. While applying the *sobel* filter the addition operation was done using the approximate adder. The output images are shown in Fig. 5. We compared *SEDAAF* against the best design in terms of error metric of *DEMAS* [29], *AA6*. We have used *structural similarity index (SSIM)* and *peak signal to noise ratio (PSNR)* as a metrics for the evaluation of output image quality as it is a widely used [7]–[11], [36]. *SEDAAF* outperforms *AA6* in terms of the output image quality as shown in Fig. 5. It has a higher *PSNR* and *SSIM* values as compared to *AA6*.

V. *SEDAAF* FOR APPROXIMATE PROCESSORS

In this section, we will discuss how the proposed approximate adder can be used in an approximate processor. In a recent work based on approximate ASIC adder [23], it was shown that approximate adders that can perform multiple approximate computations using the same hardware, can be integrated into a processor. It reduces the number of cycles [2] used while performing approximate additions. We use the same methodology proposed in [23] to show how *SEDAAF* can be integrated into a processor. We elaborate on the process of implementing *SEDAAF* in approximate processors through the example of *superscalar processors* [37]. Considering there are 8 operands $I1 - I8$, each of 8-bits, available in the *reservation station* (instructions are kept here before being executed) and 4 addition operations are to be performed as shown in Fig. 6a. The following operations $I1 + I2$, $I3 + I4$, $I5 + I6$, and $I7 + I8$ need to be performed. In Fig. 6a we can see that it will require 4 cycles to perform the addition. If these additions were to be performed approximately it would require only 2 cycles to perform the addition operation as shown in Fig. 6b. This is because *SEDAAF* can perform two

[2]In processors adders may not be in the critical path, thus adder delay does not impact the cycle time [37]

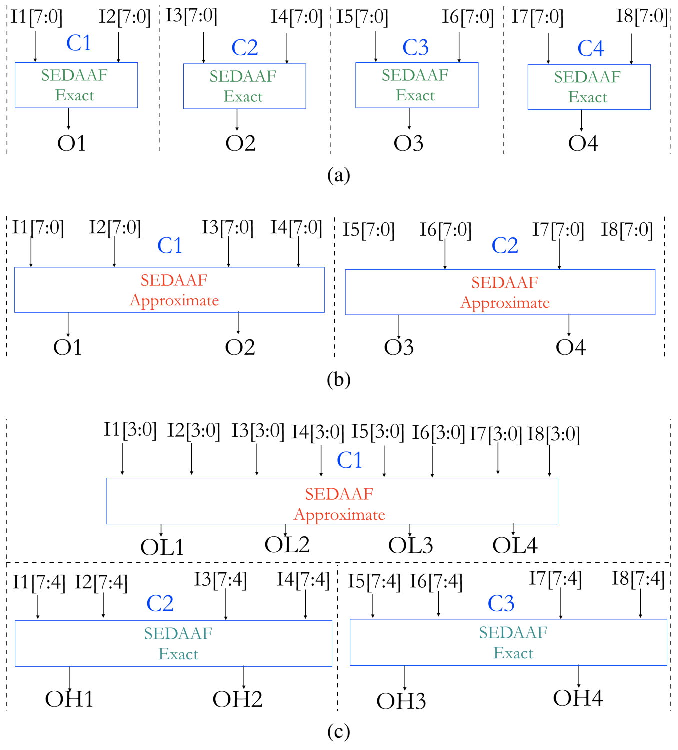


Fig. 6: (a) Exact Computation (b) 8-bit approximation (c) 4-bit approximation

approximate computations per cycle. Thus we can gain 2× improvement in performance. Fig. 6c we show that *SEDAAF* can also be configured to introduce 4-bit approximation. Since all the operands are available in the reservation station the 4 least significant bits (LSBs) of each operand can be added using *SEDAAF* in approximate mode. While in the other two cycles, two additions per cycle, we can perform the exact additions. We can either use the other exact adders present in the execution pipeline to perform the exact addition or can reconfigure *SEDAAF* at runtime to configure between exact and approximate modes.

VI. CONCLUSION

In this work, we proposed *SEDAAF*, a runtime configurable approximate adder for FPGAs. We exploited the structures present in the FPGA to design an approximate adder with bounded maximum error. On average we gain 25% in power and 17% in *PDP* as compared to existing state of the art. We also showed that *SEDAAF* can be included inside a processor to further gain benefits in performance while running approximate applications. In future we would like to extend the design of SEDAAF for implementing other widely used arithmetic circuits.

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