

Research Interest

Design of In Memory Computing Architectures for Caches and DRAM.

Design of Circuit and Architectures for Approximate Computing.

CAD Tool Design for VLSI Circuits and Architectures.

Education

2018-Present **PhD, Electrical Engineering**, IIT Gandhinagar, GPA:9.06/10.

2014-2018 **BTech, Electronics and Communication Engineering**, NIT Arunachal Pradesh, GPA: 9.54/10.

2013-2014 **Class 12th, AISSE**, Kendriya Vidyalaya Tenga Valley, Marks: 91%.

2011-2012 **Class 10th, AISSE**, Kendriya Vidyalaya Tenga Valley, GPA: 10/10.

Experience

Aug 2018- **Teaching Assistant**, IIT Gandhinagar.

Present Courses: Digital System, Embedded System, Microelectronics Lab, Computer Organisation and Architecture, VLSI Design, IC Design Lab

Instructor: Dr. Joyce Mekie, Assistant Professor, IIT Gandhinagar

Oct 2020- **Teaching Assistant**, LDCE College.

Present Courses: VLSI Lab, C - Programming

Instructor: Kirit Patel, Kamlesh Gavit, Assistant Professor, LDCE

Publications

Published

K. Prasad*, C.K. Jha*, V. Srivastava, and J. Mekie, "FPAD: a Multistage Approximation Methodology for Designing Floating Point Approximate Dividers," 2020 IEEE International Symposium on Circuits and Systems, Seville, Spain..

C.K. Jha, **K. Prasad**, A. Tomar, and J. Mekie, "SEDAAF: FPGA Based Single Exact Dual Approximate Adders for Approximate Processors," 2020 IEEE International Symposium on Circuits and Systems, Seville, Spain..

K. Prasad, A.Biswas, and J. Mekie, "Analysis of Word Line Shaping Techniques for In-Memory Computing in SRAMs" (28th IEEE International Conference on Electronics Circuits and Systems, Dubai) .

Submitted or Under Preparation

K. Prasad*, C.K. Jha*, V. Srivastava, and J. Mekie, "VosTrOF: A Unified Framework for Design Space Exploration of Approximate Circuits" (Manuscript Under Preparation) .

K. Prasad, N.Puri, and J. Mekie, "High Performance and Robust 6T SRAM based In-Memory Computing Architecture" (Manuscript Under Preparation) .

K. Prasad, R.Borkar, and J. Mekie, "High Performance In-Memory Computing in Embedded DRAM" (Manuscript Under Preparation) .

A.Parmar, **K. Prasad**, N.Rao, and J. Mekie, "FastMem: A Fast Architecture-aware Memory Layout Design"(Submitted to ISQED 2021) .

A.Parmar, **K. Prasad**, N.Rao, and J. Mekie, "An Automated Approach to Compare Bit Serial and Bit Parallel In-Memory Computing for DNNs"(Submitted to ISCAS 2021) .

* Equal Contribution as Primary Author.

Technical Skills

EDA Tools Xilinx Vivado, Design Compiler, VCS, Liberate, Innovus, MATLAB, Cadence Virtuoso, Calibre, Keil uVision, Custom Compiler, ModelSim, Sentaurus TCAD.

Programming Python, Verilog, C, TCL, Bash, HTML/CSS.

Microcontroller Raspberry Pi 3, ARM7, Arduino, AVR, ARM Cortex M0, 8085.

Relevant Coursework

VLSI Design, Physics of Transistors, Computer Architecture, Machine Learning, MicroFabrication, Computer Networking, Microelectronics Lab, IC Design Lab, Analog IC Design, Mathematical Foundation for Computer Vision.

Fellowships and Grants

Nov 2021 **DAC Young Fellow**, *DAC 2021*.

Oct 2020 **Prime Minister's Research Fellowship**, *MoE*.

Aug 2020 **Intel India Research Fellowship**, *Intel India*.

Jan 2020 **VLSID Full Fellowship**, *VLSID 2020*.

Jun 2019 **Undergraduate Mentoring Workshop Fellowship**, *ISCA 2019*.

Aug 2018 **Start Early PhD Fellowship**, *IIT Gandhinagar*.

2014-2018 **Merit Cum Means Scholarship**, *NIT Arunachal Pradesh*.

Awards

Dec 2018 **Chairman Gold Medal**, *NIT Arunachal Pradesh*.

Dec 2018 **Institute Gold Medal**, *NIT Arunachal Pradesh*.

Nov 2017 **Winner Addovedi Robowar**, *NIT Arunachal Pradesh*.

Aug 2015 **Student of the Year**, *NIT Arunachal Pradesh*.

Mar 2014 **Chief Minister's Talent Award**, *Govt. of Arunachal Pradesh*.

Extra Curricular

Apr 2020 **Online Python Video Tutorial Series**, Indian Institute of Technology, Gandhinagar.

Oct 2017 **Organized Technoyuva**, *A District Level Competition*, NIT Arunachal Pradesh.

Oct 2017 **Web Developer**, *Atulyam 2017, Annual Cultural Festival*, NIT Arunachal Pradesh.

Service

2019-Present **Lab/System administrator**, *nanoDC lab, IIT Gandhinagar*.