Kailash Prasad

Prime Minister Research Fellow | SRC Research Scholar

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Education

2018-2023 **PhD in Electrical Engineering**, Indian Institute of Technology, Gandhinagar, GPA:9.13/10.
Recipient of the Prime Minister's Research Fellowship and Intel India Research Fellowship 2020

2014-2018 **BTech in Electronics and Communication Engineering**, National Institute of Technology, Arunachal Pradesh, GPA: 9.54/10.
Recipient of the Chairman and Institute Gold Medal for achieving the first rank in the Batch of 2014-2018 at NIT Arunachal Pradesh.

2013-2014 **Class 12th, AISSCE**, Kendriya Vidyalaya Tenga Valley, Marks: 91%.

2011-2012 **Class 10th, AISSE**, Kendriya Vidyalaya Tenga Valley, GPA: 10/10.
Honored with the Chief Minister Talent Award by the Government of Arunachal Pradesh for exceptional academic performance.

Experience

Aug 2018-Present **Teaching Assistant**, Indian Institute of Technology Gandhinagar.
Courses: Digital System, Embedded System, Microelectronics Lab, Computer Organisation and Architecture, VLSI Design, IC Design
Instructor: Dr. Joycee Mekie, Associate Professor, Indian Institute of Technology Gandhinagar

Jul 2022-Present **Teaching Assistant**, National Programme on Technology Enhanced Learning (NPTEL).
Course: Design and Analysis of VLSI Subsystems : Instructor: Dr. Madhav Rao, Professor IIIT Bangalore
Course: Digital Electronics : Instructor: Dr. Shantanu Chattopadhyay, Professor Indian Institute of Technology Kharagpur

Jan 2022-May 2022 **Graduate Teaching Fellow**, Indian Institute of Technology Gandhinagar.
Course: Digital IC Design Lab (Awarded Outstanding Graduate Teaching Fellow for Teaching this course)

Oct 2020-Jul 2022 **Teaching Assistant**, LDCE College.
Courses: VLSI Lab, C Programming, Basic Electronics : Instructor: Kirit Patel, Kamlesh Gavit, Assistant Professor,LDCE

May 2017-Jul 2017 **Student Research Associate**, Indian Institute of Technology Kanpur.
Topic: Compact Modelling and TCAD simulation of semiconductor devices.
Supervisor: Dr. Yogesh Singh Chauhan, Associate Professor, Indian Institute of Technology Kanpur

Publications

Papers

2023 Sai Shubham, Shubham Pandit, **Kailash Prasad**, and Joycee Mekie, "PVC-RAM:Process Variation Aware Charge Domain In-Memory Computing 6T-SRAM for DNNs" **60th Design Automation Conference**.

2023 **Kailash Prasad**, Aditya Biswas, Arpita Kabra and Joycee Mekie, "PIC-RAM: Process-Invariant Capacitive Multiplier Based Analog In Memory Computing in 6T SRAM" **26th Design, Automation and Test in Europe Conference** , **Nominated for Best paper Award**.

2023 **Kailash Prasad**, Sai Shubham, Aditya Biswas, and Joycee Mekie, "Process Variation Resilient Current-Domain Analog In Memory Computing" **26th Design, Automation and Test in Europe Conference**.

2023 **Kailash Prasad***, Tom Glint*, Jinay Dagli, Krishil Gandhi, Aryan Gupta, Vrajesh Patel, Neel Shah and Joycee Mekie, "Hardware-Software Codesign of DNN Accelerators Using Approximate Posit Multipliers." **28th Asia and South Pacific Design Automation Conference**, **Nominated for Best paper Award**.

2023 **Kailash Prasad**, Ayush Srivastava, Nistha Baruah and Joycee Mekie, "Fast and Robust Sense Amplifier Design for Digital IMC" **36th International Conference on VLSI Design**.

2022 S.Singh, N.Surana, **Kailash Prasad**, Joycee Mekie, M.Awasthi, "HyGain: High Performance, Energy-Efficient Hybrid Gain Cell-based Cache Hierarchy," **ACM Transactions on Architecture and Code Optimization**, **Selected for ACM Transaction for Kudos**.

2022 **Kailash Prasad**, Jinay Dagli, Neel Shah, Mallikarjun Pidagannavar, and Joycee Mekie "Impact of approximation and commutativity on Neural Network and Image Processing Applications." **26th International Symposium on VLSI Design and Test**.

2022 **Kailash Prasad***, Alok Parmar*, Nanditha Rao, and Joycee Mekie, "An Automated Approach to Compare Bit Serial and Bit Parallel In-Memory Computing for DNNs" **2022 International Symposium on Circuits and Systems** .

2022 Alok Parmar, **Kailash Prasad**, Nanditha Rao, and Joycee Mekie, "FastMem: A Fast Architecture-aware Memory Layout Design" **23rd International Symposium on Quality Electronic Design** .

2021 **Kailash Prasad**, Aditya Biswas, and Joycee Mekie, "Analysis of Word Line Shaping Techniques for In-Memory Computing in SRAMs" **28th IEEE International Conference on Electronics, Circuits, and Systems**.

2020 **Kailash Prasad***, Chandan Kumar Jha*, V. Srivastava, and Joycee Mekie, "FPAD: a Multistage Approximation Methodology for Designing Floating Point Approximate Dividers," **2020 International Symposium on Circuits and Systems**.

2020 Chandan Kumar Jha, **Kailash Prasad**, A. Tomar, and Joycee Mekie, "SEDAAF: FPGA Based Single Exact Dual Approximate Adders for Approximate Processors," **2020 International Symposium on Circuits and Systems**.

Posters

2022 **Kailash Prasad** and Joycee Mekie, "Energy Efficient Domain-Specific Hardware Design" (DATE 2023 PhD Forum).

2022 **Kailash Prasad**, Aditya Biswas, Arpita Kabra, and Joycee Mekie, "Energy and Area Efficient Column-Major IMC Architecture" (DAC 2022).

2022 **Kailash Prasad**, Aditya Biswas, and Joycee Mekie, "Analysis of Word Line Shaping Techniques for In-Memory Computing in SRAMs" (DAC 2022).

2022 **Kailash Prasad**, Aditya Biswas, Rahul M. Rao, and Joycee Mekie, " IMC-Enabled SRAM PUF based on Bitline Computing and Write-back" (DAC 2022).

* Equal Contribution as Primary Author.

Tapeout

Aug 2022 - Dec 2022 **UMC 65nm Tapeout: Memory Macros, Processors, and In-Memory Computing Circuits**.

- Led a team of 14 members (B.Tech, M.Tech, and PhD) to design processors, In Memory Computing SRAM Memory with various Sense Amplifiers and compute circuits, CWS PUF based on IMC, and three types of processors (radiation-hardened, synchronous, and asynchronous).
- Designed schematic and layout of digital IMC and PUF circuits using Cadence Virtuoso.
- Expertly handled the backend Innovus tools involving placement, routing, CTS of Memory Macros with Processor, and final GDS generation.

Jun 2020 - Sep 2020 **UMC 65nm Tapeout : Memory Macros, Processors**.

- Led a team of 16 members (B.Tech, M.Tech, and PhD) to design processors,SRAM Memory Array (SRAM 6T, DPDICE, RDICE), and three types of processors (radiation-hardened, synchronous, and asynchronous).
- Successfully ported the OpenRAM Memory Compiler to UMC65nm, enabling the generation of various memory layouts using different cells, such as SRAM 6T, DPDICE, and RDICE.
- Proficiently managed the backend Innovus tools, including placement, routing, and clock tree synthesis (CTS) of Memory Macros with the Processor, resulting in the final GDS generation.

Research Experience

Dec 2020 - May 2023 **Digital In Memory Computing (IMC) in 6T SRAM**.

- Performed Compute Disturb Analysis and Proposed Mitigation techniques for SRAM 6T-based Digital IMC
- Designed IMC Architecture including Decoder and Peripherals
- Designed Compute Circuits for performing bit-serial addition, multiplication, and MAC operation
- Designed a Compute-enabled Sense Amplifier that is robust to process variation

Dec 2020 - May 2023 **Analog In Memory Computing in 6T SRAM**.

- Proposed a column-major analog IMC for multi-bit multiplication with minimal change in peripheral circuits
- Developed a compute-disturb free IMC architecture with high dynamic range and resilience to process variations
- Identified wordline degradation as a major source of non-linearity in analog and digital IMC
- Implemented four wordline shaping techniques to improve access time and reduce inconsistency in bitline discharge
- Proposed a novel process variation tracking method for analog IMC to compensate for process variation

May 2019- May 2023 **Simulator Design for Digital IMC**.

- Designed i-CACTI simulator for application-level analysis of Digital IMC
- Build FastMem simulator for accurate and fast SRAM modeling integrated with Digital IMC Compute Logic with Bit Serial and Bit Parallel paradigms of computation
- Build NeuroCACTI-IMC calculates performance metrics for in-memory computations for SRAM-based memory sub-system and observes 8X improvement in EDP for BPA and BSA by modifying memory array structure.

Aug 2020 - May 2021 **Automatic Analog Circuit Design Tool using Machine Learning** .

- Utilized machine learning to model technology parameters for automatic analog circuit design
- Created a design space of circuits (Common Source and Two Stage Operational Amplifier) using the machine learning model
- Employed Bayesian optimization to find the optimum design in the design space
- Implemented active learning plugin for dataset generation when it was not readily available

Feb 2020 - Sep 2020 **Developed SRAM Memory Compiler**.

- Analyzed the performance metrics of SRAM arrays generated by OpenRAM compiler in NCSU45nm, ranging from 8B to 4KB.
- Ported OpenRAM memory compiler to UMC65nm and UMC28nm at both schematic and layout levels, and performed a detailed analysis across multiple technologies.
- Optimized the performance of the complete Memory subsystem by properly sizing transistors in custom library cells and implementing circuit-level changes.

Mar 2019 - May 2020 **Developed VosTrOF: A Unified Tool for Design Space Exploration of Approximate Arithmetic Circuits.**.

- Designed VosTrOF, a tool that unifies four approximation strategies (Truncation, Overclocking, Voltage Overscaling, and Functional Approximation) for adders, multipliers, and dividers, enabling holistic analysis and design space exploration.
- Utilized VosTrOF for eight separate image processing applications and demonstrated optimized designs compared to state-of-the-art frameworks.

Technical and Soft Skills

EDA Tools: Cadence Virtuoso, Calibre, Design Compiler, Genus, VCS, NCSIM, Innovus, Abstract, Liberate, Xilinx Vivado, MATLAB, Keil uVision, Sentaurus TCAD.

Programming: Python, Verilog, System Verilog, C, TCL, Bash, HTML/CSS.

Microcontroller : Raspberry Pi 3, ARM7, Arduino, AVR, ARM Cortex M0, 8085.

Sysadmin: Managed lab/system infrastructure, ensuring optimal functionality and availability for efficient operations.

Leadership: Lead a Team of more than 14 members for two Tapeouts in UMC 65nm.

Mentorship: Mentored more than 70 students, publishing with more than 15 students for work on circuit design, architecture, and tool design .

Relevant Coursework

VLSI Design, Asynchronous Circuit Design, Physics of Transistors, Computer Architecture, Machine Learning, MicroFabrication and Semiconductor Processes, Computer Networking, Microelectronics Lab, IC Design Lab, Analog IC Design, Mathematical Foundation for Computer Vision.

Fellowships and Grants

Mar 2023 **Travel Grant to attend DATE 2023**, *DATE 2023*.
Nov 2022 **VLSID Full Fellowship**, *VLSID 2023*.
May 2022 **DAC Young Fellowship**, *DAC 2022*.
Jan 2022 **Graduate Teaching Fellow**, *IIT Gandhinagar*.
Nov 2021 **DAC Young Fellowship**, *DAC 2021*.
Oct 2020 **Prime Minister's Research Fellowship**, *Ministry of Education, GOI*.
Aug 2020 **Intel India Research Fellowship**, *Intel India*.
Jan 2020 **VLSID Full Fellowship**, *VLSID 2020*.
Jun 2019 **Undergraduate Mentoring Workshop Fellowship**, *ISCA 2019*.
Aug 2018 **Start Early PhD Fellowship**, *IIT Gandhinagar*.
2014-2018 **Merit Cum Means Scholarship**, *NIT Arunachal Pradesh*.

Awards

Oct 2022 **Outstanding Graduate Teaching Fellow Award**, *IIT Gandhinagar*.
Dec 2021 **Best Research Video Award**, *DAC 2021*.
Dec 2018 **Chairman Gold Medal**, *NIT Arunachal Pradesh*.
Dec 2018 **Institute Gold Medal**, *NIT Arunachal Pradesh*.
Nov 2017 **Winner Addovedi Robowar**, *NIT Arunachal Pradesh*.
Aug 2015 **Best Student**, *NIT Arunachal Pradesh*.
Mar 2014 **Chief Minister's Talent Award**, *Govt. of Arunachal Pradesh*.

Invited Talk

Apr 2023 **Enabling In Memory Computing for AI: Digital and Analog Approaches**, University of Bremen, Germany.
Jul 2022 **Design and Evaluation of Memory-Centric Architecture for Caches**, University of California San Diego.

Extra Curricular

Feb 2023 **Co-ordinated Inaugration of VLSI Society of India, Gujarat Chapter**, Indian Institute of Technology, Gandhinagar.
Apr 2020 **Online Python Video Tutorial Series**, Indian Institute of Technology, Gandhinagar.
Oct 2017 **Organized Technoyuva**, *A District Level Competition*, NIT Arunachal Pradesh.
Oct 2017 **Web Developer**, *Atulyam 2017, Annual Cultural Festival*, NIT Arunachal Pradesh.

Service

2019-Present **Lab/System administrator**, *nanoDC lab, IIT Gandhinagar*.
2020-Present **Reviewer**, *IEEE TCAS I, TCAS II, ISCAS 2021, ISCAS 2022, ISCAS 2023, AICAS 2023*.