PhD Scholar

Research Interest

Design of In Memory Computing Architectures for Caches and Embedded DRAM.

Design of Circuit and Architectures for Approximate Computing.

CAD Tool Design for VLSI Circuits and Architectures.

Education

2018-Present PhD, Electrical Engineering, IIT Gandhinagar, GPA:9.13/10.

2014-2018 BTech, Electronics and Communication Engineering, NIT Arunachal Pradesh, GPA: 9.54/10.

2013-2014 Class 12th, AISSCE, Kendriya Vidyalaya Tenga Valley, Marks: 91%.

Experience

Jan 2022- Graduate Teaching Fellow, IIT Gandhinagar.

May 2022 Course: Digital IC Design Lab

Aug 2018- **Teaching Assistant**, IIT Gandhinagar.

Present Courses: Digital System, Embedded System, Microelectronics Lab, Computer Organisation and Architecture, VLSI

Design, IC Design Lab

Instructor: Dr. Joycee Mekie, Associate Professor, IIT Gandhinagar

Oct 2020- Teaching Assistant, LDCE College.

Present Courses: VLSI Lab, C - Programming, Basic Electronics

Instructor: Kirit Patel, Kamlesh Gavit, Assistant Professor, LDCE

Publications

Papers

K. Prasad*, C.K. Jha*, V. Srivastava, and J. Mekie, "FPAD: a Multistage Approximation Methodology for Designing Floating Point Approximate Dividers," (ISCAS 2020).

C.K. Jha, **K. Prasad**, A. Tomar, and J. Mekie, "SEDAAF: FPGA Based Single Exact Dual Approximate Adders for Approximate Processors," (ISCAS 2020).

K. Prasad, A.Biswas, and J. Mekie, "Analysis of Word Line Shaping Techniques for In-Memory Computing in SRAMs" (ICECS 2021) .

K. Prasad*, A.Parmar*, N.Rao, and J. Mekie, "An Automated Approach to Compare Bit Serial and Bit Parallel In-Memory Computing for DNNs" (ISCAS 2022) .

A.Parmar, **K. Prasad**, N.Rao, and J. Mekie, "FastMem: A Fast Architecture-aware Memory Layout Design" (ISQED 2022) .

K.Prasad, J.Dagli, N.Shah, M.Pidagannavar, and J.Mekie "Impact of approximation and commutativity on Neural Network and Image Processing Applications." (VDAT 2022).

Posters

K. Prasad, A.Biswas, A.Kabra, and J. Mekie, "Energy and Area Efficient Column-Major IMC Architecture" (To Be presented at DAC 2022).

Submitted

S.Singh, N.Surana, **K.Prasad**, J.Mekie, M.Awasthi.", HyGain: High Performance, Energy-Efficient Hybrid Gain Cell-based Cache Hierarchy (To Be Submitted to TACO).

* Equal Contribution as Primary Author.

Technical Skills

EDA Tools Xilinx Vivado, Design Compiler, VCS, Liberate, Innovus, MATLAB, Cadence Virtuoso, Calibre, Keil uVision, Custom Compiler, ModelSim, Sentaurus TCAD.

Programming Python, Verilog, C, TCL, Bash, HTML/CSS.

Microcontroler Raspberry Pi 3, ARM7, Arduino, AVR, ARM Cortex M0, 8085.

Relevant Coursework

VLSI Design, Asynchronous Circuit Design, Physics of Transistors, Computer Architecture, Machine Learning, MicroFabrication and Semiconductor Processes, Computer Networking, Microelectronics Lab, IC Design Lab, Analog IC Design, Mathematical Foundation for Computer Vision.

Fellowships and Grants

- May 2022 DAC Young Fellowship, DAC 2022.
- Jan 2022 Graduate Teaching Fellow, IIT Gandhinagar.
- Nov 2021 DAC Young Fellowship, DAC 2021.
- Oct 2020 Prime Minister's Research Fellowship, Ministry of Education, GOI.
- Aug 2020 Intel India Research Fellowship, Intel India.
- Jan 2020 VLSID Full Fellowship, VLSID 2020.
- Jun 2019 Undergraduate Mentoring Workshop Fellowship, ISCA 2019.
- Aug 2018 Start Early PhD Fellowship, IIT Gandhinagar.
- 2014-2018 Merit Cum Means Scholarship, NIT Arunachal Pradesh.

Awards

- Dec 2021 Best Research Video Award, DAC 2021.
- Dec 2018 Chairman Gold Medal, NIT Arunachal Pradesh.
- Dec 2018 Institute Gold Medal, NIT Arunachal Pradesh.
- Nov 2017 Winner Addovedi Robowar, NIT Arunachal Pradesh.
- Aug 2015 Student of the Year, NIT Arunachal Pradesh.
- Mar 2014 Chief Minister's Talent Award, Govt. of Arunachal Pradesh.

Extra Curricular

- Apr 2020 Online Python Video Tutorial Series, Indian Institute of Technology, Gandhinagar.
- Oct 2017 Organized Technoyuva, A District Level Competition, NIT Arunachal Pradesh.
- Oct 2017 Web Developer, Atulyam 2017, Annual Cultural Festival, NIT Arunachal Pradesh.

Service

2019-Present Lab/System administrator, nanoDC lab, IIT Gandhinagar.