VLSI Full Course Curriculum

Offered by TechProjectsHub

🎓 1-Month VLSI Foundation Course

Goal: Learn VLSI fundamentals, RTL design using Verilog, FPGA prototyping, and complete a mini-project.

Week 1: VLSI Basics + HDL Programming

- Introduction to VLSI Design & CMOS Technology
- pMOS, nMOS, CMOS Logic Families
- Digital Logic Design Basics (Gates, FFs, FSM)
- Verilog HDL Programming (Combinational + Sequential Logic)
- Simulation with ModelSim

Week 2: RTL Design + Simulation

- Writing and Testing Testbenches
- RTL Design Flow
- FSM Design in Verilog
- Synthesis Concepts
- Mini Project: ALU / Counter / Traffic Light Controller

Week 3: FPGA Design & Vivado Tools

- Introduction to FPGA Architecture
- Xilinx Vivado Toolchain: Synthesis → Implementation

- Timing Constraints, I/O Planning
- Programming FPGA Boards (e.g., Basys 3)
- Hands-on Project Deployment

Week 4: Mini Project Completion

- Design + Simulate + FPGA Implement
- Documentation and Report Writing
- Viva + Presentation Preparation

🔹 2-Month VLSI Core Course

Goal: Extend 1-Month with Back-End (Layout), Analog, and Mixed-Signal concepts + more tools.

Month 1: Same as 1-Month Course

Week 5: Introduction to Back-End (Layout) Design

- VLSI Design Flow: RTL to GDSII
- DSCH & Microwind Basics
- CMOS Inverter Layout
- Standard Cell Design & Stick Diagrams

Week 6: Physical Design + Verification

- Floorplanning, Placement & Routing
- Design Rule Check (DRC), LVS Basics
- Tools: Cadence Virtuoso / Tanner EDA

- Hands-on: NAND/NOR Layout, DRC Clean Design

Week 7: Analog & Mixed-Signal Design

- OpAmp Design Principles
- ADC/DAC Architectures
- PLL (Phase-Locked Loop) Introduction
- Schematic Capture & Simulation in Cadence

Week 8: Domain-Based Project

- Choose: Analog, Back-End, or Mixed-Signal Project
- Simulation + Layout + Optimization
- Final Project Review + Report + Certificate

🔹 3-Month VLSI Pro Course

Goal: Full-stack chip design from RTL to Layout + STA, DFT, IEEE Paper-Ready Project.

Month 1 & 2: Same as Above

Week 9: SoC Design Concepts

- Introduction to System-on-Chip Architecture
- Hierarchical Floorplanning
- Power Planning and Clock Tree Design
- Functional Verification Basics

Week 10: Design Optimization

- Static Timing Analysis (STA)
- Setup and Hold Violation Fixes
- Low-Power Design Techniques
- Timing Closure Challenges

Week 11: Advanced Project Design

- Choose: SoC Block / Analog Subsystem / Custom Layout
- Start IEEE Paper-based Project
- RTL + Layout + Simulation + Report Drafting

Week 12: Final Wrap-Up

- IEEE Paper Guidance (Format + Submission Help)
- Resume Building + Career Guidance for VLSI Jobs
- Viva + Final Presentation

📚 Tools Covered

- **Front-End:** Verilog, ModelSim, Vivado
- **Back-End:** DSCH, Microwind, Cadence Virtuoso, Tanner EDA
- **Analog:** Cadence Spectre, Tanner T-Spice
- **Verification:** Vivado Simulator, Manual Testbenches
- **Project Support:** Documentation, Viva, IEEE Paper Format

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✅ Ideal For

- B.Tech / M.Tech Students (Mini & Major Projects)
- VLSI Job Aspirants (RTL, DFT, Layout, Analog)
- Academic Thesis / IEEE Paper Writers

🏢 About TechProjectsHub

TechProjectsHub is a leading academic and industry-aligned platform dedicated to empowering students and professionals with hands-on project experience across cutting-edge technology domains. We specialize in VLSI Design, Cloud Computing, Full Stack Development, AI/ML, Embedded, and more.

Why Choose Us?

- Project-Driven Learning
- Live Tool Demonstrations
- Real-Time Project Guidance
- Resume & Career Development
- End-to-End Support from Concept to Deployment

Contact Us