PERFORMANCE ANALYSIS

TESTING PERFORMANCE OF THE FLAPPY BIRD GAME AND STOCK TRADING PROJECTS USING HARDWARE PREFETCHER AND ADJACENT CACHE LINE

Prefetch mechanisms through the BIOS

Hardware prefetcher: *The hardware prefetcher operates transparently, without programmer intervention, to fetch streams of data and instruction from memory into the unified second-level cache. The prefetcher is capable of handling multiple streams in either the forward or backward direction.*

Adjacent Cache-Line Prefetch: *The Adjacent Cache-Line Prefetch mechanism, like automatic hardware prefetch, operates without programmer intervention. When enabled through the BIOS, two 64-byte cache lines are fetched into a 128-byte sector, regardless of whether the additional cache line has been requested or not.*

Parameters Analysed in Flappy Bird

We test the prefetchers and the adjacent cache line, and plot two diagrams for Timestep (frames) vs. training time (seconds) -> [Figure-1] and the plot another graph for epsilon vs. training time(seconds) -> [Figure-2].

***Epsilon**: Represents the exploration rate of the agent. Start from 0.1 to 0.0001.*

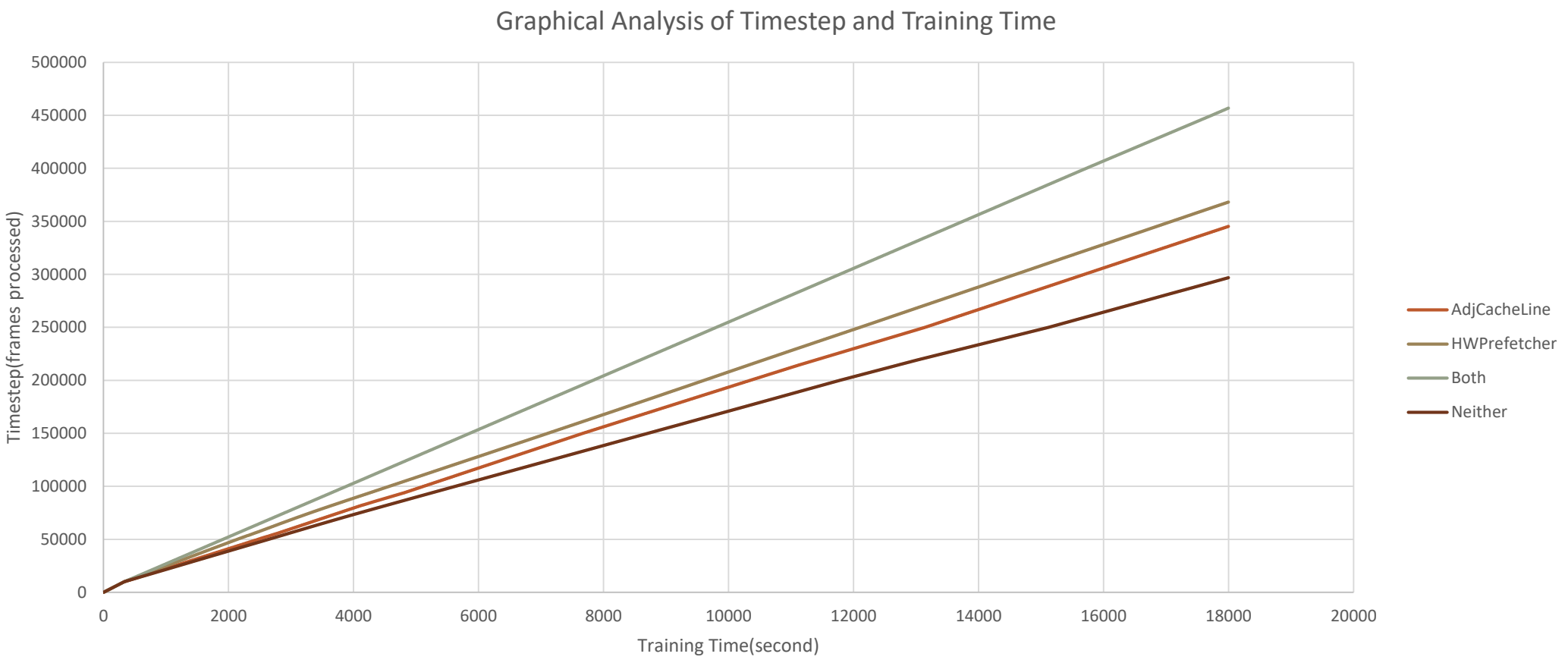
***Training time**: Represents the time of executing the project.*

***Timestep**: Number of frames processed during the training.*

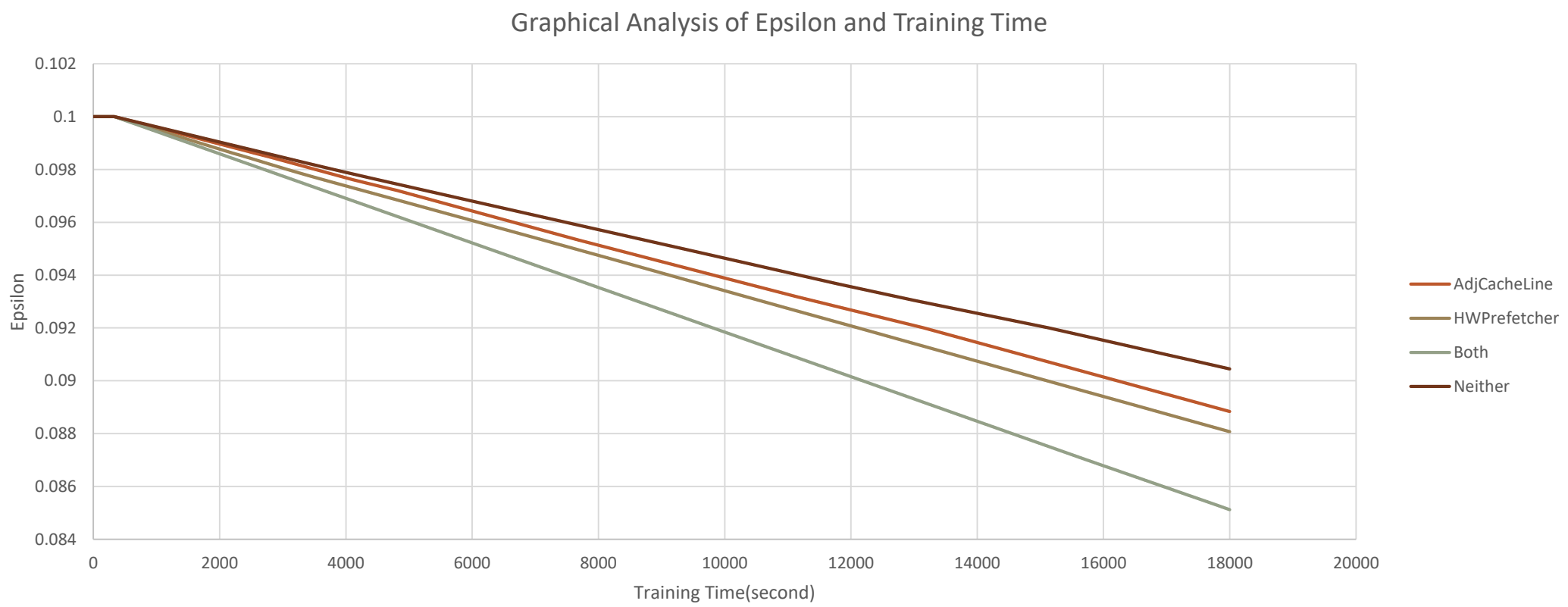
The four situations were both are enabled, just cache line is enabled, just prefetcher is enabled and neither are enabled.

The model is tested for 5 hours for each constraint mentioned above.

Performance of Flappy Bird (Figure-1)



Performance of Flappy Bird (Figure-2)



Parameters Analysed in Stock Trading

We test the prefetchers and the adjacent cache line, and plot two diagrams for Episode vs. training time (seconds) -> [Figure-3] and the plot another graph for epsilon vs. training time(seconds) -> [Figure-4].

***Epsilon**: Represents the exploration rate.*

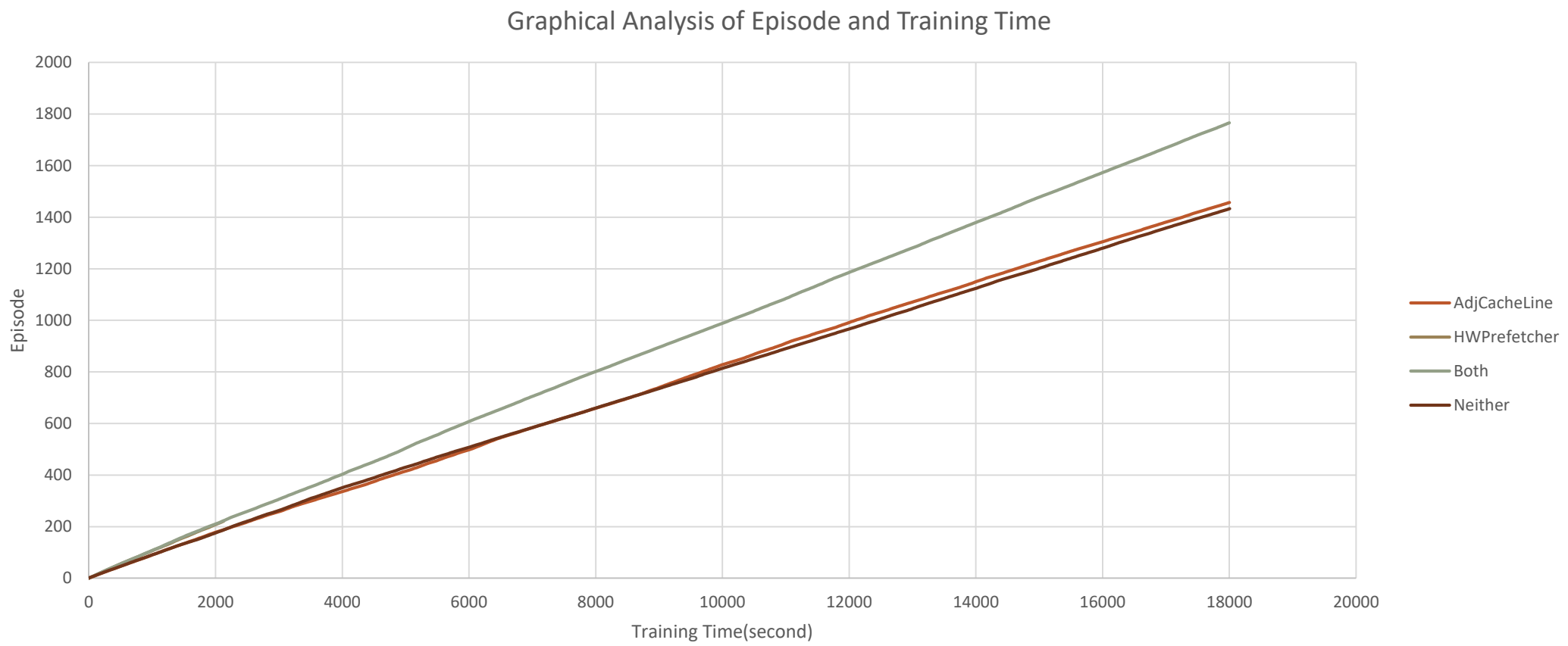
***Training time**: Represents the time of executing the project.*

***Episode**: Number of stages in training process.*

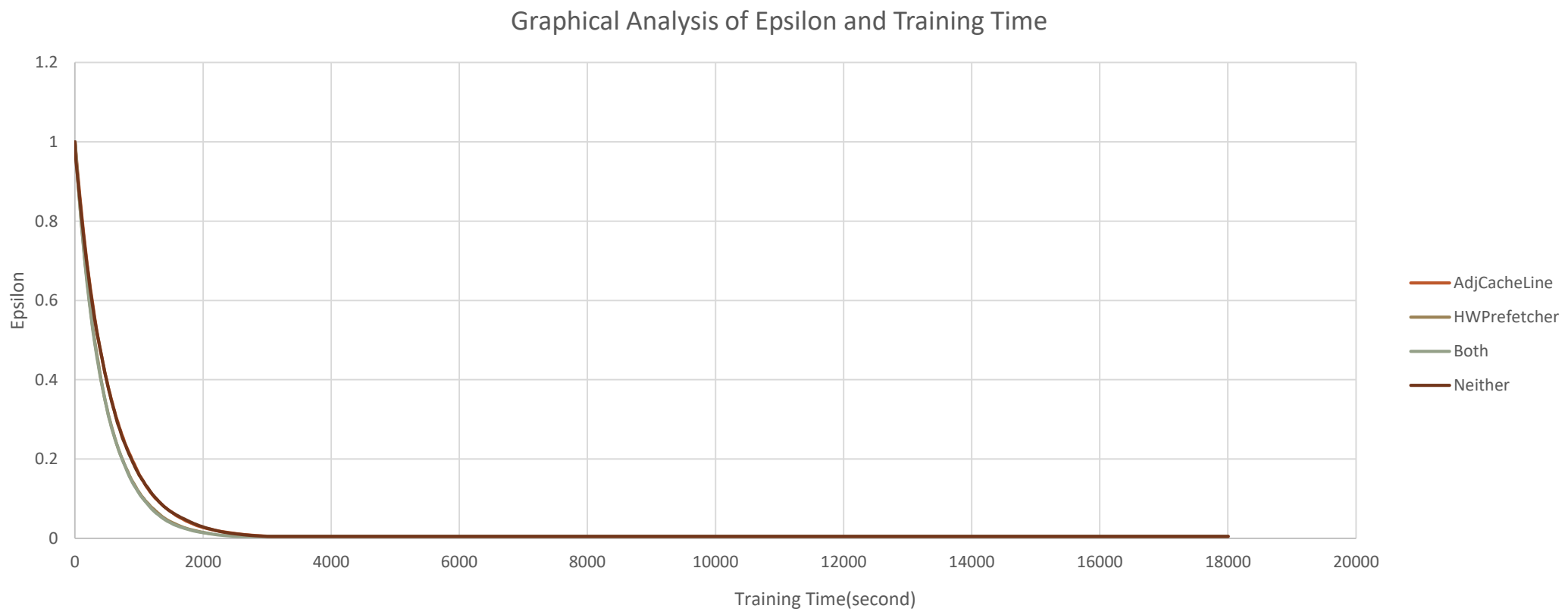
The four situations were both are enabled, just cache line is enabled, just prefetcher is enabled and neither of them are enabled.

The model is tested for 5 hours for each constraint mentioned above.

Performance for Stock Trading(Figure-3)



Performance for Stock Trading(Figure-4)



Result Analysis

Two Prefetch mechanisms from the Prefetching Support in Intel NetBurst® Microarchitecture switching to the BIOS are implemented to test the performance.

When enabled both hardware prefetcher and the adjacent cache line prefetch, it is observed that the performance for the training is the best compared to other 3 constraints.

The Hardware prefetcher performs better than the adjacent cache line prefetch when only one of the mechanisms are enabled.