Qualcomm® Snapdragon™ 410E Processor APQ8016E System Power Overview

Qualcomm Technologies, Inc.

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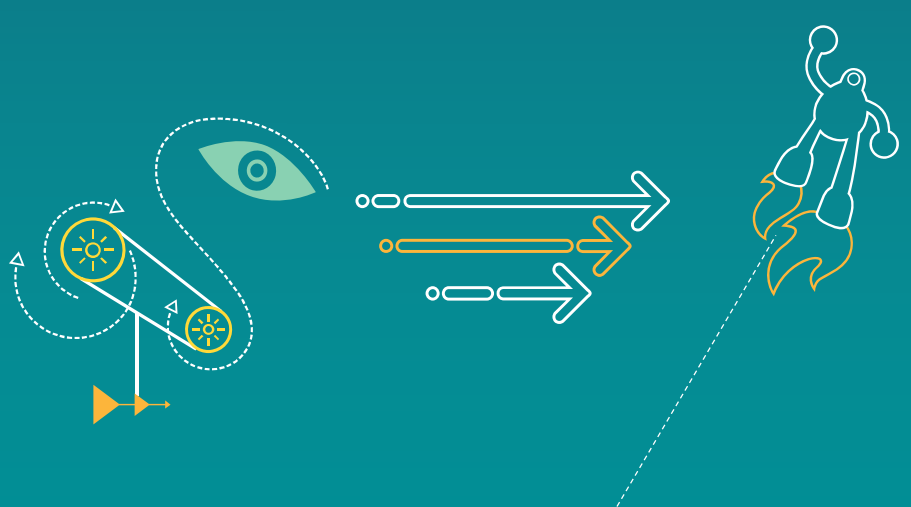

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Revision History

Revision	Date	Description
A	November 2017	Initial release

Contents

Introduction

Overview

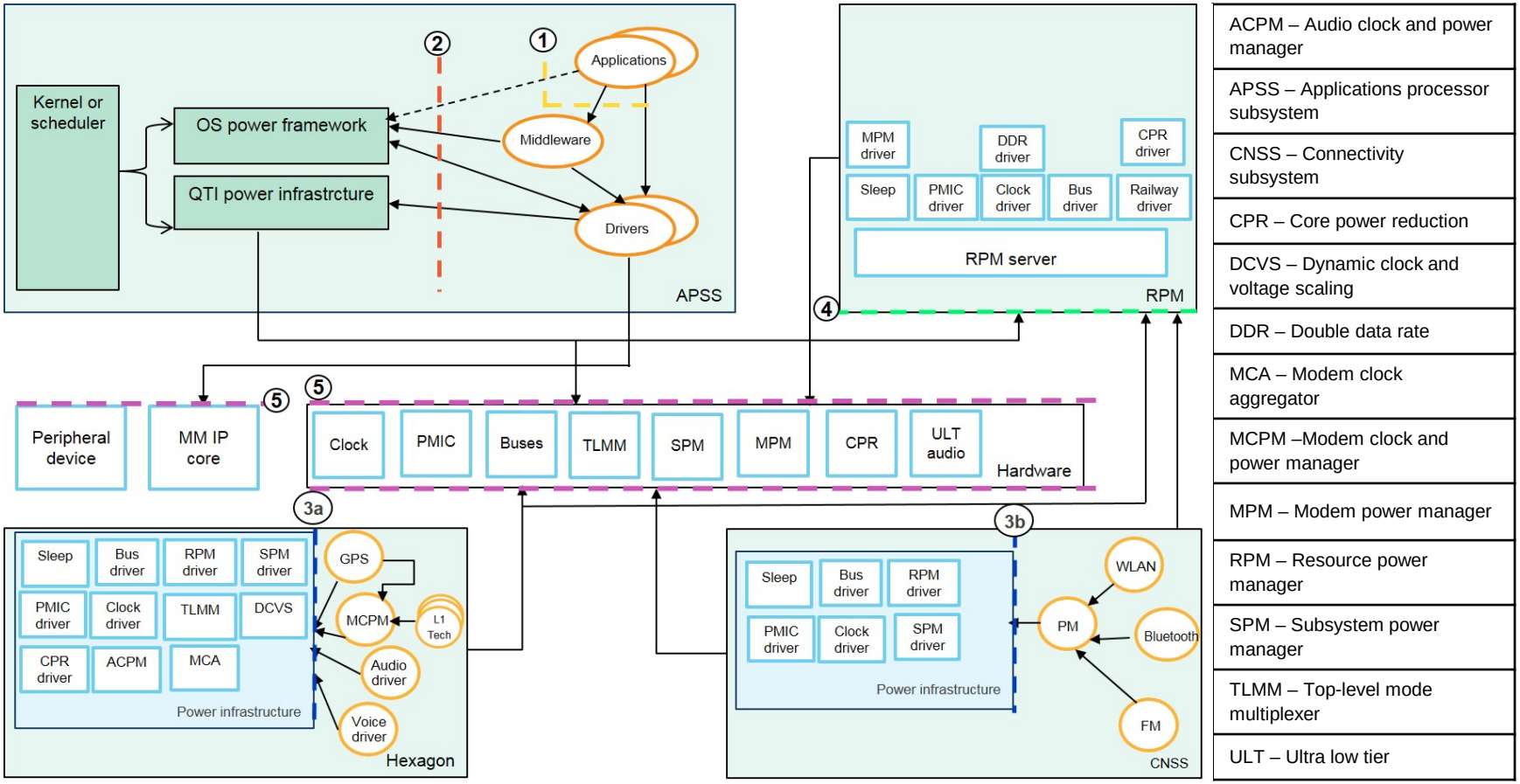
- At the end of this presentation, you will understand the APQ8016E system power management architecture, features, and modes.
- This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software.

Note: Enabling some features may require additional licensing fees.

Power Management Software Architecture

Architecture Diagram

The following figure depicts a high-level view of the software architecture. The flow between interfaces is explained in slides 9 and 10 *Architecture flow*.



ACPM – Audio clock and power manager

APSS – Applications processor subsystem

CNSS – Connectivity subsystem

CPR – Core power reduction

DCVS – Dynamic clock and voltage scaling

DDR – Double data rate

MCA – Modem clock aggregator

MCPM –Modem clock and power manager

MPM – Modem power manager

RPM – Resource power manager

SPM – Subsystem power manager

TLMM – Top-level mode multiplexer

ULT – Ultra low tier

Architecture Flow (1 of 2)

1. High-level operating system (HLOS) application interface
   - Determines the applications that run using the interface.
   - Handles display and backlight.
   - Provides a way to influence system-wide suspend. Currently for the Android devices, it is done via command prompt:
     - `echo mem > /sys/power/autosleep`
2. APSS power infrastructure interface
   - Enables usage for multimedia clients such as audio, video, display, low-power audio subsystem (LPASS) and so on. The clients that use the interface are determined by HLOS.
   - The interface is much richer than the HLOS application interface and allows all the software drivers and middleware that control hardware to request the required power resources, for example, CPU, bus bandwidth, and so on.
3. QTI native power infrastructure interface.
   - Acts as an interface to the power infrastructure used by clients on processors other than the APSS. This interface must be the same across different processors.

Architecture Flow (2 of 2)

4. RPM interface
   - Enables the interprocessor communication interface between RPM and the other processors in the system. It is a shared memory interface. All software components access this interface through the RPM driver.
   - Handles requests for shared resources.
5. Hardware interface
   - Acts as the hardware-software interface.
   - Enables all the hardware drivers to access the hardware. For example, it enables the PMIC drivers to set the PMIC voltages or clocks.

Power Management Software Features

Power Management Software Features (1 of 5)

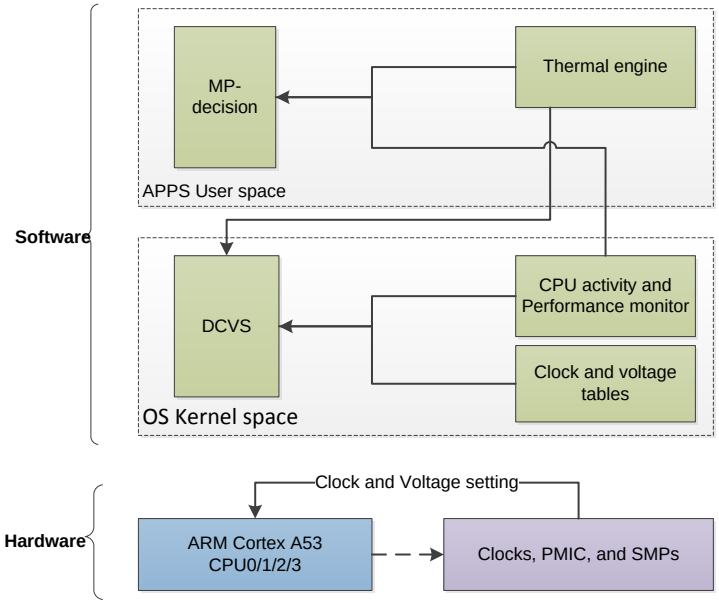
- XO Shutdown mode
  - A low-power mode that helps in reducing the power consumption when the device is idle.
  - During this mode, the core crystal oscillator (CXO) buffers at PMIC are switched off, leaving CXO running.
  - CXO still needs to be generated as it generates the 32 kHz sleep clock in PMIC.
  - No clock is fed to APQ except the 32 kHz sleep clock, which is required for the always-on processor.
  - To enter XO shutdown, all master processors must be in the Power Collapse mode and respective master dedicated clocks should be switched off, and shared clocks should have the off vote from their clients.
- Vdd minimization
  - Deepest low-power mode that can be achieved in the system by minimizing the digital rail (VddCx) and memory rail (VddMx) to their lowest possible voltage.
  - When Vdd minimization is achieved, the chip is not operational, except for detecting wake-up interrupt/timer expiration; however, all hardware (supplied by VddCx or VddMx) states are still maintained. These two power domains cannot be power-collapsed, so they are put to a lower voltage that can sustain the contents in memories.
  - Lowering the voltage saves leakage current, and therefore, reduces the power consumption when device is idle.
  - To enter Vdd minimization, all master processors should vote for XO Shutdown as well as retention voltages on VddCx or VddMx voltage rails.

Power Management Software Features (2 of 5)

- Static voltage scaling (SVS)
  - The voltage can be scaled when the performance needs of the chip are scaled.
  - This feature helps run the device at lower voltages when device performance needs are lower and thus helps in reducing power consumption.
- Processor power collapse
  - A processor uses the SPM hardware to power collapse. This removes power to the processor core.
  - When the processor no longer performs, the Sleep task runs. Within Sleep, the SPM is set up and the software wait for interrupt (SWFI) instruction is executed. This sends a signal to the SPM to start the SPM state machine, and this state machine continues the power-down process.
- DCVS
  - The DCVS technique is used to lower or raise the voltage when performance changes are made to the core, which cause the frequency requirements to drop or rise.
  - This feature helps to reduce the leakage current during active use cases.

Power Management Software Features (3 of 5)

- CPU DCVS with MP-decision
  - The MP-decision algorithm is a user space algorithm that monitors the load on CPUs to determine if any additional cores should be powered-up or a core needs to be power-collapsed.
  - MP-decision can hotplug a core depending on the thermal conditions.
  - DCVS (CPU frequency governor)
    - Scales the clock to a minimum frequency for all the active cores that meet the required quality of service (QoS).
    - Adjusts the corresponding (statically determined) voltage.
    - Depending on the temperature of the core, DCVS can cap the maximum operating frequency of the CPU.



Power Management Software Features (4 of 5)

- Host subsystem DCVS
  - Also referred as CPU dynamics, it scales the CPU clock based on the measured CPU utilization and million instructions per second (MIPS) request from the clients. As a consequence of a CPU clock change, CPU dynamics makes implicitly instantaneous bus bandwidth requests to the bus arbiter for CPU data and instruction access from CPU to DDR.
  - The following table lists the supported frequencies that the host (Qualcomm Hexagon™ DSP) runs according to the load conditions:

	Frequency (MHz)
Hexagon DSP	19.20
	115.20
	144.00
	230.40
	288.00
	384.00
	576.00
	691.20

Power Management Software Features (5 of 5)

- GPU DCVS
  - This is a low overhead algorithm that dynamically scales the GPU frequency based on the load, and therefore, reduces the system power consumption for the active GPU use cases without negatively impacting the performance.
  - The following table lists all the supported frequencies for the GPU core. For more information, refer to *Qualcomm Snapdragon 410E Processor APQ8016E Clock Plan* (LM80-P0436-55).

	Frequency (MHz)
GPU	19.200
	50.000
	80.000
	100.000
	160.00
	177.780
	200.000
	266.670
	310.00
	400.000

Power Management Hardware Features

Power Management Hardware Features (1 of 2)

- Single CXO
  - The CXO at a frequency of 19.2 MHz acts as a source to the clocks supplied to different functional blocks on APQ SoC and is always on. Its buffers are turned off when the XO Shutdown mode is exercised.
  - The sleep clock is derived from CXO and is used to clock the always-on domains such as the MPM, parts of the host core, and timer circuits. The sleep clock, at a frequency of 32 kHz, is used when the device is in the XO Shutdown mode.
- Multiple voltage domains
  - VddMx: Represents the on-chip memories. This power domain is never switched off but can be minimized to a lower power, typically when APQ is in deep sleep.
  - VddCx: Represents all the digital logic circuits and cores of APQ that must retain a minimum voltage, even when APQ is in deep sleep (with XOs off).
  - VddApss: Supplies voltage to APSS cores and the respective L1 cache memories.
  - VddModem: Supplies voltage to the modem processor subsystem core.

Power Management Hardware Features (2 of 2)

- DDR Self-refresh
  - In the Self-refresh mode, the power state allows DDR to be the lowest idle mode. The voltage supply to the DDR power rail is minimized to reduce the leakage current and retain the contents of DDR.
  - DDR is configured to self-refresh during selection of XO Shutdown or Vdd Minimization low-power modes.
- Rapid bridge core power reduction (RBCPR)
  - It is the hardware block that provides a feedback loop to optimize the voltage setting for a core.
  - RBCPR hardware uses the sensors embedded in APQ that provide real-time feedback on the chip performance based on the process and temperature.
  - Closed-loop feedback is processed by the software to make granular-level voltage adjustments.
  - RBCPR helps to reduce power consumption for active use cases by reducing voltage of a core.
- Global distributed head switch (GDHS) and bulk head switch (BHS)
  - For processors on shared domain that do not have a dedicated power rail and therefore, share one power rail, GDHS and BHS circuits are provided to enable individual power-collapse.

Power Management Modes

Low-Power Modes in Applications CPU Subsystem (1 of 3)

- SWFI
  - SWFI is an ARM-supported instruction. After execution, ARM will be in Halt state and the clock is gated for the individual core.
  - CPU core SWFI is done through ARM WFI instruction. CPU internal memory including CPU registers, and L1 and L2 cache contents is fully maintained. Before entering the SWFI state, the memory access is completed to avoid potential deadlocks. If the memory access causes an interrupt, the CPU core maintains the L2 coherence. While in SWFI state, all debug channels such as JTAG and ETM are active. Any debug request can wake up the CPU core.
  - Qualcomm generic interrupt controller (QGIC) and timers associated with the CPU core in the SWFI state are active. Any interrupts and activated timers can get the CPU core out of the SWFI state. Once restored, the CPU core can continue on the idle tasks.
  - SWFI state is entered during system suspend if power collapse is not enabled for the system suspend.
  - SWFI state is entered during system idle if power collapse exit latency cannot meet the PM_QoS_DMA_Latency requirement.

Low-Power Modes in Applications CPU Subsystem (2 of 3)

- Stand-alone power collapse (without RPM notification)
  - In this state, the CPU core power rail is off and the clock is gated while the shared resources (XO buffers, L2 cache, VddCx, and VddMx) remain intact. However, the CPU core internal memory (registers and L1 cache) contents are lost. When interrupts wake the CPU core, the voltage and clock are restored and the CPU core goes through the warm boot sequence, and continues execution from where it had halted on power collapse entry. Compared to SWFI, the extra latency is added because of the CPU core power-off and restore, and required warm boot sequence.
- Power collapse (with RPM notification)
  - Similar to stand-alone power collapse, the CPU core power rail and clock are off during this state. The RPM is notified of the CPU core power state change and the shared resources power state is impacted.
  - After RPM is notified of the shared resources required by the CPU core, the CPU core issues the WFI instruction to kick off the power collapse sequence.

Low-Power Modes in Applications CPU Subsystem (3 of 3)

- Invocation of low-power mode
  - Hotplugging – CPU can go into the Low-power mode through hotplugging.
    - The Linux CPU hotplug provides the option to turn nonboot CPUs online or offline to user space processes.
    - MP-decision process can hotplug the core based on the CPU load. Core can be removed or brought back through a file node (/sys/devices/system/cpuX/online) access.
  - Idle – A state with no thread to run; the Low-power mode is selected in sleep task based on the following:
    - PM_QoS_DAM_Latency requirement.
    - Long idle residency to break even on energy cost.
    - Minimal impact on current system performance.
  - Suspend – Invoked by the user or user interface; Once invoked, the deepest available Low-power mode is selected.

C-States and CPU Low-Power Modes

- C-state is CPU idle state with different power levels. The larger the C-state number, the lower the steady state power level, and higher the latency and energy cost of entry and exit.
- The steady-state power level, entry and exit latency, and energy cost depends on the platform chipset hardware architecture and implementation (For example, CPU core, digital core, bus, memory leakage, or PMIC efficiency).
- With more supported C-states, a finer tradeoff can be made between power consumption and performance. The following table lists the C-states implemented on the APQ8016E chipset.

C-state	Name	Description
C0	Halt/SWFI	• CPU core clock domains are off • Power domains and QGIC clocks are on • VddMx and VddCx are the active voltages
C1	Stand-alone power collapse (GDHS)	• CPU core clock domains and power domains are off • QGIC clock, CXO, or L2 cache on. • VddMx and VddCx are the active voltages
C2	Power collapse with the RPM notification	• CPU core clock domains and power domains CXO and L2 cache are off. • VddMx and VddCx vote for retention voltages.

Low-Power Modes in Modem Subsystem

- DSP subsystem supports multiple low-power modes such as Power Collapse, WFI, L2 Retention and Non-retention. The sleep module enables the system to enter these modes based on latency and power penalty to enter or exit these modes.
- Power Collapse
  - Ensures complete power collapse of all the hardware blocks, which helps to reduce the hardware leakages.
  - During power collapse enter and exit calls, the modem hardware performs modem PLL on/off, and CPU clock save or restore.
- WFI
  - Similar to the WFI instruction on ARM, DSP subsystem offers a WAIT instruction that can bring the processor to a Low-power mode.
  - In this mode, the processor clock stops and no instruction is fetched and executed. However, the register states are preserved. When the *wait* instruction is executed, the thread to be idled should complete the packet it is processing before entering the Wait mode.
- L2 Retention and Non-retention
  - DSP subsystem has L1 and L2 cache, and L1 cache is maintained in the Processor WFI mode. L2 is power-collapsed when the processor is power-collapsed.
  - L2 cache can be in either Retention or Non-retention mode when the processor is power collapsed.

Support

Acronyms (1 of 2)

Acronym or term	Expansion
ACPM	Audio clock and power manager
APSS	Applications processor subsystem
BHS	Bulk head switch
CNSS	Connectivity subsystem
CPR	Core power reduction
CXO	Core crystal oscillator
DCVS	Dynamic clock and voltage scaling
DDR	Double data rate
GDHS	Global distributed head switch
HLOS	High-level operating system
LPASS	Low-power audio subsystem
MCA	Modem clock aggregator
MCPM	Modem clock and power manager
MIPS	Million instructions per second
MPM	Modem power manager

Acronyms (2 of 2)

Acronym or term	Expansion
QGIC	Qualcomm generic interrupt controller
QoS	Quality of service
RBCPR	Rapid bridge core power reduction
RPM	Resource power manager
SPM	Subsystem power manager
SVS	Static voltage scaling
SWFI	Software wait for interrupt
TLMM	Top-level mode multiplexer
ULT	Ultra low tier

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