Group 4 - Cache simulator (Full associative / LRU)

Program Output Debugging

Test Case 1 (Normal Case)

Input:

Block Size: 2
Main Memory Size: 8
Cache Memory Size: 4
Program Flow: 1,7,5,0,2,1,5,6,5,2,2,0
Cache Access Time(ns): 1
Memory Acces Time(ns): 10

Result:

Cache Hits: 4
Cache Misses: 8
Miss Penalty = 1ns + 10ns + 10ns + 1ns = 22ns
Average Memory Access Time = (0.33 * 1ns) + (0.67 * 22ns) = 15.00ns
Total access time = (4 * 2 * 1ns) + (8 * 2 * 10ns +1ns) + (8 * 1ns) = 192.00ns

Test Case 2 (Different Input)

Input:

Block Size: 2
Main Memory Size: 8
Cache Memory Size: 4
Program Flow: 1,7,5,0,2,1,5,6,5,2,2,0
Cache Access Time(ns): five
Memory Acces Time(ns): 10

Result:

Please enter a valid cache access time greater than or equal to 0.

Test Case 3 (Incomplete Input)

Input:

Block Size: -
Main Memory Size: 16
Cache Memory Size: -
Program Flow: 1,2,3,4,5,6,7
Cache Access Time(ns): 1
Memory Acces Time(ns): 10

Result:

Please enter a valid block size greater than 0.
Please enter a valid cache memory size greater than 0.

Program Analysis:

The website is a Cache simulator designed for Block-set-associative in Least Recently Used. The user will be input the size of the block, main memory, cache memory, the program flow followed by the access time of cache and memory. The program will calculate the cache hits and misses, its miss penalty, average and total memory access time, and a cache snapshot from the given input. The user also has an option to download the text file of the recently calculated values.

This program was designed using javascript, and CSS to style and layout the web page. The webpage is deployed using Vercel through this link: https://csarch2spcachesimulatorfalru-kaitiepiees-projects.vercel.app/ and is also runnable locally using CMD.