ERICSSON

LULEÅ UNIVERSITY OF TECHNOLOGY
DIVISION OF EMBEDDED INTERNET SYSTEMS

DESIGN AND IMPLEMENTAION OF A DDR SDRAM CONTROLLER FOR SYSTEM ON CHIP

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Contents

- Double Data Rate Interfaces
- DDR SDRAM Architecture and Functionality
- DDR Memory Controller
- Data Resynchronization
- Floorplan and Place & Route
- Future Work
- Conclusion

Double Data Rate Interfaces

New

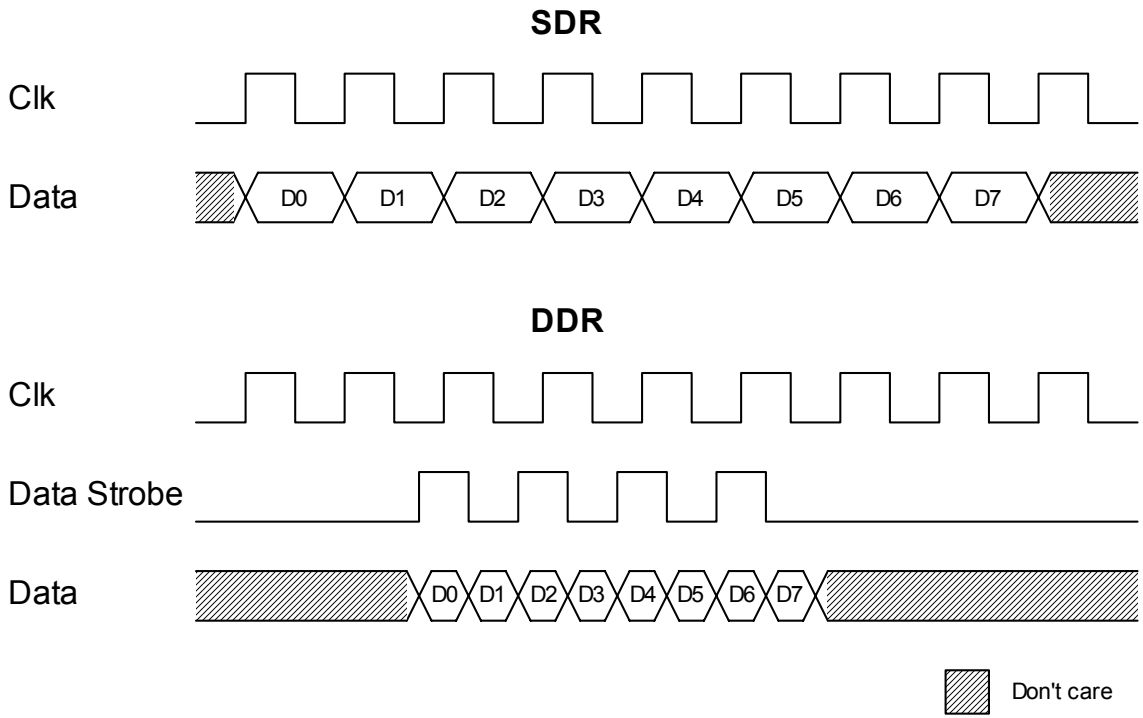
- Data Transmissions on rising and falling edge
- Data Strobe

Advantages

- Time of Flight
- Clock Skew
- Pin Count
- Bandwidth

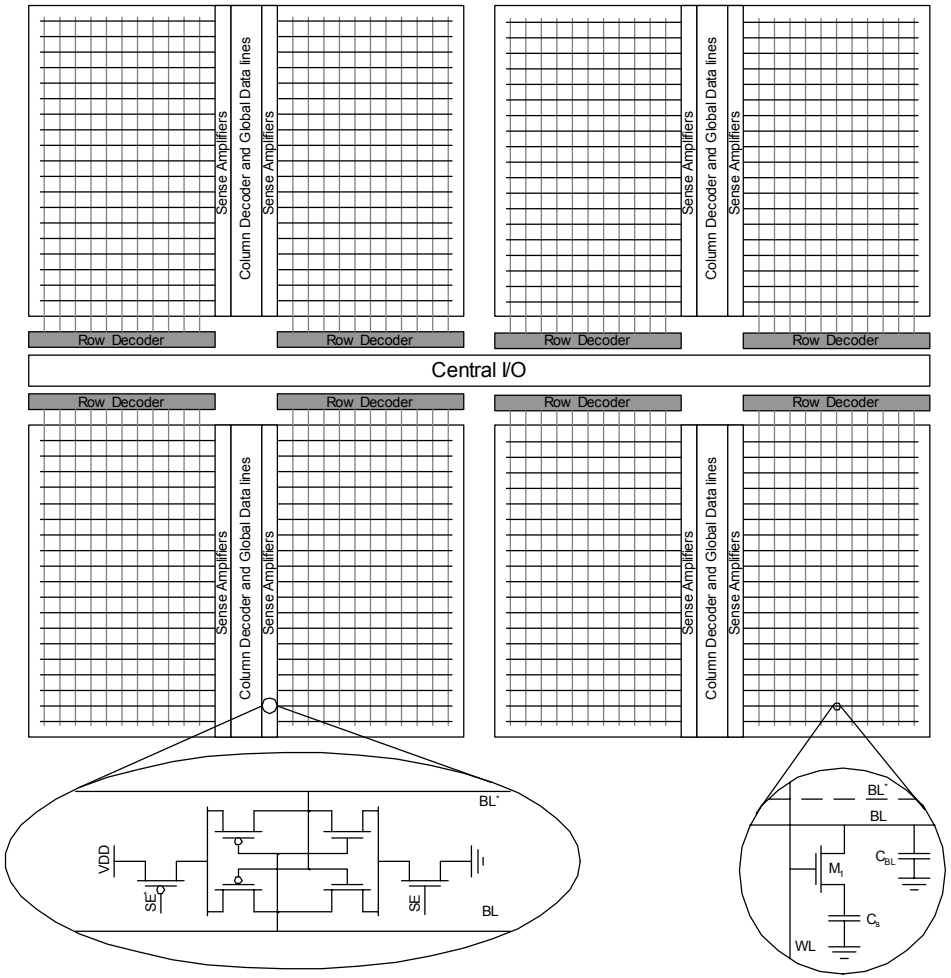
Disadvantage

- Synchronization



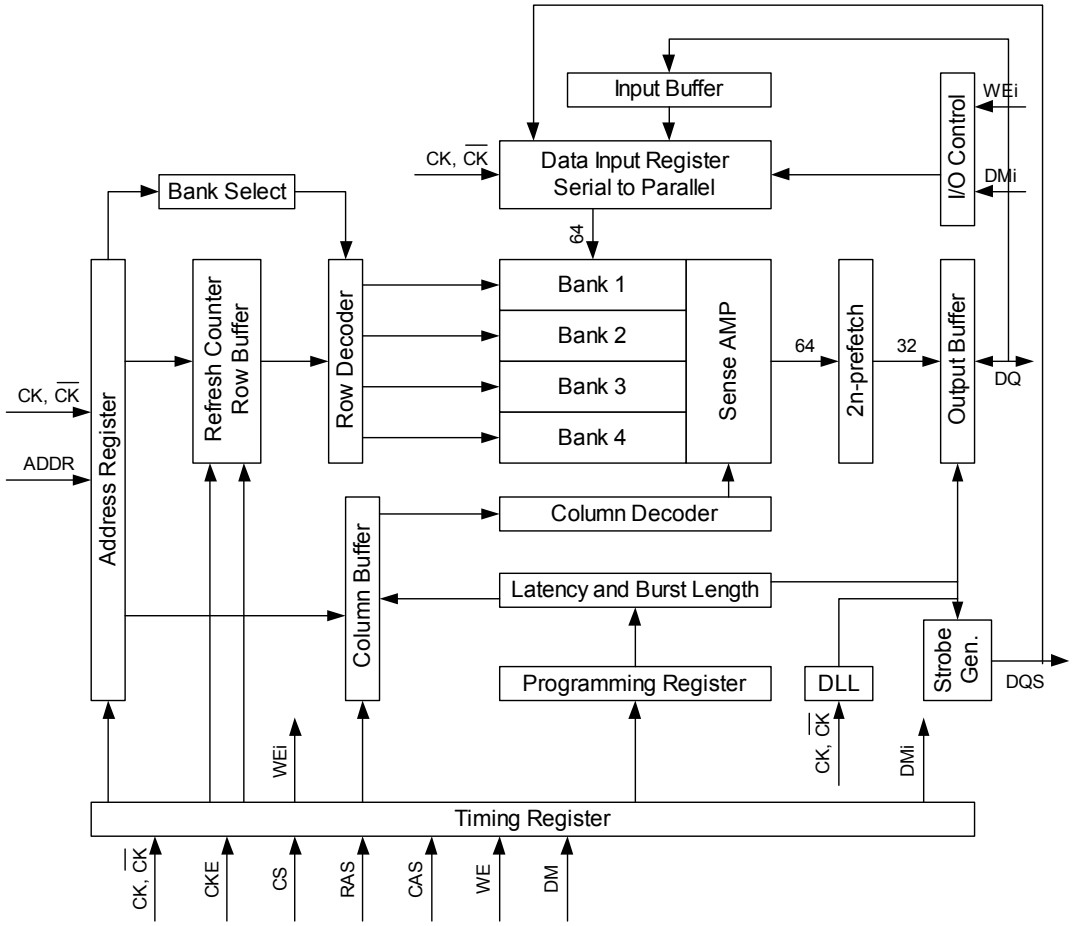
SDRAM Architecture

- Four Banks
- Row and Column Select Lines
- 1T Memory Cells
- Sense Amplifiers
- Global Data Path



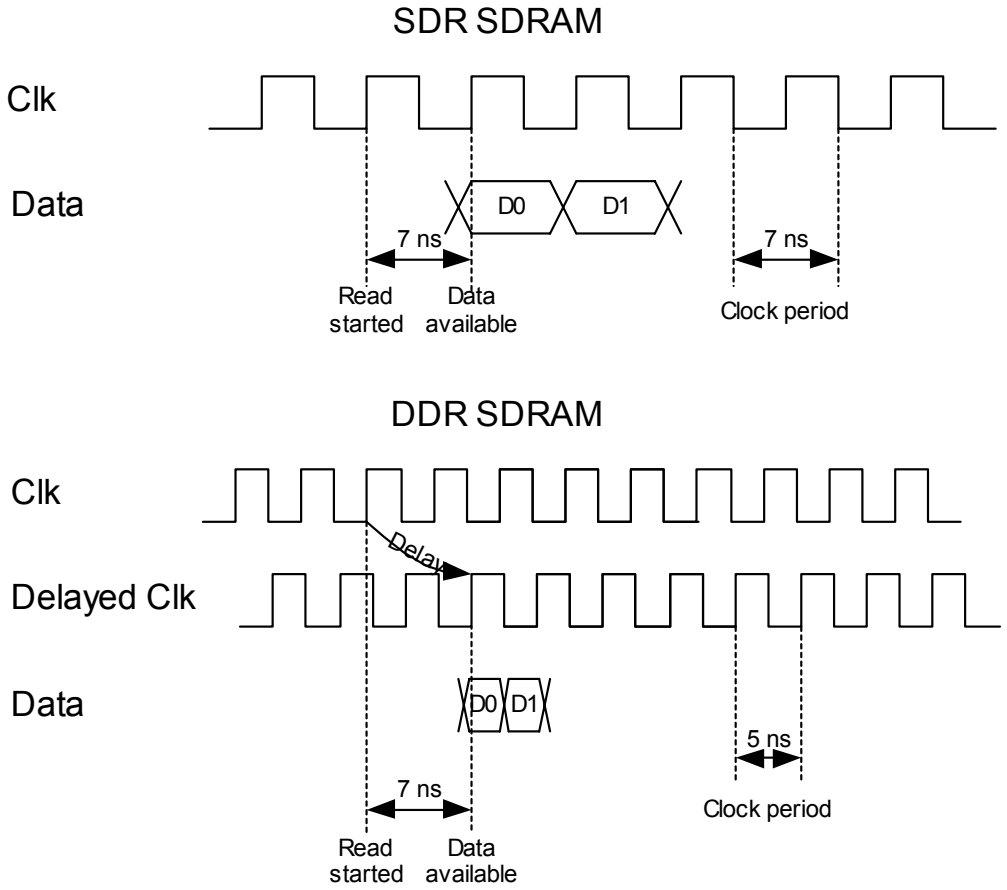
DDR SDRAM Architecture

- 2n-prefetch
- Delay Lock Loop



DDR SDRAM Improvements

- Long Delay in Column Decode and Data Lines
- Added a Delay Lock Loop to Increase Clock Frequency



DDR SDRAM Commands

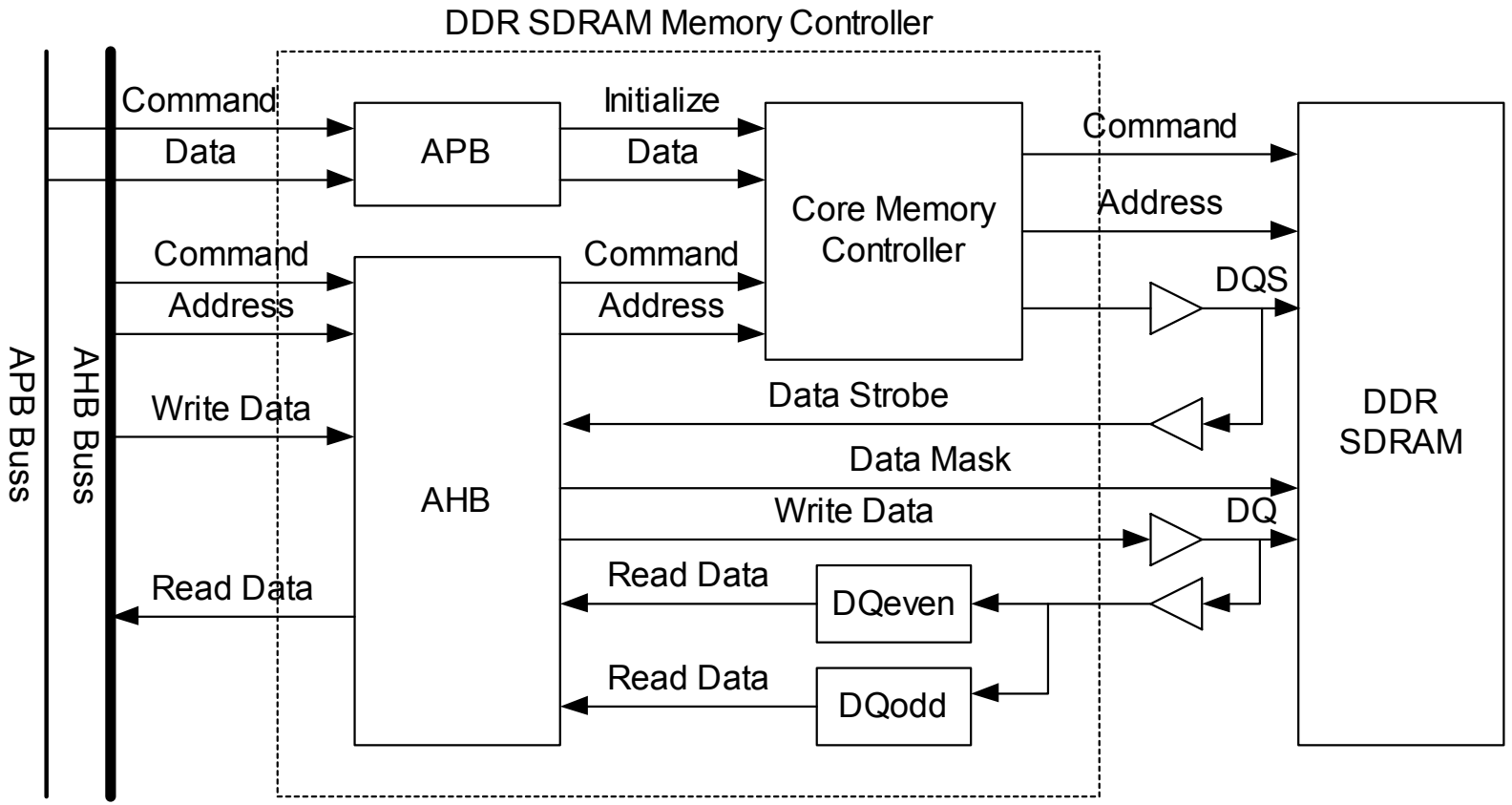
Same Commands as for Standard SDRAM

- READ
- WRITE
- ACTIVATE
- PRECHARGE
- REFRESH
- MRS (Mode Register Set)

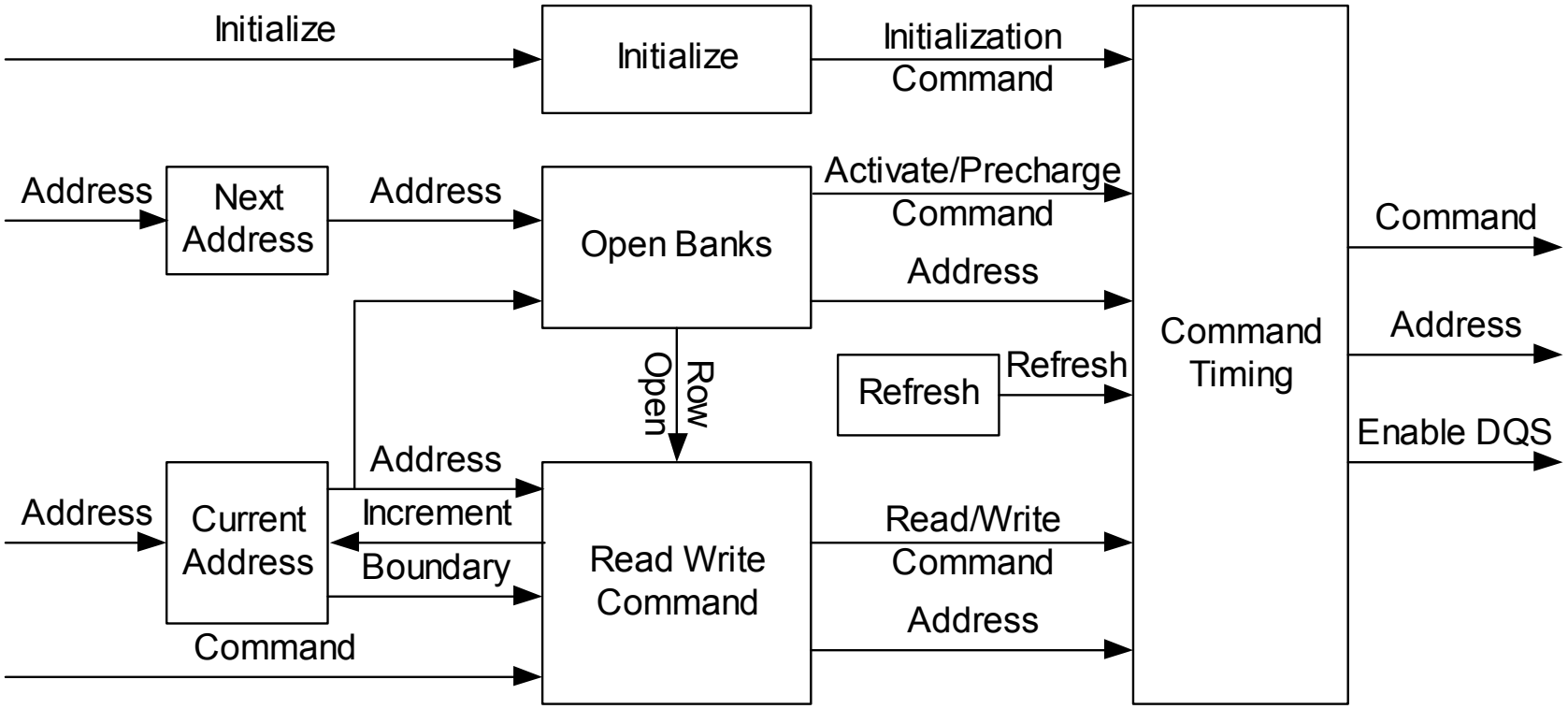
Added

- EMRS (Extended MRS)

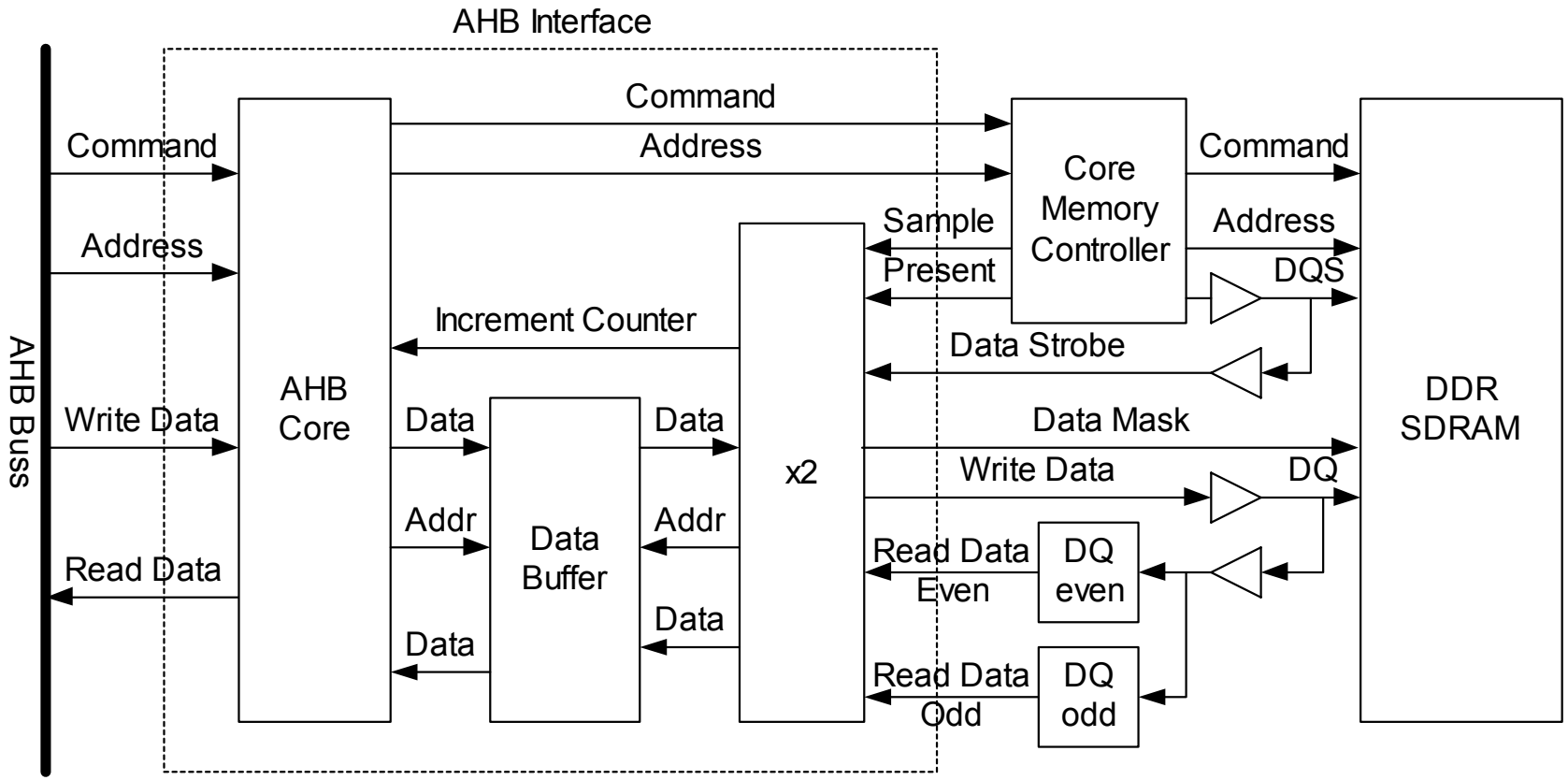
DDR SDRAM Memory Controller



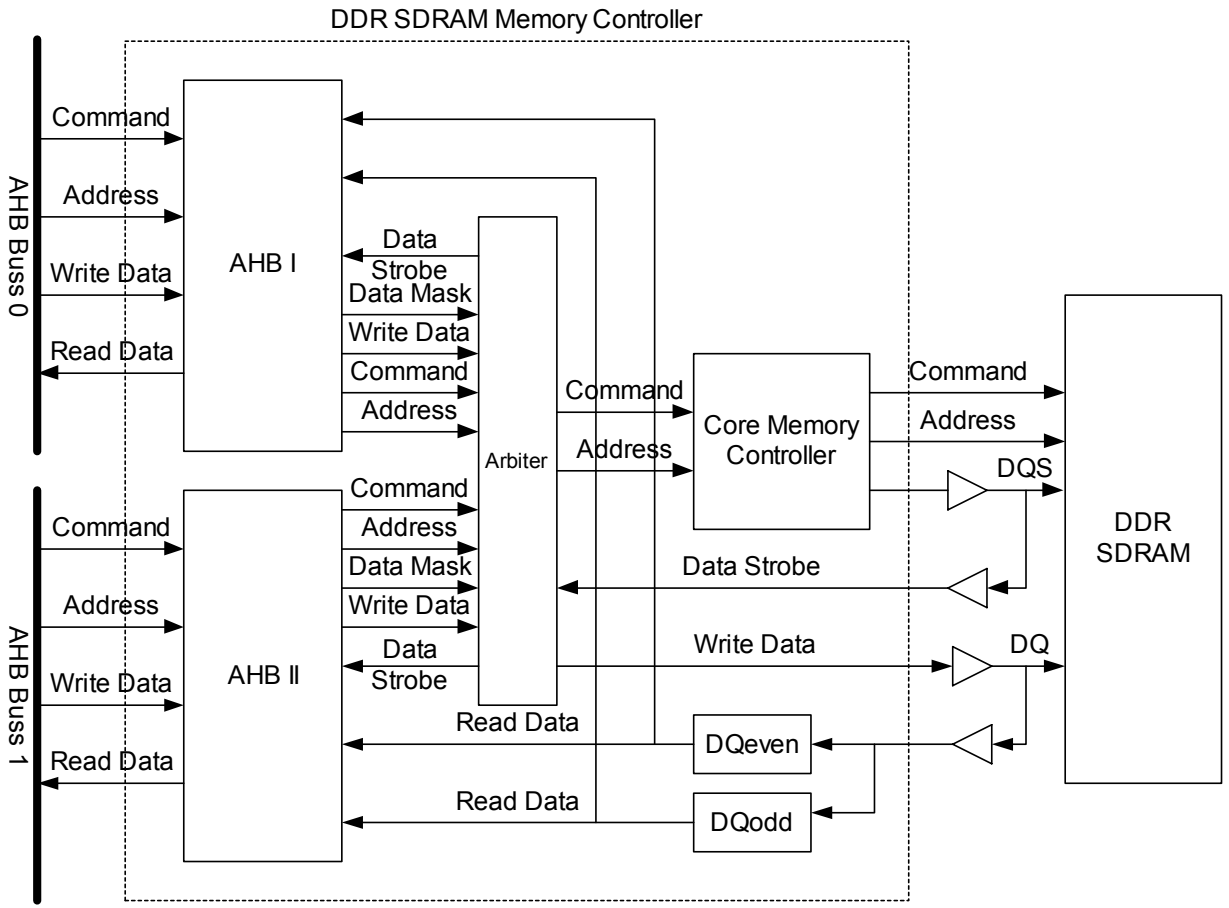
Core Memory Controller



AHB Interface

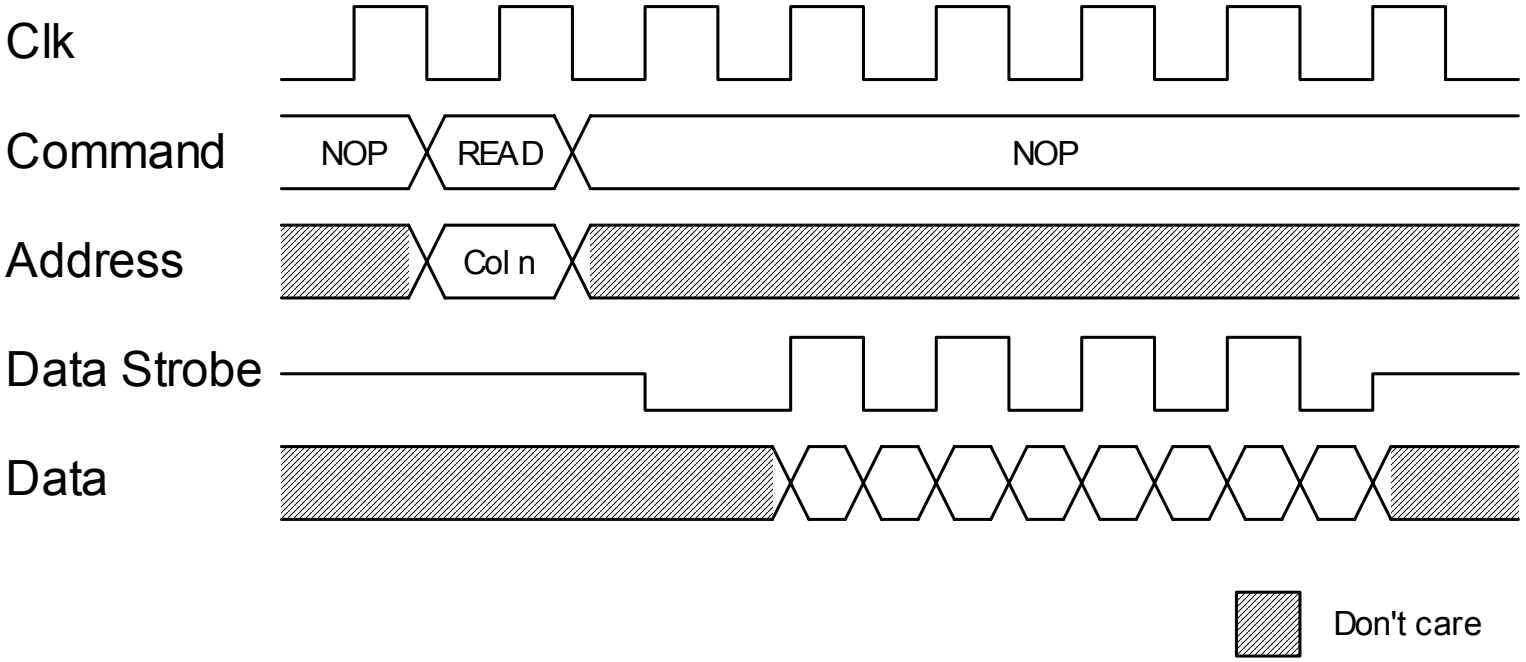


Arbiter


DDR SDRAM Memory Controller
AHB Buss 0
Command
Address
Write Data
Read Data
AHB I
Data Strobe
Data Mask
Write Data
Command
Address
Arbiter
Command
Address
Core Memory Controller
Command
Address
DQS
DDR SDRAM
AHB Buss 1
Command
Address
Write Data
Read Data
AHB II
Command
Address
Data Mask
Write Data
Data Strobe
Data Strobe
Write Data
DQ
Read Data
DQeven
Read Data
DQodd

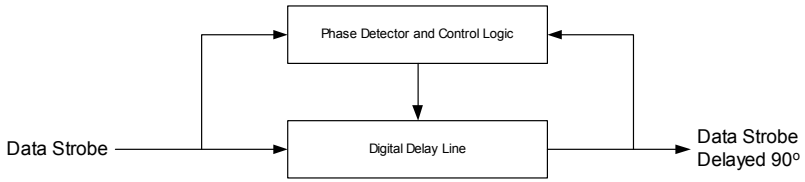
Capturing the Data

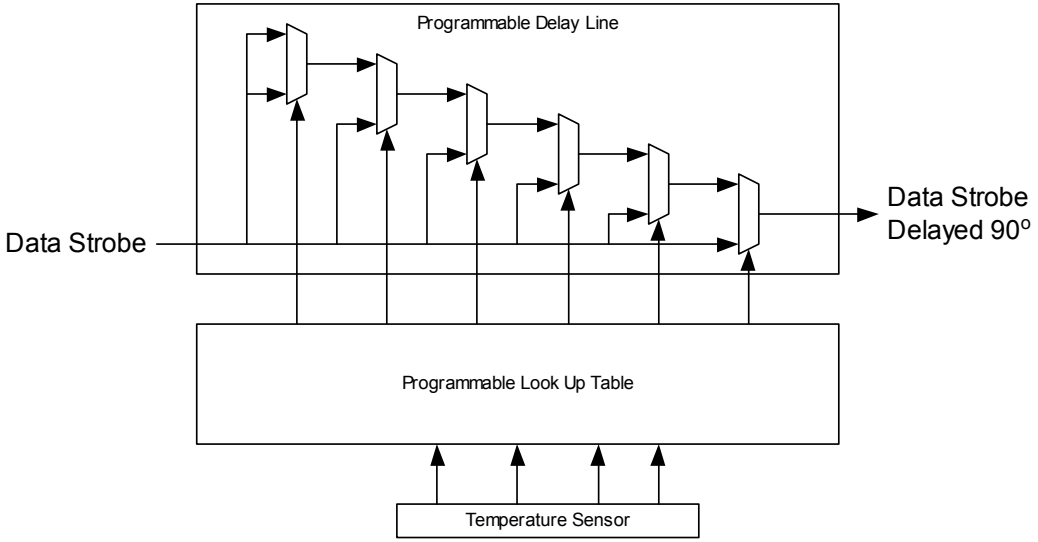
- Phase Shift the Data Strobe
- Resynchronize the Data



Phase Shift the Data Strobe

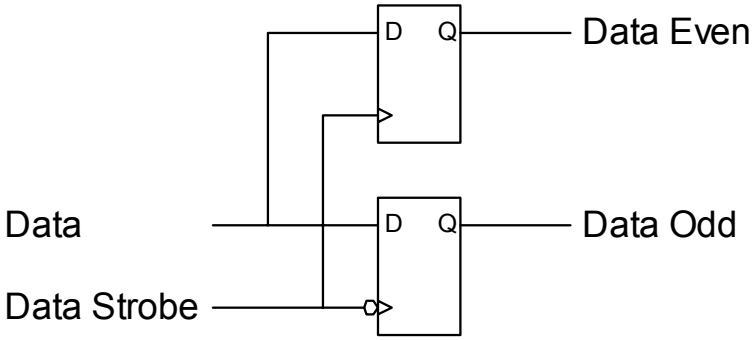
- Delay Lock Loop
- Inverter Delay
- PCB Line Delay
- Programmable Delay Line with Temperature Sensing

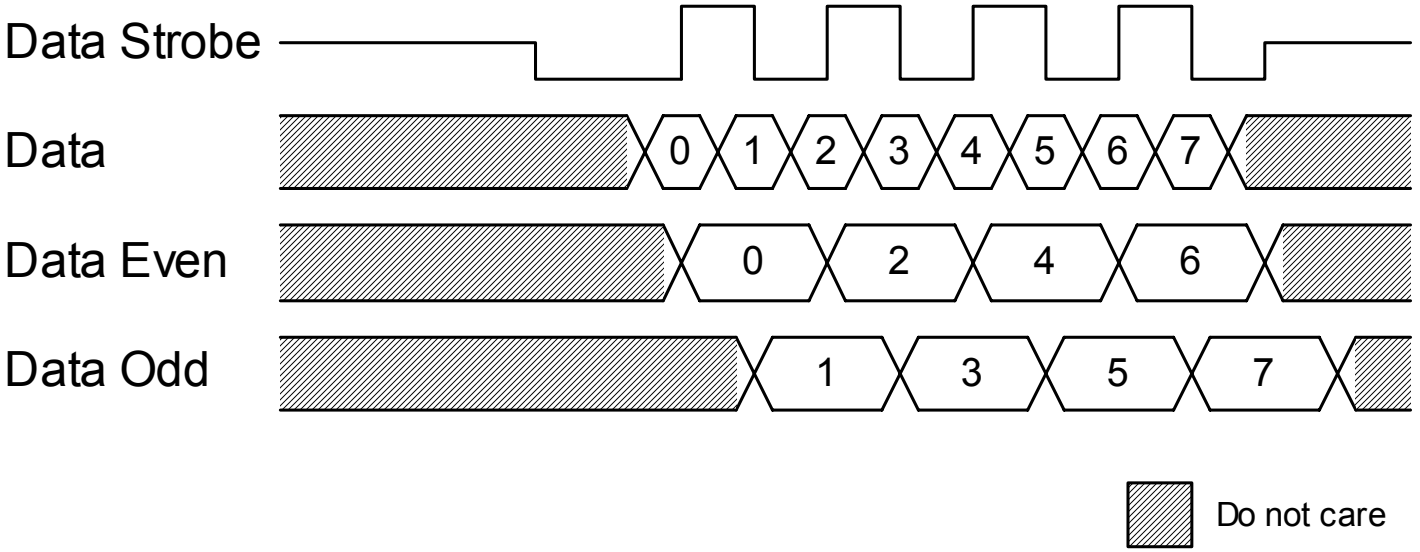




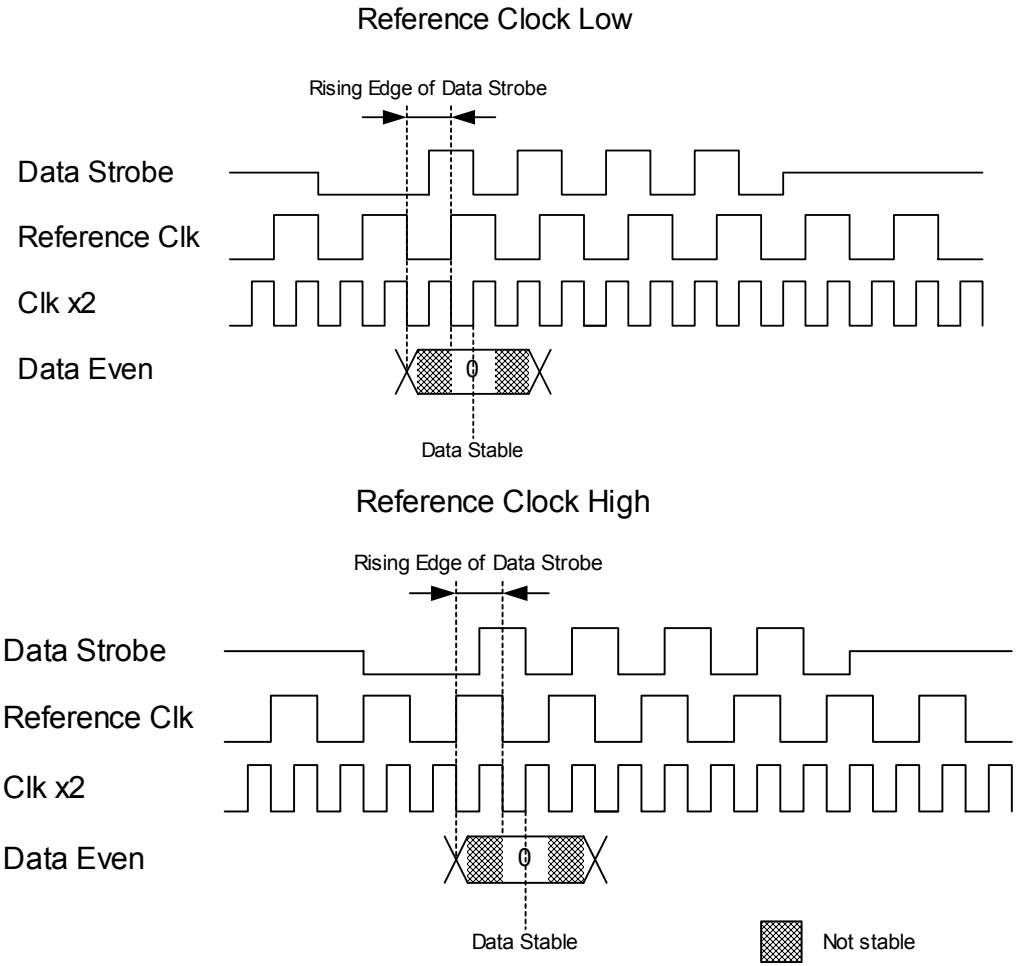
Synchronization of the Data

One Flip-Flop for each Flank to Sample



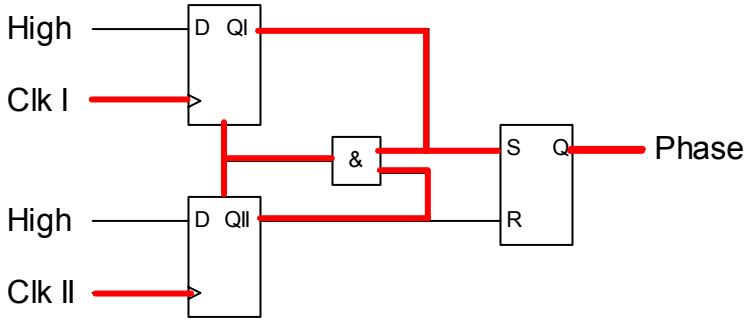


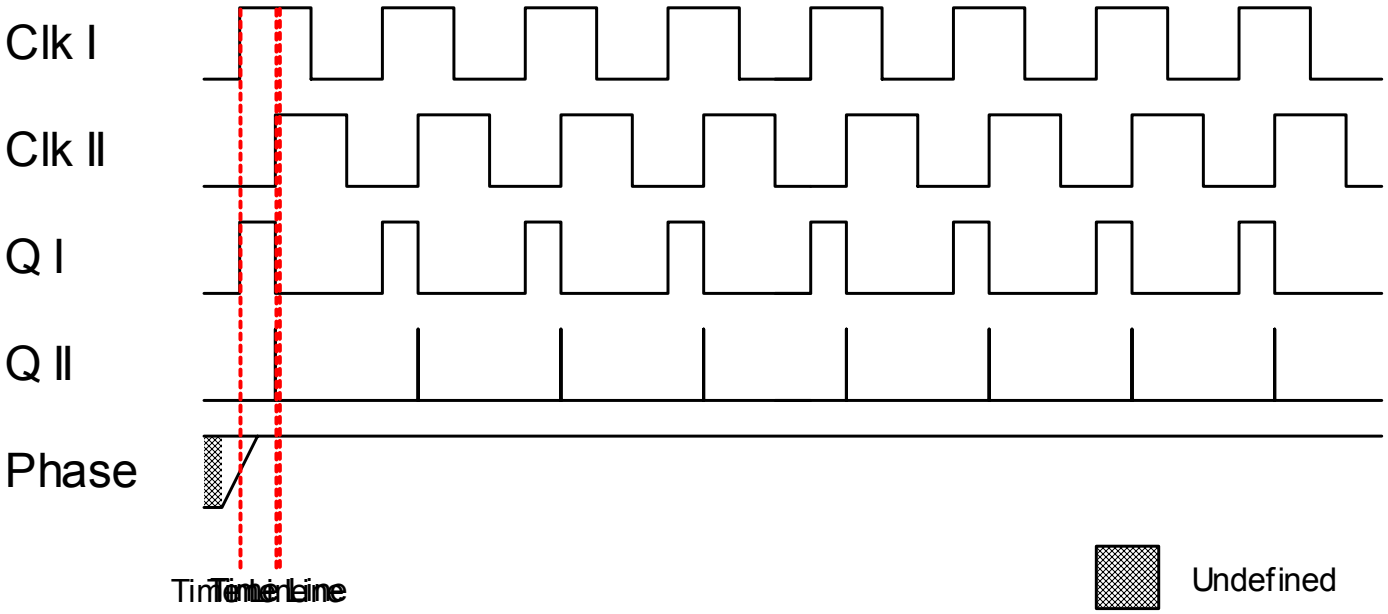
Synchronization of the Data Continued



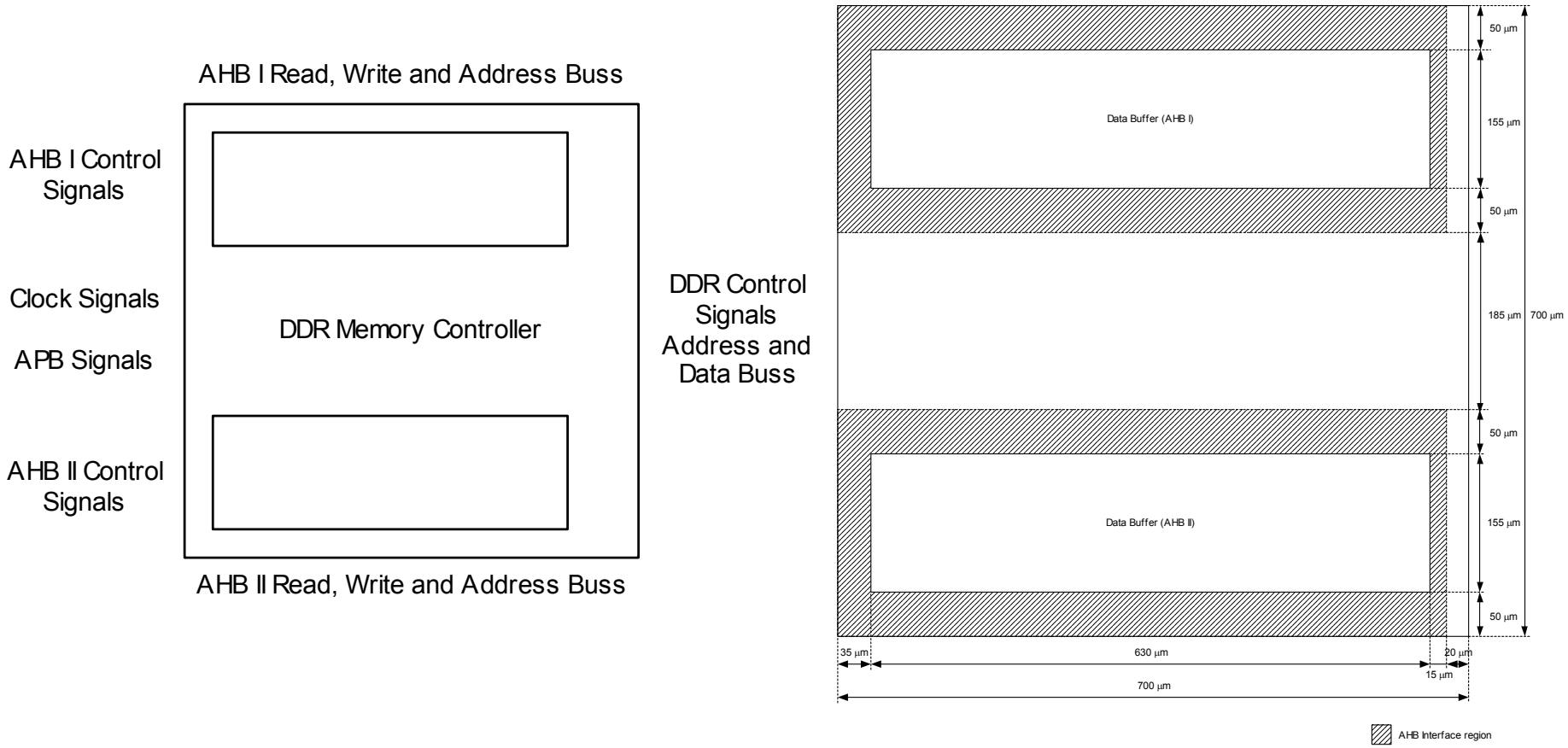
Synchronization of the Data Continued

Simplified Phase Detector

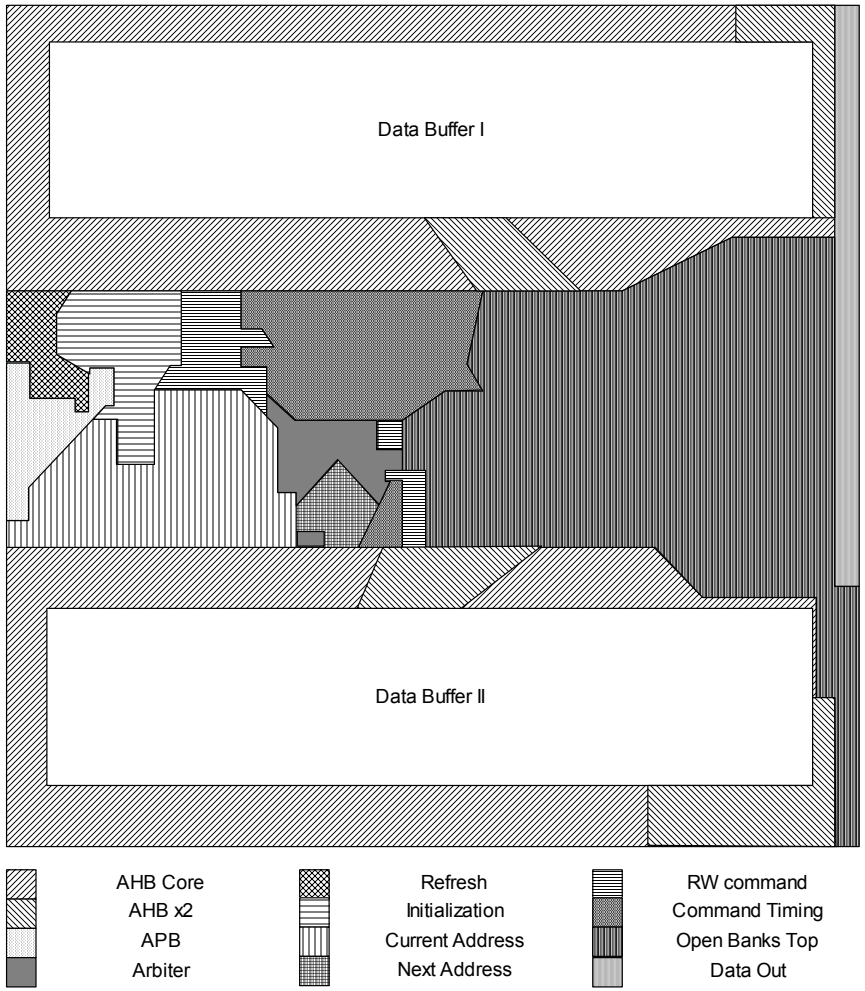




Floorplan


AHB I Read, Write and Address Buss
AHB I Control Signals
Clock Signals
APB Signals
AHB II Control Signals
DDR Memory Controller
AHB II Read, Write and Address Buss
DDR Control Signals Address and Data Buss
Data Buffer (AHB I)
Data Buffer (AHB II)
50 µm
155 µm
50 µm
185 µm
700 µm
50 µm
155 µm
50 µm
35 µm
630 µm
20 µm
15 µm
700 µm
AHB Interface region

Place & Route


Data Buffer I
Data Buffer II
AHB Core
AHB x2
APB
Arbiter
Refresh
Initialization
Current Address
Next Address
RW command
Command Timing
Open Banks Top
Data Out

Future Work

- Improved Refresh Handling
- Attempt to Reduce Initial Latency for Bursts
- Improved Buffer Handling

Conclusion

- Working Implementation
- Smaller Changes to Improve Performance
- Highlights Difficulties and Solutions

Questions ?