EE309 Microprocessors IITB-RISC-22

Design Document

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Hardware Flowcharts:

PC -> IM.A(Instruction memory),ALU.A K -> ALU.B ALU.C->T IM.D->IR	S0

T -> PC IR_{11-9} -> RF_A1 IR_{8-6} -> RF_A2 RF_D1 -> ALU.A RF_D2 -> ALU.B ALU.C -> T	S1

T->RF-D3 IR_{5-3} -> RF_A3	S2

T->PC IR_{11-9} -> RF_A1 IR_{8-6} -> RF_A2 RF_D1 -> ALU.A RF_D2 ->1SL(shift left)-> ALU.B ALU.C -> T	S3

T->PC IR_{5-0} -> SE-16 -> ALU.A IR_{8-6} -> RF_A1 RF_D1 -> ALU.B ALU.C -> T	S4

T-> RF_D3 IR_{11-9} -> RF_A3	S5

IR_{8-0} ->SE9-16 -> 7s -> RF_D3 IR_{11-9} -> RF_A3	S6

T->PC IR_{5-0} -> SE_{6-16} -> ALU.A IR_{8-6} -> RF_A1 RF_D1 -> ALU.B ALU.C -> T	S7

T->DM.A IR_{11-9} -> RF_A3 DM.D -> RF.D3	S8

T->IM.A IR_{11-9} -> RF_A2 RF_D2 -> DM.A	S9

PC->IM.A IM.D -> IR	S10

IR_{11-9} -> RF_A2 IR_{8-6} -> RF_A1 RF_D1 -> ALU.A RF_D2 -> ALU.B ALU.C -> T	S11

PC->ALU.B IR_{5-0} -> SE6-16 -> ALU.A ALU.C -> T	S12

T->PC	S13

IR_{11-9} -> RF_A3 T-> RF_D3	S14

PC -> ALU.B IR_{8-0} -> SE9-16 -> ALU.A ALU.C -> T RF_D1 -> ALU.A RF_D2 -> ALU.B ALU.C -> T	S15

IR_{8-6} -> RF_A2 RF_D2 -> PC	S16

IR_{11-9} -> RF_A1 IR_{8-0} -> SE9-16 -> ALU.A RF_D1 -> ALU.B ALU.C -> T	S17

T->PC IR_{7-0} -> T2 IR_{11-9} -> RF_A1 RF_D1 ->T3	S18

T3->DM.A T_4 -> RF_A3, INC DM.D -> RF_D3 T_2 -> 1SR	S19

INC->T4 T3 -> ALU.A K -> ALU.B ALU.C -> T	S20

T-> T_3 B -> T2	S21

T4 -> INC	S22

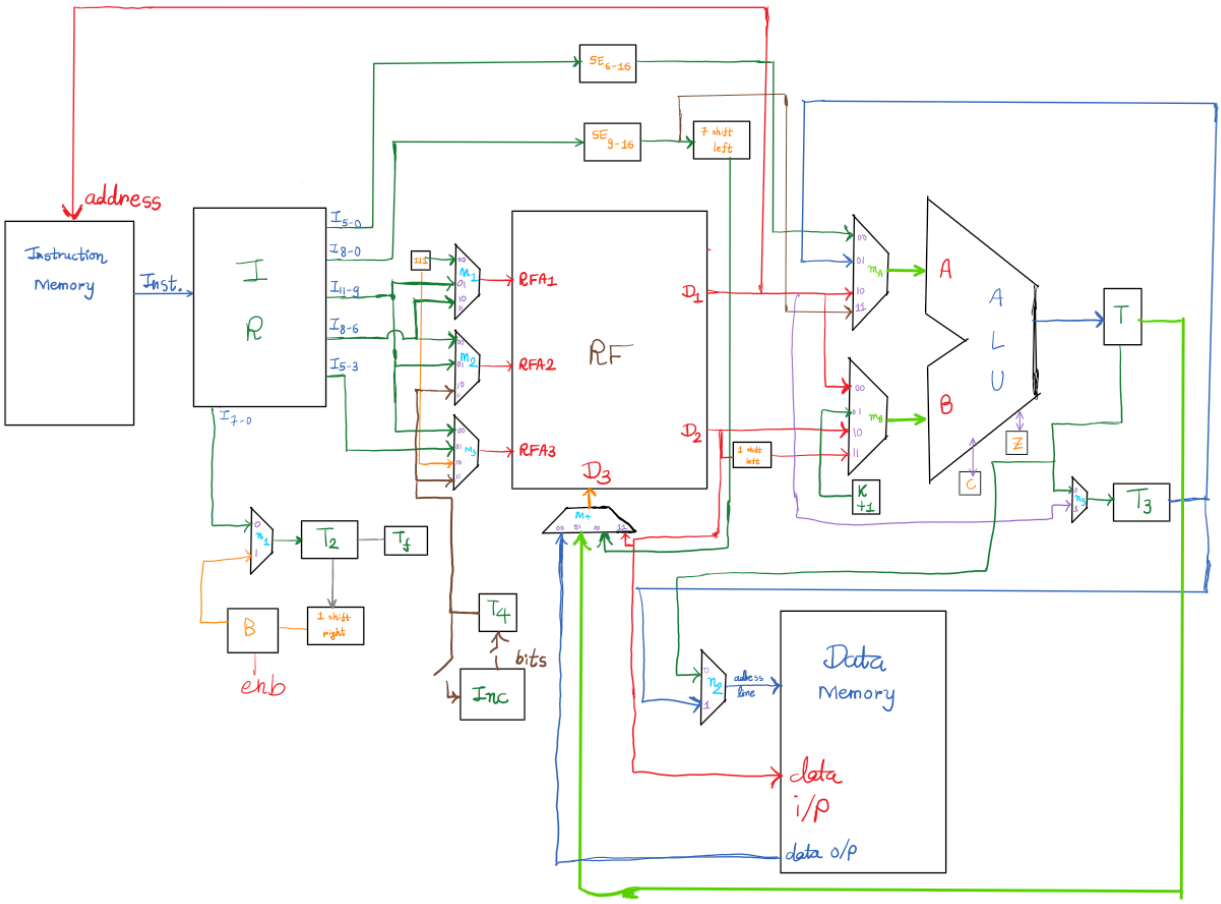
INC -> T4 B -> T2	S23

T3 -> memA T4 -> RFA2, INC RFD2 -> memD T2 -> 1S(R)	S24

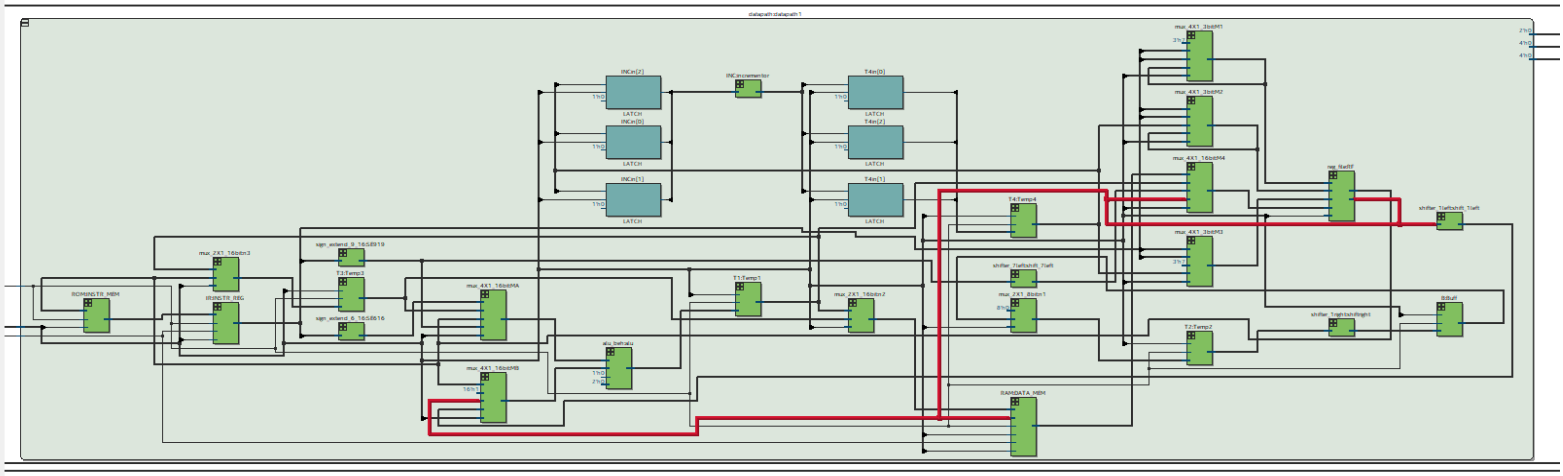
Instructions:

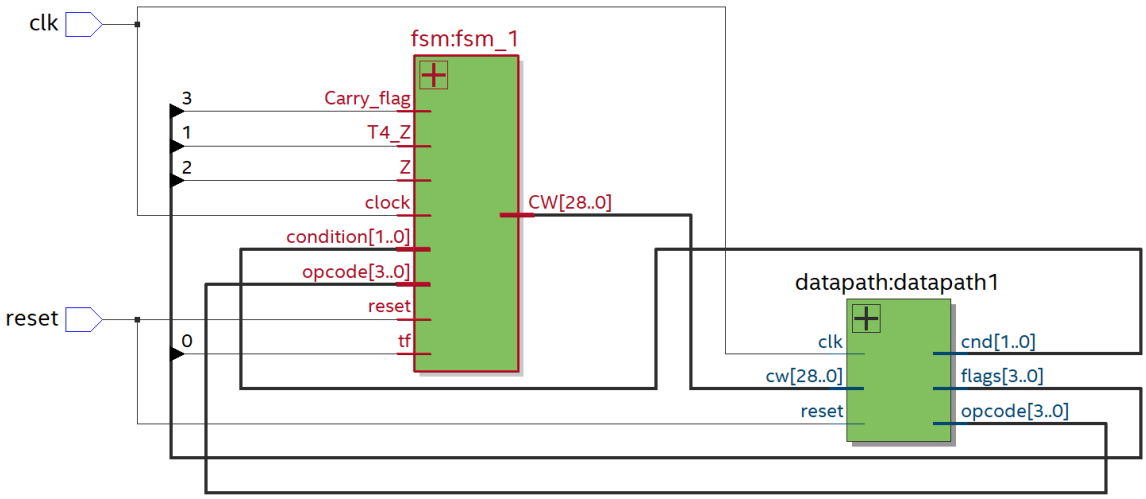
1. ADD:(0001)=>(S0,S1,S2)
2. ADZ:(0001)=>(S0,S1,S2)
3. ADC:(0001)=>(S0,S1,S2)
4. ADL: (0001)=>(S0,S3,S2)
5. ADI(0000)=>(S0,S4,S5)
6. NDU:(0010)=>(S0,S1,S2)
7. NDC:(0010)=>(S0,S1,S2)
8. NDZ: (0010) =>(S0,S1,S2)
9. LHI:(0100)=>(S0,S13,S6)
10. LW:(0111)=>(S0,S7,S8)
11. SW: (0101)=>(S0,S7,S9)
12. LM: (1100)=>(S0,S18, {If Tf=1 then S19,S20,S21 loop} {if Tf=0 then S22, S23, S19})
13. SM: (1101)=>(S0,S18, {If Tf=1 then S24,S20,S21 loop} {if Tf=0 then S22, S23})
14. BEQ: (1000)=>(S10,S11, {if z==1 then S12, S13} else {S0})
15. JAL: (1001) =>(S0,S14,S15,S13)
16. JLR: (1010)=>(S0,S14,S16)
17. JRI: (1011)=>(S0,S17,S13)

Datapath Design:

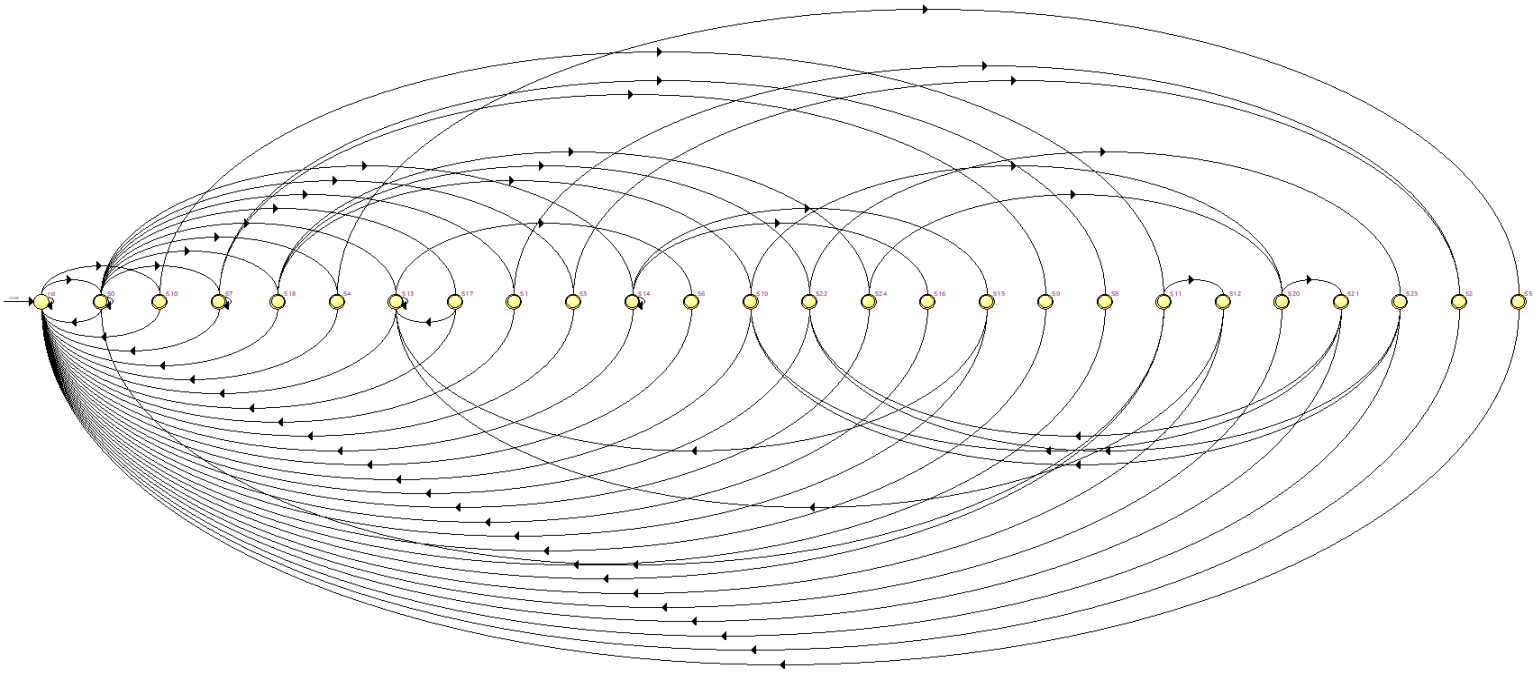


RTL viewer:




clk
fsm:fsm_1
3
Carry_flag
1
T4_Z
2
Z
clock
CW[28..0]
condition[1..0]
opcode[3..0]
reset
reset
tf
0
datapath:datapath1
clk
cnd[1..0]
cw[28..0]
flags[3..0]
reset
opcode[3..0]

State Transition Diagram:



State Transition Table:

Source State	Destination State	Condition
rst	S10	(!opcode[0]).(!opcode[1]).(!opcode[2]).(opcode[3]).(!reset)
rst	rst	(reset)
rst	S0	(!opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(!reset) + (!opcode[0]).(!opcode[1]).(opcode[2]).(!reset) + (!opcode[0]).(opcode[1]).(!reset) + (opcode[0]).(!reset)
S0	S18	(!opcode[1]).(opcode[2]).(opcode[3]).(!reset)
S0	S17	(opcode[0]).(opcode[1]).(!opcode[2]).(opcode[3]).(!reset)
S0	S14	(!opcode[0]).(opcode[1]).(!opcode[2]).(opcode[3]).(!reset) + (opcode[0]).(!opcode[1]).(!opcode[2]).(opcode[3]).(!reset)
S0	S13	(!opcode[0]).(!opcode[1]).(opcode[2]).(!opcode[3]).(!reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(!condition[0]).(condition[1]).(!Carry_flag).(!reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(condition[0]).(!condition[1]).(!Z).(!reset) + (opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(!condition[0]).(condition[1]).(!Carry_flag).(!reset) + (opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(condition[0]).(!condition[1]).(!Z).(!reset)
S0	S7	(opcode[0]).(opcode[2]).(!opcode[3]).(!reset)
S0	S4	(!opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(!reset)
S0	S3	(opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(condition[0]).(condition[1]).(!reset)

S0	rst	(!opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(reset) + (!opcode[0]).(!opcode[1]).(!opcode[2]).(opcode[3]) + (!opcode[0]).(!opcode[1]).(opcode[2]).(reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(!condition[0]).(reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(condition[0]).(!condition[1]).(reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(condition[0]).(condition[1]) + (!opcode[0]).(opcode[1]).(!opcode[2]).(opcode[3]).(reset) + (!opcode[0]).(opcode[1]).(opcode[2]).(reset) + (opcode[0]).(reset)
S0	S0	(!opcode[0]).(opcode[1]).(opcode[2]).(!reset) + (opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(!reset) + (opcode[0]).(opcode[1]).(opcode[2]).(opcode[3]).(!reset)
S0	S1	(!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(!condition[0]).(!condition[1]).(!reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(!condition[0]).(condition[1]).(Carry_flag).(!reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(condition[0]).(!condition[1]).(Z).(!reset) + (opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(!condition[0]).(!condition[1]).(!reset) + (opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(!condition[0]).(condition[1]).(Carry_flag).(!reset) + (opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(condition[0]).(!condition[1]).(Z).(!reset)
S1	S2	(!reset)
S1	rst	(reset)
S2	rst	
S3	S2	(!reset)
S3	rst	(reset)
S4	S5	(!reset)
S4	rst	(reset)

S5	rst	
S6	rst	
S7	S9	(opcode[0]).(!opcode[1]).(opcode[2]).(!opcode[3]).(!reset)
S7	S8	(opcode[0]).(opcode[1]).(opcode[2]).(!opcode[3]).(!reset)
S7	S7	(!opcode[0]).(!reset) + (opcode[0]).(!opcode[2]).(!reset) + (opcode[0]).(opcode[2]).(opcode[3]).(!reset)
S7	rst	(reset)
S8	rst	
S9	rst	
S10	S11	(!reset)
S10	rst	(reset)
S11	S12	(Z).(!reset)
S11	rst	(reset)
S11	S0	(!Z).(!reset)
S12	S13	(!reset)
S12	rst	(reset)
S13	S13	(!opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(!reset) + (!opcode[0]).(!opcode[1]).(opcode[2]).(opcode[3]).(!reset) +

		(!opcode[0]).(opcode[1]).(!reset) + (opcode[0]).(!opcode[2]).(!opcode[3]).(!reset) + (opcode[0]).(opcode[2]).(!reset)
S13	S6	(!opcode[0]).(!opcode[1]).(opcode[2]).(!opcode[3]).(!reset)
S13	rst	(!opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(reset) + (!opcode[0]).(!opcode[1]).(!opcode[2]).(opcode[3]) + (!opcode[0]).(!opcode[1]).(opcode[2]).(reset) + (!opcode[0]).(opcode[1]).(reset) + (opcode[0]).(!opcode[2]).(!opcode[3]).(reset) + (opcode[0]).(!opcode[2]).(opcode[3]) + (opcode[0]).(opcode[2]).(reset)
S14	S16	(!opcode[0]).(opcode[1]).(!opcode[2]).(opcode[3]).(!reset)
S14	S15	(opcode[0]).(!opcode[1]).(!opcode[2]).(opcode[3]).(!reset)
S14	S14	(!opcode[0]).(!opcode[1]).(!reset) + (!opcode[0]).(opcode[1]).(!opcode[2]).(!opcode[3]).(!reset) + (!opcode[0]).(opcode[1]).(opcode[2]).(!reset) + (opcode[0]).(!opcode[1]).(!opcode[2]).(!opcode[3]).(!reset) + (opcode[0]).(!opcode[1]).(opcode[2]).(!reset) + (opcode[0]).(opcode[1]).(!reset)
S14	rst	(reset)
S15	S13	(!reset)
S15	rst	(reset)
S16	rst	
S17	S13	(!reset)
S17	rst	(reset)
S18	S24	(!opcode[0]).(!opcode[1]).(!opcode[2]).(tf).(!reset) + (!opcode[0]).(!opcode[1]).(opcode[2]).(!opcode[3]).(tf).(!reset) + (!opcode[0]).(opcode[1]).(tf).(!reset) + (opcode[0]).(tf).(!reset)

S18	S22	(!tf).(!reset)
S18	S19	(!opcode[0]).(!opcode[1]).(opcode[2]).(opcode[3]).(tf).(!reset)
S18	rst	(reset)
S19	S20	(!reset)
S19	rst	(reset)
S20	S21	(!reset)
S20	rst	(reset)
S21	S22	(!opcode[0]).(!opcode[1]).(!opcode[2]).(!T4_Z).(!reset) + (!opcode[0]).(!opcode[1]).(opcode[2]).(!opcode[3]).(!T4_Z).(!reset) + (!opcode[0]).(!opcode[1]).(opcode[2]).(opcode[3]).(!tf).(!T4_Z).(!reset) + (!opcode[0]).(opcode[1]).(!T4_Z).(!reset) + (opcode[0]).(!T4_Z).(!reset)
S21	S19	(!opcode[0]).(!opcode[1]).(opcode[2]).(opcode[3]).(tf).(!T4_Z).(!reset)
S21	rst	(!T4_Z).(reset) + (T4_Z)
S22	S23	(!reset)
S22	rst	(reset)
S23	S22	(!opcode[0]).(!opcode[1]).(!opcode[2]).(!T4_Z).(!reset) + (!opcode[0]).(!opcode[1]).(opcode[2]).(!opcode[3]).(!T4_Z).(!reset) + (!opcode[0]).(!opcode[1]).(opcode[2]).(opcode[3]).(!tf).(!T4_Z).(!reset) + (!opcode[0]).(opcode[1]).(!T4_Z).(!reset) + (opcode[0]).(!T4_Z).(!reset)
S23	S19	(!opcode[0]).(!opcode[1]).(opcode[2]).(opcode[3]).(tf).(!T4_Z).(!reset)

S23	rst	(!T4_Z).(reset) + (T4_Z)
S24	S20	(!reset)
S24	rst	(reset)

Control Word:

Bit No.		s0	s1	s2	s3	s4	s5	s6	s7	s8	s9	s10	s11	s12	s13	s14	s15	s16	s17	s18	s19	s20	s21	s22	s23	s24
0	m1 sel line	0	0	x	0	1	x	x	1	x	x	0	1	0	x	x	0	x	0	0	x	x	x	x	x	x
1		0	1	x	1	0	x	x	0	x	x	0	0	0	x	x	0	x	1	1	x	x	x	x	x	x
2	m2 sel line	x	0	x	0	x	x	x	x	x	0	x	0	x	x	x	x	0	x	x	x	x	x	x	x	1
3		x	0	x	0	x	x	x	x	x	1	x	1	x	x	x	x	0	x	x	x	x	x	x	x	0
4	m3 sel line	x	1	0	1	1	0	0	1	0	x	x	x	x	1	0	x	1	x	1	1	x	x	x	x	x
5		x	0	1	0	0	0	0	0	0	x	x	x	x	0	0	x	0	x	0	1	x	x	x	x	x
6	m4 sel line	x	0	0	0	0	0	1	0	0	x	x	x	x	0	0	x	1	x	0	0	x	x	x	x	x
7		x	1	1	1	1	1	0	1	0	x	x	x	x	1	1	x	1	x	1	0	x	x	x	x	x
8	RF-D3 read enable	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0
9	alu A - mux A	1	1	x	1	0	x	x	0	x	x	x	1	0	x	x	1	x	1	x	x	0	x	x	x	x
10		0	0	x	0	0	x	x	0	x	x	x	0	0	x	x	1	x	1	x	x	1	x	x	x	x
11	alu A - write enable	1	1	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	0
12	alu B - mux B	0	1	x	1	0	x	x	0	x	x	x	1	0	x	x	0	x	0	x	x	0	x	x	x	x
13		1	0	x	1	0	x	x	0	x	x	x	0	0	x	x	0	x	0	x	x	1	x	x	x	x
14	alu B - write enable	1	1	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	0
15	n1 sel line	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	1	x	1	x	1	x
16	n2 sel line	x	x	x	x	x	x	x	x	0	0	x	x	x	x	x	x	x	x	x	1	x	x	x	x	1
17	n3 sel line	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	x	x	0	x	x	x
18	T write enable	1	1	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	0
19	T2 write enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	0
20	T3 write enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0
21	T4 write enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
22	data memory write enable	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
23	data memory read enable	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
24	Instruction memory read enable	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	IR enable	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	INC to T4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
27	T4 to INC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1
28	Buffer Write Enable	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0