FPGA-Based Digital Compass Using the Nexys A7-100T and Pmod CMP32 Sensor

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Abstract – The purpose of this project is to design and implement a real-time digital compass on the Nexys A7-100T FPGA board. We'll determine and display the precise heading angle in degrees relative to magnetic north using the Pmod CMP32 magnetometer. We'll utilize the I²C communication protocol to process the raw X, Y, and Z-axis magnetic data and compute the correct directional heading. The result will be the angle in degrees delivered to the board's seven segment display for real-time feedback. This project demonstrates the use of digital logic design principles to create a hardware-based embedded system for sensor integration and real-time computation.

I. INTRODUCTION

This digital compass project applies the principles of combinational and sequential circuit design to create a fully functional hardware-based navigation system. The FPGA will acquire magnetic field data from the sensor, process it through custom logic to compute the real-time heading angle relative to magnetic north, and display the result on the board's seven-segment display. By integrating sensor interfacing, data processing, and real-time visualization, this project demonstrates how foundational digital logic concepts can be combined to implement a practical and sophisticated embedded system.

II. BACKGROUND & PRELIMINARIES

The concept of a digital compass relies on measuring the Earth's magnetic field to determine orientation relative to magnetic north. Modern electronic compasses typically rely on magnetometer sensors that output analog or digital readings corresponding to the magnetic field's strength along the X, Y, and Z axes. By processing these readings, the heading angle can be calculated using trigonometric relationships. The Pmod CMP32 magnetometer is a 3-axis magnetometer based on the LSM303DLHC chip, which communicates with external devices via the I^2C serial interface. This allows for precise and easily accessible magnetic field data.

In this project, the Nexys A7-100T FPGA serves as the central processing platform for real-time computation and display. Unlike microcontrollers, FPGA's allow for parallel digital logic design, making them ideal for custom hardware modules that handle sensor communication, signal processing, and display control simultaneously. Implementing the I^2C protocol in Verilog will enable direct communication between the FPGA board and the Pmod CMP32 sensor, while the computed angle will be displayed using the board's seven-segment display interface. An additional SPI driver will interface with the accelerometer for tilt measurement and compensation.

To achieve accurate directional readings regardless of device orientation, a tilt compensation circuit will process data from both the magnetometer and accelerometer to correct for roll and pitch angles. The heading calculation circuit will then use the compensated magnetic field data to compute the true heading relative to magnetic north. Finally, the seven-segment display driver (which will require a time-multiplexing scheme due to shared segment lines) will present the calculated heading angle in real time. Together, these modules form a complete FPGA-based embedded system capable of sensor integration, tilt correction, real-time angle computation, and visual output.

Currently, the obstacles we are encountering involve understanding how the I2C master will be programmed to effectively communicate with the CMP32 and the FPGA board. Additionally, we are struggling to decide what computational approach we will proceed with to compute the raw X/Y/Z data into a directional heading. Lastly, we are also doing more research into how to incorporate our

tilt compensation circuit to work in tandem with our on-board accelerometer as it communicates with the FPGA via SPI.

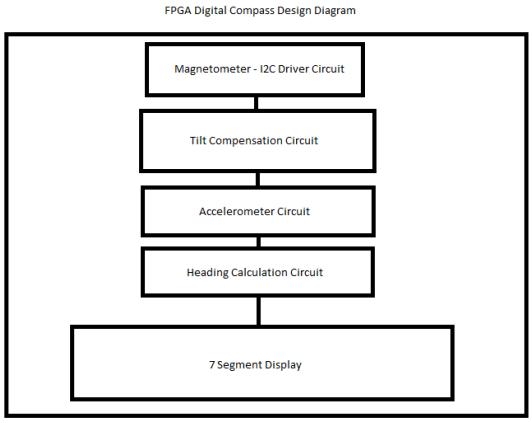

Figure 1: Rough Design Diagram of Digital Compass

III. IMPLEMENTATION

The bcd_to_7seg module is responsible for converting a 4-bit binary-coded decimal (BCD) input into the corresponding seven-segment display pattern. Each BCD input value, ranging from 0 to 9, is mapped to a unique 7-bit output pattern that determines which segments of the display should be illuminated to form the correct decimal digit. The output follows the common-cathode configuration, where a logic '0' turns on a segment and a logic '1' turns it off. This mapping is implemented through a combinational case statement inside an always block that is sensitive to any change in the BCD input. If the input value falls outside the valid BCD range, the module outputs 7'b1111111, which turns off all segments. This module plays a key role in the display system by enabling numerical data (such as the computed heading angle) to be accurately visualized on the FPGA's seven-segment display.

The binary_to_bcd module converts a 10-bit binary number into its equivalent decimal representation using three separate 4-bit outputs for the hundredths, tenths, and ones digits. Since the input range is limited to 0–511 (the maximum value representable by 9 bits), each of the output digits is computed through basic arithmetic operations: integer division and modulus. Specifically, the hundredths digit is obtained by dividing the binary input by 100, the tenth digit is derived from the remainder after removing the hundreds place, and the ones digit represents the final remainder. To ensure safe operation, a conditional check limits the maximum displayable value to 511; if the input exceeds this range, the outputs default to "511." This module serves as an intermediate stage between the computed heading angle and the display system, formatting binary angle data into readable decimal digits that can be properly decoded by the bcd_to_7seg module and shown on the seven-segment display.

The top module serves as the main control unit that integrates all functional components required to display numerical data on the Nexys A7's seven-segment display. The module accepts a 9-bit binary input from the board's switches, representing values from 0 to 511, and uses the binary_to_bcd converter to separate this value into individual hundredths, tenths, and ones digits. Each of these digits is then passed through an instance of the bcd_to_7seg decoder, which generates the corresponding segment pattern for display. To manage the multiple seven-segment displays with limited I/O pins, the design employs a time-multiplexing technique using a 20-bit refresh counter. This counter cycles rapidly through the active digits, updating one display at a time while keeping the others off. Because this switching occurs faster than the human eye can perceive, the digits appear continuously illuminated. The result is a stable three-digit display that accurately shows the binary switch input as a readable decimal number, demonstrating real-time conversion, decoding, and multiplexed display control entirely in hardware.

The top_tb module functions as a testbench designed to verify the correct operation of the binary_to_bcd converter. It simulates the behavior of the FPGA in a controlled environment, allowing for step-by-step observation of the output values without requiring physical hardware. Within the testbench, a 9-bit input signal named switches represents the binary values that would normally come from the FPGA's physical switches. These inputs are sequentially assigned different test cases ranging from 0 to 359 to ensure accurate binary-to-decimal conversion across the expected range. The resulting BCD outputs (hundredths, tenths, and ones) can then be monitored to confirm proper functionality. Although a clock signal is generated to mimic FPGA timing, it primarily serves as a placeholder for future integration with time-dependent logic. The inclusion of a reset signal ensures consistent initialization before testing begins.

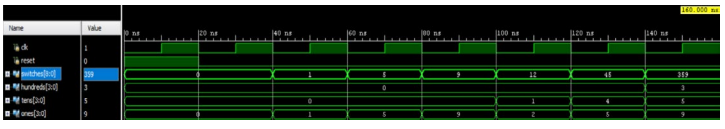

Figure 2: 7 Segment Decoder Simulation

IV. TEAM CONTRIBUTION

The project distribution percentage at this first checkpoint can be described as follows: 40% Nathan Sarkozy, 30% Christian Vanegas, 30% Kaiya Hayashida.

- Nathan Sarkozy contributed by completing the foundation of the digital compass: the seven segment decoder. With the inclusion of a binary_to_bcd and bcd_to_7seg conversion modules, the top module completes this foundational circuit and creates a functional 7 segment display.

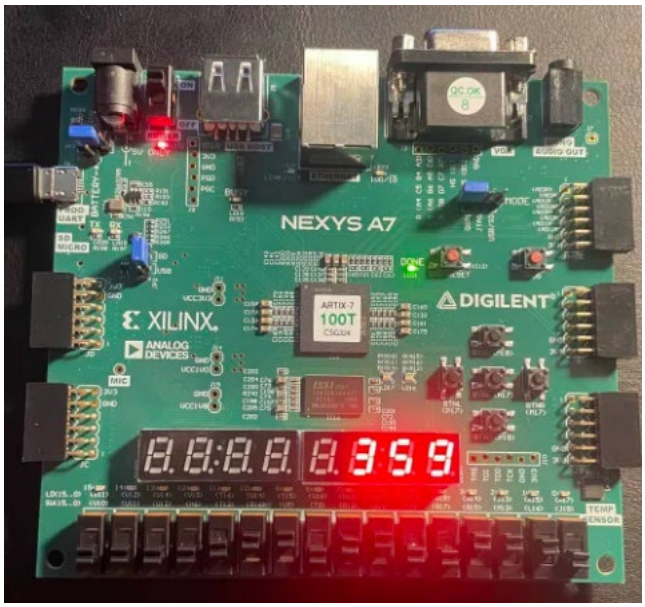

Figure 3: 7 Segment Display Output Test

- Christian Vanegas contributed by purchasing the Pmod CMP32 magnetometer and conducting extensive research into how the I2C protocol will be used have communication between the FPGA and the sensor. He also contributed with a portion of the progress report's completion.

- Kaiya Hayashida contributed by completing majority of the first progress report and also conducting research about how the SPI protocol will help with onboard communication of the FPGA and accelerometer.