BOE

浙江京东方显示技术股份有限公司
ZHEJIANG BOE DISPLAY TECHNOLOGY CO.,LTD
地址：浙江省绍兴市舜江路698号
Add: 698# Shunjiang Road,Shaoxing,zhejiang, 312000
TEL: 0086-0575-88646699 0086-0575-88650406
FAX: 0086-0575-88650409

荧光显示屏产品规格书
SPECIFICATION OF VACUUM FLUORESCENT DISPLAY

	Date	Description
1	2009.03.11	ORIGINAL
2	2009.03.12	管脚长度由5.5mm 改成 11.0mm

Customer's Approval

control No.	QG/ZBOE-VFD 030.07.3-05
Spec. No.	CIG25-1605N
MODEL	CIG25-1605N

用途 Application	AV
显示颜色 Color Of Illumination	绿色 Green X=0.250 Y=0.440

概要 Features
16Grid X 70 Anode 1 Colors Cadmium Free Phosphor Lead Free solder

外形尺寸 Outer Dimensions	长 Panel Length	$87.5^{+0.8}_{-0.5}$	mm
	宽 Panel Height	$25.0^{+0.7}_{-0.5}$	mm
	厚 Panel Thickness	6.1 ± 0.5	mm
引出端子 Lead	端子间距 Lead Pitch	2.0	mm
	端子引出形式 Lead Out	单列折弯	

极限工作条件 Absolute Maximum Condition

项目 Item	符号Symbol	引出端子符号Terminals	变动范围 Ratings	单位Unit
灯丝电压 Filament Voltage	Ef	F1,F2	2.48~3.72	Vac
逻辑供给电压 Logic Supply Voltage	V_{DD}	V_{DD}	−0.3~+6.0	Vdc
驱动供给电压 Driver Supply Voltage	V_{DISP}	V_{DISP}	−0.3~48	Vdc
逻辑输入电压 Logic Input Voltage	V_{IN}	CS,CP,DA,RESET	−0.3~V_{DD}+0.3	Vdc
使用温度 Operating Temperature	Top	————	−20 ~ +70	℃
储存温度 Storage Temperature	Tstg	————	−40 ~ +80	℃

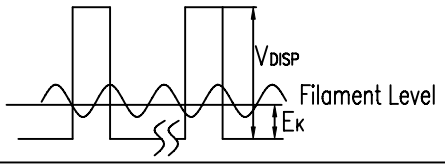
推荐工作条件 Recommended Operating Condition

项 目 Item	符 号 Symbol	条件 Condition	最小值 Min	推荐值 TYP.	最大值 Max	单位 Unit
灯丝电压 Filament Voltage	Ef	————	2.79	3.1	3.41	Vac
截止电压 Cut−off Voltage	Ek	————	5.0	——	6.0	Vdc
逻辑供给电压 Logic Supply Voltage	V_{DD}	————	3.0	3.3	3.6	Vdc
驱动供给电压 Driver Supply Voltage	V_{DISP}	————	34.0	37.0	40.0	Vdc
逻辑高电平输入 Hi−level Logic Input	V_{IH}	CS,CP,DA,RESET	$V_{DD}\times0.8$	——	——	Vdc
逻辑低电平输入 Lo−level Logic Input	V_{IL}	CS,CP,DA,RESET	——	——	$V_{DD}\times0.2$	Vdc
时钟频率 CP Frequency	fc	————	——	——	2.0	MHz
振荡器频率 Oscillation Frequency	fosc	R = 6.2 kΩ, C =39pF	3.0	4.0	5.0	MHz
扫描频率 Frame Frequency	f_{FR}	DIGIT = 1 to 20, oscillation	146	195	215	Hz
交流特性 AC Characteristics		见时序图 See Timing Chart				

control No.	QG/ZBOE−VFD 030.07.3−05
Spec. No.	SPC09.03.06−02
MODEL	CIG25−1605N

电气特性 Electrical Chardcteristics

BOE

项 目 Item	符 号 Symbol	测试条件 Test Condition			最小值 Min	典型值 Typical	最大值 Max	单位 Unit
灯丝电流 Filament Current	If	Ef=3.1 Vac			162.0	180.0	198.0	mAac
逻辑供给电流 Logic Supply Current	I_{DO1}	V_{DD}	V_{DD} =3.3V, fosc=4.0MHZ		—	—	4	mA
驱动供给电流(1) Current consumption(1)	$I_{DISP1(AVG)}$	V_{DISP}	fosc= 4 MHz	All output lights ON Typ:Tj=25℃ Max:Tj=85℃	—	8.0	16.0	mA
	$I_{DISP1(PEAK)}$				—	8.0	16.0	mA
	I_{DISP2}			All output lights OFF Typ:Tj=25℃ Max:Tj=85℃	—	1.0	15.0	μA
驱动供给电流(2) Current consumption(2)	I_{DD}	V_{DD}	Stand-by mode Typ:Tj=25℃ Max:Tj=85℃		—	1.0	1.0	μA
	I_{DISP}	V_{DISP}			—	1.0	10.0	μA
高电平输入电流 Hi-level Input Current	I_{IH}	$V_{IN}=V_{DD}$	CS,CP,DA RESET		-1.0	—	1.0	μA
低电平输入电流 Lo-level Input Current	I_{IL}	V_{IN}=0 V	CS,CP,DA RESET		-1.0	—	1.0	μA
亮度 Luminance	L(G)	Ef=3.1Vac V_{DISP}=37.0 Vdc Ek=5. 0Vdc Duty=960/1024			350 (102)	700 (204)	—	cd/m² (fl)
	—				—	—	—	cd/m² (fl)
	—				—	—	—	cd/m² (fl)
位间亮度比 Luminance Ratio	Lmin/Lmax				50	—	—	%

功能表 Function Table

功 能 Function	符 号 Symbol	输入/输出 Input/Output	描 述 Description
移位寄存器时钟信号 Shift clock input	CP	Input	Serial data is shifted on the rising edge of CP
串行数据输入 Serial Data Input	DA	Input	Serial data input (positive logic).Input from LSB
片选信号 Chip select input	CS	Input	Serial data transfer is disabled when CS pin is "H" level
复位输入 Reset Input	RESET	Input	"Low" initializes all the functions
驱动供给电源 Power Supply To VFD	V_{DISP}	—	Power Supply Pin for Drive Circuit
逻辑供给电源 Power Supply To Logic	V_{DD}	—	Power Supply Pin for Logic Circuit
电源地 Ground	L_{GND},D_{GND}	—	Ground of Circuit
振荡器输入端 oscillator input	OSC	I/O	External RC pin for RC oscillation
数据输出 Data output	DO	output	Factory test pin, leave it open
测试端 Test mode control pin	TEST	Input	Factory test pin, leave it open

注：驱动方式 动态
Drive mode:Dynamic state

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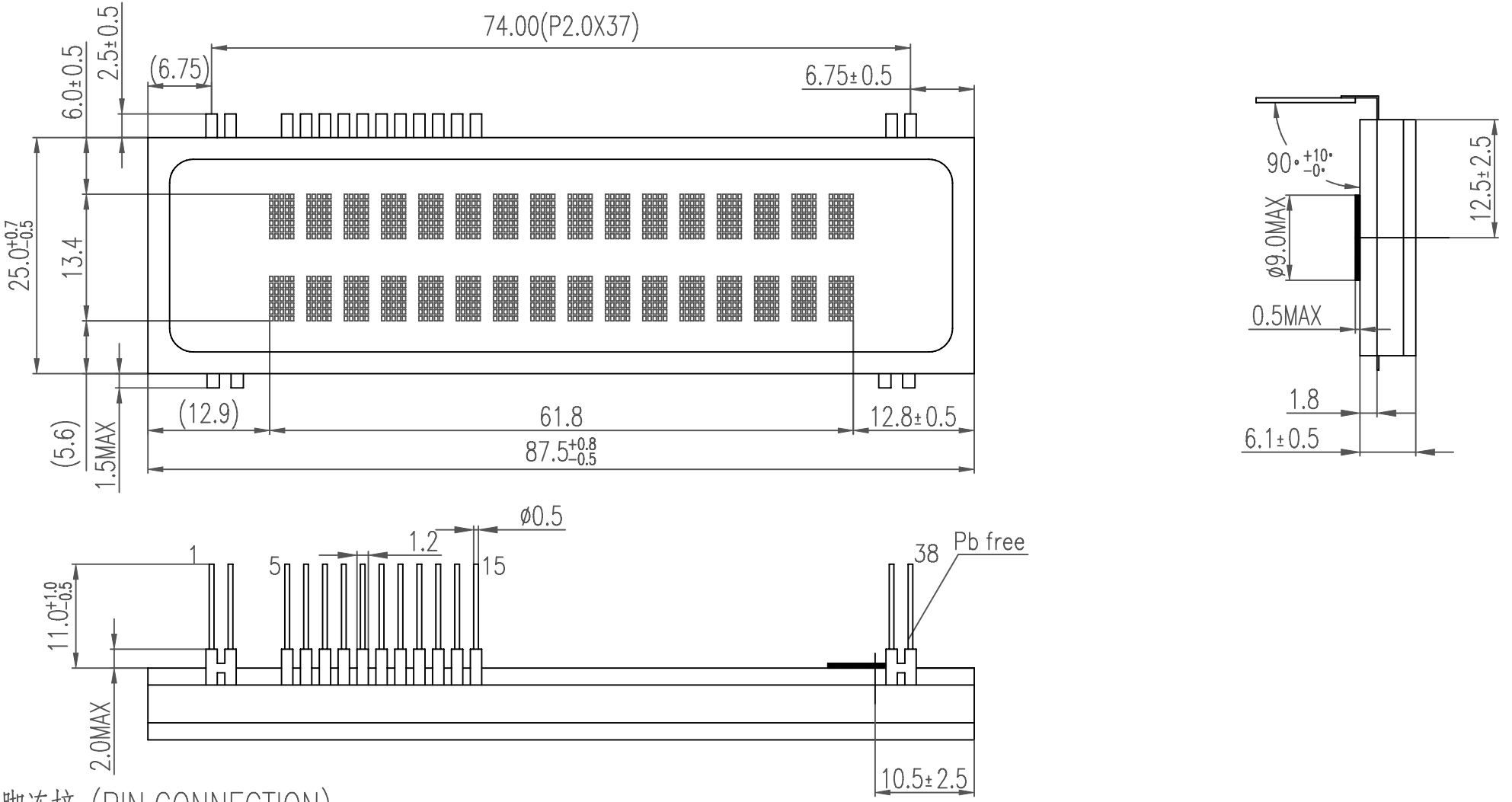
附图1：外形图 Outline Drawing (Unit:mm)



管脚连接 (PIN CONNECTION)

端子序号 (PIN NO.)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16~36	37	38
连接 (CONNECTION)	F1	F1	NP	NP	LGND	DGND	VDISP	VDD	OSC	RESET	CS	CP	DA	DO	TEST	NP	F2	F2

注：F: 灯丝 (Filament) NP: 无引出脚 (No pin)

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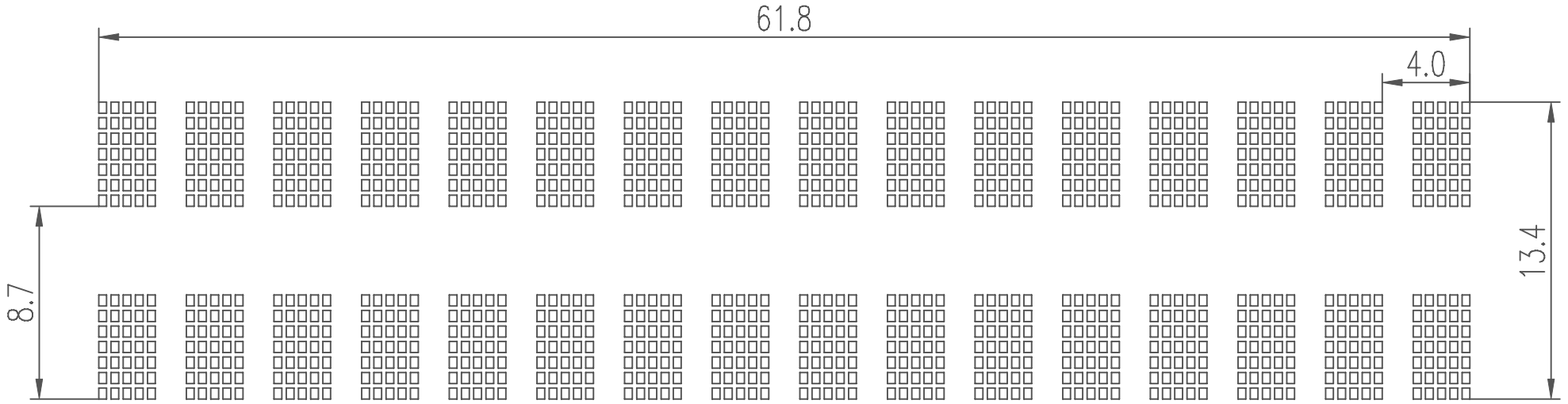
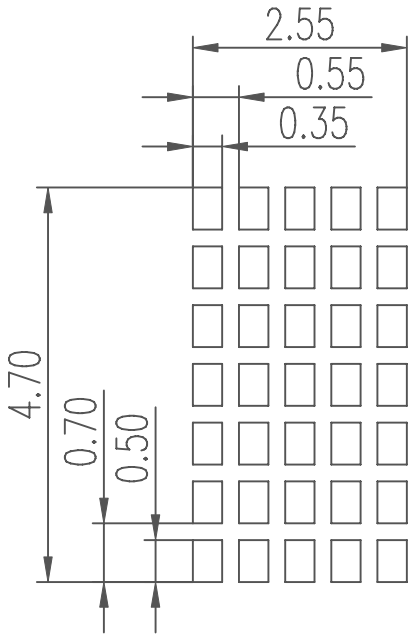
附图2：显示内容 Display Pattern(Unit:mm)





显示颜色 Color of Illumination:

绿色 Green: x=0.250, y=0.440 全部 ALL

Cadmium Free Phosphor used

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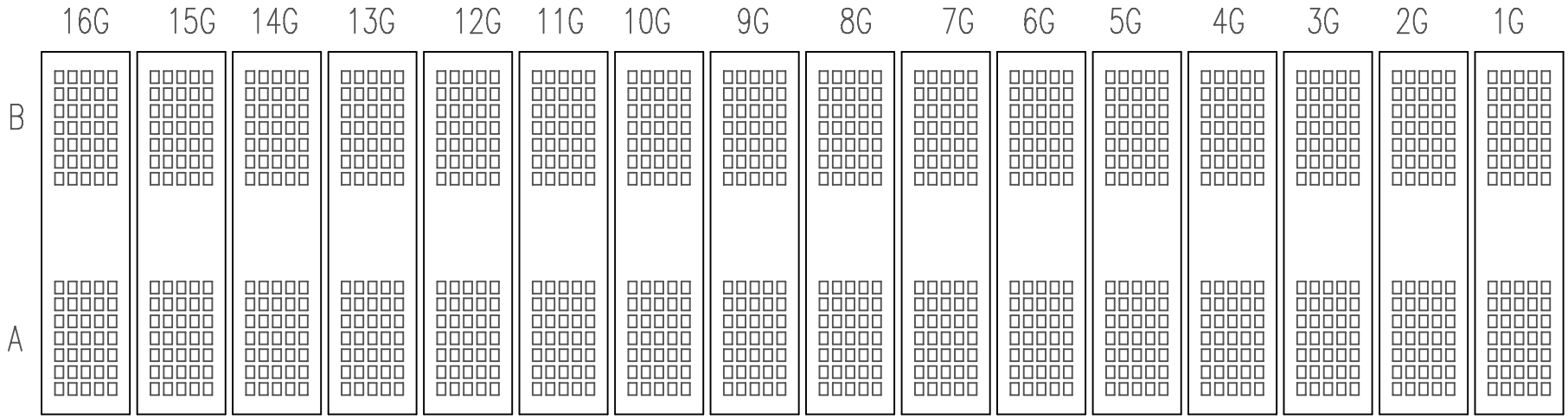
附图3：栅网分割 Grid Assignment



B1	B2	B3	B4	B5	A1	A2	A3	A4	A5
B6	B7	B8	B9	B10	A6	A7	A8	A9	A10
B11	B12	B13	B14	B15	A11	A12	A13	A14	A15
B16	B17	B18	B19	B20	A16	A17	A18	A19	A20
B21	B22	B23	B24	B25	A21	A22	A23	A24	A25
B26	B27	B28	B29	B30	A26	A27	A28	A29	A30
B31	B32	B33	B34	B35	A31	A32	A33	A34	A35
Row B					Row A				

(16G~1G)

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MODEL	CIG25-1605N

	16G~1G			16G~1G			
SEGA1	A1		SEGB1	B1		COM1	1G
SEGA2	A2		SEGB2	B2		COM2	2G
SEGA3	A3		SEGB3	B3		COM3	3G
SEGA4	A4		SEGB4	B4		COM4	4G
SEGA5	A5		SEGB5	B5		COM5	5G
SEGA6	A6		SEGB6	B6		COM6	6G
SEGA7	A7		SEGB7	B7		COM7	7G
SEGA8	A8		SEGB8	B8		COM8	8G
SEGA9	A9		SEGB9	B9		COM9	9G
SEGA10	A10		SEGB10	B10		COM10	10G
SEGA11	A11		SEGB11	B11		COM11	11G
SEGA12	A12		SEGB12	B12		COM12	12G
SEGA13	A13		SEGB13	B13		COM13	13G
SEGA14	A14		SEGB14	B14		COM14	14G
SEGA15	A15		SEGB15	B15		COM15	15G
SEGA16	A16		SEGB16	B16		COM16	16G
SEGA17	A17		SEGB17	B17		COM17	——
SEGA18	A18		SEGB18	B18		COM18	——
SEGA19	A19		SEGB19	B19		COM19	——
SEGA20	A20		SEGB20	B20		COM20	——
SEGA21	A21		SEGB21	B21		——	——
SEGA22	A22		SEGB22	B22		——	——
SEGA23	A23		SEGB23	B23		——	——
SEGA24	A24		SEGB24	B24		——	——
SEGA25	A25		SEGB25	B25		——	——
SEGA26	A26		SEGB26	B26		——	——
SEGA27	A27		SEGB27	B27		——	——
SEGA28	A28		SEGB28	B28		——	——
SEGA29	A29		SEGB29	B29		——	——
SEGA30	A30		SEGB30	B30		——	——
SEGA31	A31		SEGB31	B31		——	——
SEGA32	A32		SEGB32	B32		——	——
SEGA33	A33		SEGB33	B33		——	——
SEGA34	A34		SEGB34	B34		——	——
SEGA35	A35		SEGB35	B35		——	——

FUNCTION DESCRIPTION

COMMAND LIST

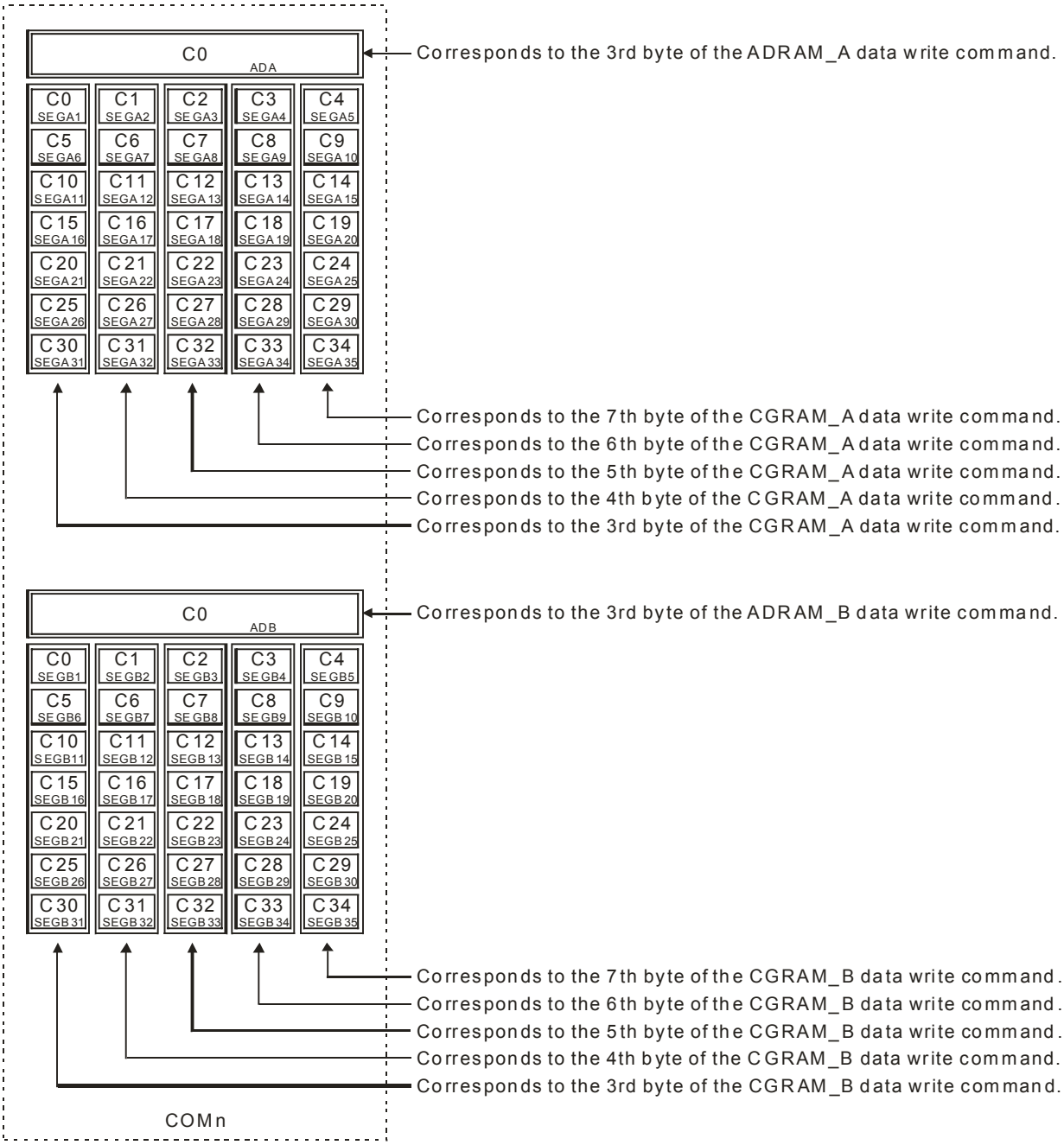
No	COMMAND	1st Byte								2nd Byte								3rd Byte								
		B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0	
1	DCRAM_A Data Write	0	0	0	1	*	*	*	*	0	0	0	X4	X3	X2	X1	X0	C7	C6	C5	C4	C3	C2	C1	C0	
2	CGRAM_A Data Write	0	0	1	0	*	*	*	*	0	0	0	0	X3	X2	X1	X0	*	C30	C25	C20	C15	C10	C5	C0	3rd byte
																		*	C31	C26	C21	C16	C11	C6	C1	4th byte
																		*	C32	C27	C22	C17	C12	C7	C2	5th byte
																		*	C33	C28	C23	C18	C13	C8	C3	6th byte
																		*	C34	C29	C24	C19	C14	C9	C4	7th byte
3	ADRAM_A Data Write	0	0	1	1	*	*	*	*	0	0	0	X4	X3	X2	X1	X0	*	*	*	*	*	*	*	C0	
5	Dsiplay Duty Set	0	1	0	1	*	*	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2									
6	Number of digits set	0	1	1	0	K3	K2	K1	K0																	
7	All lights on/off	0	1	1	1	*	*	H	L																	
8	Test Mode	1	0	0	0	T3	T2	T1	T0																	
9	DCRAM_B Data Write	1	0	0	1	*	*	*	*	0	0	0	X4	X3	X2	X1	X0	C7	C6	C5	C4	C3	C2	C1	C0	
A	CGRAM_B Data Write	1	0	1	0	*	*	*	*	0	0	0	0	X3	X2	X1	X0	*	C30	C25	C20	C15	C10	C5	C0	3rd byte
																		*	C31	C26	C21	C16	C11	C6	C1	4th byte
																		*	C32	C27	C22	C17	C12	C7	C2	5th byte
																		*	C33	C28	C23	C18	C13	C8	C3	6th byte
																		*	C34	C29	C24	C19	C14	C9	C4	7th byte
B	ADRAM_B Data Write	1	0	1	1	*	*	*	*	0	0	0	X4	X3	X2	X1	X0	*	*	*	*	*	*	*	C0	
F	Standby mode	1	1	1	1	*	*	*	*																	

*: Don't care
Xn: Address specification for each RAM
Cn: Character code specification for each RAM
Dn: Display duty specification
Kn: Number of digits specification
Tn: Test mode specification
H: All lights ON instruction
L: All lights OFF instruction

When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

Note:
The test mode is used for inspection before shipment.
It is not a user function. The user cannot use this command. Enter commands 1 to 3, 5 to 7, 9 to B, and F alone in the way described on the next page and the following pages. (The operation of this device cannot be guaranteed if other commands are used.)

POSITIONAL RELATIONSHIP BETWEEN SEGn AND ADn (one digit)

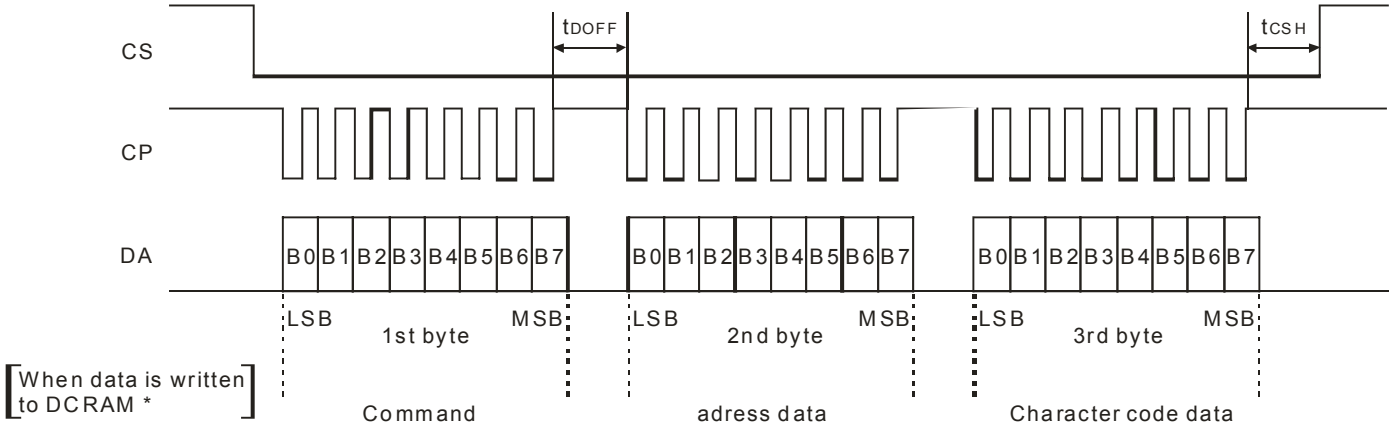


DATA TRANSFER METHOD AND COMMAND WRITE METHOD

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the CS pin to “Low” level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the CP pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the CS pin to “High” disables data transfer. Data input from the point when the CS pin changes from “High” to “Low” is recognized in 8-bit units.



Note:
When data is written to RAM (DCRAM, ADRAM, CGRAM) continuously, addresses are internally incremented automatically.
Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and later bytes.

RESET FUNCTION
Reset is executed when the RESET pin is set to “L”, (when turning power on, for example) and initializes all functions.
Initial status is as follows.

Address of each RAM.....address “00”H
Data of each RAM.....All contents are undefined
Display digit .....20 digits
Brightness adjustment 0/1024
All display lights ON or OFF.....OFF mode
Segment output.....All segment outputs go “Low”
AD output.....All AD outputs go “Low”

Be sure to execute the reset operation when turning power on and set again according to “Setting Flowchart” after reset.

DESCRIPTION OF COMMANDS AND FUNCTIONS

1 AND 9. DCRAM DATA WRITE

(Write the character code of CGROM and CGRAM to DCRAM)

DCRAM (Data Control RAM) has 20 address x 8-bit RAM to store character code of CGROM and CGRAM. Address 00H(0) to 13H(19) corresponds to COM1 to 20. The character code stored in DCRAM is CONVERTED TO A 5 x 7 dot matrix character pattern via CGROM or CGRAM.
The DCRAM can store 20 characters.

Command Format

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Select DCRAM data write mode
	0/1	0	0	1	*	*	*	*	

Note: 0: Select DCRAM_A, 1: Select DCRAM_B

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Specific DCRAM address (EX, Specific DCRAM address 00H)
	0	0	0	X4	X3	X2	X1	X0	

To specify the character code of CGROM and CGRAM continuously to the next address, specify only character code as follows. The address of DCRAM is automatically incremented.

	MSB							LSB	
3rd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 00H)
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
3rd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 01H)
	C7	C6	C5	C4	C3	C2	C1	C0	

. . .

	MSB							LSB	
3rd Byte (22th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 13H)
	C7	C6	C5	C4	C3	C2	C1	C0	

	MSB							LSB	
3rd Byte (23th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies character code of CGRAM and CGROM (written into DCRAM address 00H)
	C7	C6	C5	C4	C3	C2	C1	C0	

C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits 256 characters)
*: Don't care.

COM Positions and DCRAM Addresses

DCRAM address									COM	DCRAM address									COM
HEX	0	0	0	X_4	X_3	X_2	X_1	X_0	**position**	**HEX**	0	0	0	X_4	X_3	X_2	X_1	X_0	**position**
00H	0	0	0	0	0	0	0	0	COM1	0AH	0	0	0	0	1	0	1	0	COM11
01H	0	0	0	0	0	0	0	1	COM2	0BH	0	0	0	0	1	0	1	1	COM12
02H	0	0	0	0	0	0	1	0	COM3	0CH	0	0	0	0	1	1	0	0	COM13
03H	0	0	0	0	0	0	1	1	COM4	0DH	0	0	0	0	1	1	0	1	COM14
04H	0	0	0	0	0	1	0	0	COM5	0EH	0	0	0	0	1	1	1	0	COM15
05H	0	0	0	0	0	1	0	1	COM6	0FH	0	0	0	0	1	1	1	1	COM16
06H	0	0	0	0	0	1	1	0	COM7	10H	0	0	0	1	0	0	0	0	COM17
07H	0	0	0	0	0	1	1	1	COM8	11H	0	0	0	1	0	0	0	1	COM18
08H	0	0	0	0	1	0	0	0	COM9	12H	0	0	0	1	0	0	1	0	COM19
09H	0	0	0	0	1	0	0	1	COM10	13H	0	0	0	1	0	0	1	1	COM20

2 AND A. CGRAM DATA WRITE

(Specifies the addresses of CGRAM and write character pattern data)

CGRAM (Character Generator RAM) has 16 address x 35-bit RAM to store 5 x 7 dot matrix character patterns. A character pattern stored in CGRAM can be displayed by specifying the character code in a DCRAM. The address of CGRAM is assigned to 00H to 0FH. (All other addresses are CGROM addresses.) CGRAM can store 16 types of character patterns.

Command Format

1st Byte (1st) — Select CGRAM data write mode

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0/1	0	1	0	*	*	*	*

Note: 0: Select CGRAM_A, 1: Select CGRAM_B

2nd Byte (2nd) — Specific CGRAM address (Ex. Specific CGRAM address 00H)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	X3	X2	X1	X0

3rd Byte (3rd) — Specifies 1st column data (written into CGRAM address 00H)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C30	C25	C20	C15	C10	C5	C0

4th Byte (4th) — Specifies 2nd column data (written into CGRAM address 00H)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C31	C26	C21	C16	C11	C6	C1

5th Byte (5th) — Specifies 3rd column data (written into CGRAM address 00H)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C32	C27	C22	C17	C12	C7	C2

6th Byte (6th) — Specifies 4th column data (written into CGRAM address 00H)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C33	C28	C23	C18	C13	C8	C3

7th Byte (7th) — Specifies 5th column data (written into CGRAM address 00H)

MSB							LSB
B7	B6	B5	B4	B3	B2	B1	B0
*	C34	C29	C24	C19	C14	C9	C4

To specify the character pattern data continuously to the next address, specify only character pattern data as follows. The address of CGRAM is automatically incremented. Specification of an address is unnecessary.
The 3rd to 7th byte (character pattern data) are regarded as one data item, so 200ns is sufficient for t_{DOFF} time between bytes.

	MSB							LSB	
3rd Byte (8th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies 1st column data (written into CGRAM address 01H)
	*	C30	C25	C20	C15	C10	C5	C0	

	MSB							LSB	
7th Byte (12th)	B7	B6	B5	B4	B3	B2	B1	B0	Specifies 5th column data (written into CGRAM address 01H)
	*	C34	C29	C24	C19	C14	C9	C4	

X0 (LSB) to X3 (MSB): CGRAM address (4 bits 16 characters)
C0 (LSB) to C34 (MSB): Character pattern data (35 bits: 35 outputs per character)
*: Don't care.

CGRAM addresses and corresponding CGROM address

HEX	X3	X2	X1	X0	CGROM address
0	0	0	0	0	RAM00 (00000000B)
1	0	0	0	1	RAM01 (00000001B)
2	0	0	1	0	RAM02 (00000010B)
3	0	0	1	1	RAM03 (00000011B)
4	0	1	0	0	RAM04 (00000100B)
5	0	1	0	1	RAM05 (00000101B)
6	0	1	1	0	RAM06 (00000110B)
7	0	1	1	1	RAM07 (00000111B)
8	1	0	0	0	RAM08 (00001000B)
9	1	0	0	1	RAM09 (00001001B)
A	1	0	1	0	RAM0A (00001010B)
B	1	0	1	1	RAM0B (00001011B)
C	1	1	0	0	RAM0C (00001100B)
D	1	1	0	1	RAM0D (00001101B)
E	1	1	1	0	RAM0E (00001110B)
F	1	1	1	1	RAM0F (00001111B)

Note: Refer to ROM code tables

3 AND B. ADRAM DATA WRITE

(Writes symbol data)

ADRAM (Additional Data RAM) has 20 address x 1-bit RAM to store symbol data. Address 00H(0) to 13H(19) corresponds to COM1 to 20. Symbol data stored in ADRAM is directly output without translation of CGROM and CGRAM. The ADRAM can store 1 type of symbol patterns per each digit. The terminal to which the contents of ADRAM are output can be used as a cursor.

Command Format

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Select ADRAM data write mode
	0/1	0	1	1	*	*	*	*	

Note: 0: Select ADRAM_A, 1: Select ADRAM_B

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Specific ADRAM address (EX, Specific ADRAM address 00H)
	0	0	0	X4	X3	X2	X1	X0	

To specify symbol data continuously to the next address, specify only symbol data as follows. The address of ADRAM is automatically incremented.

	MSB							LSB	
3rd Byte (3rd)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (written into ADRAM address 00H)
	*	*	*	*	*	*	*	C0	

	MSB							LSB	
3rd Byte (4th)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (written into ADRAM address 01H)
	*	*	*	*	*	*	*	C0	

.
.
.

	MSB							LSB	
3rd Byte (22th)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (written into ADRAM address 13H)
	*	*	*	*	*	*	*	C0	

	MSB							LSB	
3rd Byte (23th)	B7	B6	B5	B4	B3	B2	B1	B0	Sets symbol data (re-written into ADRAM address 00H)
	*	*	*	*	*	*	*	C0	

C0: Symbol data (1 bit: 1-symbol data per digit)

*: Don’t care.

COM Positions and ADRAM Addresses

ADRAM address									COM	ADRAM address									COM
HEX	0	0	0	X_4	X_3	X_2	X_1	X_0	**position**	**HEX**	0	0	0	X_4	X_3	X_2	X_1	X_0	**position**
00H	0	0	0	0	0	0	0	0	COM1	0AH	0	0	0	0	1	0	1	0	COM11
01H	0	0	0	0	0	0	0	1	COM2	0BH	0	0	0	0	1	0	1	1	COM12
02H	0	0	0	0	0	0	1	0	COM3	0CH	0	0	0	0	1	1	0	0	COM13
03H	0	0	0	0	0	0	1	1	COM4	0DH	0	0	0	0	1	1	0	1	COM14
04H	0	0	0	0	0	1	0	0	COM5	0EH	0	0	0	0	1	1	1	0	COM15
05H	0	0	0	0	0	1	0	1	COM6	0FH	0	0	0	0	1	1	1	1	COM16
06H	0	0	0	0	0	1	1	0	COM7	10H	0	0	0	1	0	0	0	0	COM17
07H	0	0	0	0	0	1	1	1	COM8	11H	0	0	0	1	0	0	0	1	COM18
08H	0	0	0	0	1	0	0	0	COM9	12H	0	0	0	1	0	0	1	0	COM19
09H	0	0	0	0	1	0	0	1	COM10	13H	0	0	0	1	0	0	1	1	COM20

5. DISPLAY DUTY SET

(Writes display duty value to duty cycle register)

Display duty adjusts brightness in 1024 stages using 10-bit data.

When power is turned on or when the RESET signal is input, the duty cycle register value is “0”. Always execute this instruction before turning the display on, then set a desired duty value.

Command Format

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Select display duty set mode and set duty value (lower 2 bits)
	0	1	0	1	*	*	D1	D0	

	MSB							LSB	
2nd Byte (2nd)	B7	B6	B5	B4	B3	B2	B1	B0	Sets duty value (upper 8 bits)
	D9	D8	D7	D6	D5	D4	D3	D2	

D0 (LSB) to D9 (MSB): Display duty data (10 bits: 1024 stages)

*: Don’t care

Relation Between Setup Data and Controlled COM Duty

HEX	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	COM duty
000	0	0	0	0	0	0	0	0	0	0	0/1024
001	0	0	0	0	0	0	0	0	0	1	1/1024
002	0	0	0	0	0	0	0	0	1	0	2/1024
:											:
3BE	1	1	1	0	1	1	1	1	1	0	958/1024
3BF	1	1	1	0	1	1	1	1	1	1	959/1024
3C0	1	1	1	1	0	0	0	0	0	0	960/1024
3C1	1	1	1	1	0	0	0	0	0	1	960/1024
:											:
3FF	1	1	1	1	1	1	1	1	1	1	960/1024

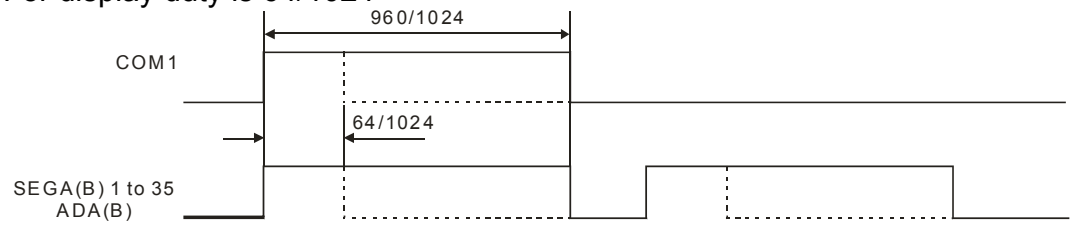
*****The state when power is turned on or when RESET signal is input.

Display Duty Output Timing

Exsample: COM1

Solid line: For display duty is 960/1024

Doted line: For display duty is 64/1024



6. NUMBER OF DIGIT SET

(Writes the number of display digit to the display digit register)

This command can set the number of display digit between 5 to 20 digits using 4-bit data. When power is tuned on or when a RESET signal is input, the number of digit register value is “0”. Always execute this instruction to change the number of digit before turning the display on.

Command Format

	MSB							LSB
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0
	0	1	1	0	K3	K2	K1	K0

Select the number of digit set mode and specifies the number of digit value

K0 (LSB) to K3 (MSB): the Number of digit data (4 bits: 5 to 20 digits)
*: Don’t care.

Relation Between Setup Data and Controlled COM

HEX	K0	K1	K2	K3	The number of digit of COM	HEX	K0	K1	K2	K3	The number of digit of COM
0	0	0	0	0	COM1 to 20	8	0	0	0	1	COM1 to 12
1	1	0	0	0	COM1 to 5	9	1	0	0	1	COM1 to 13
2	0	1	0	0	COM1 to 6	A	0	1	0	1	COM1 to 14
3	1	1	0	0	COM1 to 7	B	1	1	0	1	COM1 to 15
4	0	0	1	0	COM1 to 8	C	0	0	1	1	COM1 to 16
5	1	0	1	0	COM1 to 9	D	1	0	1	1	COM1 to 17
6	0	1	1	0	COM1 to 10	E	0	1	1	1	COM1 to 18
7	1	1	1	0	COM1 to 11	F	1	1	1	1	COM1 to 19

*****The state when power is turned on or when RESET signal is input.

7. ALL DISPLAY LIGHTS ON/OFF SET

(Turns all display lights ON or OFF)

All display lights ON mode is used primarily for display resting.
(The display duty during ON mode is the value of the duty cycle register.)

All display lights OFF mode is primarily used for display blink and to prevent malfunction when power is turned on.
(All the segment output are “Low”, but COM outputs are still driving.)

Command Format

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects all display lights ON or OFF mode
	0	1	1	1	*	*	H	L	

H, L: Display operation data
*: Don’t care.

Set Data and Display State of SEG and AD

L	H	Display state of SEG and AD
0	0	Normal display
1	0	Sets all outputs to Low
0	1	Sets all outputs to High
1	1	Sets all outputs to High

(The state when power is turned on or when RESET is input)

F. STAND-BY MODE

(Turning off all display-lights and stopped oscillation function)

This mode turns off all display-lights (fixing COM at “Low”) and stops oscillation function.
This completely stops the internal operation of the IC and attains low power consumption of V_{DD} and V_{DISP}.

Note: If the RESET signal is input while the stand-by mode in progress, the stand-by mode is released and all states are initialized.

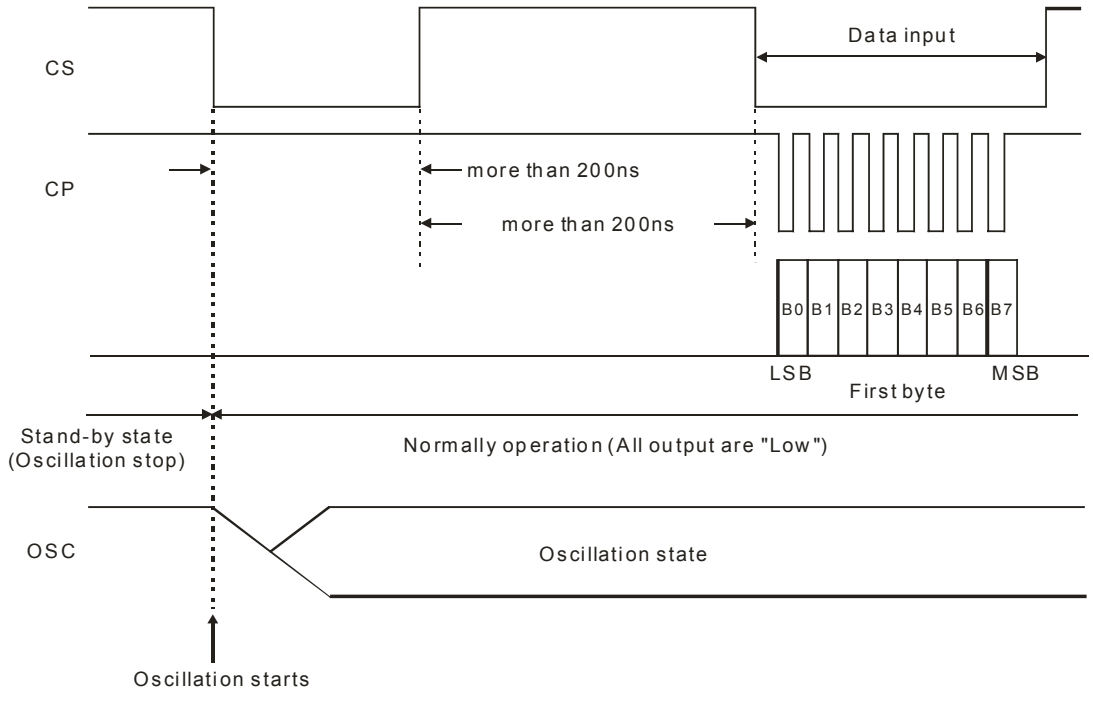
Command Format

	MSB							LSB	
1st Byte (1st)	B7	B6	B5	B4	B3	B2	B1	B0	Selects the stand-by mode
	1	1	1	1	*	*	*	*	

*: Don’t care.

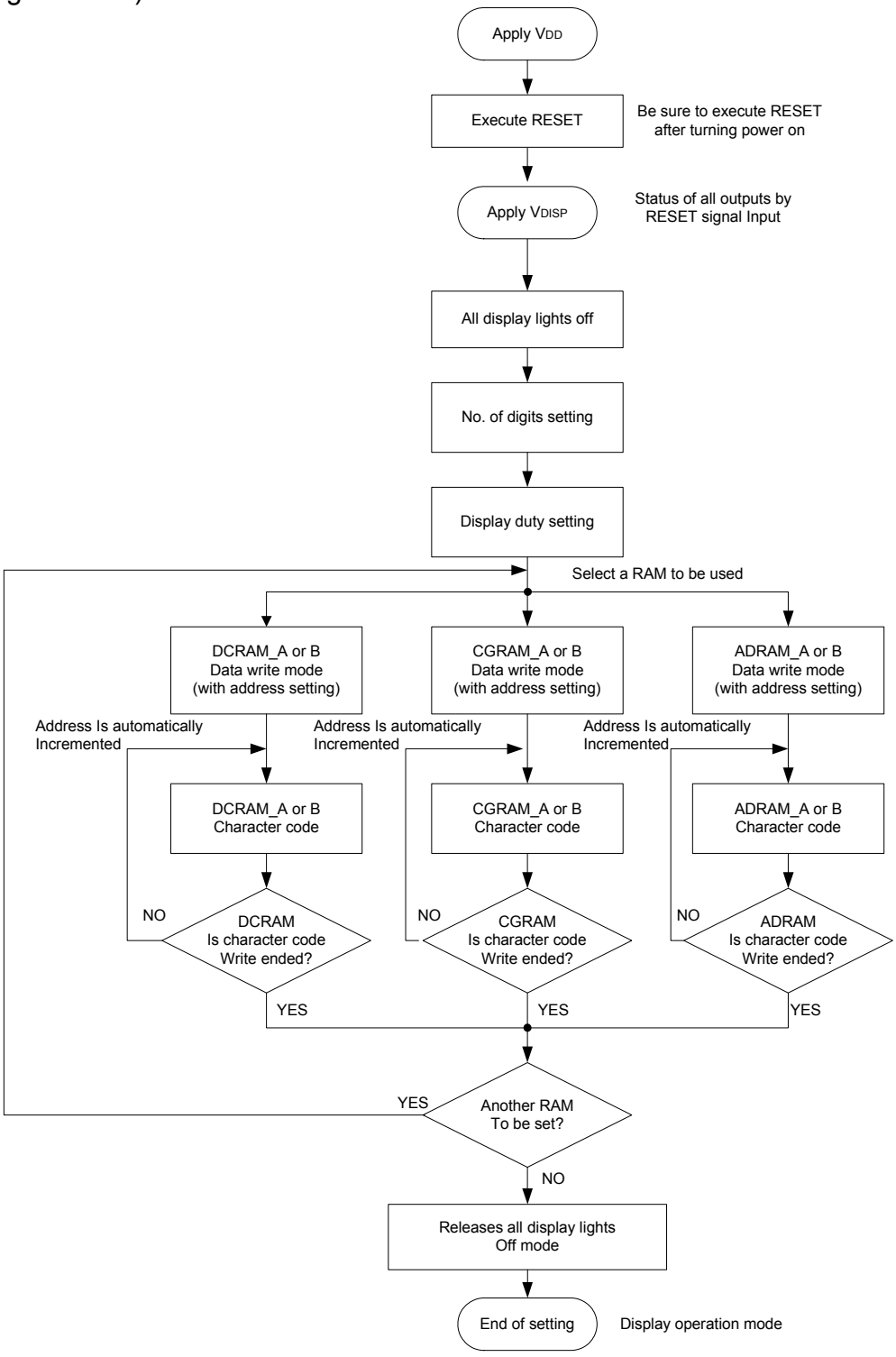
Releasing the Stand-by Mode

The timing to release the stand-by mode is shown below.
The stand-by mode is released at the falling edge of CS. (The internal oscillation starts)
When the oscillation becomes stable, the data input is enabled. (Return CS to “High” before entering data)
After the stand-by mode is released, all display-lights are turned off. Release the all display-lights OFF mode to turn on the display-lights.

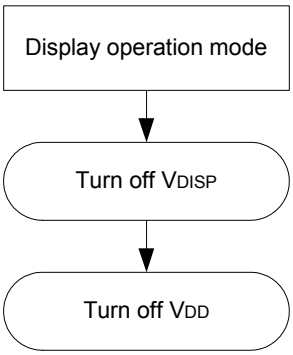


SETTING FLOWCHART

(Power applying included)



POWER-OFF FLOWCHART



AC CHARACTERISTICS

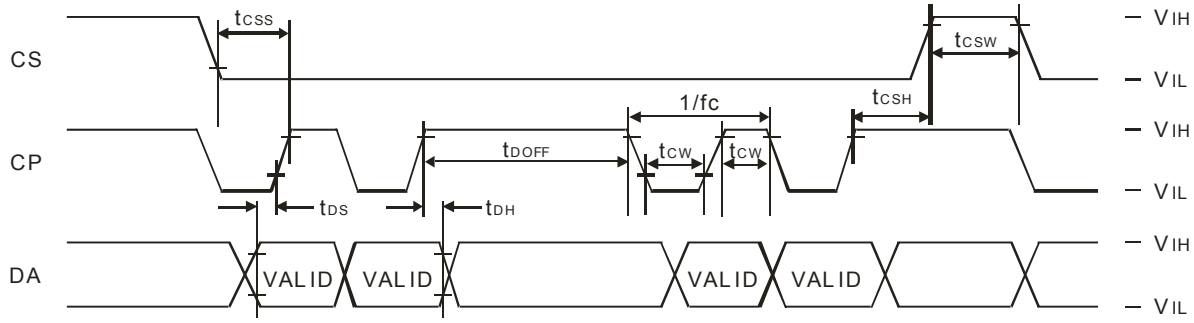
(Unless otherwise specified, V_{DD}=5.0V/3.3V±10%, V_{DISP}=30 to 60V, Tj=-40 to +125℃)

Parameter	Symbol	Condition		Min.	Max.	Unit
CP frequency	fc	-		-	2.0	MHz
CP pulse width	t_{CW}	-		200	-	ns
DA setup time	t_{DS}	-		200	-	ns
DA hold time	t_{DH}	-		200	-	ns
CS setup time	t_{CSS}	-		200	-	ns
CS hold time	t_{CSH}	Oscillation state		8	-	μs
CS wait time	t_{CSW}	-		200	-	ns
Data processing time	t_{DOFF}	Oscillation state		4	-	μs
RESET pulse width	t_{WRES}	When RESET signal is input from microcontroller etc. externally		200	-	ns
DA wait time	t_{RSOFF}	-		200	-	μs
All output slew rate	t_R	C_I=100pF	t_R=20 to 80%	-	2.0	μs
	t_F		t_F=80 to 20%	-	2.0	

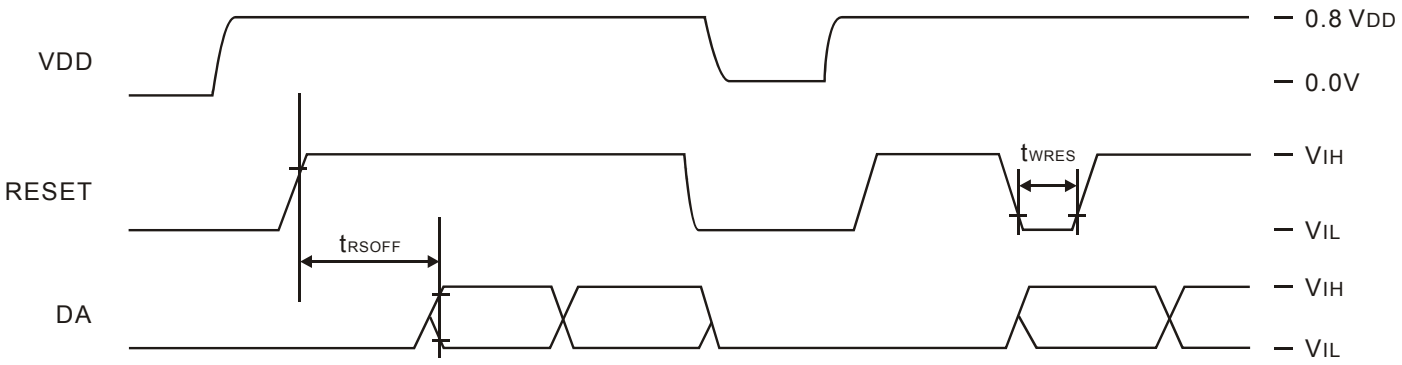
TIMING DIAGRAM

Symbol	V_{DD}=3.3V±10%	V_{DD}=5.0V±10%
V_{IH}	$0.8V_{DD}$	$0.8V_{DD}$
V_{IL}	$0.2V_{DD}$	$0.2V_{DD}$

DATA TIMING



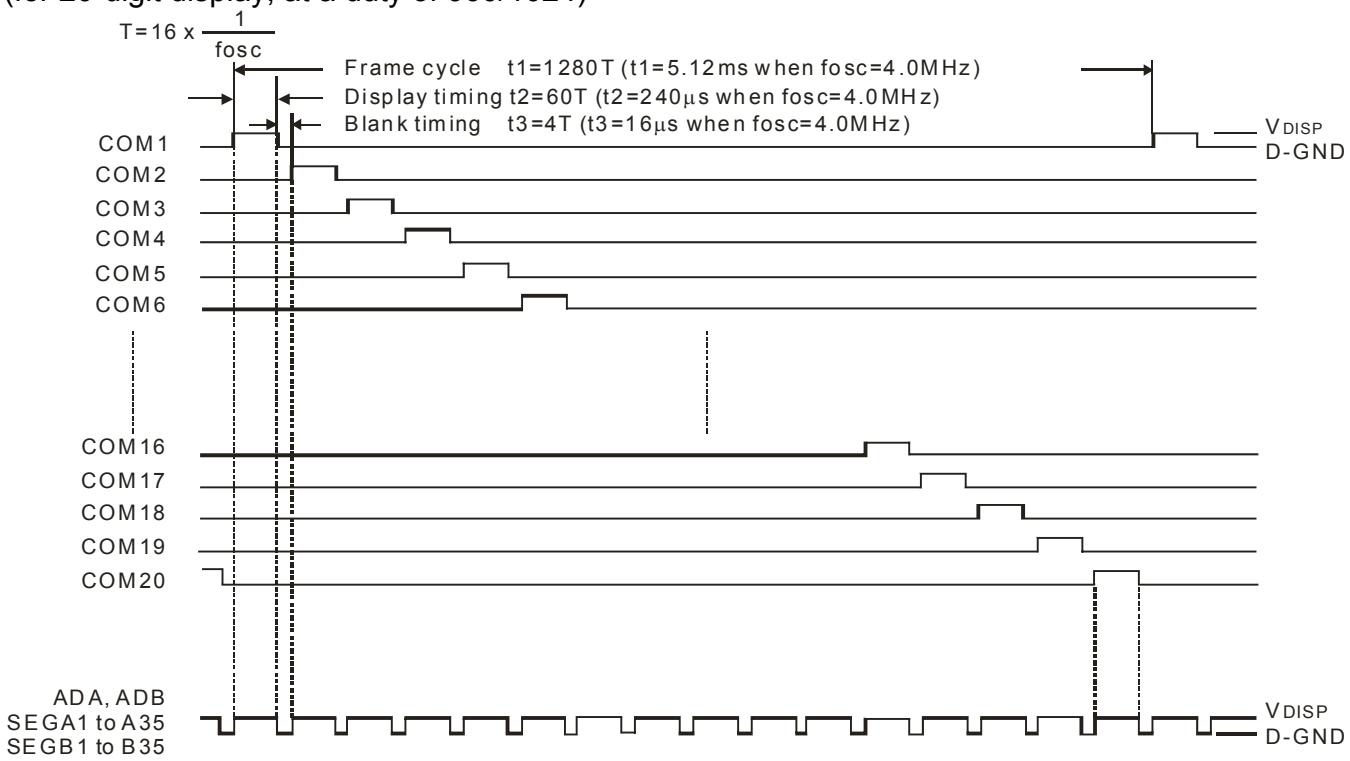
RESET TIMING



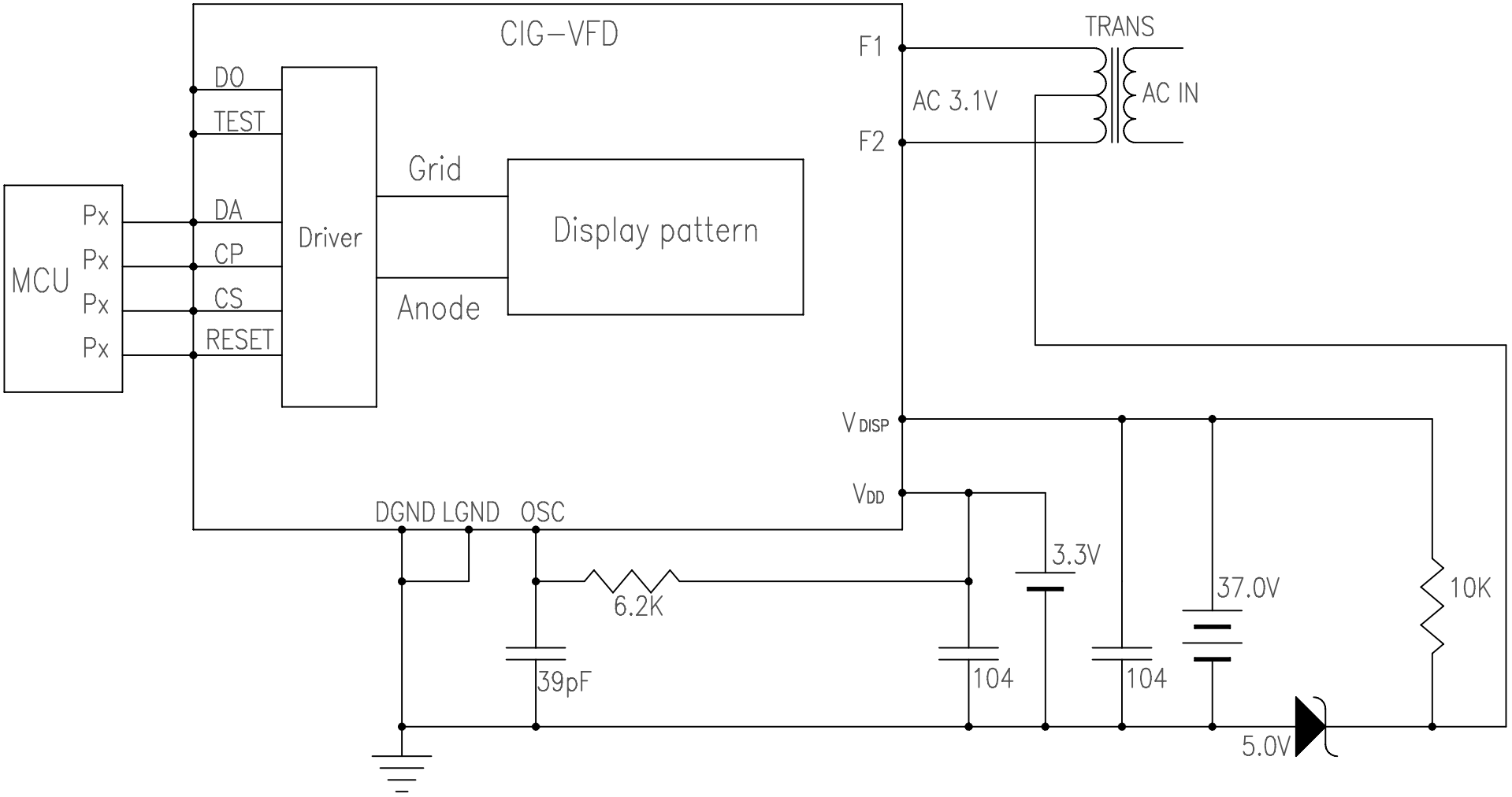
HIGH VOLTAGE OUTPUT TIMING

DIGIT OUTPUT TIMING

(for 20-digit display, at a duty of 960/1024)



APPLICATION CIRCUIT



Character Font Table