Task 1: Design Methodologies of Verilog HDL

task-1

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Task 1

Welcome to Task 1 of Soil Monitoring Bot!

The objective of this task is to understand the Verilog HDL basics and the design methodologies of Verilog HDL. In this task you have to design combinational and sequential circuits in Quartus Prime and do the RTL simulation in Modelsim.

> ***Note:*** *You can go back and read Task 0 as it will be a prerequisite for Task 1.*

This task is divided into 4 sub-tasks:

1. **Combinational Circuit :** The aim is to design a combinational circuit using 4-bit comparator, 4 input logic function and 4:1 multiplexer.
2. **Sequential Circuit :** The aim is to design a 3-bit synchronous counter using T flip-flops.
3. **Finite State Machine :** The aim is to design a Finite State Machine in Verilog HDL to detect sequence/pattern.
4. **Frequency Scaling and PWM :** The aim is to implement frequency scaling in Verilog HDL and also implement Pulse Width Modulation.

You will find separate sections for each sub-task. Detailed procedure for each sub-task is described in their respective sections.

Submission Instructions (Will be added soon):