Kajal Varma

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EDUCATION

Birla Institute of Technology and Science, Pilani, K.K. Birla Goa Campus, India Aug 2012 – May 2016

- **B.E. (Hons.) Computer Science, CGPA: 8.64 / 10.0**
- Courses: Operating Systems, Computer Architecture, Data Storage Technologies and Networks, Computer Networks, Data Structures and Algorithms

National Public School, Indiranagar, Bangalore, India Jun 1998 – Mar 2012

- Grade XII: 97.6%, Grade X: CGPA 10.0 and percentile 99.9946

PUBLICATIONS

K. Varma, G. Patil and B. Raveendran, "DTLB: Deterministic TLB for Tightly Bound Hard Real-Time Systems," 2017 30th International Conference on VLSI Design and 2017 16th International Conference on Embedded Systems (VLSID), Hyderabad, 2017, pp. 207-212.

RESEARCH EXPERIENCE

Thesis – Energy Estimation of High Performance Computing Applications Jan 2016 – Jun 2016

Guide: Dr. Santonu Sarkar, Dept. of CS & IS, BITS Pilani Goa Campus

- Research thesis on estimation of energy consumption of parallel CUDA (Compute Unified Device Architecture) programs run on NVIDIA GPUs, by predicting execution time and power level.
- Constructed a static analysis model for compiled Parallel Thread Execution (PTX) code and modelled thread execution to predict execution time. Constructed a power model by benchmarking.

Real-Time Operating Systems – Memory Design Jan 2015 – Dec 2015

Guide: Dr. Biju Raveendran, Dept. of CS & IS, BITS Pilani Goa Campus

- Research project proposing a deterministic TLB and process-aware partitioned cache design to eliminate inter-task interference, lower miss rates, and reduce energy usage.
- Implemented MemSim, a single-clock-cycle memory subsystem simulator for experimental validation.

Real-Time Operating Systems – Scheduler Design Jan 2015 – Dec 2015

Guide: Dr. Biju Raveendran, Dept. of CS & IS, BITS Pilani Goa Campus

- Implemented an improved scheduling algorithm based on the Earliest-Deadline-First algorithm and modified with Stack Resource Policy and dynamic resource locking.
- Enabled slack time extension for concurrent real-time tasks, minimizing the number of context switches for real-time tasks and leading to energy savings.

WORK EXPERIENCE

Software Engineer I – Intuit, Bangalore, India Aug 2016 – Present

- Cross-platform library and application developer for the TurboTax Desktop product on Windows and MacOS.
- Implemented a standalone C++ library for use across Intuit teams and products.

Summer Intern – Intuit, Bangalore, India May 2015 – Jul 2015

- Integrated location-based features into the TurboTax Universal Android application and built automation tools.

PROJECTS

Raspberry Pi Surveillance System with Android Interface Oct 2015 – Nov 2015

Linux Kernel Mouse Device Driver Implementation Mar 2015 – Apr 2015

Simulation of DiskSim Scheduling Algorithms Mar 2015 – Apr 2015

Phased Cache Memory Design and Simulation Oct 2014 – Nov 2014

Garbage Collector Simulation for Memory Management Aug 2014 – Dec 2014

Battleship Network Game Oct 2015 – Nov 2015

ASSISTANTSHIPS

Teaching Assistant – Computer Architecture Aug 2015 – Dec 2015

Instructor: Dr. Biju Raveendran, Dept. of CS & IS, BITS Pilani Goa Campus

- Conducted laboratory sessions and evaluated course projects.

Professional Assistant – Computer Programming Jan 2015 – May 2015

Instructor: Mr. Mahadev Gawas, Dept. of CS & IS, BITS Pilani Goa Campus

- Conducted and evaluated laboratory sessions.

SKILLS

- **Programming and Tools:** C, C++, bash, Java, Python, Git, Latex
- **Environments:** Linux/UNIX, Windows, MacOS

HONORS AND ACHIEVEMENTS

Winner – Intuit HackUtsav 2017, Intuit, India Jul 2017

Course Topper – Data Storage Technologies and Networks May 2015

All-India Rank 17 – National Cyber Olympiad, India Jun 2011

EXTRA CURRICULAR

Department of Creative Media, Mime Club, Department of Photography – BITS Pilani Goa Campus

Vice Prefect – National Public School