

Lab #5: FPGA Board

- Synthesize and run a counter on ZedBoard

4190.309A: Hardware System Design
(Spring 2018)

Tutorial: ZedBoard exploration

Preparing the Board

1. Set configuration mode pins from 01100 to **00000**
2. Insert USB-JTAG cable at J17
3. Insert power cable at J20
4. Turn the power on with SW8
 - LD13 lights up when it is on
5. Check locations of switches & LED
 - We will deal with SW0~7 & LD0~7

✘ **CAVEAT: J17 pin is very fragile!**

If you cannot pull out a USB-JTAG cable from J17, press hooks with something pointed (sharp pencil, etc.).

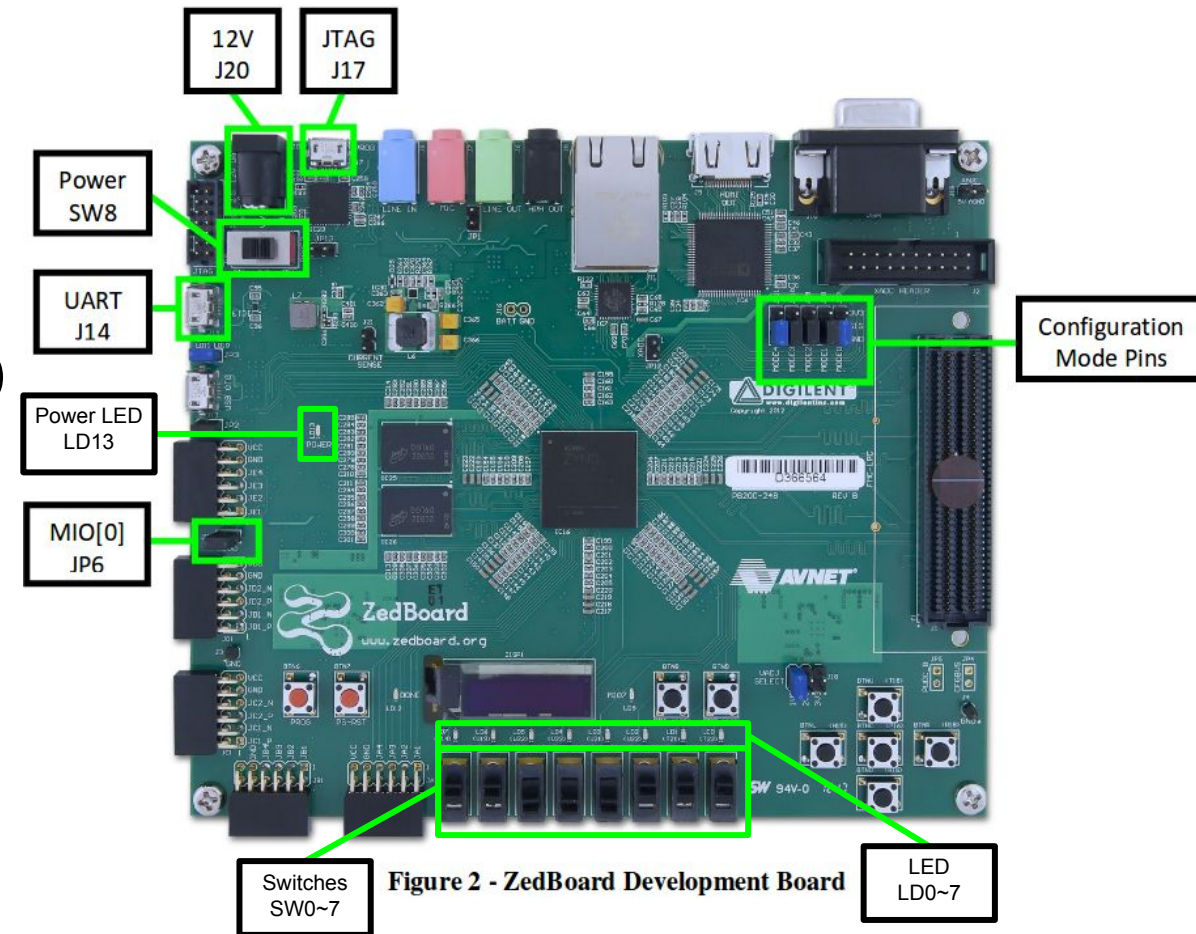
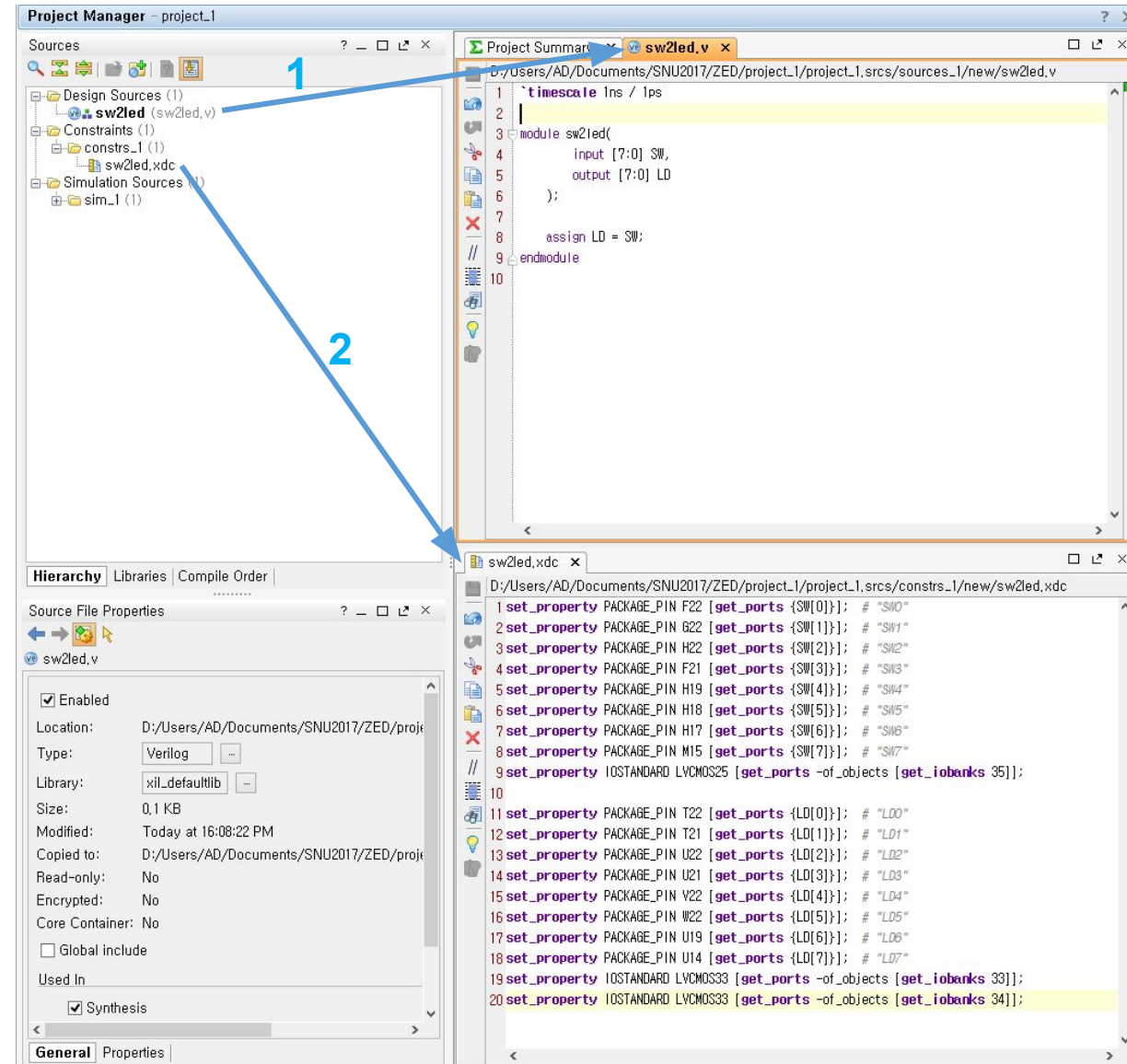


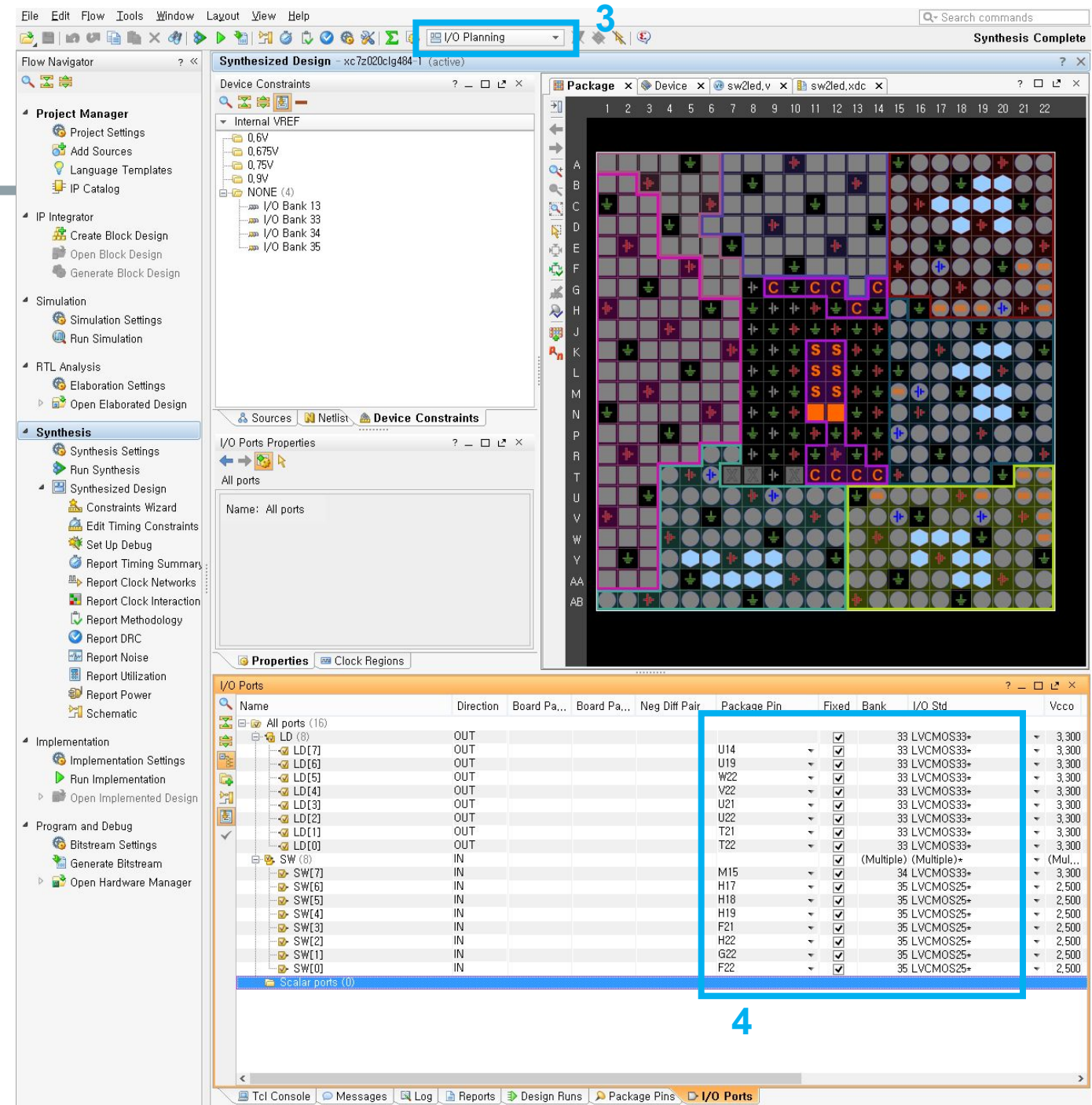
Figure 2 - ZedBoard Development Board

SW2LED Module

- sw2led.v: Verilog file
 - Create a **design source**
 - Specifying logic behavior
 - Turn LEDs on/off using switches
- sw2led.xdc: Design constraints file
 - Specify **constraints**
 - Connecting Verilog input/output ports to FPGA pins
 - 8 switches & 8 LEDs
 - Refer to User's Guide p. 4, pp. 19-20



- Synthesize and check



Implementation

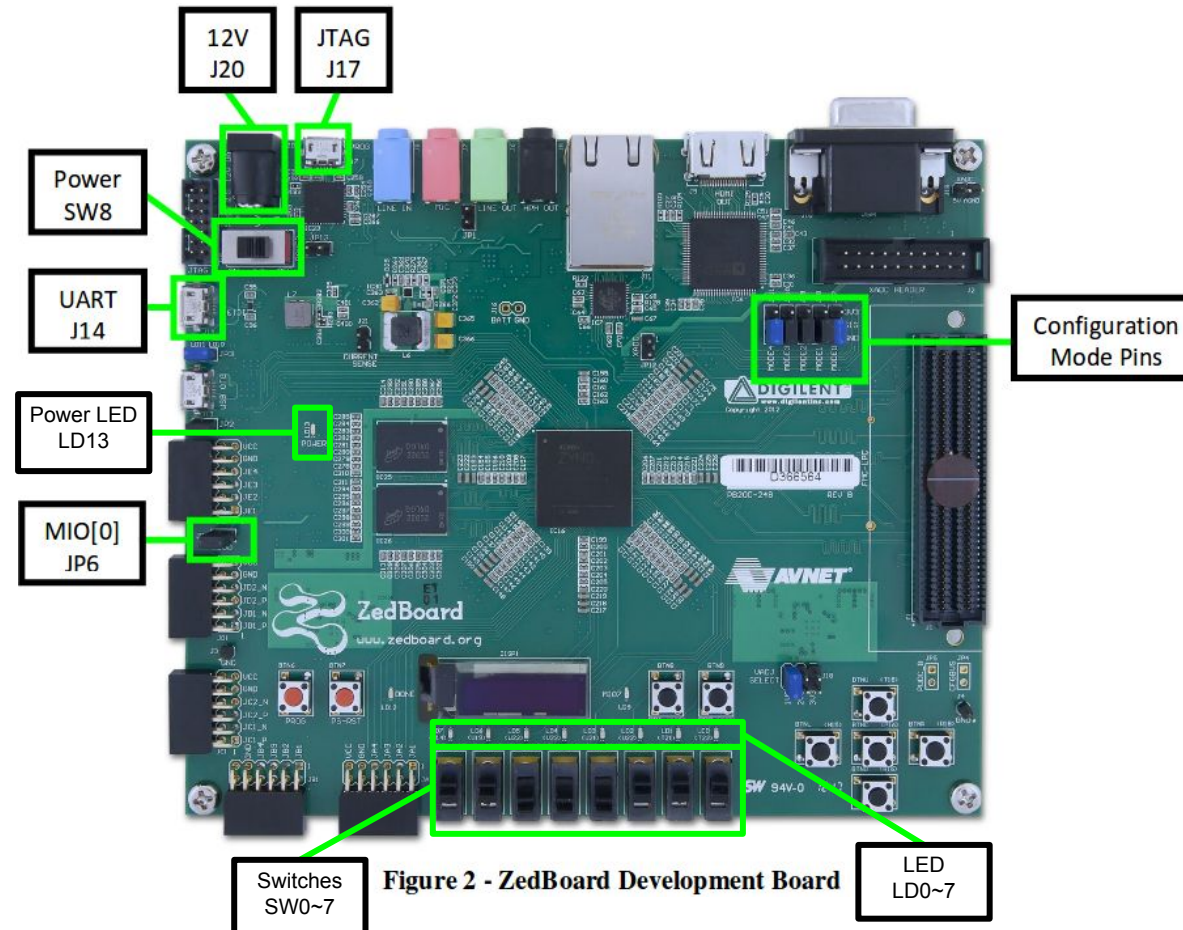
- Implement and download your design into FPGA

The following steps illustrate the implementation and download process:

- 1** In the **Flow Navigator** on the left, click **Generate Bitstream** under the **Program and Debug** section.
- 2** A dialog box titled "No Implementation Results Available" appears. Click **Yes** to launch implementation.
- 3** A dialog box titled "Bitstream Generation Completed" appears. Select **Open Hardware Manager** and click **OK**.
- 4** In the **Hardware Manager** window, which shows "No hardware target is open", click the **Open target** button. This step is labeled "4->Auto connect".
- 5** The **Hardware Manager** window now shows the target device **xc7z020_1** with a status of "Not programmed". This step is labeled "5->xc7z020_1".
- 6** Click the **Program device** button in the **Hardware Manager** window. This opens the **Program Device** dialog box, where you can select the bitstream file and debug probes file, and click **Program** to download the design.

Enjoy Your Design!

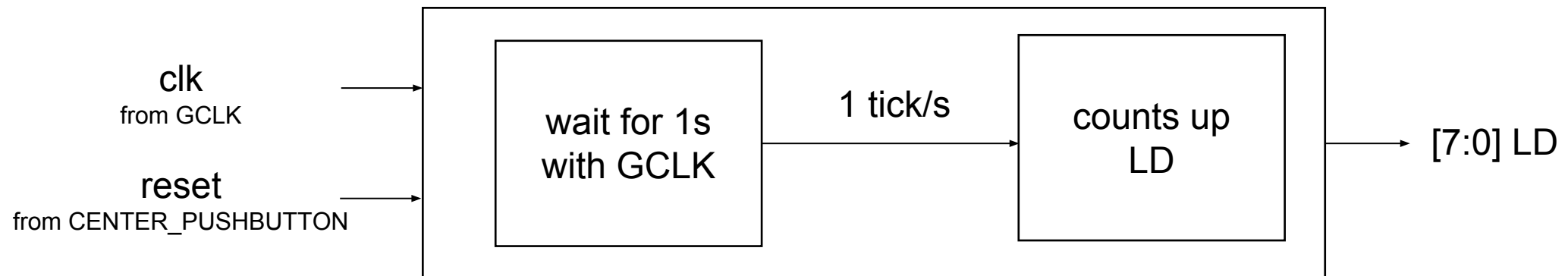
- Toggle SW0~7 and check how LD0~7 changes



Practice: Counter implementation

Design: A Simple Up-Counter

- Output [7:0] LD is incremented by one every second
- Use GCLK as an input clock and use it to wait for 1s
 - GCLK signal has frequency of 100MHz (Check User's Guide p.3).
- Use CENTER_PUSHBUTTON as a asynchronous **posedge** reset
 - counts up from 0 again after reset



Constraints

- Find **which pin to use** from User's Guide
- Find **which bank each pin is on** from User's Guide
- Start from a master constraint file from the following link:
https://github.com/Digilent/Zedboard/blob/master/Resources/XDC/zedboard_master.xdc

Grading policy

- Check lists
 - LED counts up (50 points)
 - LED counts up every 1s (20 points)
 - Reset works (20 points)
 - Finished in class (10 points)
- Submit “**counter.v**” and “**counter.xdc**” on eTL.
 - Due : 4/10 (Tue) PM **2:00**
 - Late submission will result in a penalty
- Show that your board works
 - In class / office hour (Tue) recommended
 - If you cannot come to the office hour, mail us a short video

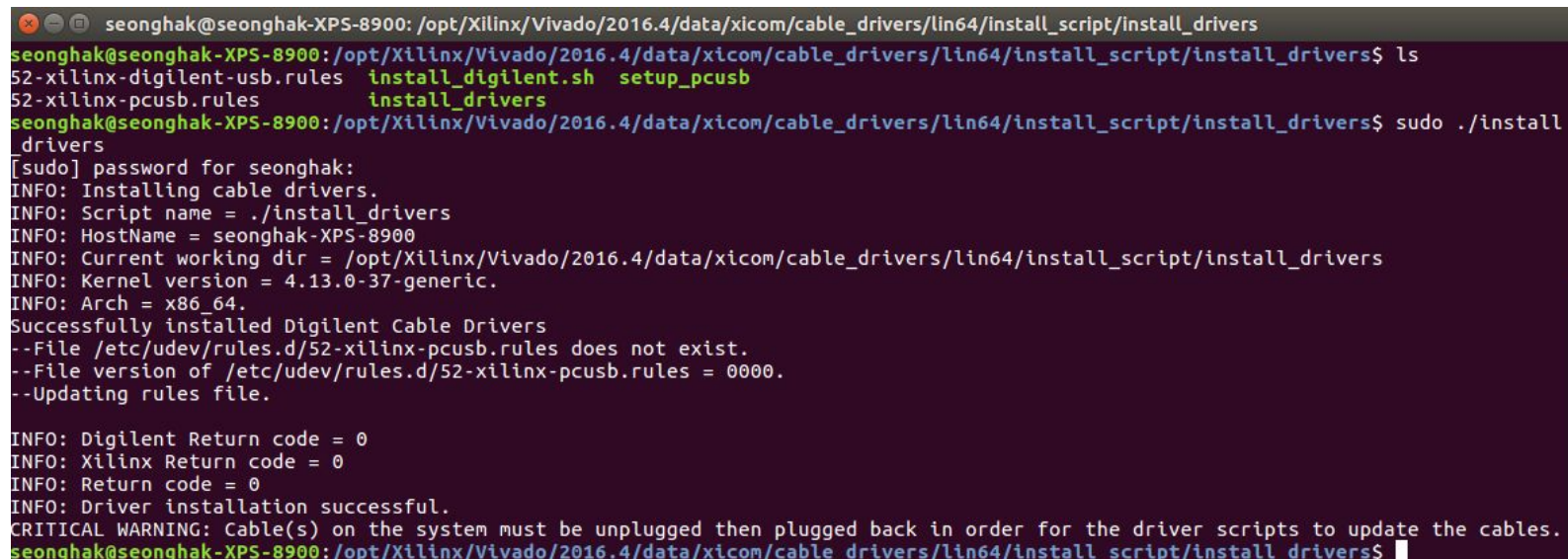
Appendix: Installing Driver

- Driver required for the host computer to recognize ZedBoard
 - i.e. Hardware Manager will not find the board without the driver

- Install using linux command line

```
sudo chmod +x $(vivado_dir)/data/xicom/cable_drivers/lin64/install_script/install_drivers
```

```
sudo $(vivado_dir)/data/xicom/cable_drivers/lin64/install_script/install_drivers
```

A terminal window screenshot showing the execution of the install_drivers script. The prompt is seonghak@seonghak-XPS-8900. The script lists files 52-xilinx-digilent-usb.rules, install_digilent.sh, and setup_pcusb. It then runs with sudo, prompting for a password. The script outputs various INFO messages about the installation process, including the script name, host name, working directory, kernel version, and architecture. It reports successful installation of Digilent Cable Drivers and updates the udev rules file. A CRITICAL WARNING is issued about unplugging and plugging back cables. The prompt returns to seonghak@seonghak-XPS-8900.

```
seonghak@seonghak-XPS-8900: /opt/Xilinx/Vivado/2016.4/data/xicom/cable_drivers/lin64/install_script/install_drivers
seonghak@seonghak-XPS-8900:/opt/Xilinx/Vivado/2016.4/data/xicom/cable_drivers/lin64/install_script/install_drivers$ ls
52-xilinx-digilent-usb.rules  install_digilent.sh  setup_pcusb
52-xilinx-pcusb.rules        install_drivers
seonghak@seonghak-XPS-8900:/opt/Xilinx/Vivado/2016.4/data/xicom/cable_drivers/lin64/install_script/install_drivers$ sudo ./install_drivers
[sudo] password for seonghak:
INFO: Installing cable drivers.
INFO: Script name = ./install_drivers
INFO: HostName = seonghak-XPS-8900
INFO: Current working dir = /opt/Xilinx/Vivado/2016.4/data/xicom/cable_drivers/lin64/install_script/install_drivers
INFO: Kernel version = 4.13.0-37-generic.
INFO: Arch = x86_64.
Successfully installed Digilent Cable Drivers
--File /etc/udev/rules.d/52-xilinx-pcusb.rules does not exist.
--File version of /etc/udev/rules.d/52-xilinx-pcusb.rules = 0000.
--Updating rules file.

INFO: Digilent Return code = 0
INFO: Xilinx Return code = 0
INFO: Return code = 0
INFO: Driver installation successful.
CRITICAL WARNING: Cable(s) on the system must be unplugged then plugged back in order for the driver scripts to update the cables.
seonghak@seonghak-XPS-8900:/opt/Xilinx/Vivado/2016.4/data/xicom/cable_drivers/lin64/install_script/install_drivers$
```