Logic Design **Autumn 2017**
M1522.000700 **CSE (Jihong Kim)**

Course Information

September 4, 2017

■ Course Goal

디지털 논리 회로는 컴퓨터 뿐 아니라 각종 디지털 전자 기기의 하드웨어를 구성하는 기본 요소이며 이 강좌를 통해서 기본 지식을 학습한다. 학생들은 논리회로를 구성하는 기본 소자, 조합회로와 순차회로의 설계 이론을 배운다. 이와 병행하여 학습한 이론을 실험을 통해 확인하여 하드웨어 설계의 기초를 공고히 한다.

■ Instructor and TA

- Instructor: Jihong Kim 김지홍 (office: Room 328 @Building 302)
  Email: jihong@davinci.snu.ac.kr Phone: 880-8792
  Office hours: 월 14:30 – 15:20 (or by appointment)

- TAs:
  Head TA: 박지성 (315-2@302, jspark@davinci.snu.ac.kr, 880-1861)
  한승욱 (315-2 @302, han103506@gmail.com, 880-1861),
  천명준 (315-2 @302, mjchun.snu@gmail.com, 880-1861)
  유정석 (315-2 @302, js_ryoo@davinci.snu.ac.kr, 880-1861)
  조유현 (315-2 @302, acemople@gmail.com, 880-1861)
  진용석 (315-2 @302, mnm102211@gmail.com, 880-1861)

  조교전체 메일링리스트: tas0217@davinci.snu.ac.kr
  Office hours: TBD (or by appointment)

■ Class Hours & Course Homepage

- [이론]: 월/수 15:30 – 16:45 @302-107
- [실습]: 수 18:30 – 20:30 @302-310-2
- Course homepage: 논리설계(001) at http://etl.snu.ac.kr
  - Important notices regarding the course will be announced in the course homepage. Please visit the course homepage regularly.
  - Lecture slides will be available before the lecture at the homepage.

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Prerequisite

- Programming experience

Textbook

- Randy H. Katz and Gaetano Borriello
  Contemporary Logic Design, 2nd Edition
  Pearson Prentice Hall

Grading

- Midterm: 20% (10/30)
- Final: 30% (12/11)
- Assignments: 35%
- [실습] 평가: 10%
- [이론] 출석: 5%
- **Course Repeat Policy: the highest grade is limited to A0.**

■ **[실습]은 출석이 매우 중요함.** 따라서 [실습]의 무단 결석에 대해서는 100 점으로 환산된 최종 성적을 다음과 같이 조정함:

- 1 회 결석당 **최종 성적에서 10 점 감점**

Course Outline

[이론]: We will cover Chapter 1 through Chapter 10 of the textbook.

Assignments

- 5 번의 이론 및 설계 숙제
- 설계 프로젝트 (3 주 소요 예정)

- **Assignment Submission Policy**
  - Each student has **3 bonus days** which can be used for any of the assignments (except for **the last assignment**). Note that you can use your bonus days only by *days*. For example, even if you are 2 hours late, you must use one full bonus day. No partial usage of a free late day is allowed.

    Once the 3 bonus days are exhausted, late submissions are accepted for the following two cases only with large penalties:

    a. If your assignment is late *by less than 12 hours*, the penalty is 30% of the TOTAL assignment point.
    b. If your assignment is late *by less than 24 hours*, the penalty is 60% of the TOTAL assignment point.

- **Cheating Policy**

  Any type of cheating (e.g., copying others' assignment/programs, stealing an examination), if found, a grade of F will be assigned. For a further disciplinary action, the College of Engineering will be notified of the cheating activity.