Lab #5: FPGA Board

- Synthesize and run a counter on ZedBoard

4190.309A: Hardware System Design
(Spring 2018)

Tutorial: ZedBoard exploration

Preparing the Board

1. Set configuration mode pins from 01100 to **00000**
2. Insert USB-JTAG cable at J17
3. Insert power cable at J20
4. Turn the power on with SW8
   - LD13 lights up when it is on
5. Check locations of switches & LED
   - We will deal with SW0~7 & LD0~7

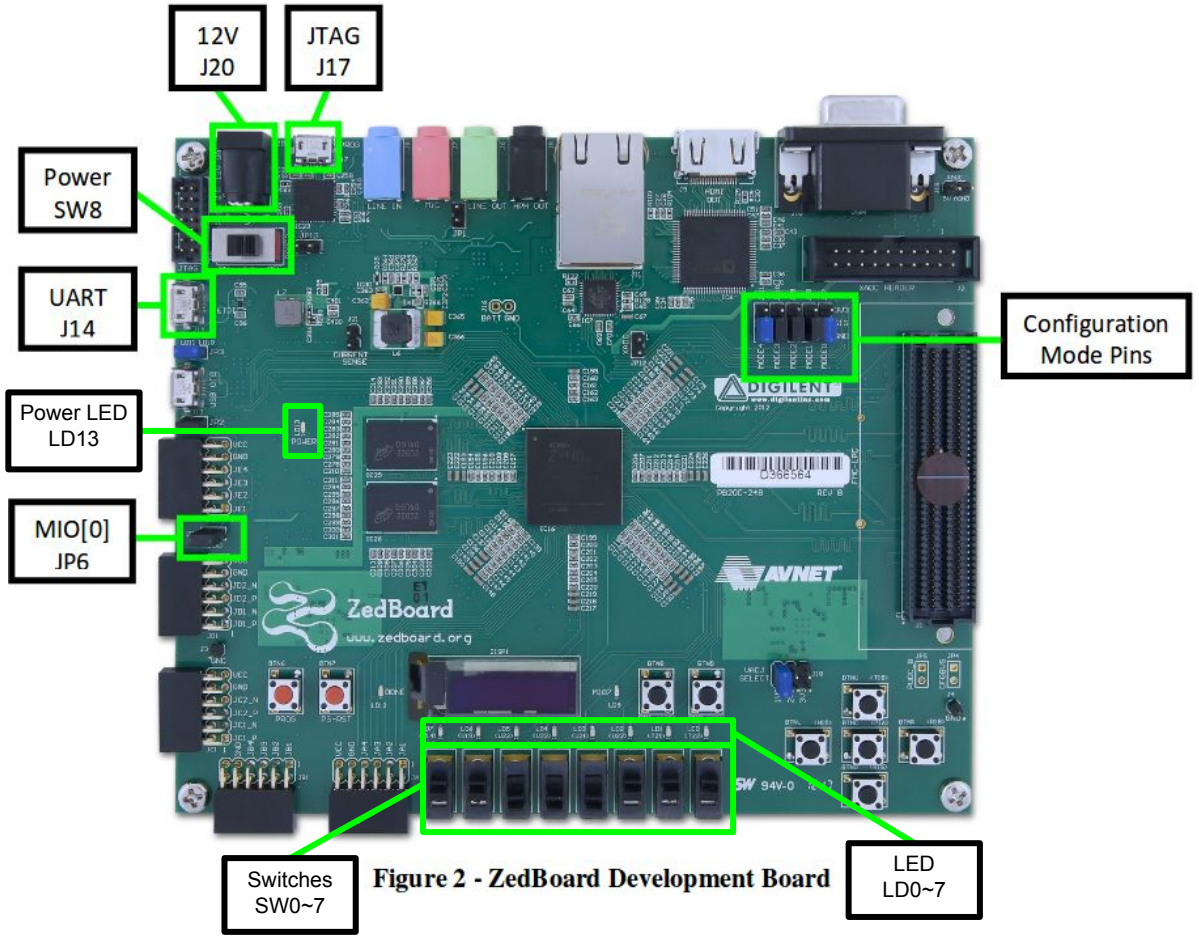


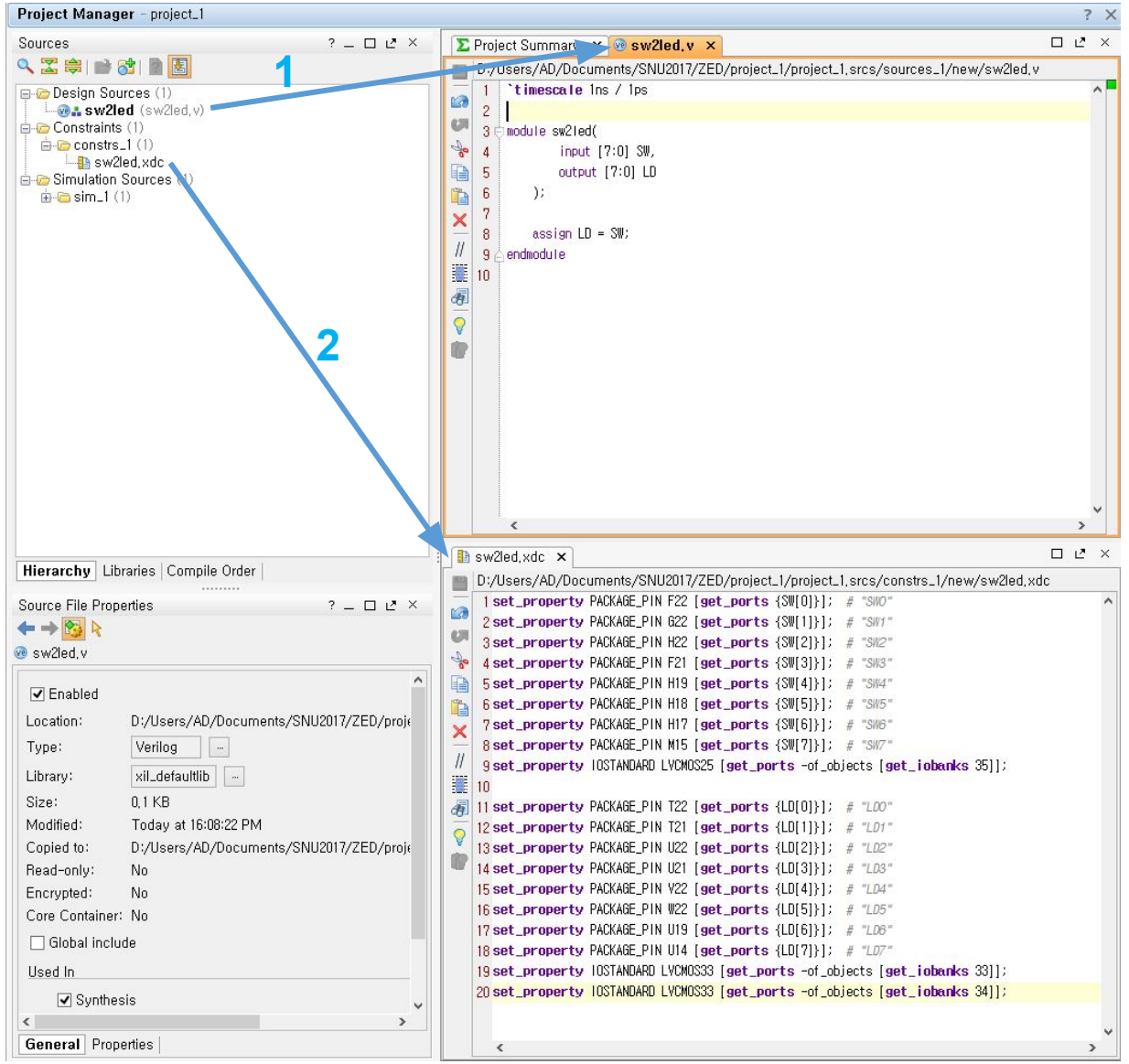
Figure 2 - ZedBoard Development Board

※ CAVEAT: J17 pin is very fragile!

If you cannot pull out a USB-JTAG cable from J17, press hooks with something pointed (sharp pencil, etc.).

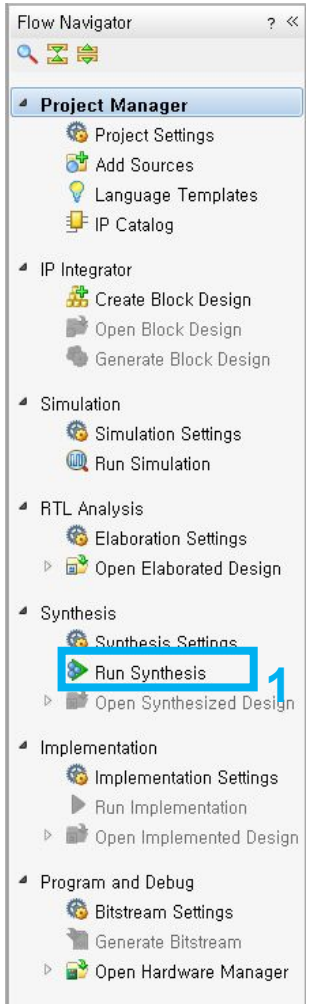
SW2LED Module

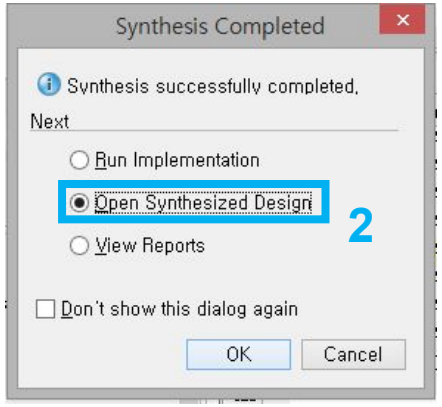
- sw2led.v: Verilog file
  - Create a **design source**
  - Specifying logic behavior
    - Turn LEDs on/off using switches
- sw2led.xdc: Design constraints file
  - Specify **constraints**
  - Connecting Verilog input/output ports to FPGA pins
  - 8 switches & 8 LEDs
    - Refer to User's Guide p. 4, pp. 19-20

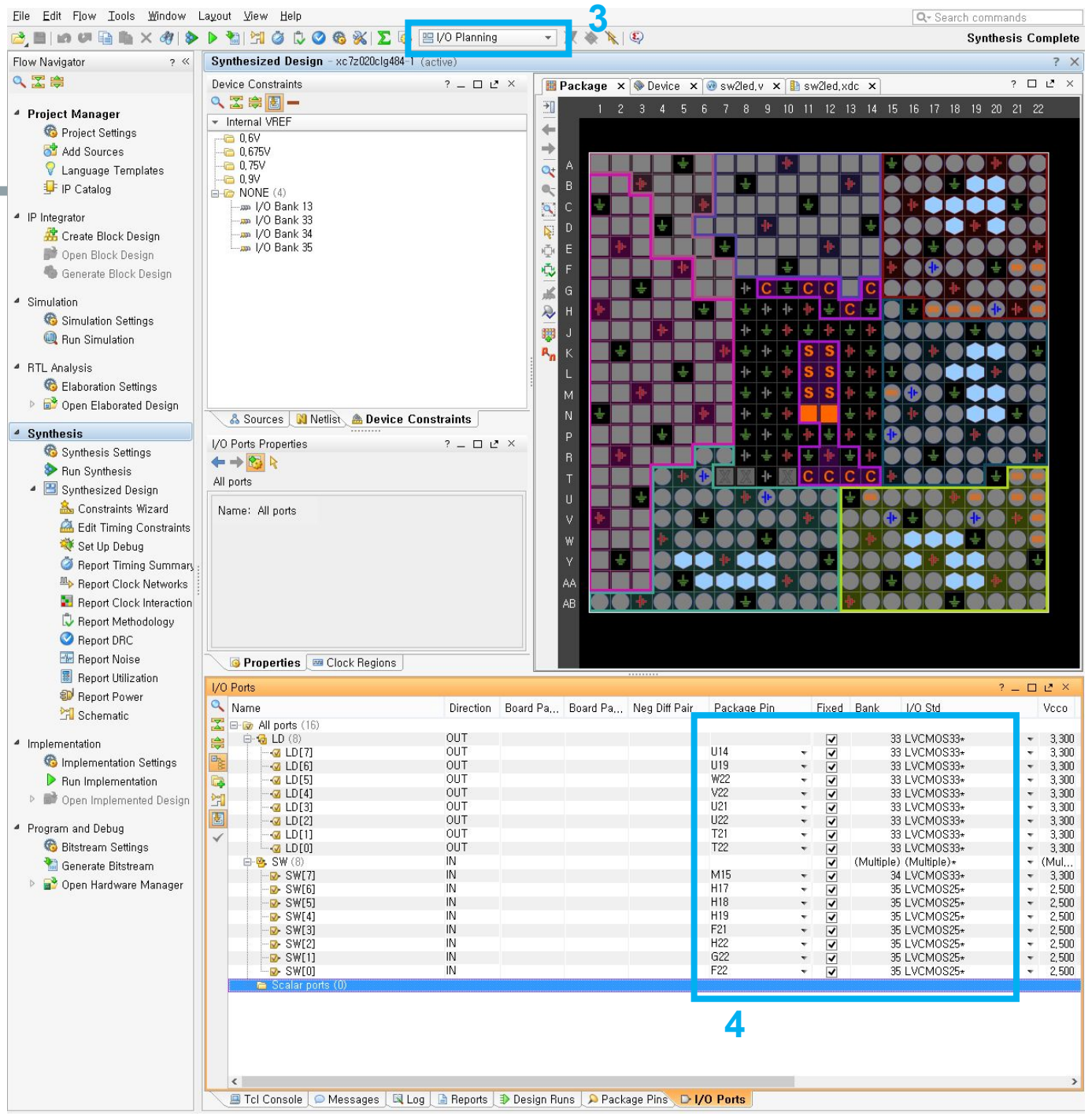


Synthesis

- Synthesize and check

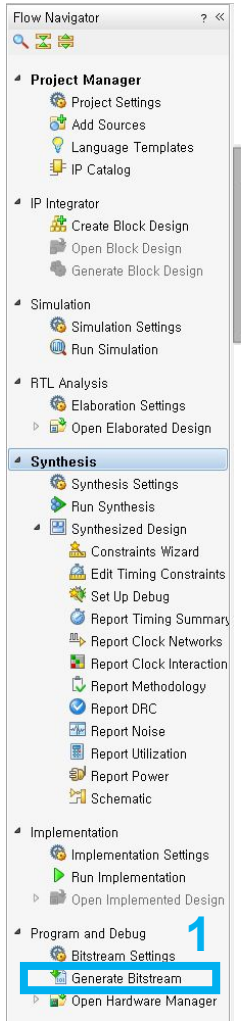


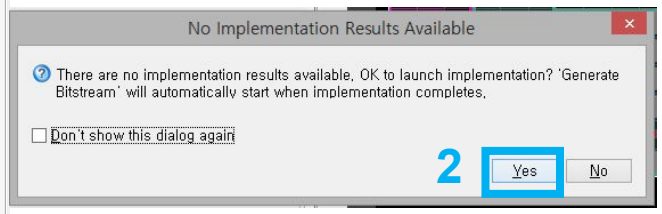


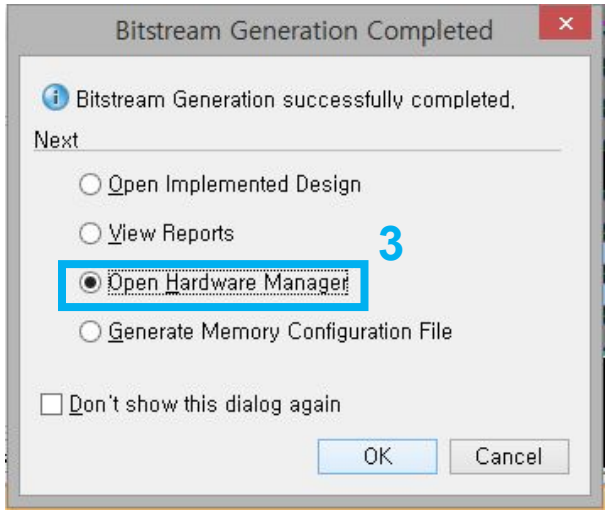


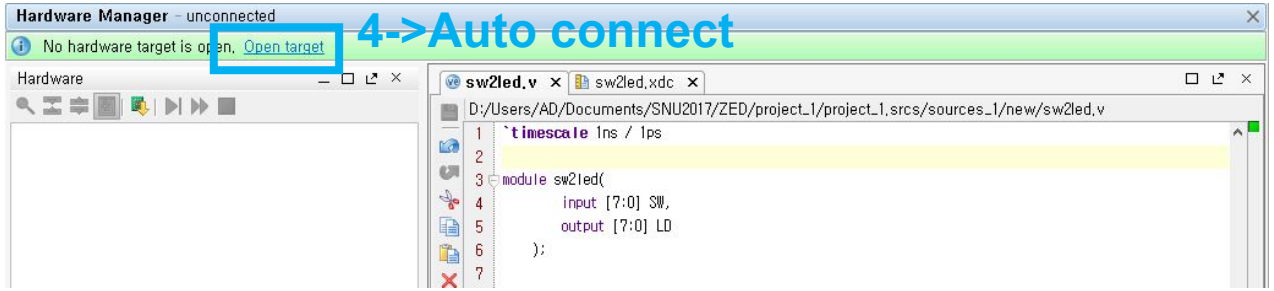
Implementation

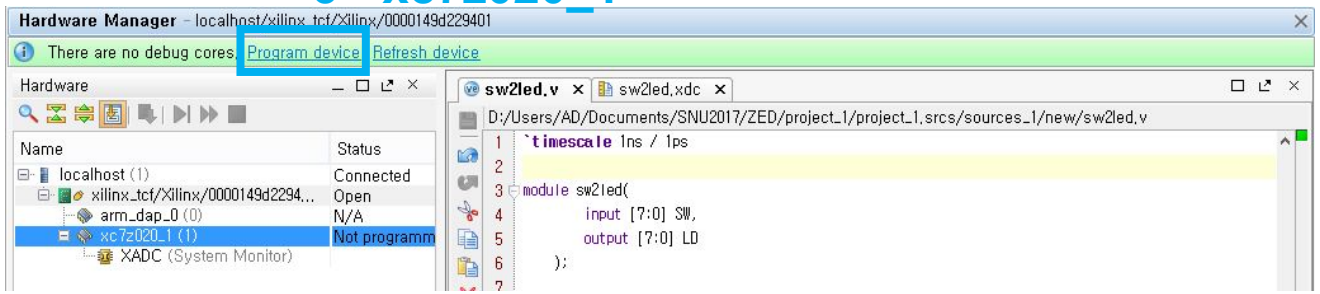
- Implement and download your design into FPGA

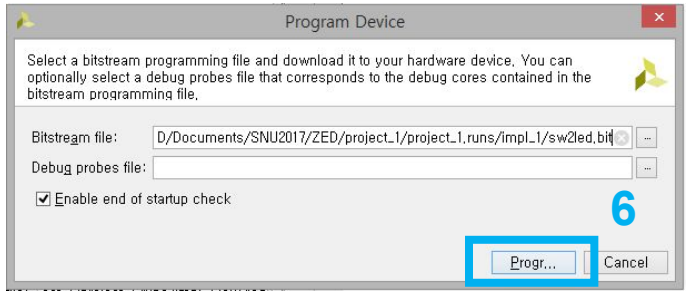












Enjoy Your Design!

- Toggle SW0~7 and check how LD0~7 changes

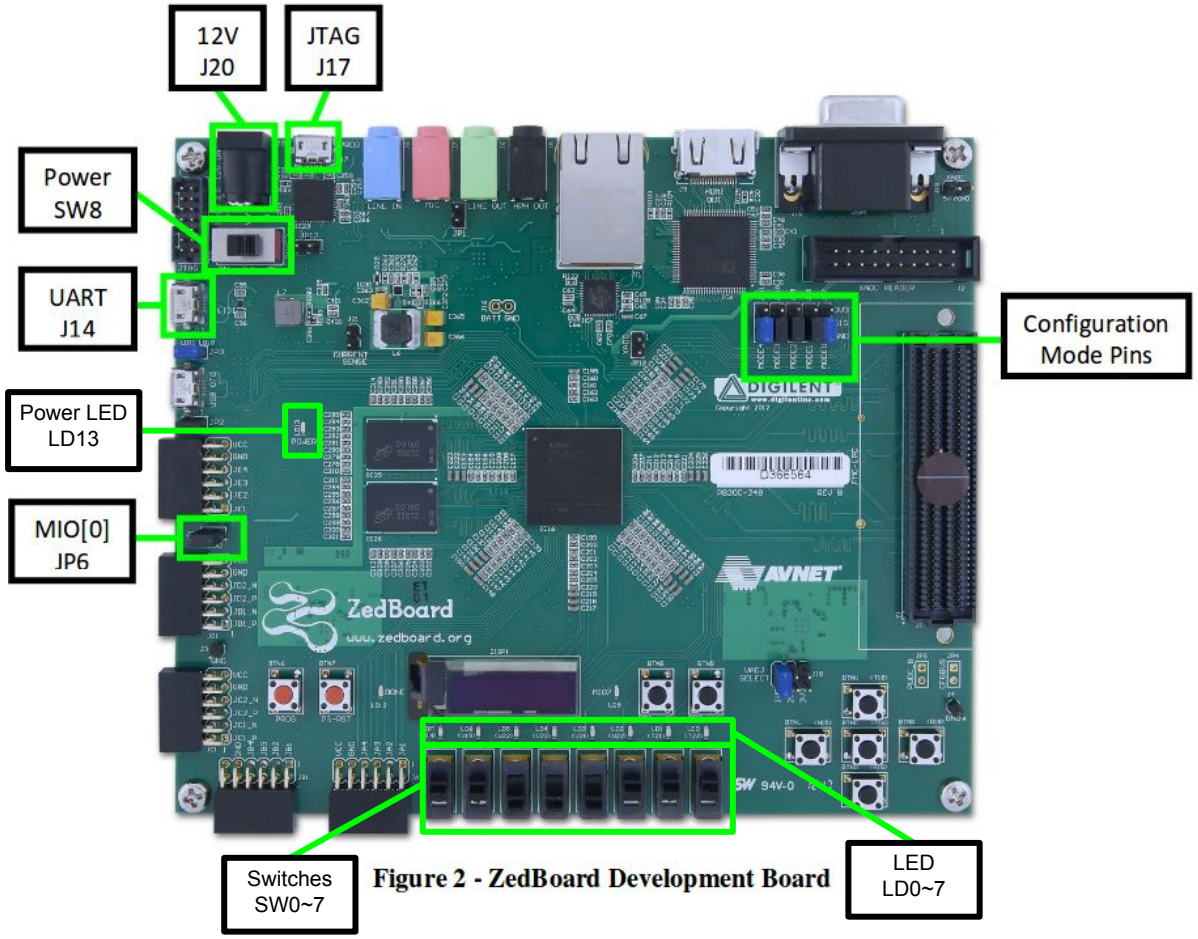
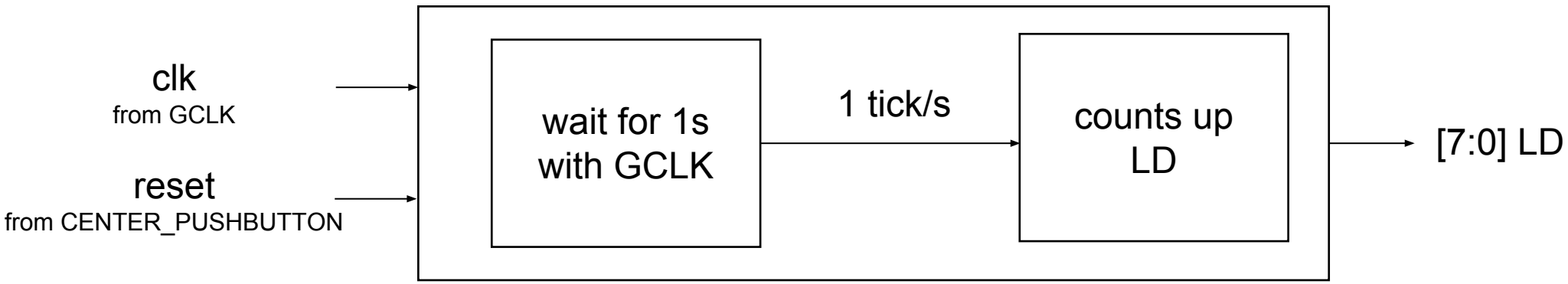


Figure 2 - ZedBoard Development Board

Practice: Counter implementation

Design: A Simple Up-Counter

- Output [7:0] LD is incremented by one every second
- Use GCLK as an input clock and use it to wait for 1s
  - GCLK signal has frequency of 100MHz (Check User's Guide p.3).
- Use CENTER_PUSHBUTTON as a asynchronous **posedge** reset
  - counts up from 0 again after reset



Constraints

- Find **which pin to use** from User's Guide
- Find **which bank each pin is on** from User's Guide
- Start from a master constraint file from the following link:

  https://github.com/Digilent/Zedboard/blob/master/Resources/XDC/zedboard_master.xdc

Grading policy

- Check lists
  - LED counts up (50 points)
  - LED counts up every 1s (20 points)
  - Reset works (20 points)
  - Finished in class (10 points)

- Submit **“counter.v”** and **“counter.xdc”** on eTL.
  - Due : 4/10 (Tue) PM 2:00
  - Late submission will result in a penalty

- Show that your board works
  - In class / office hour (Tue) recommended
  - If you cannot come to the office hour, mail us a short video

Appendix: Installing Driver

- Driver required for the host computer to recognize ZedBoard
  - i.e. Hardware Manager will not find the board without the driver

- Install using linux command line

sudo chmod +x $(vivado_dir)/data/xicom/cable_drivers/lin64/install_script/install_drivers

sudo $(vivado_dir)/data/xicom/cable_drivers/lin64/install_script/install_drivers