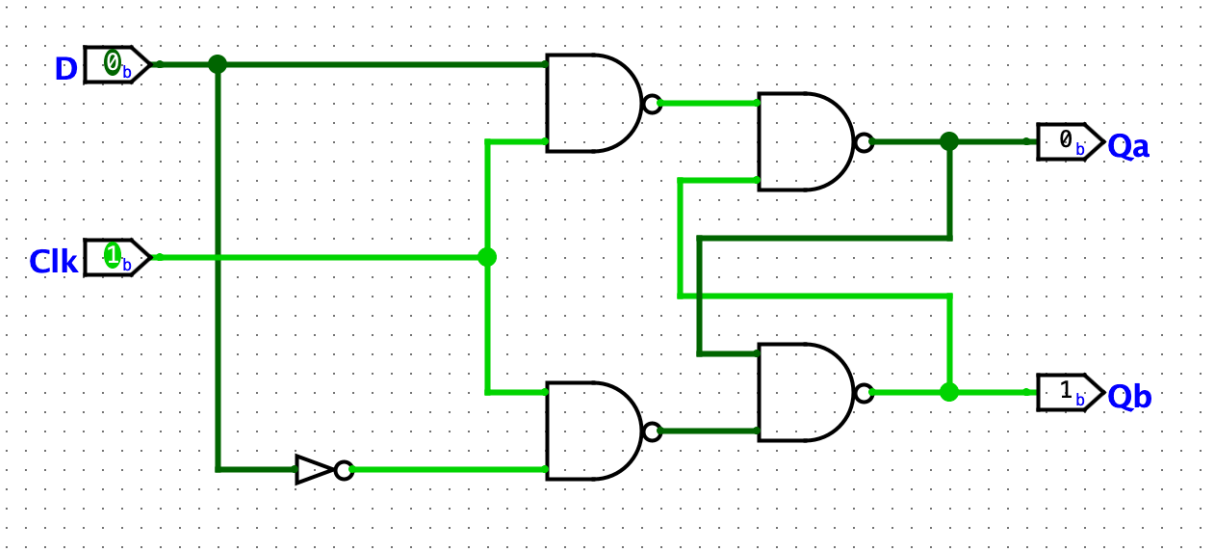
Lab 4. Latches, Flip-flops, and Registers

Student Name: Zewen Ma.

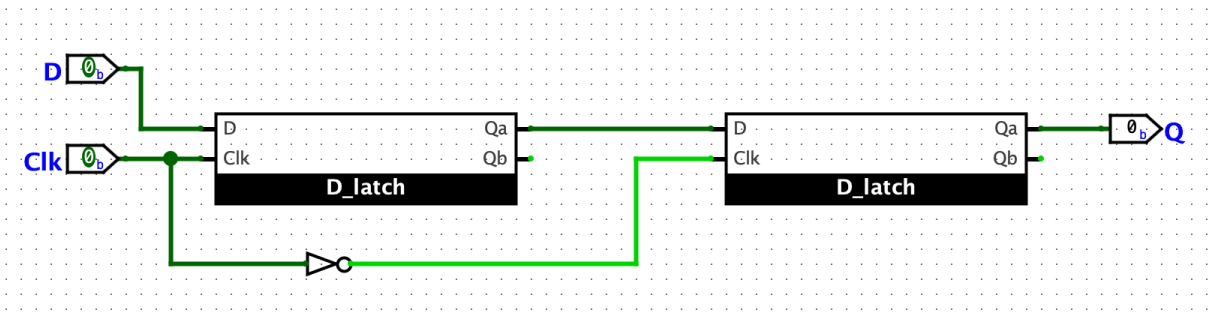
Student Number: 1005968375

Part 1:

1. Schematic of gated D latch:



Schematic of master slave flip-flop:



3. We know that, from the SR latch, the outputs of the SR latch are different when S and R are different (i.e. the are complement to each other).

As we can tell from the D latch, it directly makes 2 complement inputs. Therefore, when Clk is

first set to 0, then both $\bar{S}$ and $\bar{R}$ are 1, then after both ouput value enter the 2nd NAND Gate, there would be an error. (Because NAND outputs 1 as long as there exists a '0' input, which means that if we have a 0 input for the NAND gate, we know the output would be 1, but if we only have a 1 input, we cannot anticipate the output values.

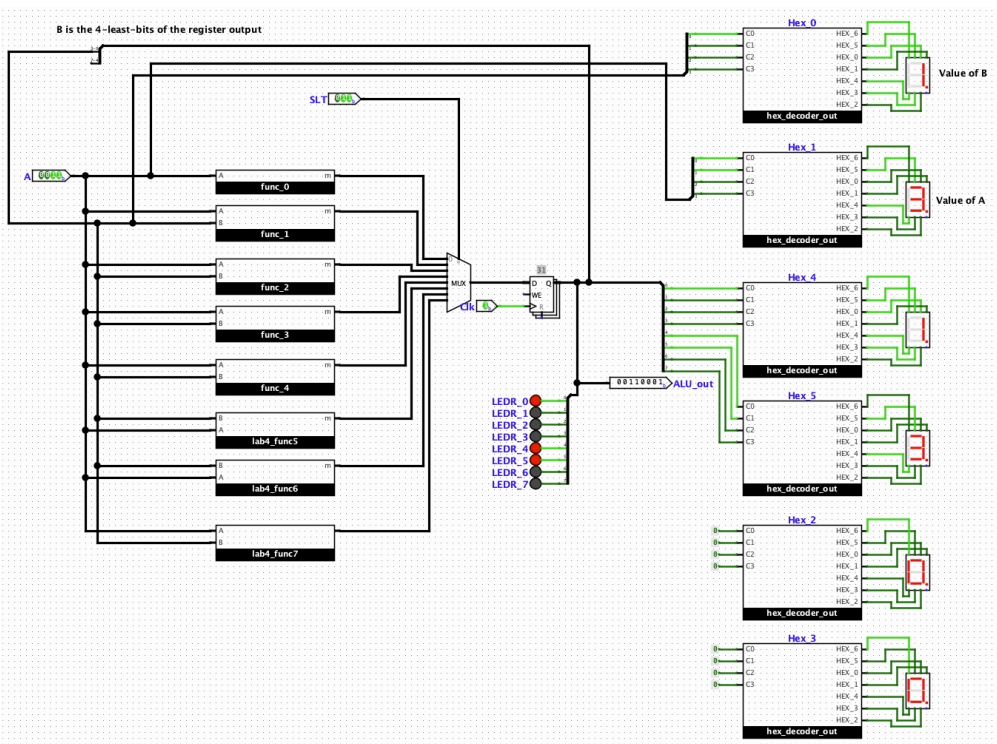
Therefore Clk=0 cannot be first tested.

When Clk=1, regardless of what D value is, the outputswill automatically generate a complement (i.e [Qa=1 and Qb=0] or [Qa=0 and Qb=1])

Then, when clk changes back to 0, the output values stores in Qa and Qb, respectively.

Part 2.

1.



2. (a). If there isn't a register, i.e B continuously is the four least-significant digits of the ALU output. As A changes, the ALU output changes immediately, where B changes immediately, which results in an infinite loop because B keeps changing.

(b). Assume A and B are both n-bit binary number, then the maximum value of them would be $2^n - 1$.

Therefore the largest value of their multiplication would be $(2^n-1)^2$. which is:

$$\begin{aligned}(2^n-1)^2 &= (2^n)^2 - 2\cdot 2^n + 1 \\ &= 2^{2n} - 2^{n+1} + 1. \\ &< 2^{2n}\end{aligned}$$

Thus the number of bits we need to store a value would be $\log_2 2^{2n} = \underline{\underline{2n}}$

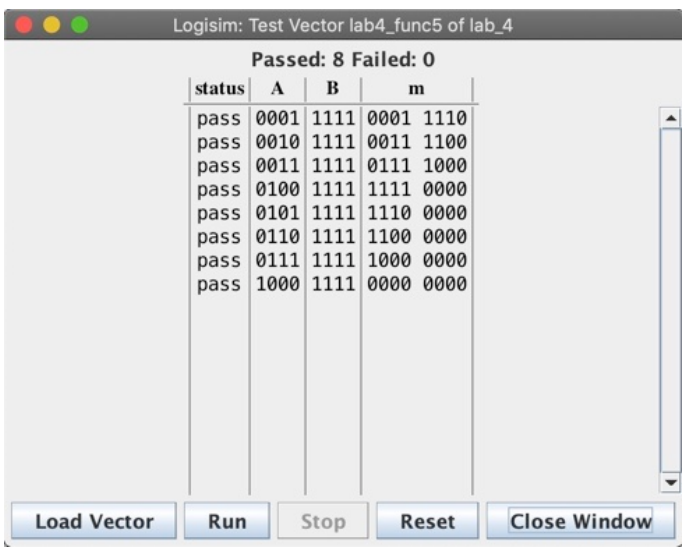
3. (a)

	A	SLT	CLK.	ALU_out.	B
func_0	0000	000	1	00000001	0001
func_1	0001	001	0	00000001	0001
	0001	001	1	00000010	0010
func_2	0001	010	0	00000010	0010
	0001	010	1	00000011	0011
func_3	1110	011	0	00000011	0011
	1110	011	1	11111101	1101

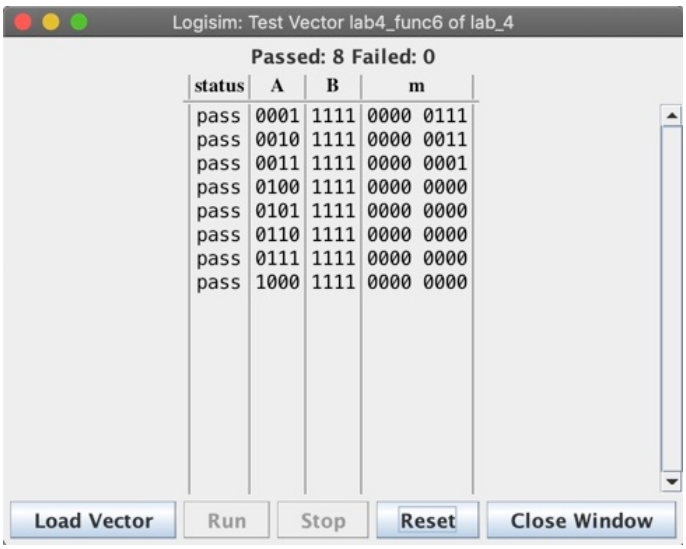
func-4	1110	100	0	111110	1101
	1110	100	1	00000001	0001
func-5	0001	101	0	00000001	0001
	0001	101	1	00000010	0010
func-6	0001	110	0	00000010	0010
	0001	110	1	00000001	0001
func-7	1111	111	0	00000001	0001
	1111	111	1	00001111	1111
	1111	111	0	00001111	1111
	1111	111	1	11100001	0001

(b). Tests for Lab4 functions:

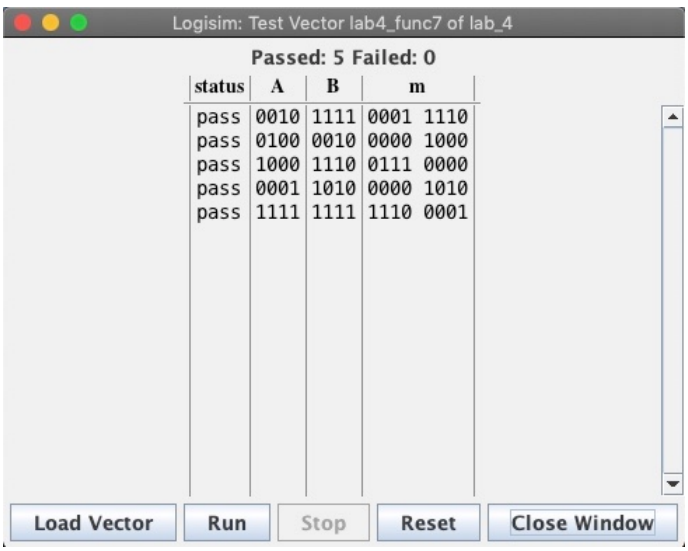
func-5:



func_6:



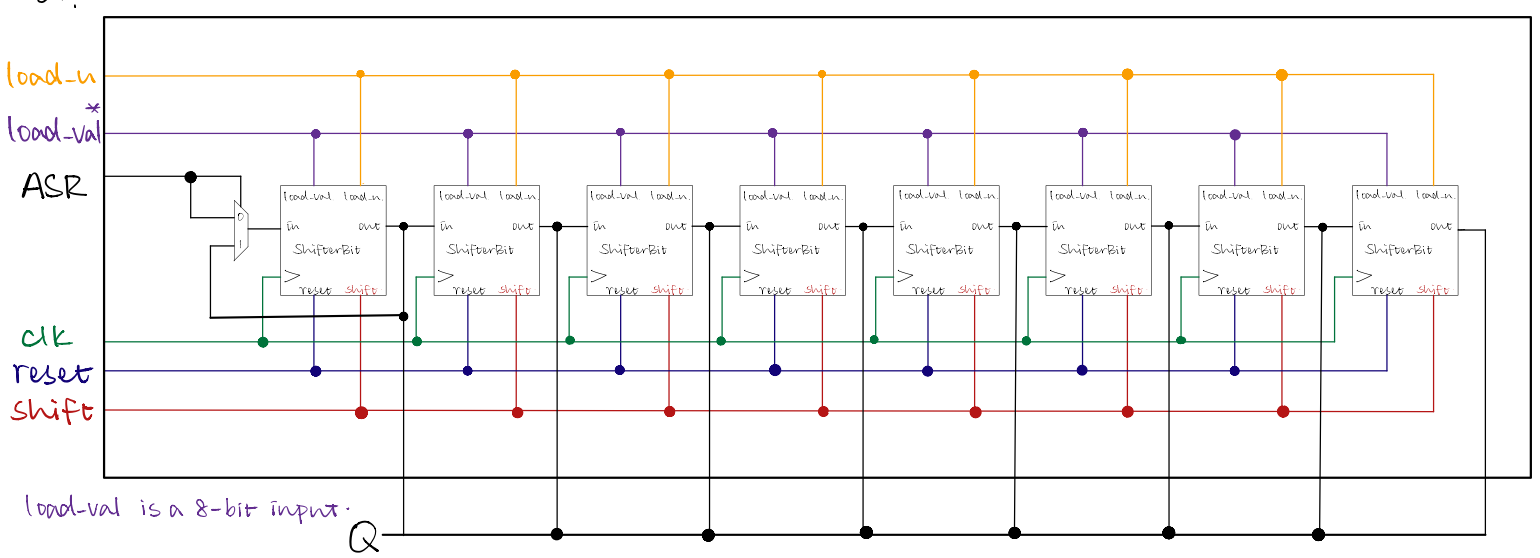
func_7.



Part 3.

1. When shift = 0. The output remains (no shifting).

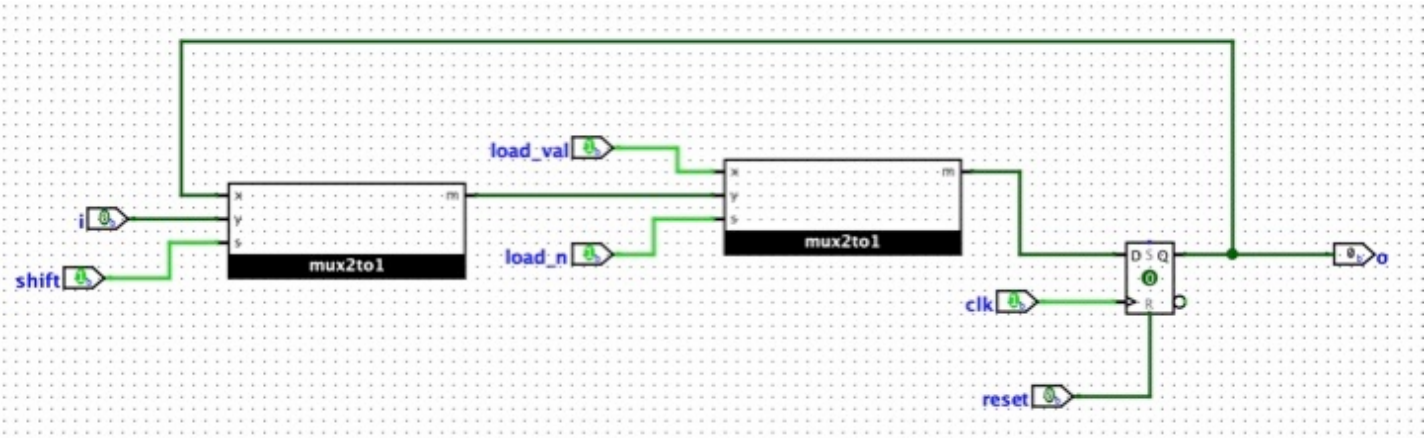
2.



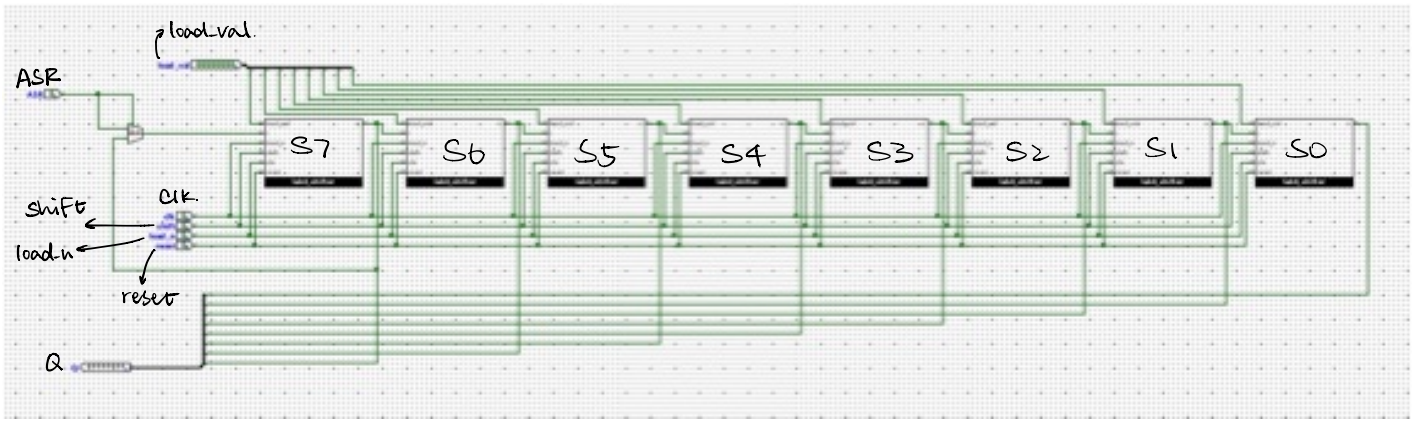
* load_val is a 8-bit input.

* Q is an 8-bit output

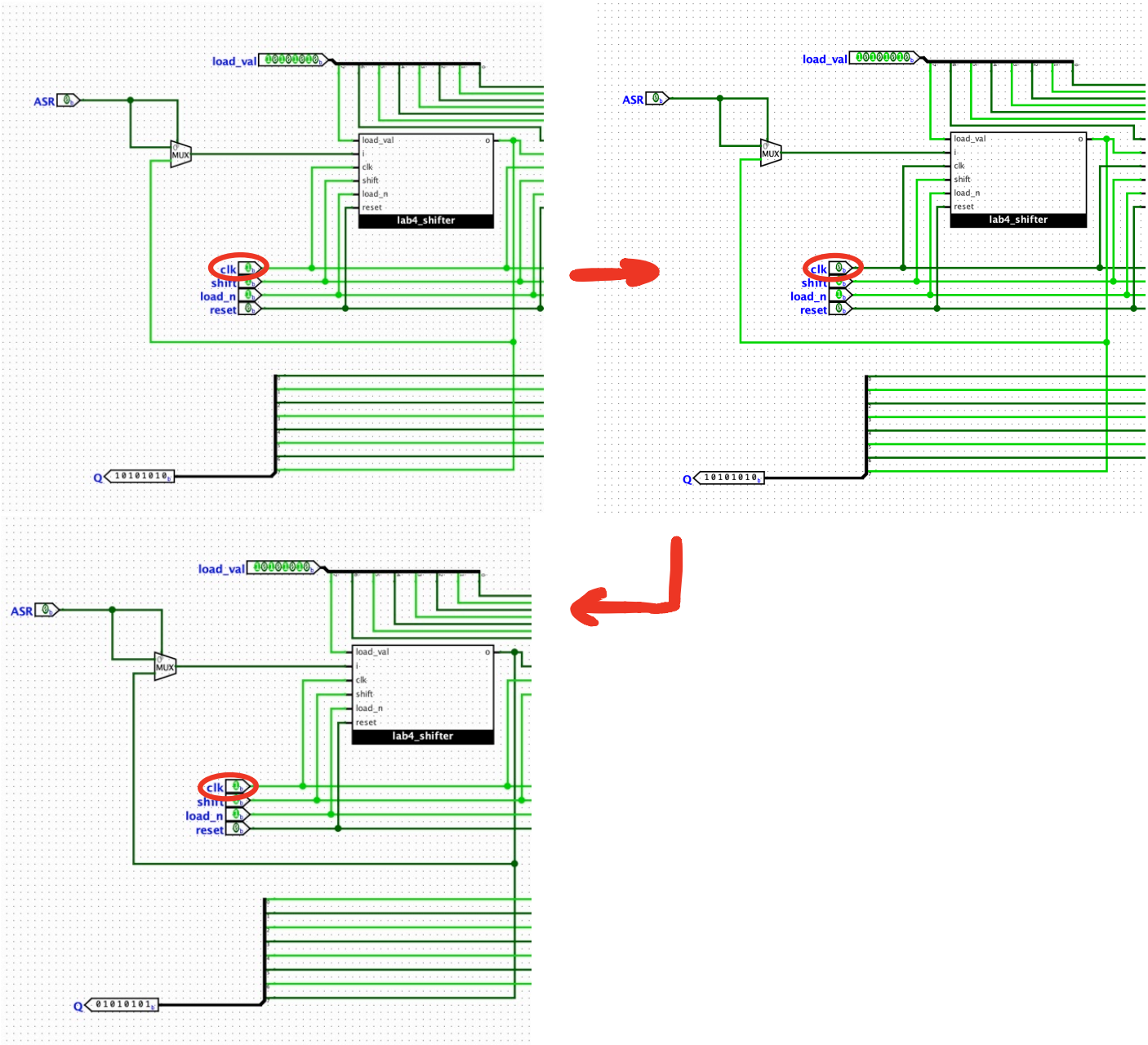
3. Single-bit shifter:



4.



5. Test where ASR=0.



After reset. Test where ASR=1.