

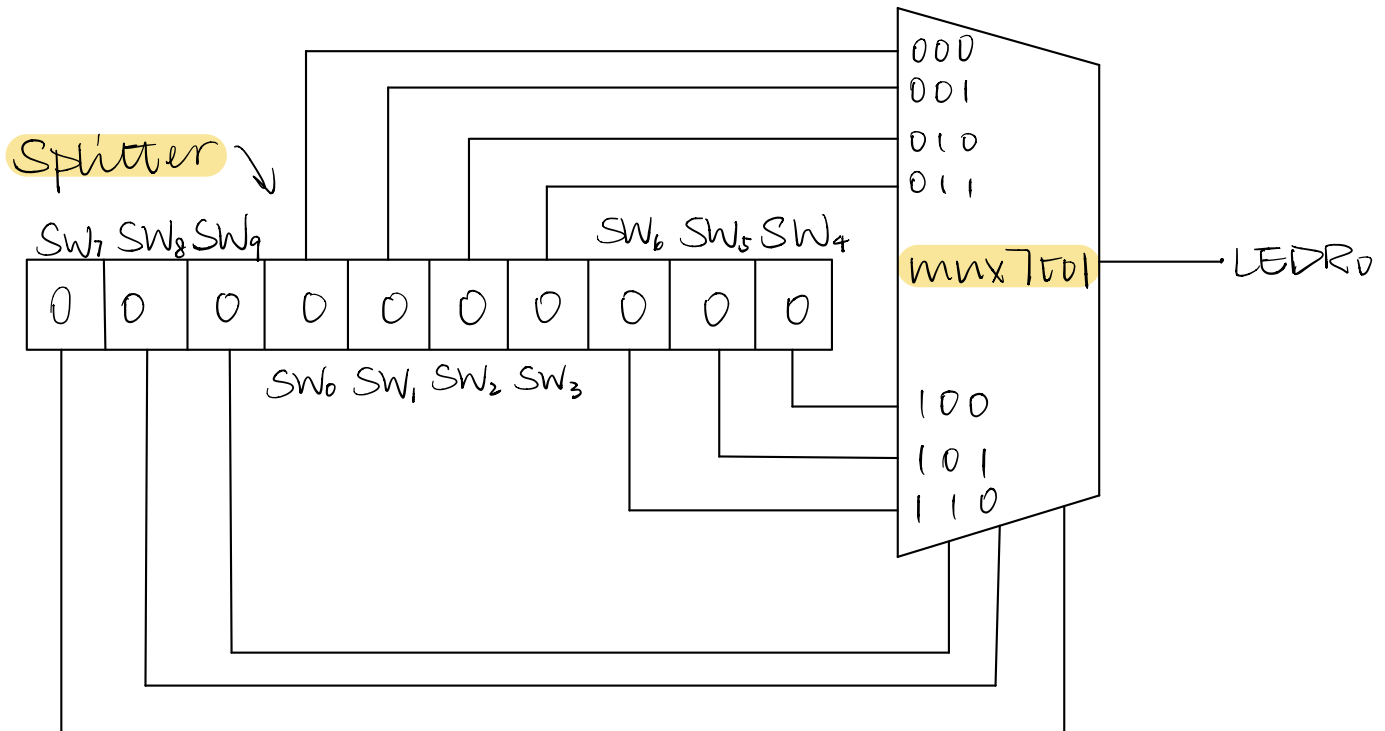
Lab 3. Splitters, Adders and ALUs.

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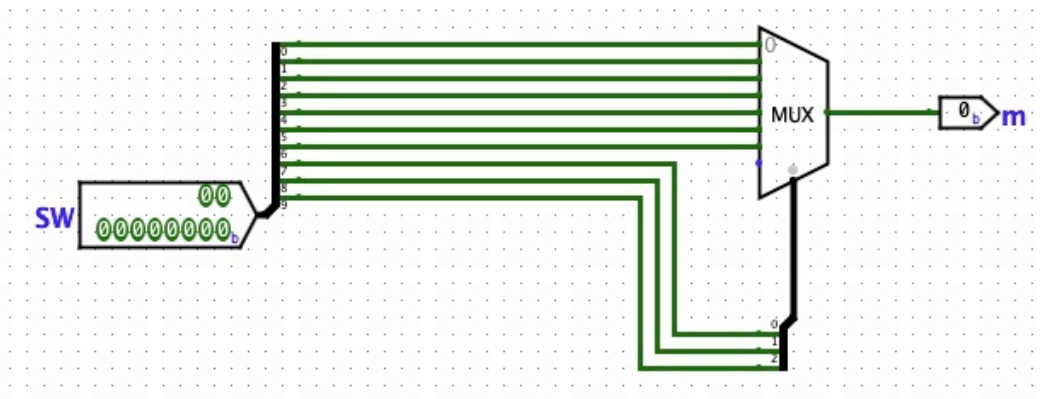
Part 1:

1. The schematic below is for the 7-to-1 multiplexer:



- (b) We need 10 multi-bit input to be provide all the inputs to the 7-to-1 multiplexer.

2. Logisim design for Question 1:



3. Here's the test result:

Logisim: Test Vector mux7to1 of Lab3

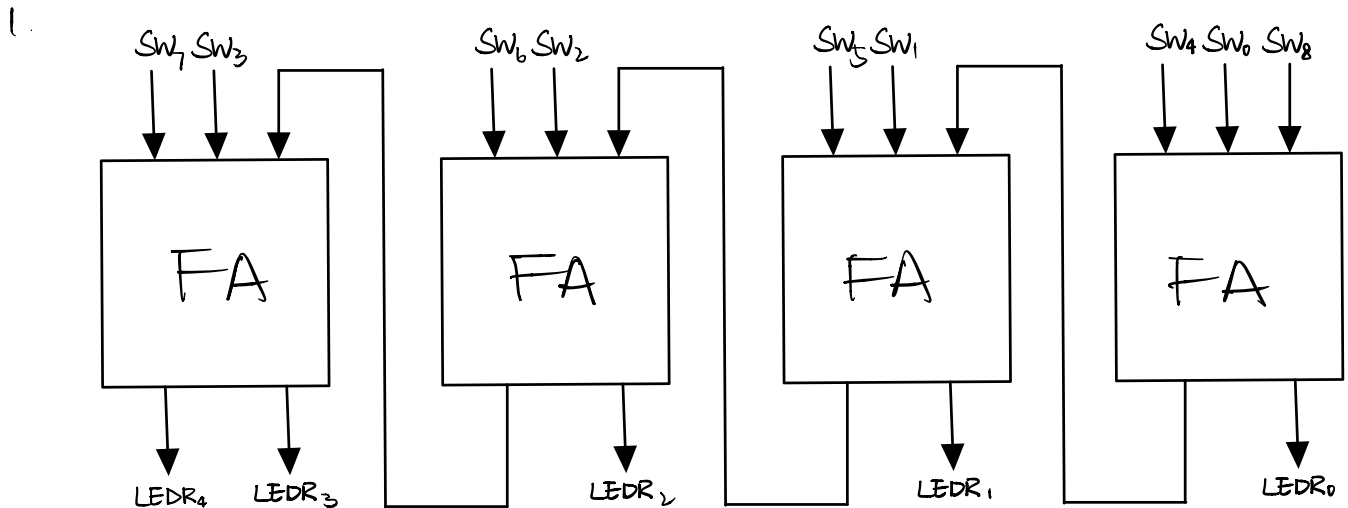
Passed: 14 Failed: 0

status	SW	m
pass	00 0000 0001	1
pass	00 0111 1110	0
pass	00 1000 0010	1
pass	00 1111 1101	0
pass	01 0000 0100	1
pass	01 0111 1011	0
pass	01 1000 1000	1
pass	01 1111 0111	0
pass	10 0001 0000	1
pass	10 0110 1111	0
pass	10 1010 0000	1
pass	10 1101 1111	0
pass	11 0100 0000	1
pass	11 0011 1111	0

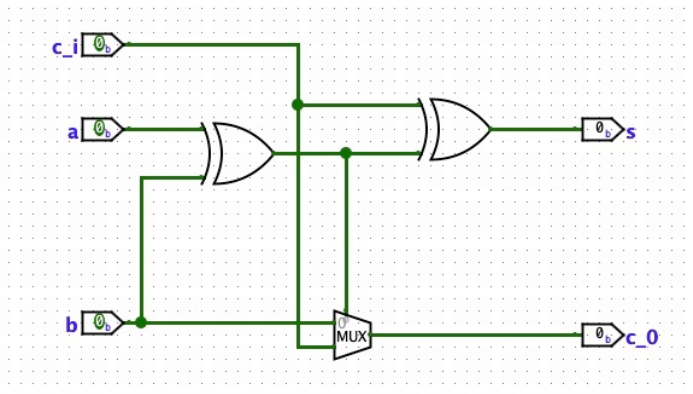
Load Vector Run Stop Reset Close Window

In this test, the columns are matching the inputs from SW₉ to SW₀. And m is the output.

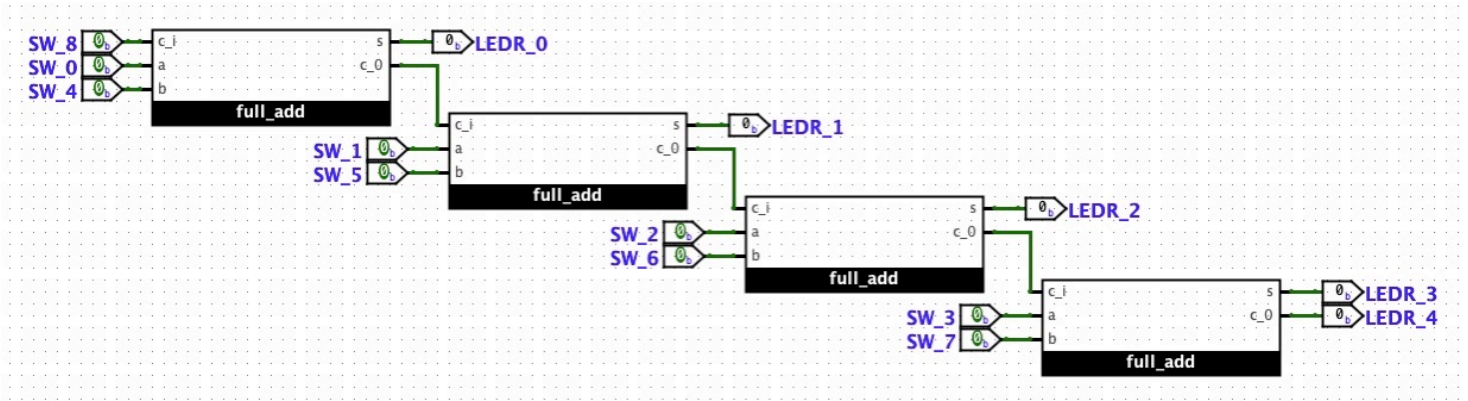
Part 2:



2. Below are the two circuits built in Logisim:



Circuit for the full adder.



Circuit for the 4-bit ripple-carry

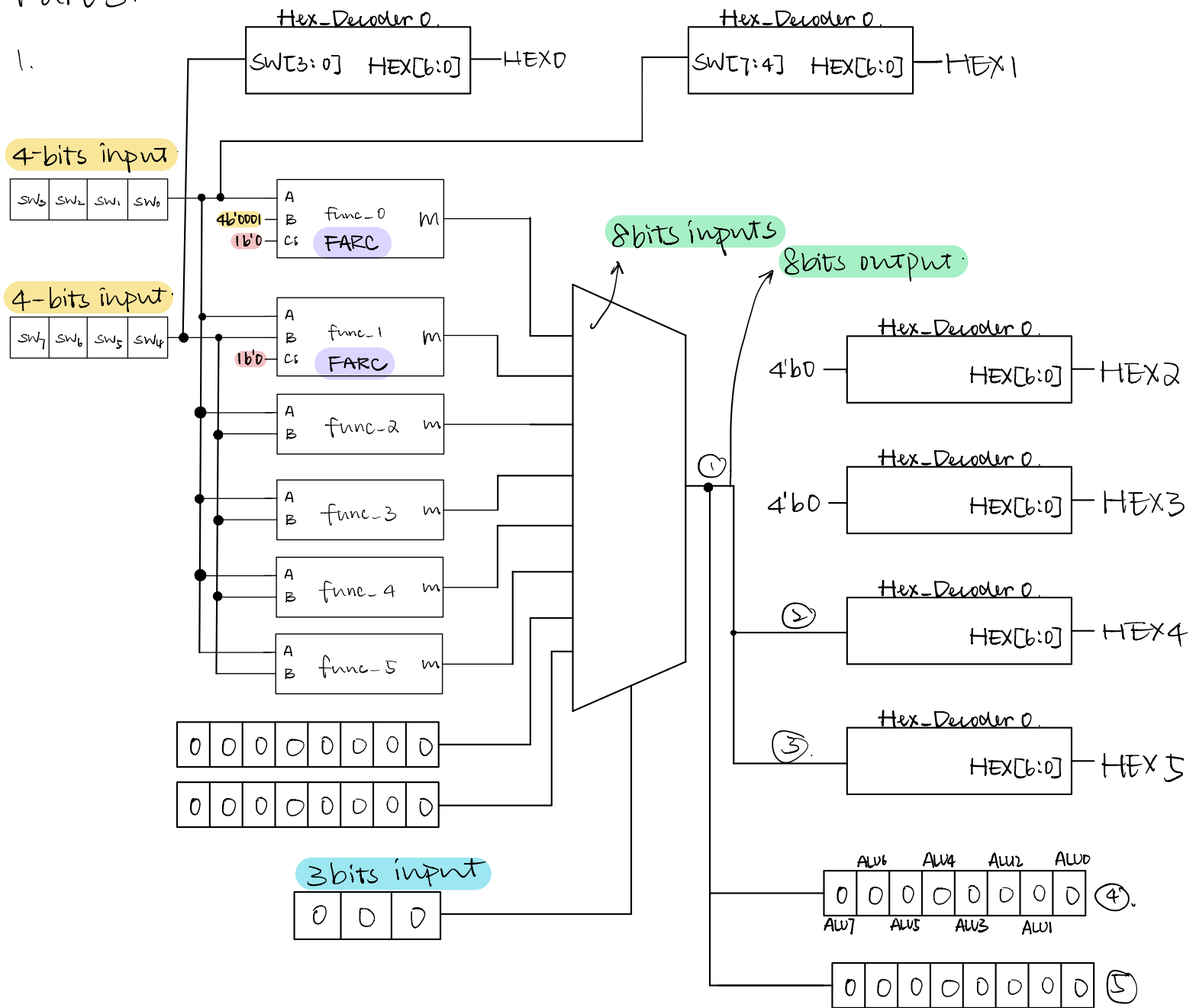
3. Test of some cases:

Logisim: Test Vector ripple_carry of Lab3										
Passed: 14 Failed: 0										
status	SW_8	SW_0	SW_4	SW_1	SW_5	SW_2	SW_6	SW_3	SW_7	LEI
pass	0	0	0	0	0	0	0	0	0	
pass	1	0	0	0	0	0	0	0	0	
pass	0	1	0	0	0	0	0	0	0	
pass	0	0	1	0	0	0	0	0	0	
pass	0	1	1	0	0	0	0	0	0	
pass	0	0	0	0	1	0	0	0	0	
pass	0	0	0	1	1	0	0	0	0	
pass	0	0	0	0	0	0	1	0	0	
pass	0	0	0	0	0	0	1	1	0	
pass	0	0	0	0	0	0	0	1	0	
pass	0	0	0	0	0	0	0	1	1	
pass	0	0	0	0	0	0	0	0	1	
pass	0	0	0	0	0	0	0	0	0	1

Load Vector Run Stop Reset Close Window

Part 3:

1.



* Note: • SLT: select bits.

• ①: ALU out

• ②: ALU out [3:0]

• ③: ALU out [7:4]

• A matches to $SW[3:0]$

• B matches to $SW[7:4]$

• ④ LEDR[7:0].

• ⑤. ALU-out: ALU output.

• HEX0: displaying B.

• HEX1: displaying A

• HEX2: displaying 0

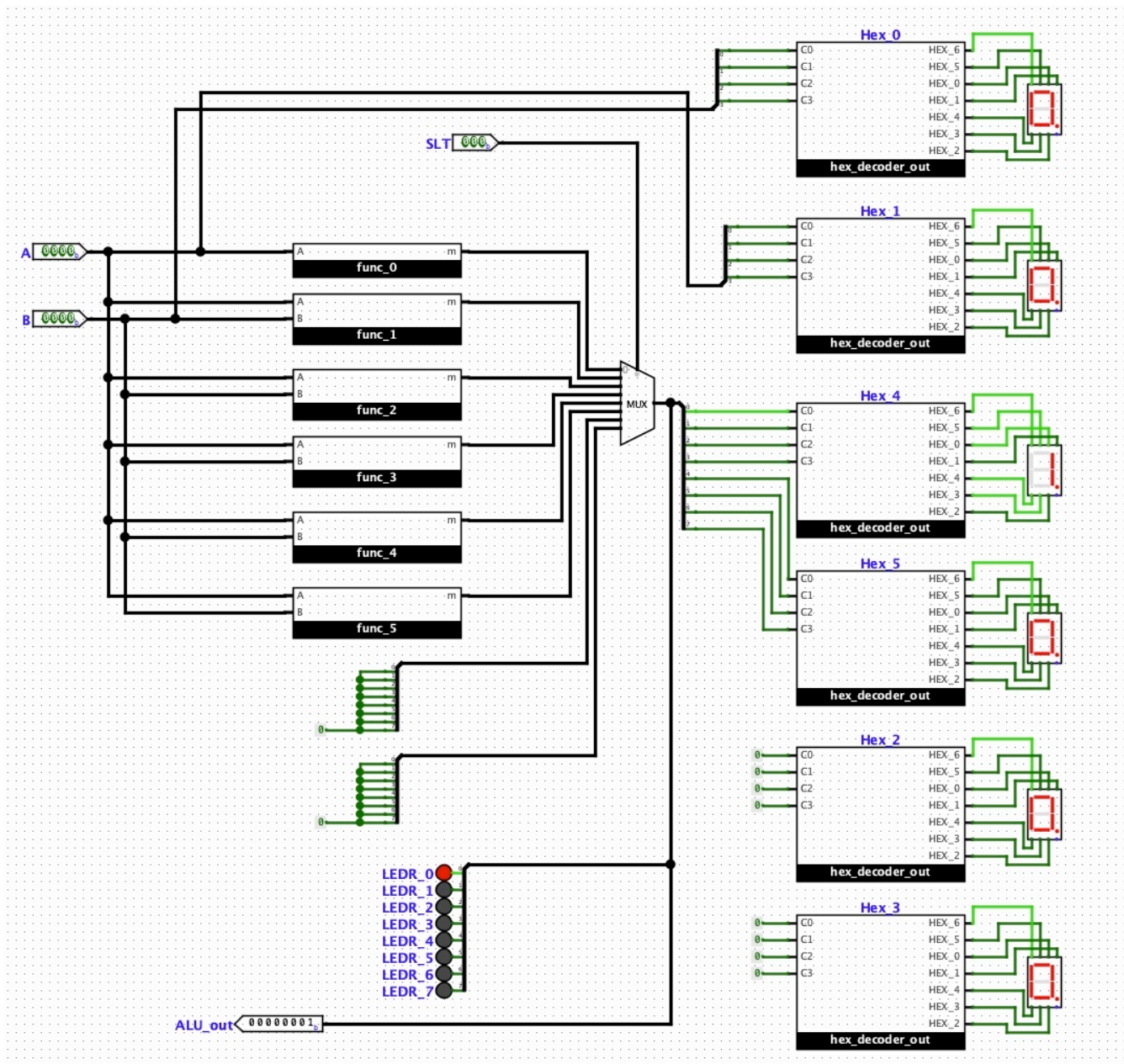
• HEX3: displaying 0

• HEX4: displaying ALU[3:0]

• HEX5: displaying ALU[7:4]

• FARC: full adder ripple carry.

2. Here are the circuit of ALU:



3. Here are the tests I made to test my ALU:

Logisim: Test Vector ALU of Lab3

Passed: 15 Failed: 0

status	A	B	SLT	ALU_out
pass	0000	0000	000	0000 0001
pass	1111	0000	000	0001 0000
pass	0000	0000	001	0000 0000
pass	1111	1111	001	0001 1110
pass	0000	0000	010	0000 0000
pass	1111	1111	010	0001 1110
pass	1010	0101	011	1111 1111
pass	1111	1110	011	1111 0001
pass	0000	0000	100	0000 0000
pass	0001	0010	100	0000 0001
pass	1001	0101	100	0000 0001
pass	1111	1111	100	0000 0001
pass	0000	0001	101	0000 0001
pass	0100	1010	101	0100 1010
pass	1111	1111	101	1111 1111

Load Vector Run Stop Reset Close Window