

Lab 2. Multiplexer, Design Hierarchy, and HEX Displays.

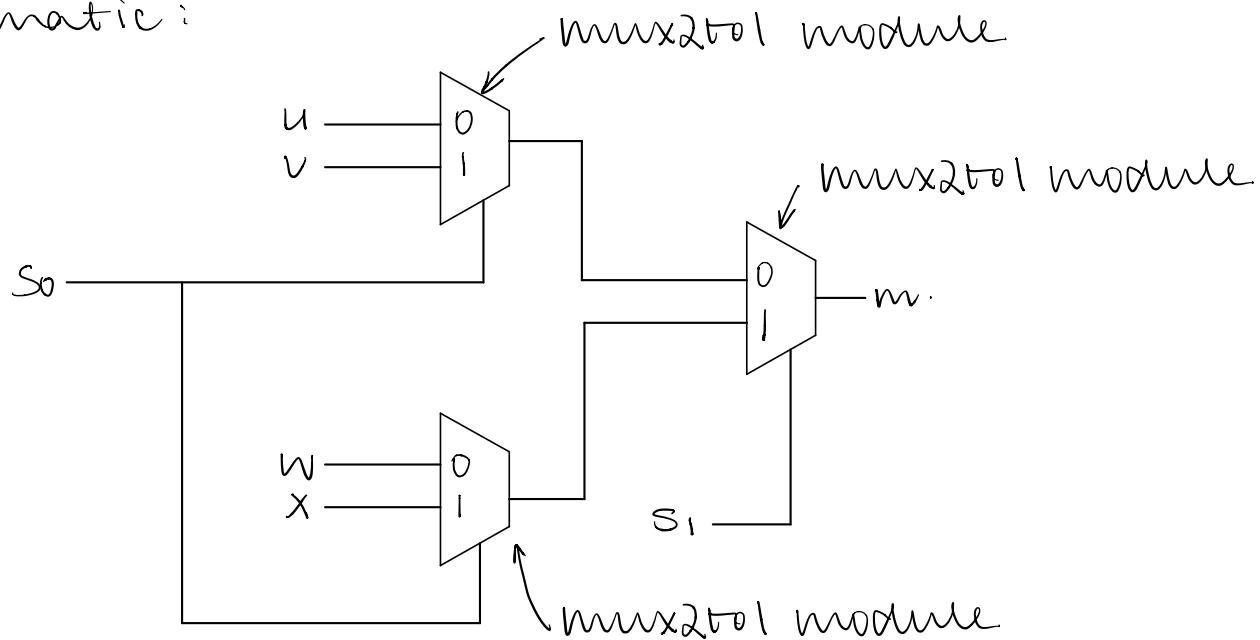
Student Name: Zewen Ma.

Student #: 1005968375.

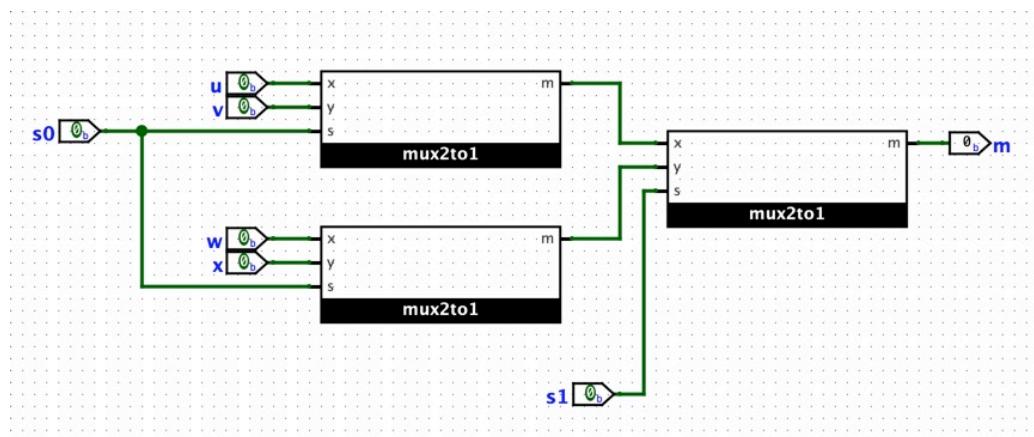
Part II.

1. Since Table 1 contains 6 variables, therefore there would be 2^6 rows.
2. Connect the mux2to1 modules to build the 4-to-1 multiplexer.

Schematic:



3. Circuit build in Logisim:



4. Test:

Logisim: Test Vector part2_module of mux

Passed: 16 Failed: 0

| status | u | v | w | x | s0 | s1 | m |
|--------|---|---|---|---|----|----|---|
| pass | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| pass | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| pass | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| pass | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| pass | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| pass | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| pass | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| pass | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| pass | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| pass | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| pass | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| pass | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| pass | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| pass | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| pass | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| pass | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

Load Vector **Run** **Stop** **Reset** **Close Window**

5. In the following DE1-SoC board, I re-labelled pins

u, v, w, x, m, s₀, s₁ as:

u → SW₀; v → SW₁; w → SW₂; x → SW₃.

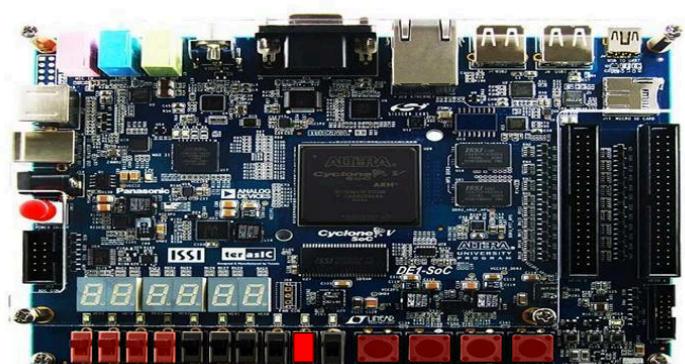
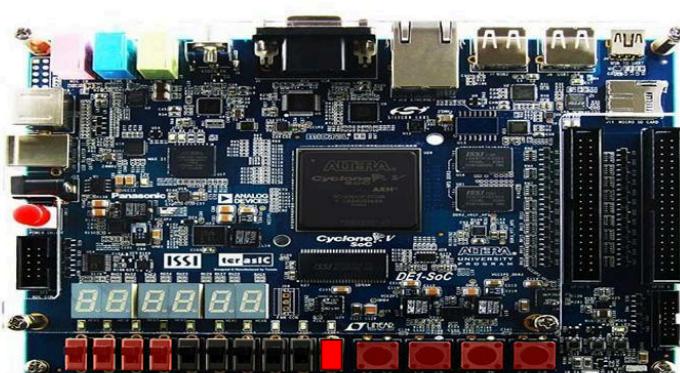
S₀ → SW; S₁ → SWq; m → LEDR₀

Below are the map of my Logisim design.

Component to FPGA board mapping

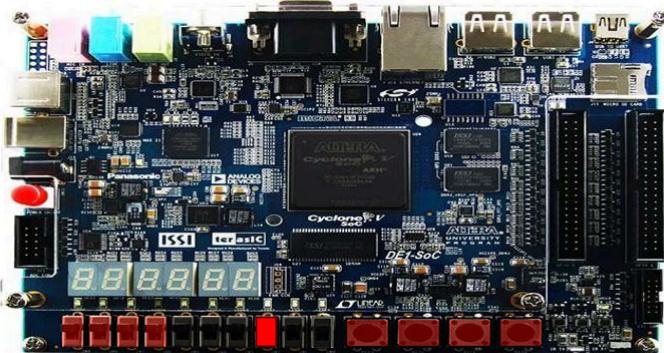
| Unmapped Components: | Mapped Components: | Command: | Unmapped Components: | Mapped Components: | Command: |
|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| SW ₀ | PIN: /LEDR_0#LEDO PIN: /SW_0#Button0 PIN: /SW_1#Button0 PIN: /SW_2#Button0 PIN: /SW_3#Button0 PIN: /SW_8#Button0 PIN: /SW_9#Button0 | Release component Release all components Load Map Save Map Cancel Done | SW ₁ | PIN: /LEDR_0#LEDO PIN: /SW_0#Button0 PIN: /SW_1#Button0 PIN: /SW_2#Button0 PIN: /SW_3#Button0 PIN: /SW_8#Button0 PIN: /SW_9#Button0 | Release component Release all components Load Map Save Map Cancel Done |

No messages



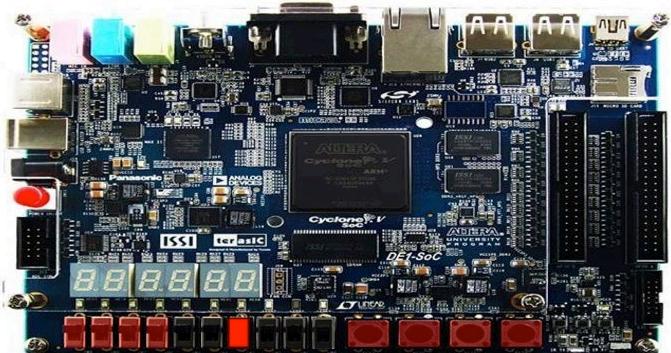
| Component to FPGA board mapping | | |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Unmapped Components: | Mapped Components: | Command: |
| | PIN: /LEDR_0#LED0 PIN: /SW_0#Button0 PIN: /SW_1#Button0 PIN: /SW_2#Button0 PIN: /SW_3#Button0 PIN: /SW_8#Button0 PIN: /SW_9#Button0 | Release component Release all components Load Map Save Map Cancel Done |
| | | 1.0x 1.5x 2.0x |

No messages



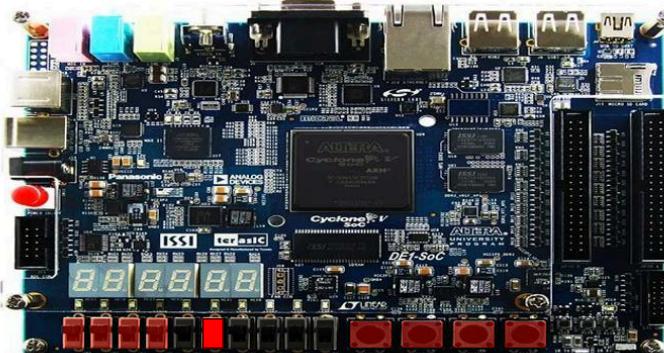
| Component to FPGA board mapping | | |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Unmapped Components: | Mapped Components: | Command: |
| | PIN: /LEDR_0#LED0 PIN: /SW_0#Button0 PIN: /SW_1#Button0 PIN: /SW_2#Button0 PIN: /SW_3#Button0 PIN: /SW_8#Button0 PIN: /SW_9#Button0 | Release component Release all components Load Map Save Map Cancel Done |
| | | 1.0x 1.5x 2.0x |

No messages



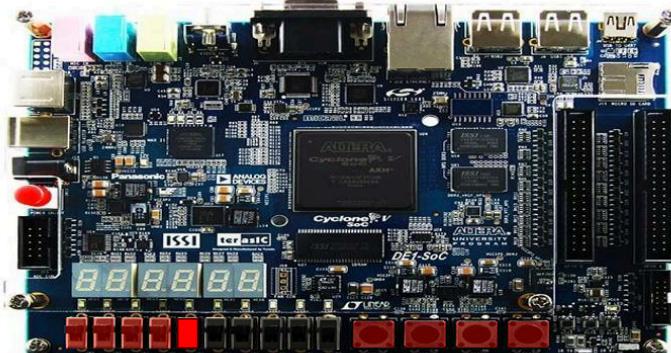
| Component to FPGA board mapping | | |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Unmapped Components: | Mapped Components: | Command: |
| | PIN: /LEDR_0#LED0 PIN: /SW_0#Button0 PIN: /SW_1#Button0 PIN: /SW_2#Button0 PIN: /SW_3#Button0 PIN: /SW_8#Button0 PIN: /SW_9#Button0 | Release component Release all components Load Map Save Map Cancel Done |
| | | 1.0x 1.5x 2.0x |

No messages



| Component to FPGA board mapping | | |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Unmapped Components: | Mapped Components: | Command: |
| | PIN: /LEDR_0#LED0 PIN: /SW_0#Button0 PIN: /SW_1#Button0 PIN: /SW_2#Button0 PIN: /SW_3#Button0 PIN: /SW_8#Button0 PIN: /SW_9#Button0 | Release component Release all components Load Map Save Map Cancel Done |
| | | 1.0x 1.5x 2.0x |

No messages



| Component to FPGA board mapping | | |
|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Unmapped Components: | Mapped Components: | Command: |
| | PIN: /LEDR_0#LED0 PIN: /SW_0#Button0 PIN: /SW_1#Button0 PIN: /SW_2#Button0 PIN: /SW_3#Button0 PIN: /SW_8#Button0 PIN: /SW_9#Button0 | Release component Release all components Load Map Save Map Cancel Done |
| | | 1.0x 1.5x 2.0x |

No messages



Part 3:

1 Part 3 Truth Table:

| C ₃ | C ₂ | C ₁ | C ₀ | HEX0 | HEX1 | HEX2 | HEX3 | HEX4 | HEX5 | HEX6 | Character |
|----------------|----------------|----------------|----------------|------|------|------|------|------|------|------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 3 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 6 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 9 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | A |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | b |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | C |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | d |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | E |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | F |

Using the truth table, we can generate the Karnaugh maps for HEX0-6:

Karnaugh map for HEX0:

| | $\bar{C}_1\bar{C}_0$ | \bar{C}_1C_0 | C_1C_0 | $C_1\bar{C}_0$ |
|----------------------|----------------------|----------------|----------|----------------|
| $\bar{C}_3\bar{C}_2$ | 0 | 1 | 0 | 0 |
| \bar{C}_3C_2 | 1 | 0 | 0 | 0 |
| C_3C_2 | 0 | 1 | 0 | 0 |
| $C_3\bar{C}_2$ | 0 | 0 | 1 | 0 |

Expression: $\bar{C}_3\bar{C}_2\bar{C}_1\bar{C}_0 + \bar{C}_3C_2\bar{C}_1\bar{C}_0 + C_3C_2\bar{C}_1C_0 + C_3\bar{C}_2C_1C_0$.

Karnaugh map for HEX1:

| | $\bar{C}_1\bar{C}_0$ | \bar{C}_1C_0 | C_1C_0 | $C_1\bar{C}_0$ |
|----------------------|----------------------|----------------|----------|----------------|
| $\bar{C}_3\bar{C}_2$ | 0 | 0 | 0 | 0 |
| \bar{C}_3C_2 | 0 | 1 | 0 | 1 |
| C_3C_2 | 1 | 0 | 1 | 1 |
| $C_3\bar{C}_2$ | 0 | 0 | 1 | 0 |

Expression: $C_3C_2\bar{C}_0 + C_3C_1C_0 + C_3\bar{C}_1\bar{C}_0 + \bar{C}_3C_2\bar{C}_1C_0$

Karnaugh map for HEX2:

| | $\bar{C}_1\bar{C}_0$ | \bar{C}_1C_0 | C_1C_0 | $C_1\bar{C}_0$ |
|----------------------|----------------------|----------------|----------|----------------|
| $\bar{C}_3\bar{C}_2$ | 0 | 0 | 0 | 1 |
| \bar{C}_3C_2 | 0 | 0 | 0 | 0 |
| C_3C_2 | 1 | 0 | 1 | 1 |
| $C_3\bar{C}_2$ | 0 | 0 | 0 | 0 |

Expression: $C_3C_2C_1 + C_3\bar{C}_2\bar{C}_0 + \bar{C}_3\bar{C}_2C_1\bar{C}_0$

Karnaugh map for HEX 3:

| | $\bar{C}_1\bar{C}_0$ | \bar{C}_1C_0 | C_1C_0 | $C_1\bar{C}_0$ |
|----------------------|----------------------|----------------|----------|----------------|
| $\bar{C}_3\bar{C}_2$ | 0 | 1 | 0 | 0 |
| \bar{C}_3C_2 | 1 | 0 | 1 | 0 |
| C_3C_2 | 0 | 0 | 1 | 0 |
| $C_3\bar{C}_2$ | 0 | 1 | 0 | 1 |

Expression: $\bar{C}_2\bar{C}_1C_0 + C_2C_1C_0 + \bar{C}_3C_2\bar{C}_1\bar{C}_0 + C_3\bar{C}_2C_1\bar{C}_0$

Karnaugh map for HEX 4:

| | $\bar{C}_1\bar{C}_0$ | \bar{C}_1C_0 | C_1C_0 | $C_1\bar{C}_0$ |
|----------------------|----------------------|----------------|----------|----------------|
| $\bar{C}_3\bar{C}_2$ | 0 | 1 | 1 | 0 |
| \bar{C}_3C_2 | 1 | 1 | 1 | 0 |
| C_3C_2 | 0 | 0 | 0 | 0 |
| $C_3\bar{C}_2$ | 0 | 1 | 0 | 0 |

Expression: $\bar{C}_3C_0 + \bar{C}_3C_2\bar{C}_1 + \bar{C}_2\bar{C}_1C_0$.

Karnaugh map for HEX 5:

| | $\bar{C}_1\bar{C}_0$ | \bar{C}_1C_0 | C_1C_0 | $C_1\bar{C}_0$ |
|----------------------|----------------------|----------------|----------|----------------|
| $\bar{C}_3\bar{C}_2$ | 0 | 1 | 1 | 1 |
| \bar{C}_3C_2 | 0 | 0 | 1 | 0 |
| C_3C_2 | 0 | 1 | 0 | 0 |
| $C_3\bar{C}_2$ | 0 | 0 | 0 | 0 |

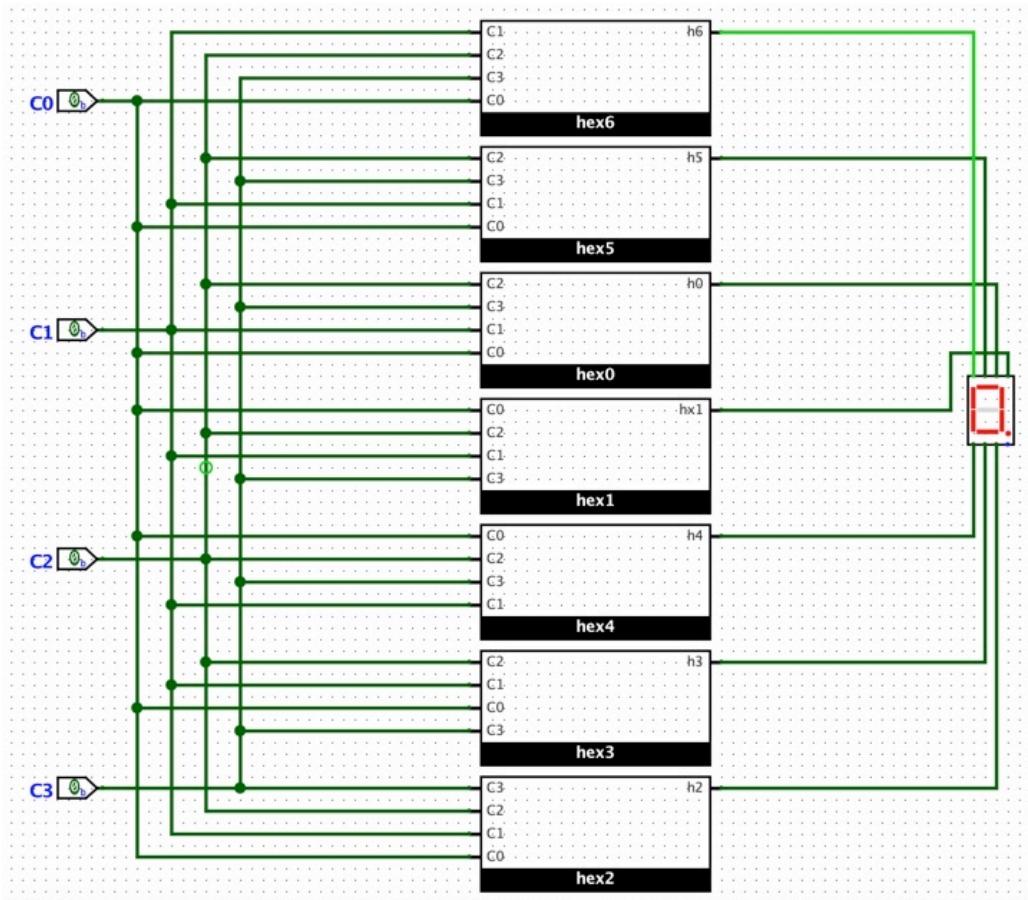
Expression: $\bar{C}_3\bar{C}_2C_0 + \bar{C}_3\bar{C}_2C_1 + \bar{C}_3C_1C_0 + C_3C_2\bar{C}_1C_0$

Karnaugh map for HEX 6:

| | $\bar{C}_1 \bar{C}_0$ | $\bar{C}_1 C_0$ | $C_1 \bar{C}_0$ | $C_1 C_0$ |
|-----------------------|-----------------------|-----------------|-----------------|-----------|
| $\bar{C}_3 \bar{C}_2$ | 1 | 1 | 0 | 0 |
| $\bar{C}_3 C_2$ | 0 | 0 | 1 | 0 |
| $C_3 \bar{C}_2$ | 1 | 0 | 0 | 0 |
| $C_3 C_2$ | 0 | 0 | 0 | 0 |

Expression: $\bar{C}_3 \bar{C}_2 \bar{C}_1 + \bar{C}_3 C_2 C_1 \bar{C}_0 + C_3 \bar{C}_2 \bar{C}_1 \bar{C}_0$

2. Here's the 7-segment decoder I built. Since C_3, C_2, C_1, C_0 are all low and since the 7-seg display when DE1 is active low, it displays 0. [In my lab project I set it as active low]



3. The following screen shots are my test for my 7-seg:

