

# Lab 1. Building Circuits using Logisim Evolution.

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Part 1: Given the following Boolean function, which is a logic expression for a 2-to-1 multiplexer:

$$f = xs' + ys$$

Performing:

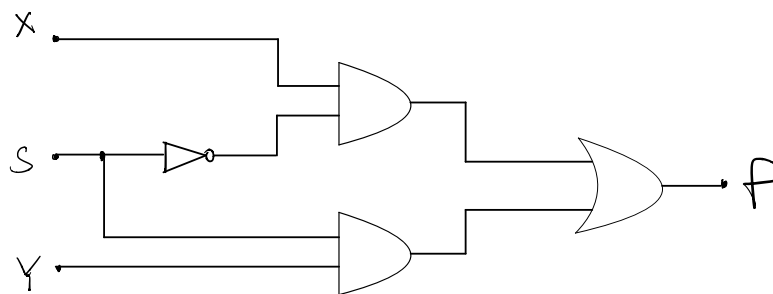
1. Draw the gate diagram using the AND, OR, and NOT gates.

— We express the function using logic words:

$$f = (x \text{ AND } (\text{NOT } s)) \text{ OR } (y \text{ AND } s)$$

Therefore, according to the expression above,

we can draw:



2. Truth Table.

x	s	y	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Part 2: Given the following Boolean expression:

$$f = (a+b)' + cb'$$

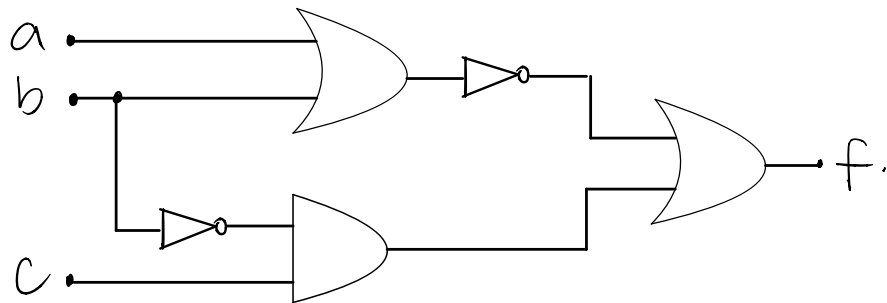
Performing:

1. Draw the gate diagram using the AND, OR and NOT gates.

— We express the function using logic words:

$$f = (\text{NOT}(a \text{ OR } b)) \text{ OR } (c \text{ AND } (\text{NOT } b))$$

Therefore, according to the expression above, we can draw:



2. Truth Table:

a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

3. Yes, there is a cheaper implementation for the design that use fewer gates:

$$f = (a+b)' + cb'$$

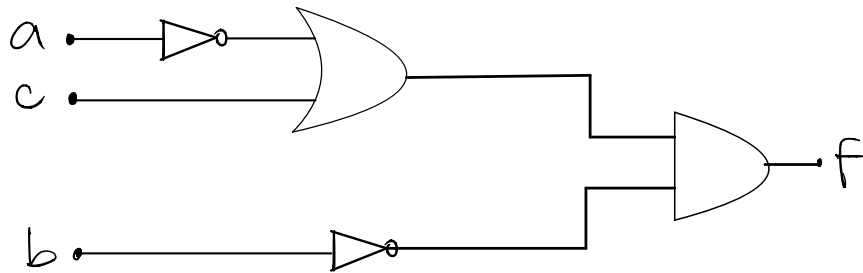
$$= (a'b') + cb' \quad \left( \begin{array}{l} \text{Since we know } \text{NOT}(a \text{ OR } b) \text{ has the} \\ \text{same output as } (\text{NOT } a) \text{ AND } (\text{NOT } b) \end{array} \right)$$

$$= b'(a'+c)$$

Therefore  $f = b'(a'+c)$  i.e

$$f = (\text{NOT } b) \text{ AND } ((\text{NOT } a) \text{ OR } c)$$

- According to the expression above, we can draw:

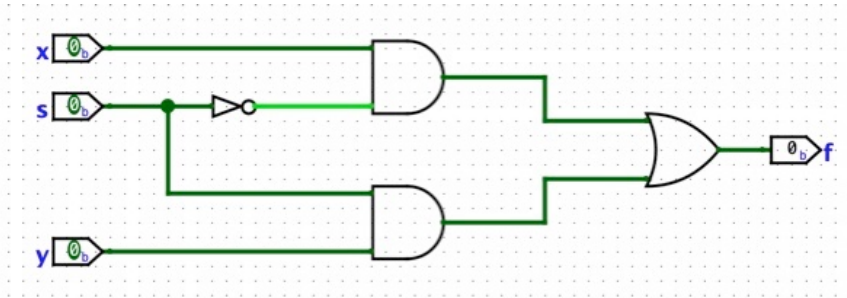


- Truth table:

a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

# Part 3. Circuits from Part 1 and Part 2 implemented in Logisim and their test result.

①. Circuit from Part 1 and its test result.



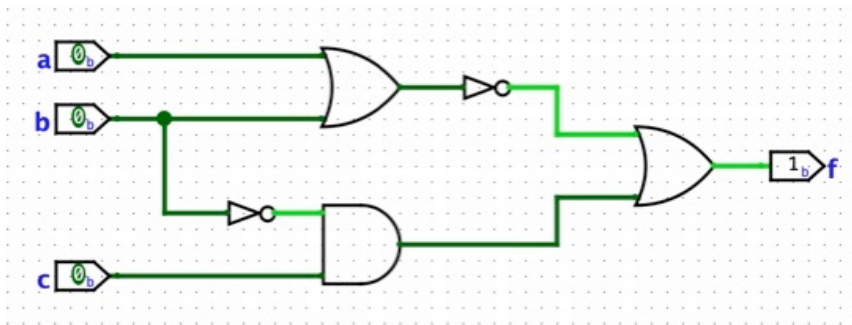
Logisim: Test Vector main of part1

Passed: 8 Failed: 0

status	x	s	y	f
pass	0	0	0	0
pass	0	0	1	0
pass	0	1	0	0
pass	0	1	1	1
pass	1	0	0	1
pass	1	0	1	1
pass	1	1	0	0
pass	1	1	1	1

Load Vector Run Stop Reset Close Window

②. Circuit from Part 2 and its test result.



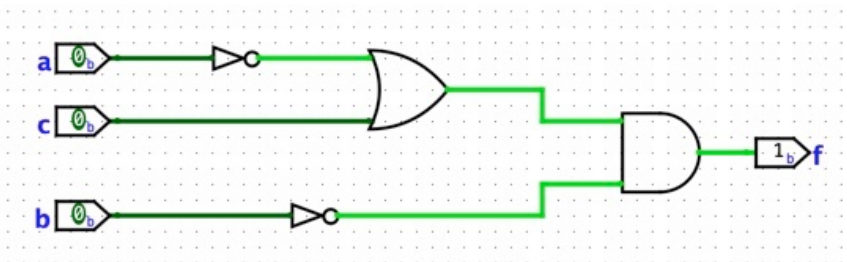
Logisim: Test Vector main of Untitled

Passed: 8 Failed: 0

status	a	b	c	f
pass	0	0	0	1
pass	0	0	1	1
pass	0	1	0	0
pass	0	1	1	0
pass	1	0	0	0
pass	1	0	1	1
pass	1	1	0	0
pass	1	1	1	0

Load Vector Run Stop Reset Close Window

③. Cheap Implementation of Circuit in Part 2. and its test result.



Logisim: Test Vector main of Untitled

Passed: 8 Failed: 0

status	a	b	c	f
pass	0	0	0	1
pass	0	0	1	1
pass	0	1	0	0
pass	0	1	1	0
pass	1	0	0	0
pass	1	0	1	1
pass	1	1	0	0
pass	1	1	1	0

Load Vector Run Stop Reset Close Window