Lab 5.

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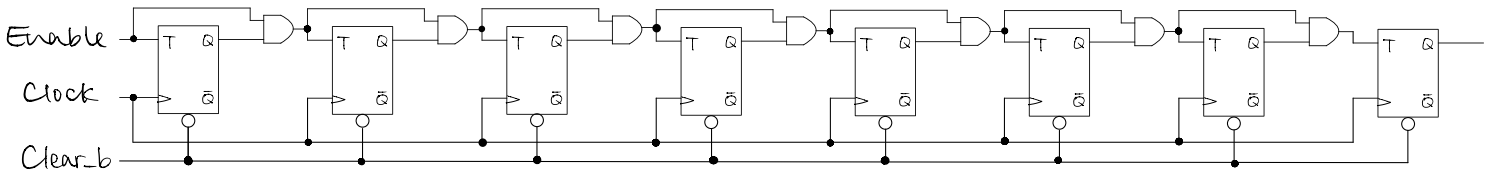
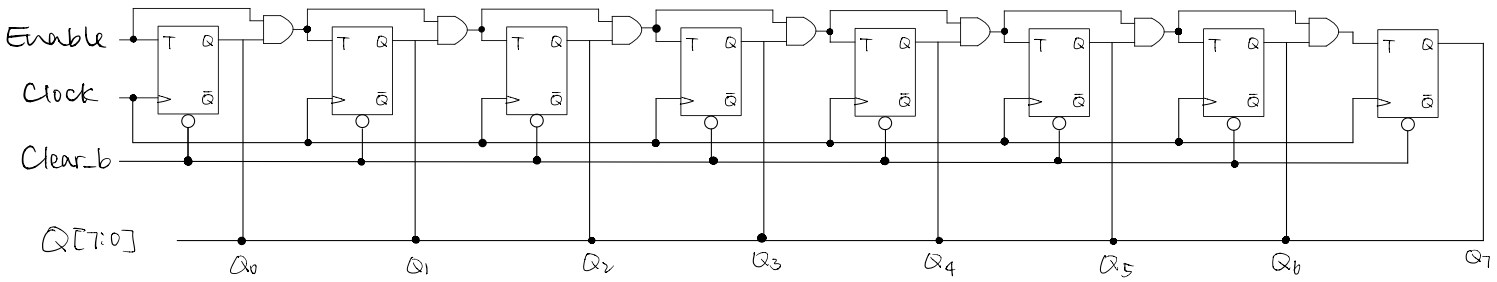
Part 1.

1. Schematic of a 8-bit counter:

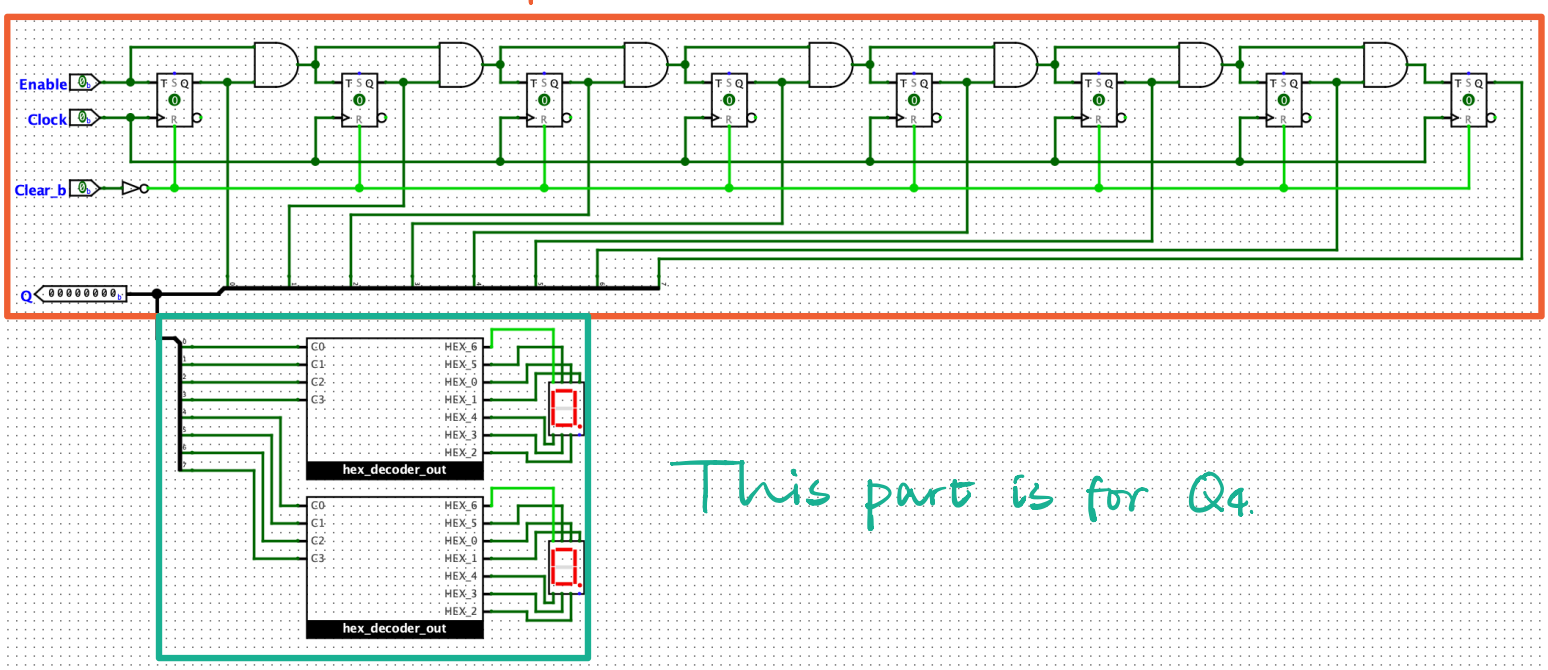


2.



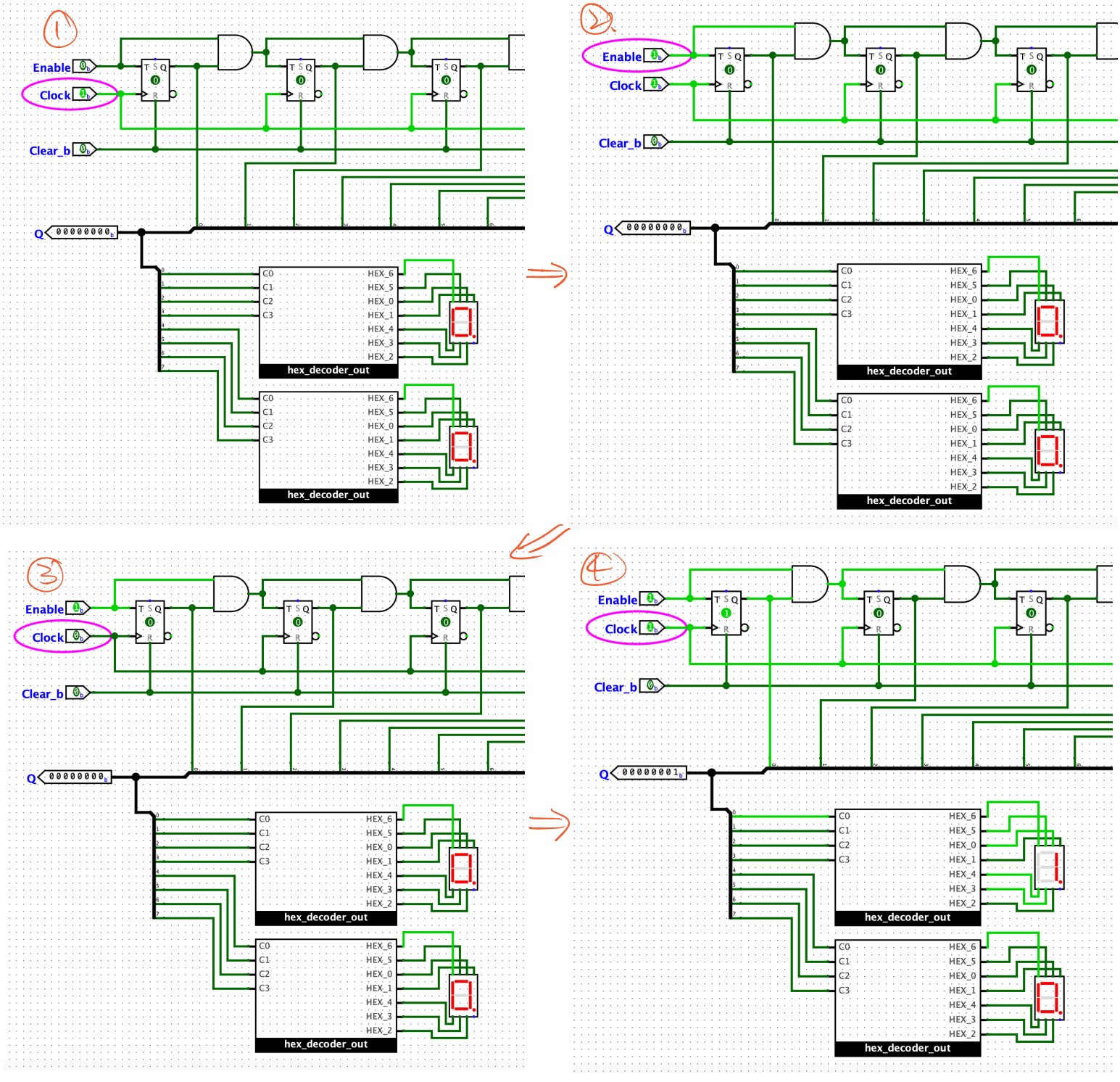
3, 4.

this part is for Q3



This part is for Q4.

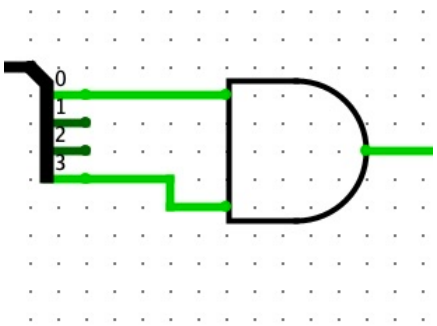
5. Test:


1
2
3
4
Enable
Clock
Clear_b
Q
00000000
00000001
T S Q
R
C0
C1
C2
C3
HEX_6
HEX_5
HEX_0
HEX_1
HEX_4
HEX_3
HEX_2
hex_decoder_out

Part 2.

A1. Since the counter has only 4 bits, adding 1 to 1111 would result in 0000, where we are getting back to the default position.

A2. Since 9=1001 in binary, I just disconnect the 2 middle inputs, therefore the AND gate outputs 1 when counting to 1001 (As the pic shown below) Then the output of the OR gate becomes 1, which loads the value [M1].



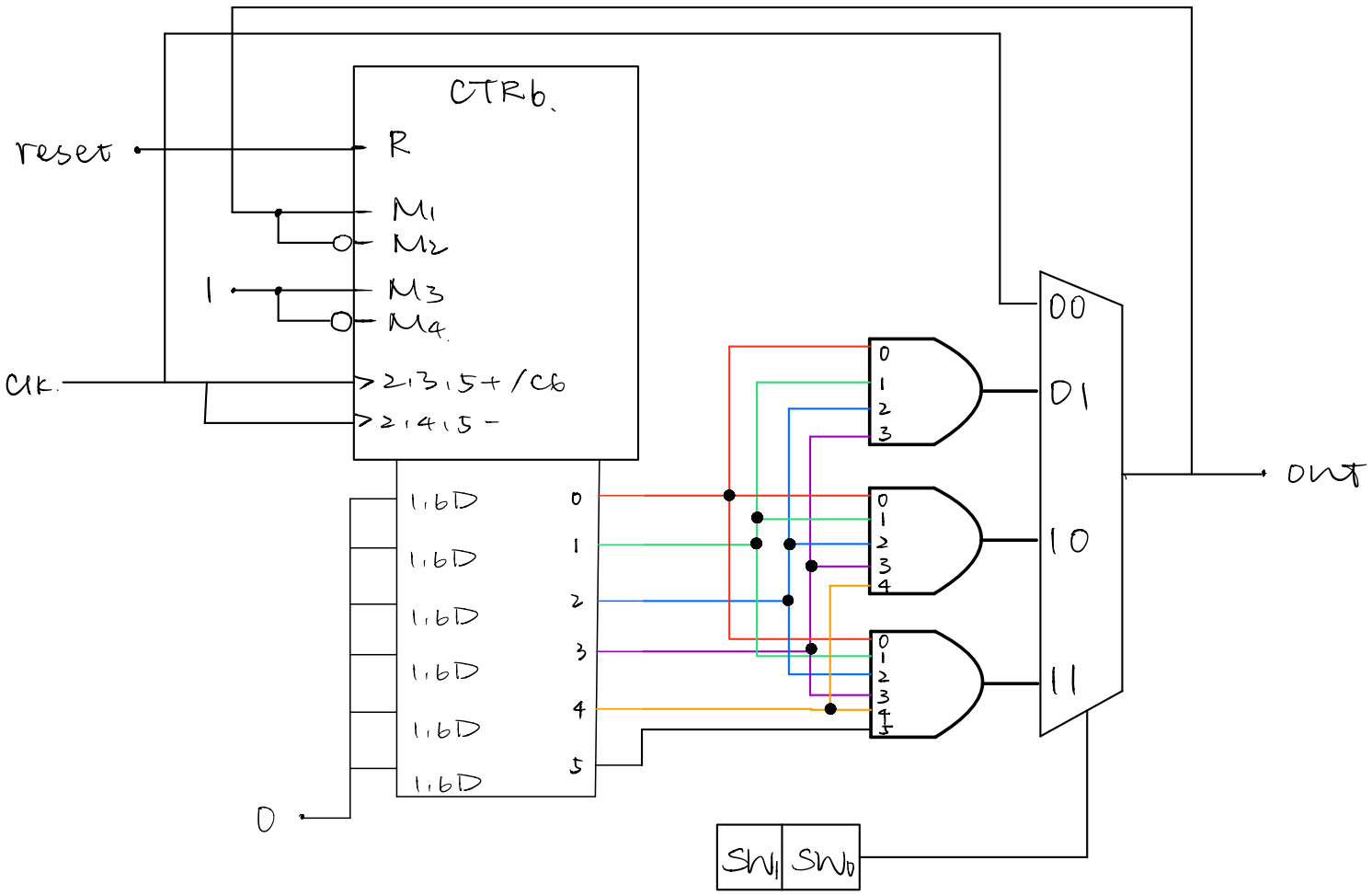
A3. In our lab, the "Action On Overflow" attribute of the counter is the behaviour when the counter attempts to increment beyond the maximum value. Our action in this lab is "Wrap around", which is: The next value would be 0 if the circuit is incrementing.

A4: How large a counter would be required to count 50 million clock cycles?

How many bits would you need to represent such a value?

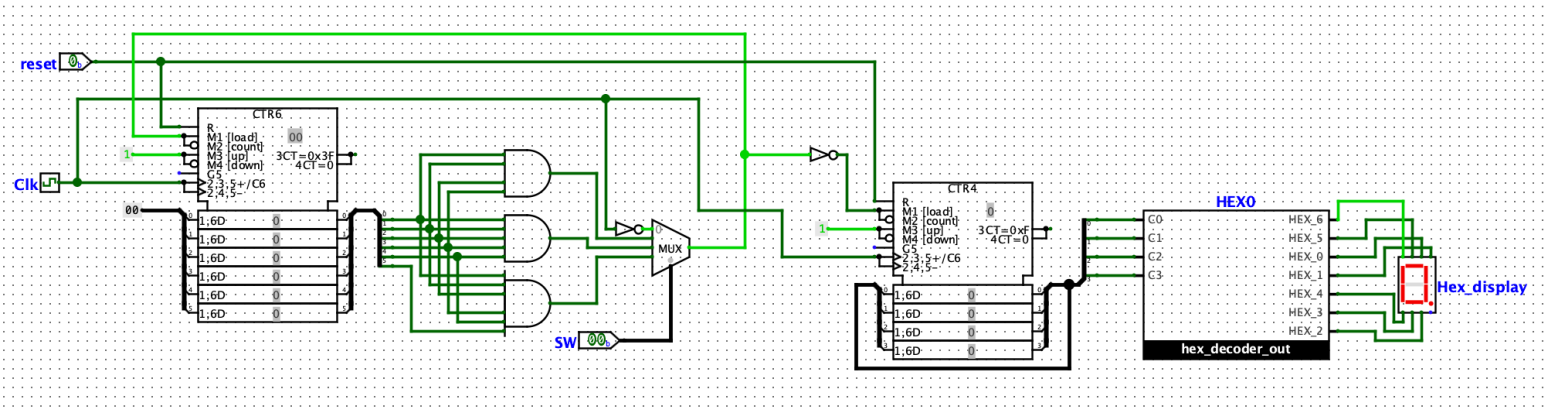
Since $\lceil \log_2 50\,000\,000 \rceil = 26$. We need a counter with 26 bits to represent the value.

B1.



My design for the Rate Divider.

B2. Logisim circuit.



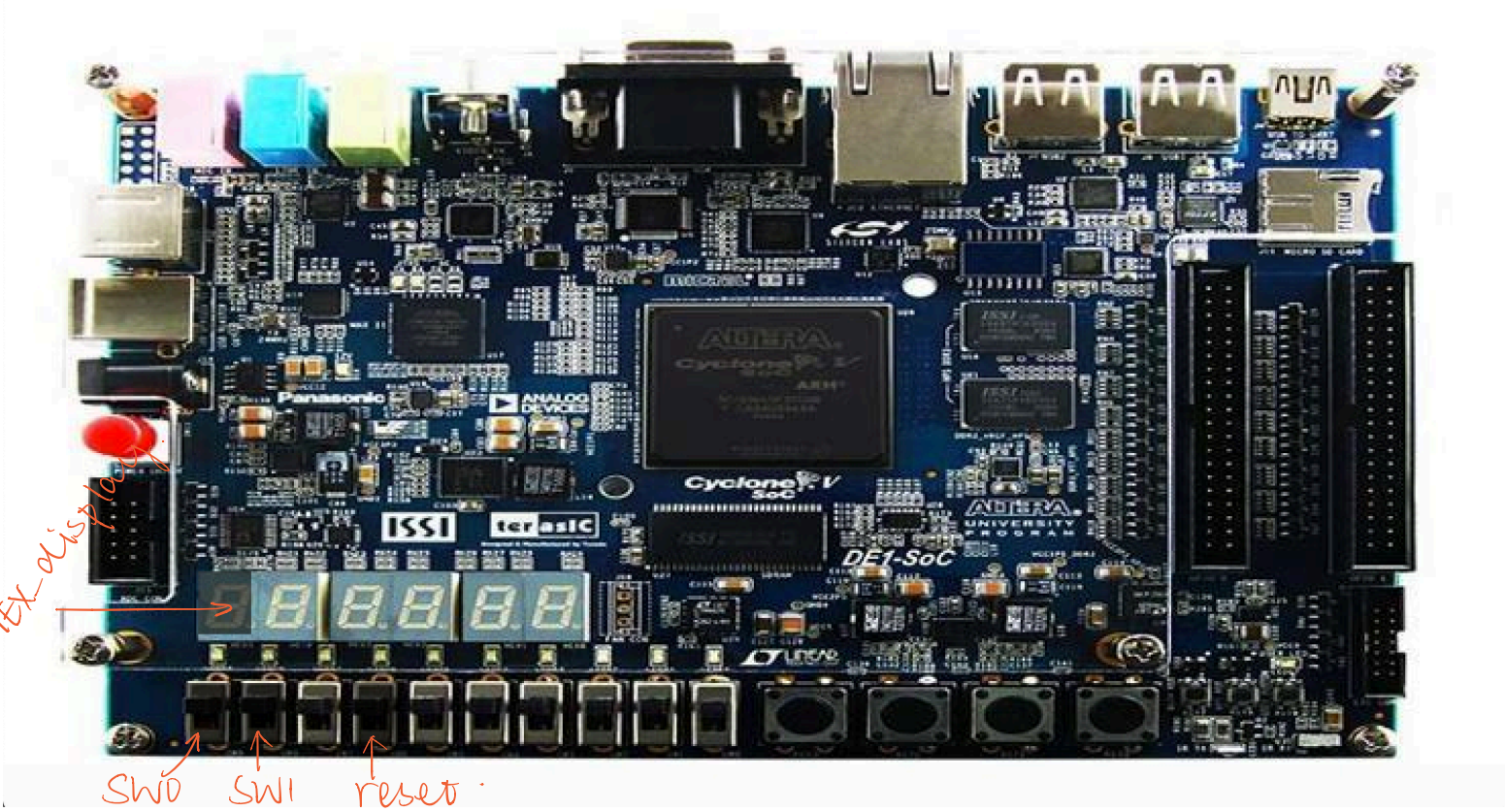
B4. Map.

Component to FPGA board mapping

Unmapped Components:	Mapped Components:	Command:
	BUS: /SW#Pin0 BUS: /SW#Pin1 PIN: /reset#Button0 SEVENSEGMENT: /Hex_display	Release component Release all components Load Map Save Map Cancel Done

1.0x 1.5x 2.0x

No messages



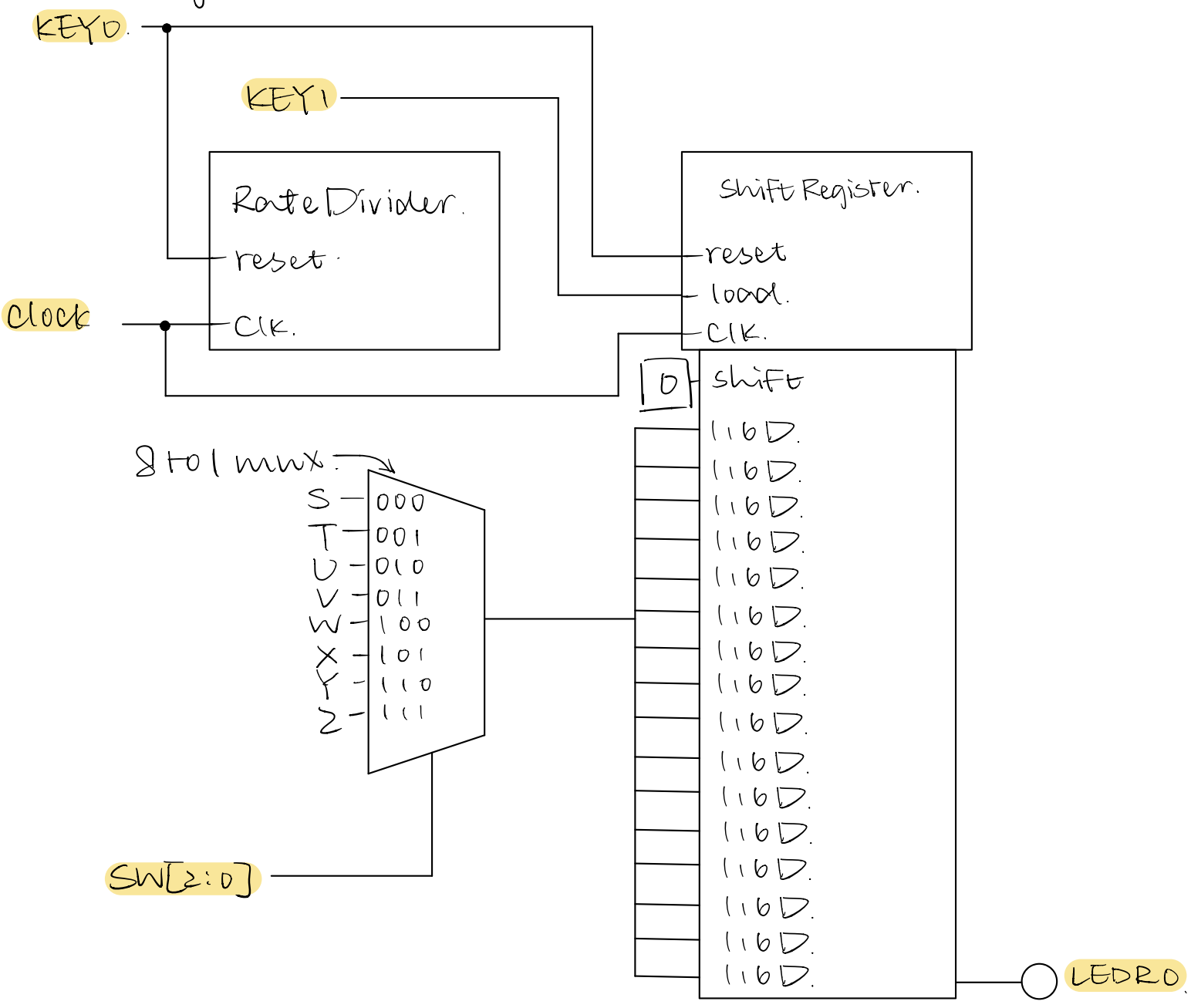
Part 3.

1.

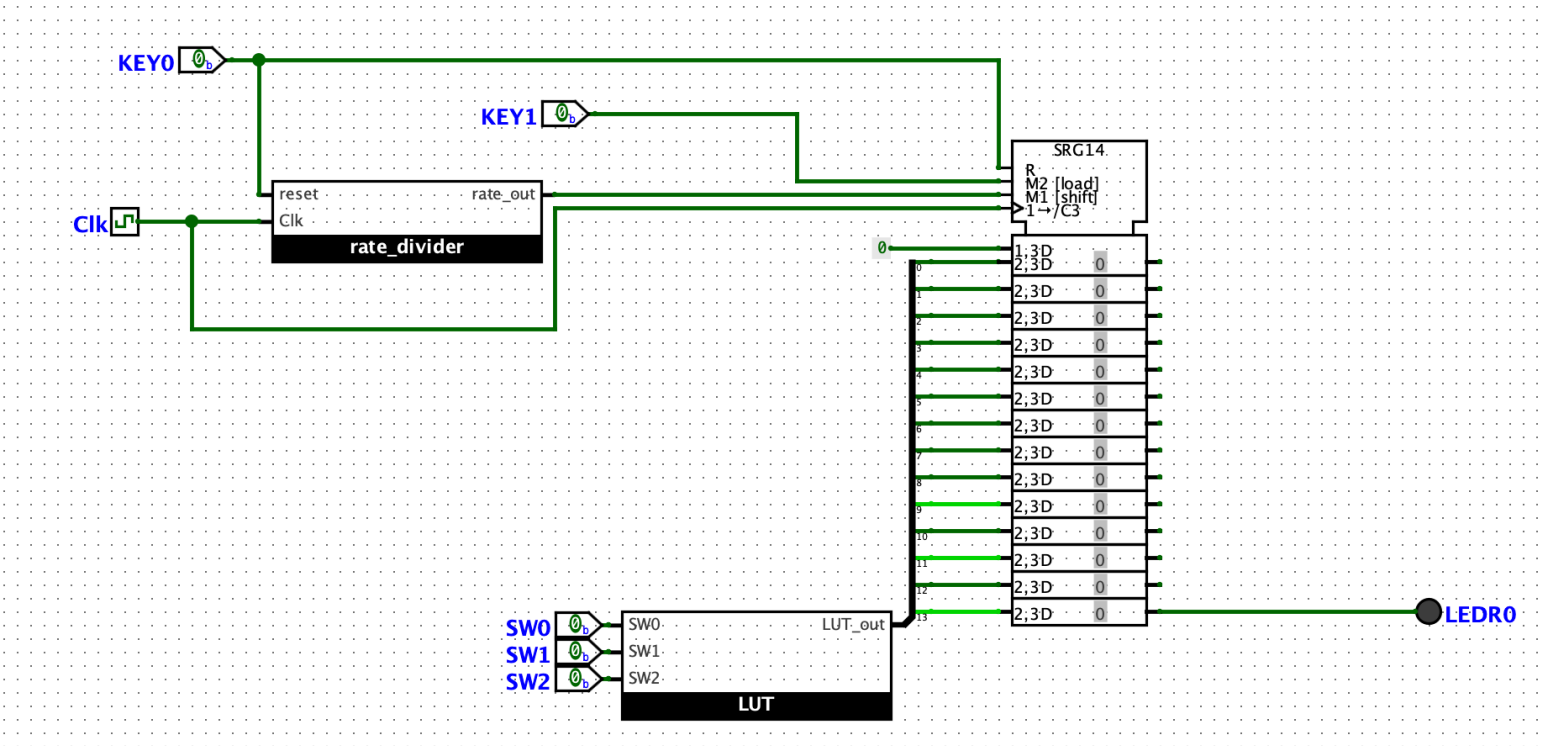
Letter	Morse Code	Pattern Representation (sequence length is 14. bits)
S	• • •	10101000000000.
T	—	11100000000000.
U	• • —	10101110000000
V	• • • —	10101011100000.
W	• — —	10111011100000
X	— • • —	11101010111000
Y	— • — —	11101011101110
Z	— — • •	11101110101000

Table 1: Morse Pattern Representation with fixed bit-width **(PRELAB)**

2. Design circuit.



3. Logisim Circuit.



4. Map.