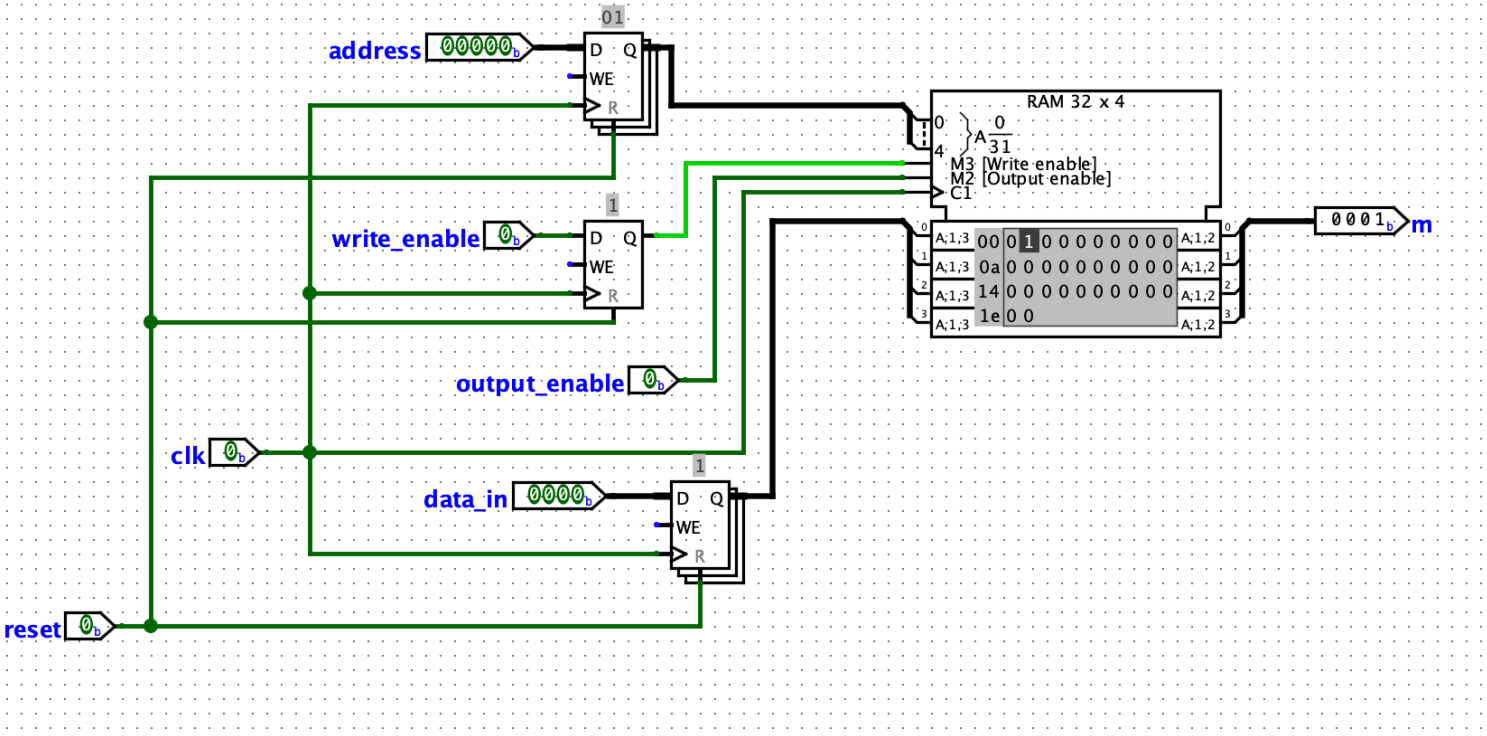
Lab-7. Memory and RGB Video.

Student Name: Jewen Ma.

Student Number: 1005968375

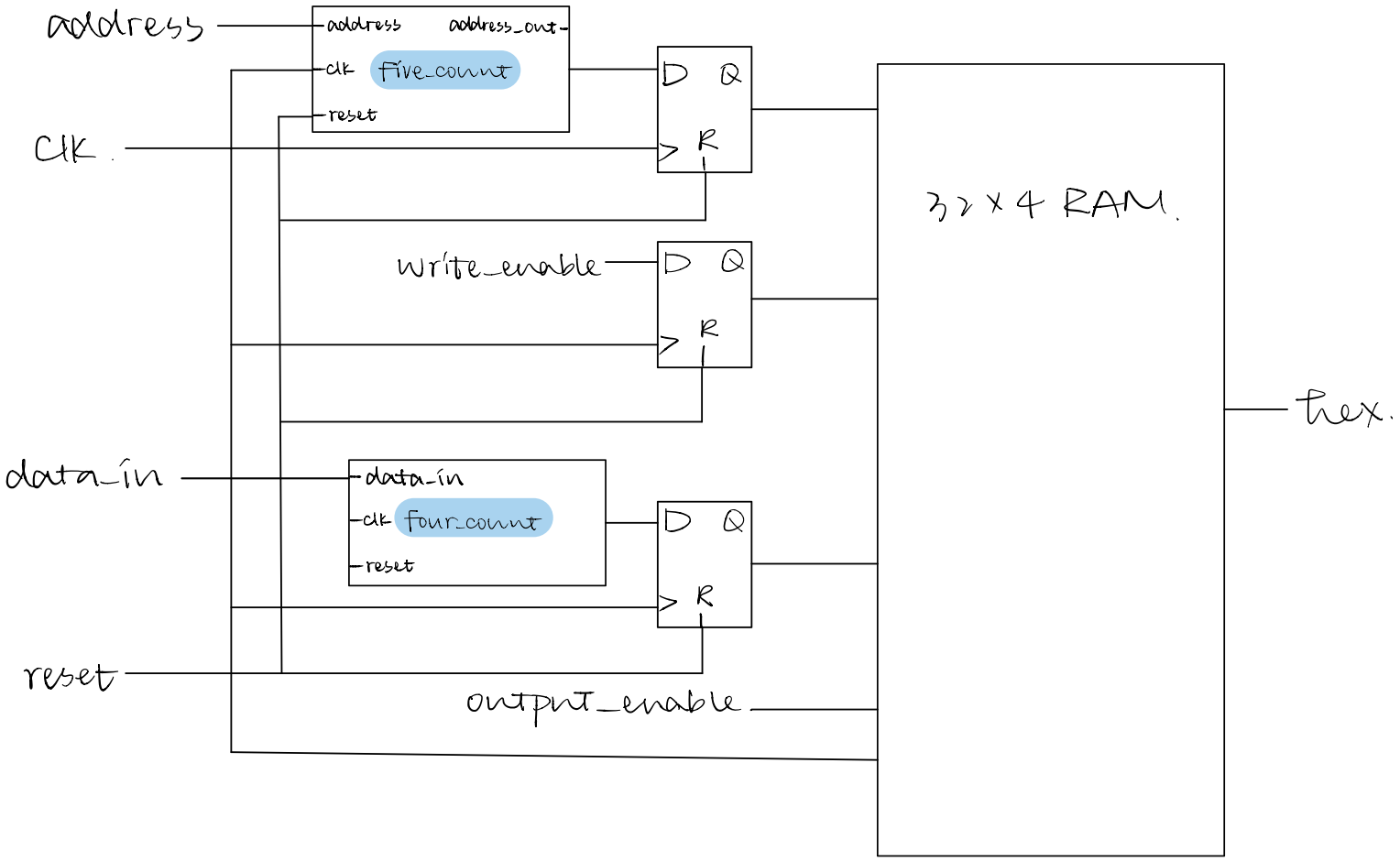
Part I.

1.



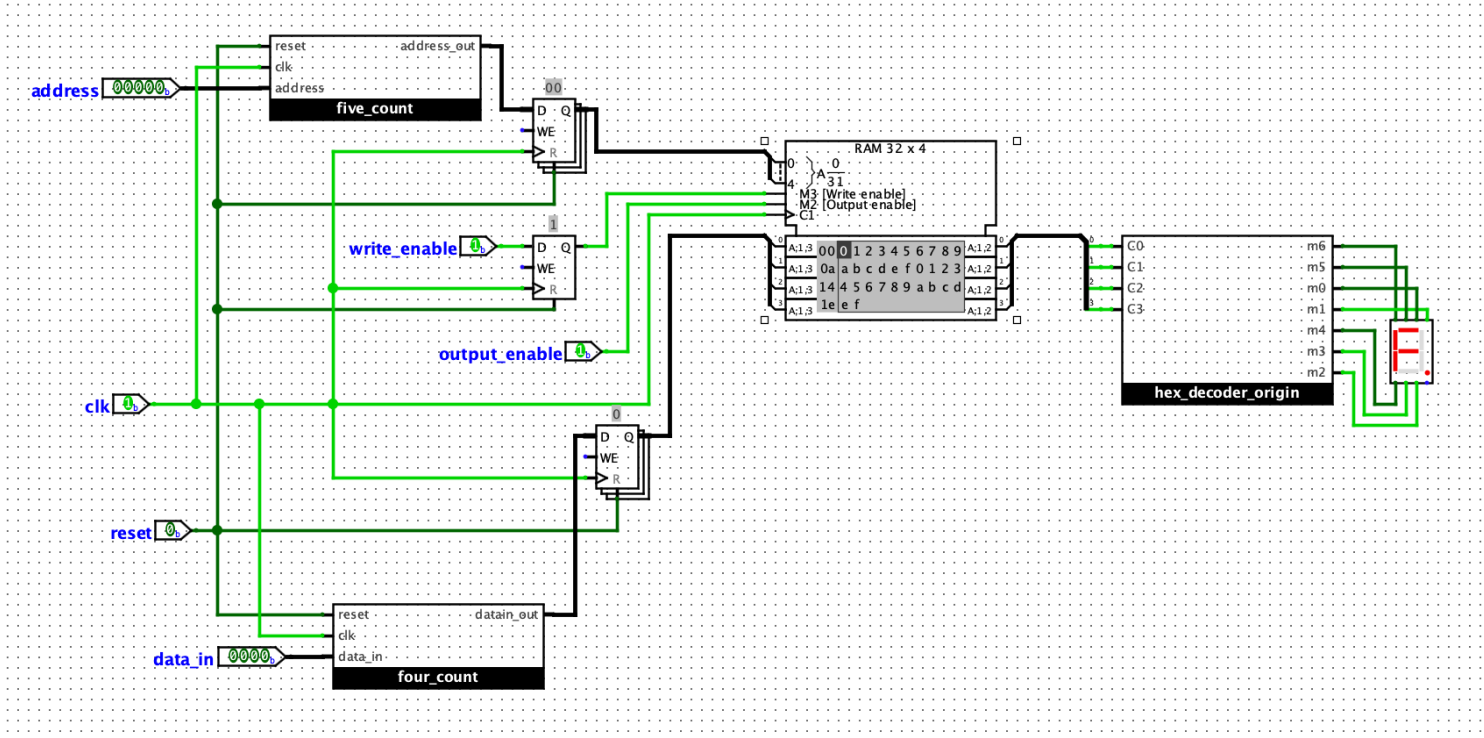
2. When the clock goes high, if both of the write enable and output enable signals are off, then the output m will remain the same. If both signals are high, then the output m will change into what "data_in" inputs.

5.



Note: · The five_count and four_count are the counters that automatically generates address and data_in.

6.

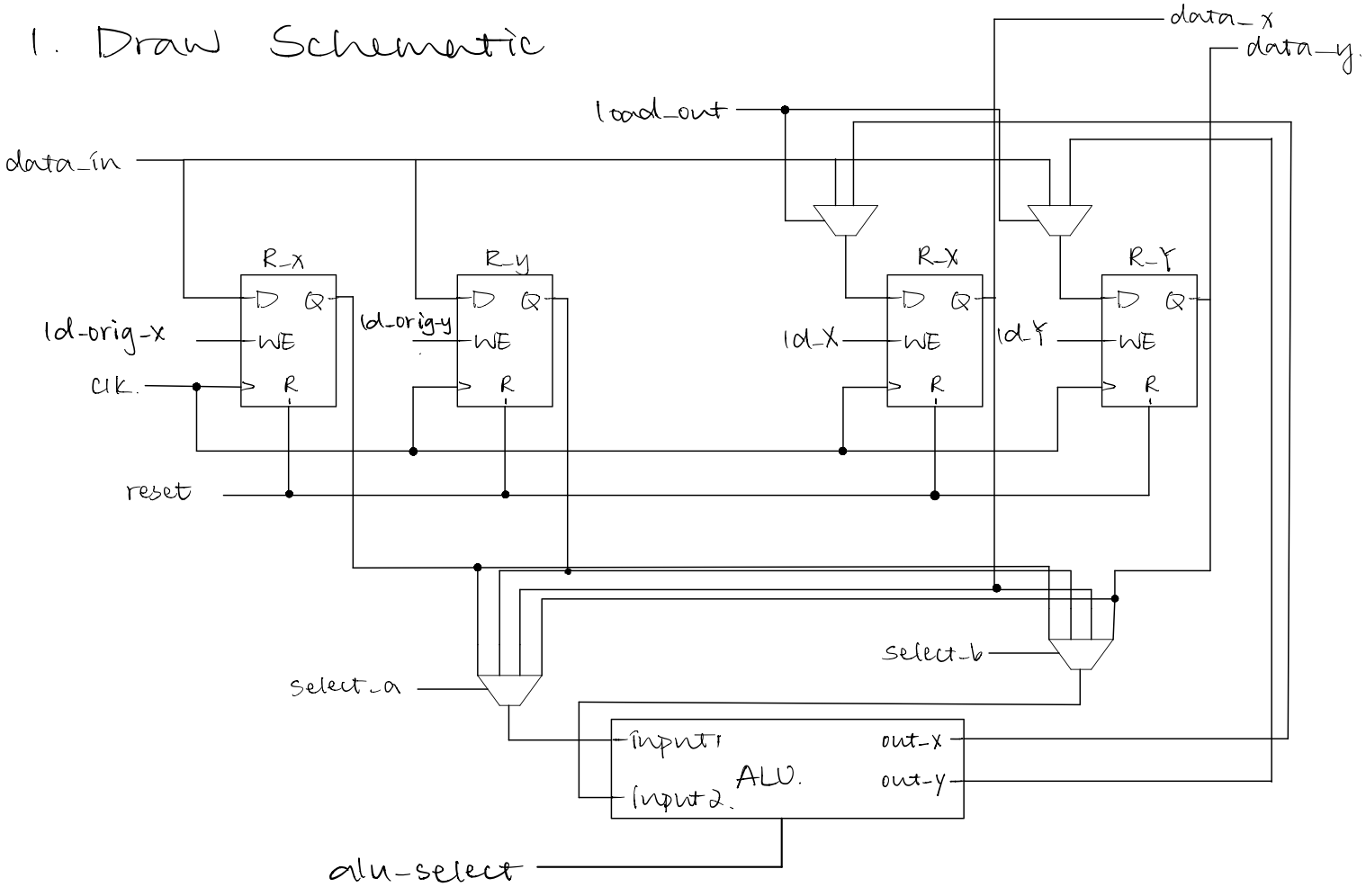


Part 2.

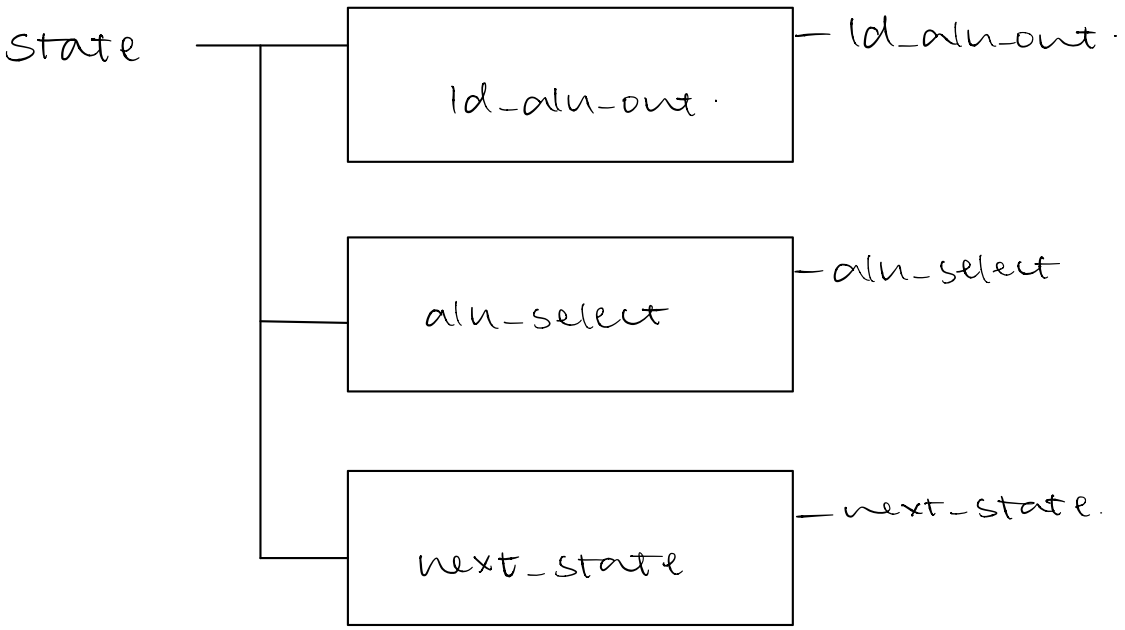
1. If the WE isn't turned off before updating X and Y, as we change the XY, the new point will not appear until we pass a clk cycle.
2. Nothing on the RGB video will change.
3. Only the last point added exists on the RGB video.

---

1. Draw Schematic



2. FSM:



1 — ld_origin_x

1 — ld_origin_y.

1 — ld_X

1 — ld_Y.

00 — select_a

01 — select_b.

3.