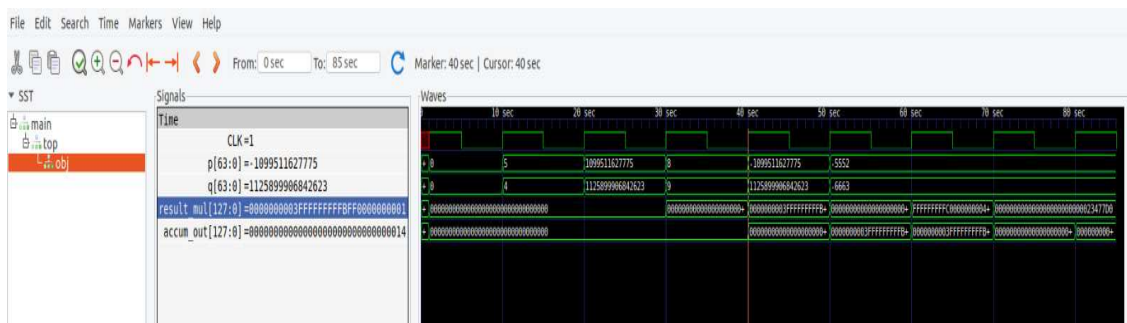


Results for IMAC_with_3stage_pipeline:

Simulation results: Below figure shows the outputs for corresponding input pairs.

```
bindu@bindu-VirtualBox:~/CAD_VLSI$ cd Pipelined-64-bit-signed-IMAC/Sources/IMAC_with_3stage_pipeline/
bindu@bindu-VirtualBox:~/CAD_VLSI/Pipelined-64-bit-signed-IMAC/Sources/IMAC_with_3stage_pipeline$ bsc -u -verilog -g mkBooth_wallace_3tb booth_wallace_3tb.bsv
checking package dependencies
All packages are up to date.
bindu@bindu-VirtualBox:~/CAD_VLSI/Pipelined-64-bit-signed-IMAC/Sources/IMAC_with_3stage_pipeline$ bsc -e mkBooth_wallace_3tb -verilog -vsim iverlog mkBooth_wallace_3tb.v
Verilog binary file created: a.out
bindu@bindu-VirtualBox:~/CAD_VLSI/Pipelined-64-bit-signed-IMAC/Sources/IMAC_with_3stage_pipeline$ ./a.out +bsvcvd
VCD info: dumpfile dump.vcd opened for output.
Input1 Is:0000000000000000 Input2 Is:0000000000000000 accun output Is:00000000000000000000000000000000
Input1 Is:0000000000000000 Input2 Is:0000000000000004 accun output Is:00000000000000000000000000000000
Input1 Is:0000000000000000 Input2 Is:0000000000000009 accun output Is:00000000000000000000000000000000
Input1 Is:0000000000000008 Input2 Is:0000000000000009 accun output Is:00000000000000000000000000000000
Input1 Is:ffffff0000000001 Input2 Is:0003fffffffffffff accun output Is:00000000000000000000000000000014
Input1 Is:ffffff000000ffea50 Input2 Is:ffffff0000fffef59 accun output Is:0000000003fffffffbbf000000015
Input1 Is:ffffff0000fffea50 Input2 Is:ffffff0000ffe5f9 accun output Is:0000000003fffffffbbf00000005d
Input1 Is:ffffff0000fffea50 Input2 Is:ffffff0000ffe5f9 accun output Is:000000000000000000000000000005c
Input1 Is:ffffff0000fffea50 Input2 Is:ffffff0000ffe5f9 accun output Is:0000000000000000000000000234782c
```

Graphical results: Below figure shows the input and output waveforms in gtkwave.



- Latency= 3 clock cycles for accumulator output

Area results: Below figure shows the synthesized area in Openlane tool

```
brahma_teja@brahmateja: ~/OpenLane

sky130_fd_sc_hd_buf_2      21
sky130_fd_sc_hd_buf_4      3
sky130_fd_sc_hd_conb_1     2
sky130_fd_sc_hd_dfxtp_2    1346
sky130_fd_sc_hd_inv_2      1057
sky130_fd_sc_hd_mux2_2     49
sky130_fd_sc_hd_nand2_2    1222
sky130_fd_sc_hd_nand2b_2   12
sky130_fd_sc_hd_nand3_2    128
sky130_fd_sc_hd_nand3b_2   2
sky130_fd_sc_hd_nand4_2    2
sky130_fd_sc_hd_nor2_2     1965
sky130_fd_sc_hd_nor2b_2    2
sky130_fd_sc_hd_nor3_2     106
sky130_fd_sc_hd_nor3b_2    2
sky130_fd_sc_hd_nor4_2     95
sky130_fd_sc_hd_o211a_2    982
sky130_fd_sc_hd_o211a_4    123
sky130_fd_sc_hd_o211ai_2   60
sky130_fd_sc_hd_o21a_2     227
sky130_fd_sc_hd_o21a_4     1
sky130_fd_sc_hd_o21ai_2    159
sky130_fd_sc_hd_o21ba_2    744
sky130_fd_sc_hd_o21bai_2   45
sky130_fd_sc_hd_o221a_2    560
sky130_fd_sc_hd_o221ai_2   2
sky130_fd_sc_hd_o22a_2     24
sky130_fd_sc_hd_o22ai_2    46
sky130_fd_sc_hd_o2bb2a_2   157
sky130_fd_sc_hd_o311a_2    2
sky130_fd_sc_hd_o31a_2     108
sky130_fd_sc_hd_o31ai_2    2
sky130_fd_sc_hd_o32a_2     2
sky130_fd_sc_hd_or2_2      1620
sky130_fd_sc_hd_or2_4      1
sky130_fd_sc_hd_or2b_2     742
sky130_fd_sc_hd_or3_2      133
sky130_fd_sc_hd_or3b_2     550
sky130_fd_sc_hd_or4_2      6
sky130_fd_sc_hd_or4b_2     1
sky130_fd_sc_hd_xnor2_2    1355
sky130_fd_sc_hd_xor2_2     572

Chip area for module '\mkBooth_wallace_3': 215405.340800

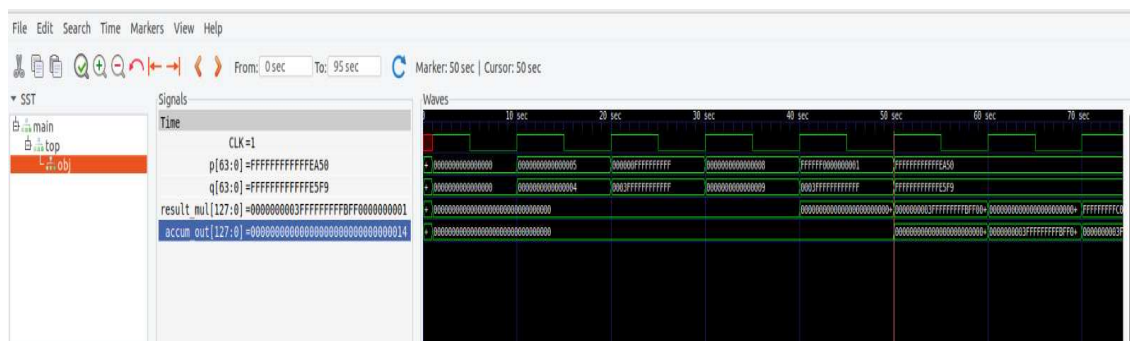
END)
```

Results for IMAC_with_4stage_pipeline:

Simulation results: Below figure shows the outputs for corresponding input pairs.

[illegible]

Graphical results: Below figure shows the input and output waveforms in gtkwave.



- Latency = 4 clock cycles for accumulator output

Area results: Below figure shows the synthesized area in Openlane tool

```
brahma_teja@brahmateja: ~/OpenLane
```

sky130_fd_sc_hd_and4_2	3
sky130_fd_sc_hd_and4_4	1
sky130_fd_sc_hd_and4b_2	1
sky130_fd_sc_hd_buf_1	3533
sky130_fd_sc_hd_buf_2	1
sky130_fd_sc_hd_buf_4	1
sky130_fd_sc_hd_conb_1	2
sky130_fd_sc_hd_dfxtp_2	3425
sky130_fd_sc_hd_inv_2	1701
sky130_fd_sc_hd_mux2_2	32
sky130_fd_sc_hd_nand2_2	1064
sky130_fd_sc_hd_nand2b_2	9
sky130_fd_sc_hd_nand3_2	99
sky130_fd_sc_hd_nand3b_2	1
sky130_fd_sc_hd_nand4_2	1
sky130_fd_sc_hd_nor2_2	1932
sky130_fd_sc_hd_nor2b_2	3
sky130_fd_sc_hd_nor3_2	62
sky130_fd_sc_hd_nor3b_2	3
sky130_fd_sc_hd_o211a_2	1402
sky130_fd_sc_hd_o211a_4	123
sky130_fd_sc_hd_o211ai_2	2
sky130_fd_sc_hd_o21a_2	196
sky130_fd_sc_hd_o21a_4	1
sky130_fd_sc_hd_o21ai_2	69
sky130_fd_sc_hd_o21ba_2	1455
sky130_fd_sc_hd_o21bai_2	52
sky130_fd_sc_hd_o221a_2	599
sky130_fd_sc_hd_o22a_2	3
sky130_fd_sc_hd_o311a_2	3
sky130_fd_sc_hd_o31a_2	5
sky130_fd_sc_hd_o31ai_2	3
sky130_fd_sc_hd_o32a_2	1
sky130_fd_sc_hd_or2_2	2359
sky130_fd_sc_hd_or2_4	1
sky130_fd_sc_hd_or2b_2	922
sky130_fd_sc_hd_or3_2	83
sky130_fd_sc_hd_or3b_2	986
sky130_fd_sc_hd_or4_2	11
sky130_fd_sc_hd_or4b_2	1
sky130_fd_sc_hd_xnor2_2	960
sky130_fd_sc_hd_xor2_2	266

Chip area for module '\mkBooth_wallace_4': 274638.400000

END)

Observations:

- In bluespec code, final output must be returned in the interface for the entire design to be properly synthesized in the Openlane tool.
- If final output is not returned properly, Simulation results might still be the same. But most of the components might not get synthesized.
- Here we implemented two designs, one with 3stage pipeline and other with 4stage pipeline.

Area of IMAC_with_3stage_pipeline:215405.30800 units

Area of IMAC_with_4stage_pipeline:274638.40000 units

- One can choose anyone of them based on there area and frequency requirements.
- Since area is the given constraint in the problem statement, We prefer IMAC_with_3stage_pipeline.