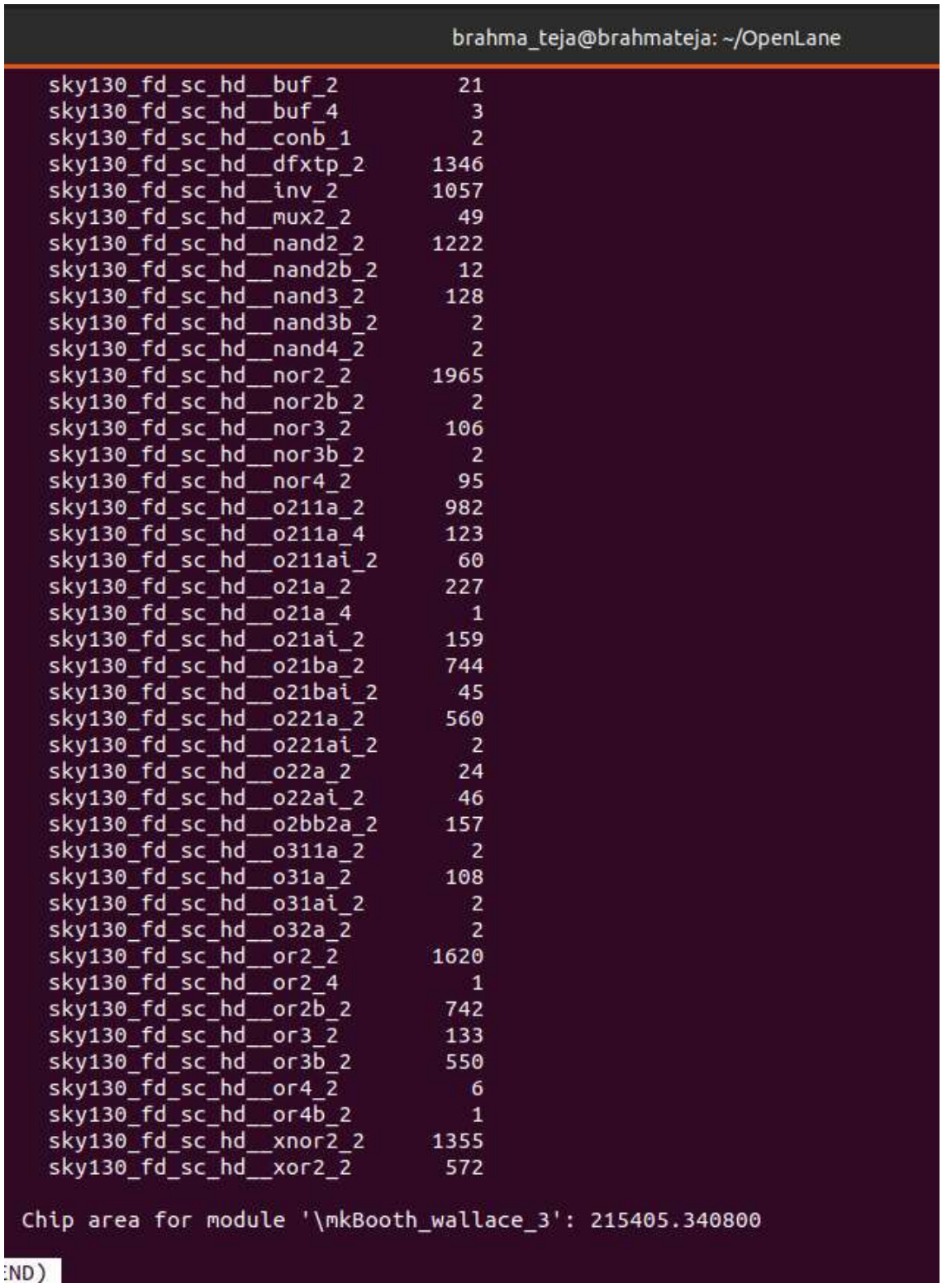
Results for IMAC_with_3stage_pipeline:

Simulation results: Below figure shows the outputs for corresponding input pairs.

Graphical results: Below figure shows the input and output waveforms in gtkwave.

- Latency= 3 clock cycles for accumulator output

Area results: Below figure shows the synthesized area in Openlane tool



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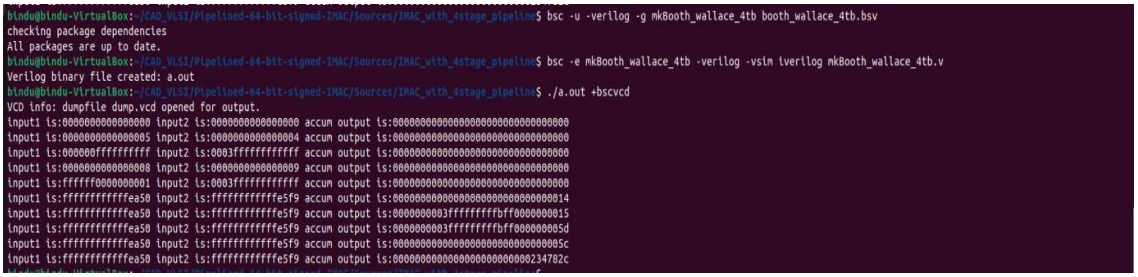
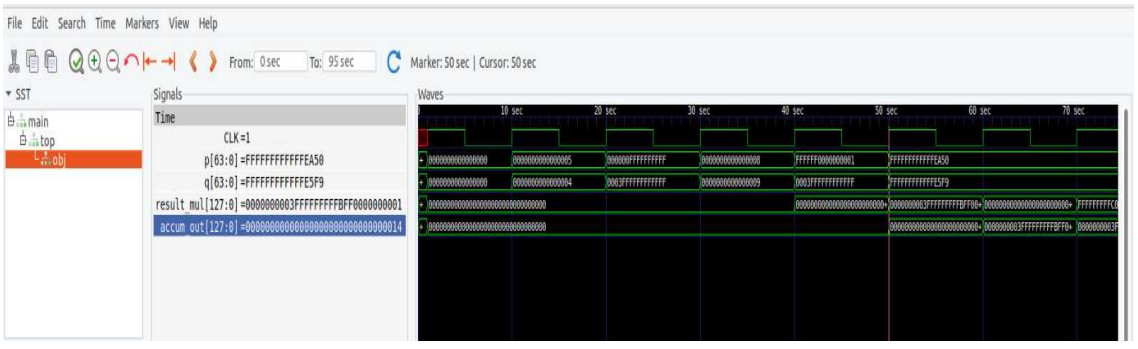
Results for IMAC_with_4stage_pipeline:

Simulation results: Below figure shows the outputs for corresponding input pairs.

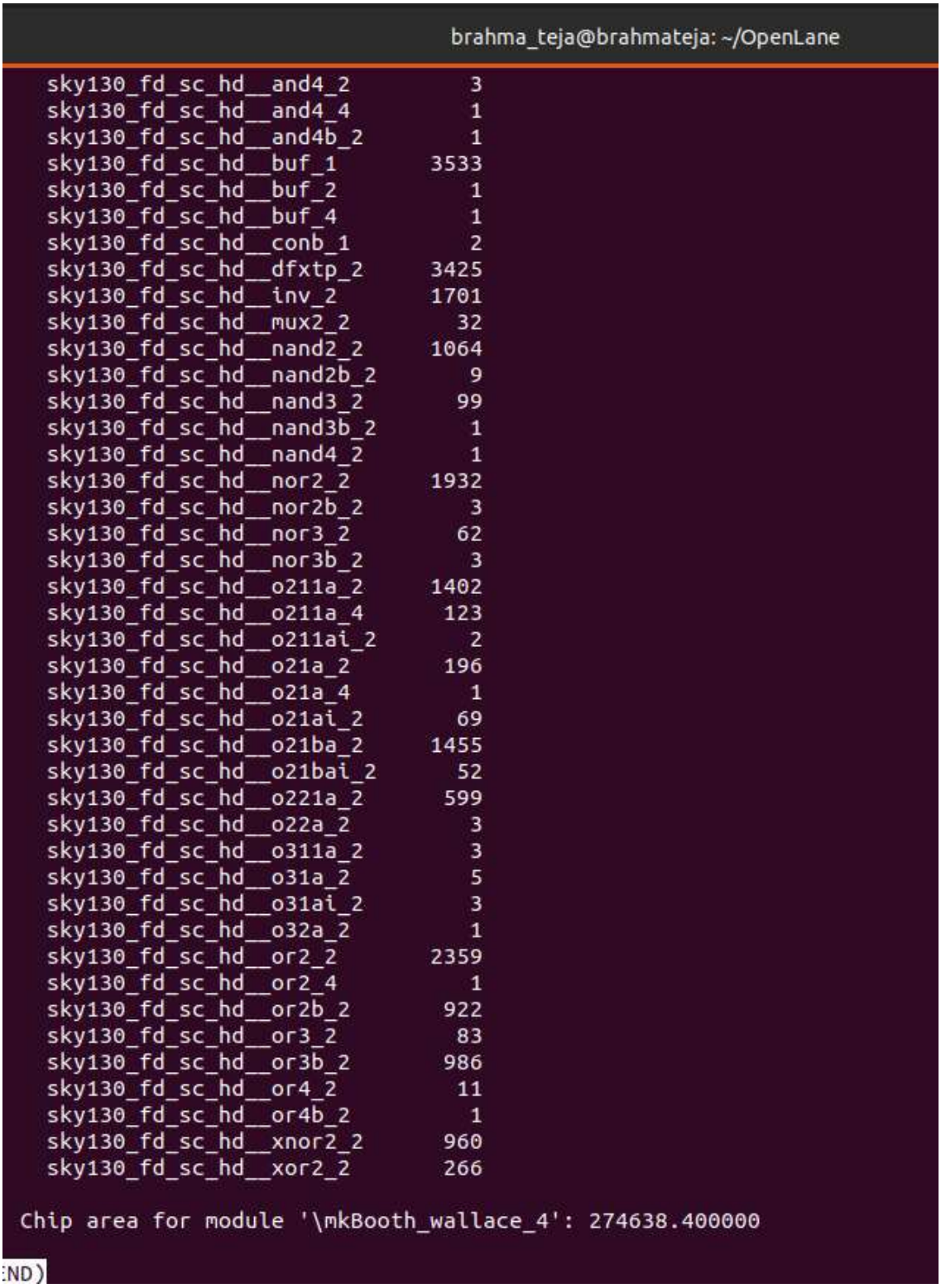


Graphical results: Below figure shows the input and output waveforms in gtkwave.



- Latency =4 clock cycles for accumulator output

Area results: Below figure shows the synthesized area in Openlane tool



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Observations:

- In bluespec code, final output must be returned in the interface for the entire design to be properly synthesized in the Openlane tool.
- If final output is not returned properly, Simulation results might still be the same. But most of the components might not get synthesized.
- Here we implemented two designs, one with 3stage pipeline and other with 4stage pipeline.

Area of IMAC_with_3stage_pipeline:215405.30800 units

Area of IMAC_with_4stage_pipeline:274638.40000 units

- One can choose anyone of them based on there area and frequency requirements.
- Since area is the given constraint in the problem statement, We prefer IMAC_with_3stage_pipeline.