EE-671-VLSI Design

Assignment-4

Procedure-

- The circuit is designed and simulated using Quartus Prime light
- The three logic sub-blocks- AND gate, XOR gate and A+BC were designed with a delay of 100ps as mentioned in the question.
- Finally, the Brent-Kung adder was designed using these sub blocks in 6 stages- stage-0 to stage-5.
- The right most blocks of all levels use the available value of carry_in to compute the output carry directly and term these as the G values for computation of P and G for the next stage.
- The circuit was tested using with a test bench which reads pairs of 32-bit words and a single bit input carry from a file, adds them and compares the result with the expected 32-bit sum and 1 bit carry values stored in the same file.
- The output was tested and verified again 64 randomly generated inputs (generated using a python code) and outputs.
- Assert statement is used for identify any mismatch in the expected and calculated output values.
- The block diagram of the adder for generating carry_out (along with the G and P variable names as used in the VHDL code) is shown below-

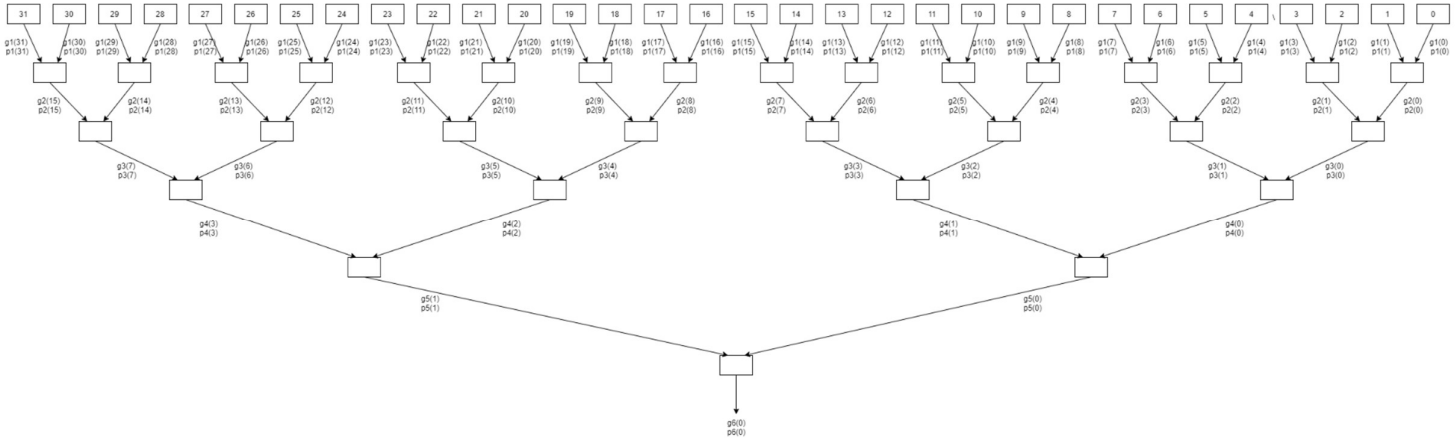

Figure 1. Block Diagram for carry_out calculation

Observations and Results-

Since the output of the logic sub-blocks AND, XOR and A+BC is 100ps each, the delay at each stage is 100ps.

The expected delay in calculation of final carry_out = Delay at each stage * Total stages

= 100ps * 6

= 600ps =0.6ns

The expected delay of 0.6ns is also observed in the simulation results.

Output waveform-

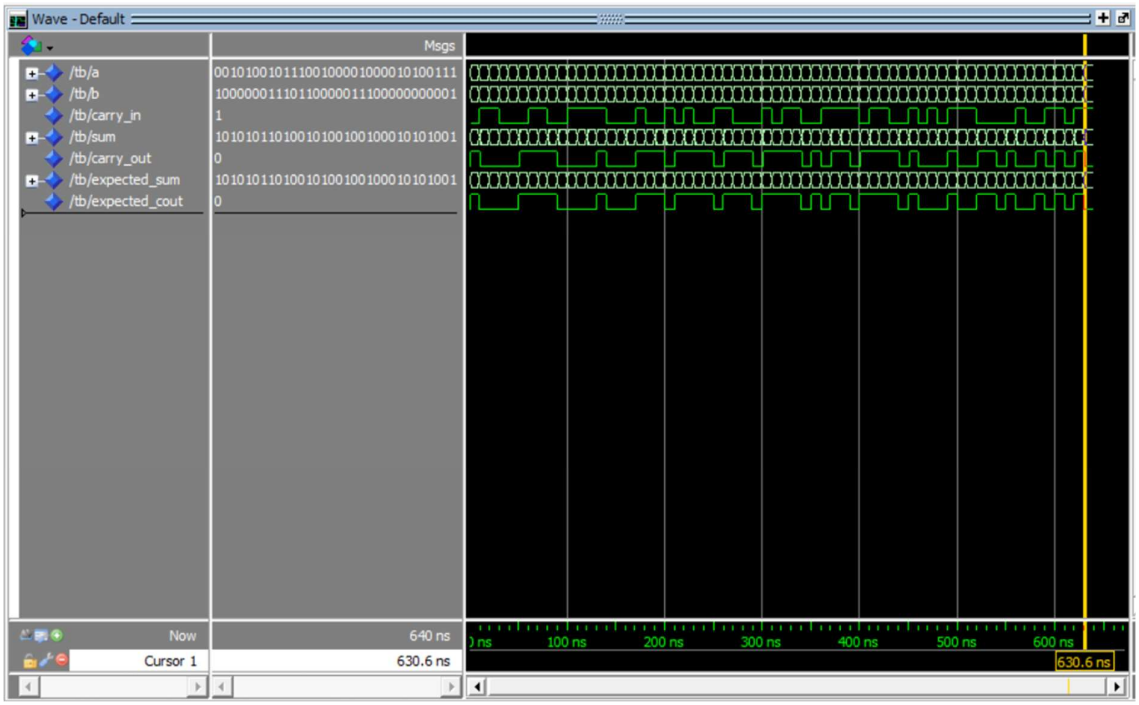

Figure 2. Output waveform for test input signals

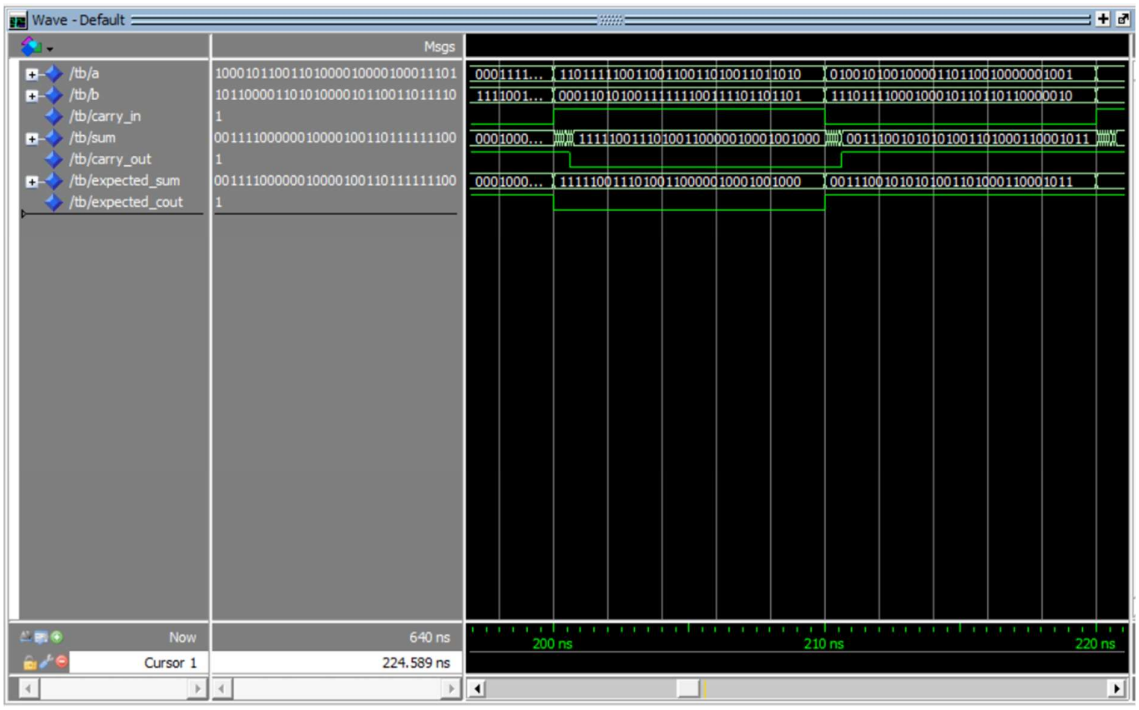

Figure 3. Output waveform (zoomed in)

RTL Netlist-

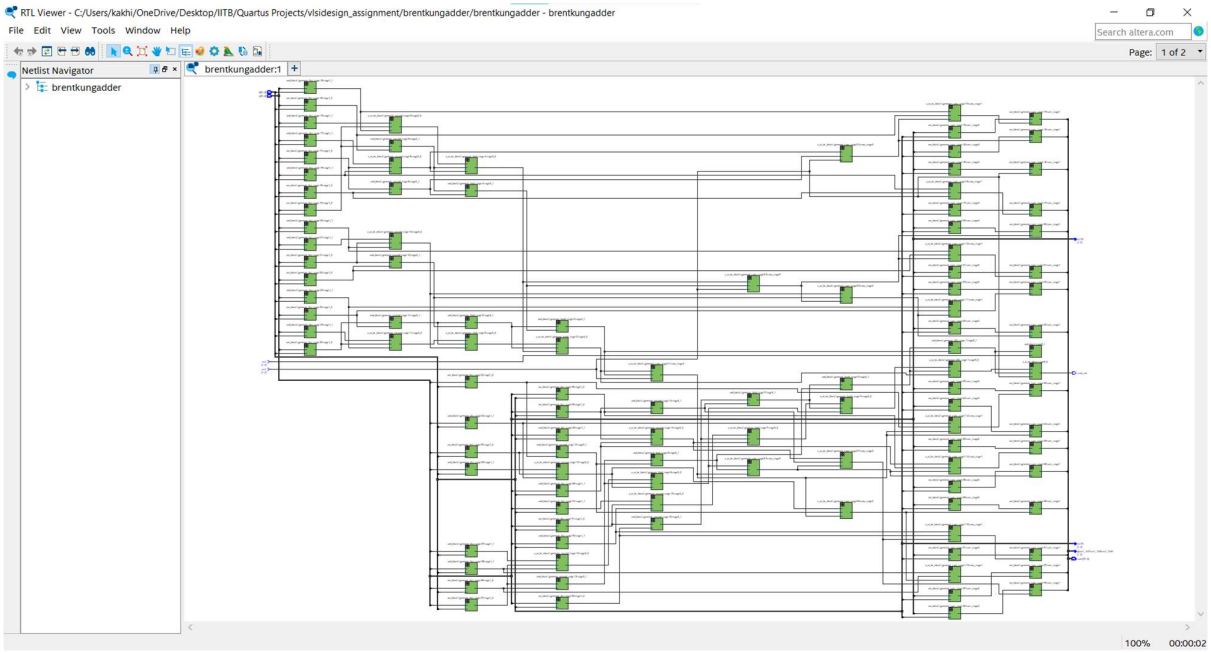

Figure 4. RTL netlist of the designed Brent-Kung Adder