

# LC717A10AR

## Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors

### Overview

The LC717A10AR is a high-performance and low-cost capacitance-digital-converter LSI for electrostatic capacitive touch sensor, especially focused on usability.

It has 16 channels capacitance-sensor input. This makes it ideal for use in the products that need many switches. Since the calibration function and the judgment of ON/OFF are automatically performed in LSI internal, it can make development time more short. A detection result (ON/OFF) for each input can be read out by the serial interface (I<sup>2</sup>C™ compatible bus or SPI).

Also, measurement value of each input can be read out as 8-bit digital data. Moreover, gain and other parameters can be adjusted using serial interface.

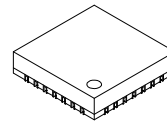
### Features

- Detection System: Differential Capacitance Detection (Mutual Capacitance Type)
- Input Capacitance Resolution: Can Detect Capacitance Changes in the Femto Farad Order
- Measurement Interval (16 Differential Inputs):
  - ◆ 30 ms (Typ) (at Initial Configuration)
  - ◆ 6 ms (Typ) (at Minimum Interval Configuration)
- External Components for Measurement: Not Required
- Current Consumption:
  - ◆ 570  $\mu$ A (Typ) ( $V_{DD}$  = 2.8 V)
  - ◆ 1.3 mA (Typ) ( $V_{DD}$  = 5.5 V)
- Supply Voltage: 2.6 V to 5.5 V
- Detection Operations: Switch
- Interface: I<sup>2</sup>C Compatible Bus or SPI Selectable



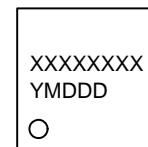
**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)



**VCT28  
CASE 601AE**

### MARKING DIAGRAM



XXXXXX = Specific Device Code  
Y = Year  
M = Month  
DDD = Additional Traceability Data

### ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

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## Specifications

**Table 1. ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	$V_{DD}$	-0.3 to +6.5	V	
Input Voltage	$V_{IN}$	-0.3 to $V_{DD} + 0.3$	V	(Note 1)
Output Voltage	$V_{OUT}$	-0.3 to $V_{DD} + 0.3$	V	(Note 2)
Power Dissipation	$P_{d\text{ max}}$	160	mW	$T_A = +105^\circ\text{C}$ , Mounted on a substrate (Note 3)
Storage Temperature	$T_{stg}$	-55 to +125	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Apply to  $C_{in0}$  to 15,  $C_{ref}$ ,  $C_{refAdd}$ ,  $nRST$ ,  $SCL$ ,  $SDA$ ,  $SA0$ ,  $SA1$ ,  $SCK$ ,  $SI$ ,  $nCS$ .
2. Apply to  $C_{drv}$ ,  $SDA$ ,  $SO$ ,  $INTOUT$ .
3. 4-layer glass epoxy board ( $40 \times 50 \times 0.8\text{ mm}$ ).

**Table 2. RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remarks
Operating Supply Voltage	$V_{DD}$		2.6	–	5.5	V	
Supply Ripple + Noise	$V_{PP}$		–	–	$\pm 20$	mV	(Note 4)
Operating Temperature	$T_{opr}$		-40	25	105	$^\circ\text{C}$	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Inserting a high-valued capacitor and a low-valued capacitor in parallel between  $V_{DD}$  and  $V_{SS}$  is recommended. In this case, the small-valued capacitor should be at least  $0.1\text{ }\mu\text{F}$ , and is mounted near the LSI.

**Table 3. ELECTRICAL CHARACTERISTICS**

( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 2.6$  to  $5.5\text{ V}$ ,  $T_A = -40$  to  $+105^\circ\text{C}$ , Unless otherwise specified, the  $C_{drv}$  drive frequency is  $f_{CDRV} = 143\text{ kHz}$ .  
Not tested at low temperature before shipment.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remarks
Capacitance Detection Resolution	N		–	–	8	bit	
Output Noise RMS	$N_{RMS}$	Minimum gain setting	–	–	$\pm 1.0$	LSB	(Notes 5, 7)
Input Offset Capacitance Adjustment Range	$Coff_{RANGE}$		–	$\pm 8.0$	–	pF	(Notes 5, 7)
Input Offset Capacitance Adjustment Resolution	$Coff_{RESO}$		–	8	–	bit	
$C_{in}$ Offset Drift	$C_{inDRIFT}$	Minimum gain setting	–	–	$\pm 8$	LSB	(Note 5)
$C_{in}$ Detection Sensitivity	$C_{inSENSE}$	Minimum gain setting	0.04	–	0.12	LSB/ff	(Note 6)
$C_{in}$ Pin Leak Current	$I_{Cin}$	$C_{in} = Hi-Z$	–	$\pm 25$	$\pm 500$	nA	
$C_{in}$ Allowable Parasitic Input Capacitance	$C_{inSUB}$	$C_{in}$ against $V_{SS}$	–	–	30	pF	(Notes 5, 7)
$C_{drv}$ Drive Frequency	$f_{CDRV}$		100	143	186	kHz	
$C_{drv}$ Pin Leak Current	$I_{CDRV}$	$C_{drv} = Hi-Z$	–	$\pm 25$	$\pm 500$	nA	
$nRST$ Minimum Pulse Width	$t_{NRST}$		1	–	–	$\mu\text{s}$	
Power-on Reset Time	$t_{POR}$		–	–	20	ms	
Power-on Reset Operation Condition: Hold Time	$t_{POROP}$		10	–	–	ms	(Note 5)
Power-on Reset Operation Condition: Input Voltage	$V_{POROP}$		–	–	0.1	V	(Note 5)
Power-on Reset Operation Condition: Power Supply Rise Rate	$t_{VDD}$	0 V to $V_{DD}$	1	–	–	V/ms	(Note 5)

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**Table 3. ELECTRICAL CHARACTERISTICS** (continued)

( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 2.6\text{ to }5.5\text{ V}$ ,  $T_A = -40\text{ to }+105^\circ\text{C}$ , Unless otherwise specified, the Cdrv drive frequency is  $f_{CDRV} = 143\text{ kHz}$ .  
Not tested at low temperature before shipment.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remarks
Pin Input Voltage	$V_{IH}$	High input	$0.8 V_{DD}$	–	–	V	(Notes 5, 8)
	$V_{IL}$	Low input	–	–	$0.2 V_{DD}$		
Pin Output Voltage	$V_{OH}$	High output ( $I_{OH} = +3\text{ mA}$ )	$0.8 V_{DD}$	–	–	V	(Note 9)
	$V_{OL}$	Low output ( $I_{OL} = -3\text{ mA}$ )	–	–	$0.2 V_{DD}$		
SDA Pin Output Voltage	$V_{OL} I^2C$	SDA Low output ( $I_{OL} = -3\text{ mA}$ )	–	–	0.4	V	
Pin Leak Current	$I_{LEAK}$		–	–	$\pm 1$	$\mu\text{A}$	(Note 10)
Current Consumption	$I_{DD}$	When initial setting and non-touch $V_{DD} = 2.8\text{ V}$	–	570	700	$\mu\text{A}$	(Notes 5, 7)
		When initial setting and non-touch $V_{DD} = 5.5\text{ V}$	–	1.3	1.6	mA	
	$I_{STBY}$	During Sleep process	–	–	1	$\mu\text{A}$	(Note 7)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Design-guaranteed values (not tested before shipment).
6. Measurements conducted using the test mode in the LSI.
7.  $T_A = +25^\circ\text{C}$ .
8. Apply to nRST, SCL, SDA, SA0, SA1, SCK, SI, nCS.
9. Apply to Cdrv, SO, INTOUT.
10. Apply to nRST, SCL, SDA, SA0, SA1, SCK, SI, nCS.

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**Table 4. I<sup>2</sup>C COMPATIBLE BUS TIMING CHARACTERISTICS**

(V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 2.6 to 5.5 V, T<sub>A</sub> = -40 to +105°C, Not tested at low temperature before shipment.)

Parameter	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit	Remarks
SCL Clock Frequency	f <sub>SCL</sub>	SCL		–	–	400	kHz	
START Condition Hold Time	t <sub>HD;STA</sub>	SCL, SDA		0.6	–	–	μs	
SCL Clock Low Period	t <sub>LOW</sub>	SCL		1.3	–	–	μs	
SCL Clock High Period	t <sub>HIGH</sub>	SCL		0.6	–	–	μs	
Repeated START Condition Setup Time	t <sub>SU;STA</sub>	SCL, SDA		0.6	–	–	μs	(Note 11)
Data Hold Time	t <sub>HD;DAT</sub>	SCL, SDA		0	–	0.9	μs	
Data Setup Time	t <sub>SU;DAT</sub>	SCL, SDA		100	–	–	ns	(Note 11)
SDA, SCL Rise/Fall Time	t <sub>r</sub> / t <sub>f</sub>	SCL, SDA		–	–	300	ns	(Note 11)
STOP Condition Setup Time	t <sub>SU;STO</sub>	SCL, SDA		0.6	–	–	μs	
STOP-to-START Bus Release Time	t <sub>BUF</sub>	SCL, SDA		1.3	–	–	μs	(Note 11)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Design-guaranteed values (not tested before shipment).

**Table 5. SPI BUS TIMING CHARACTERISTICS**

(V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 2.6 to 5.5 V, T<sub>A</sub> = -40 to +105°C, Not tested at low temperature before shipment.)

Parameter	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit	Remarks
SCK Clock Frequency	f <sub>SCK</sub>	SCK		–	–	5	MHz	
SCK Clock Low Time	t <sub>LOW</sub>	SCK		90	–	–	ns	(Note 12)
SCK Clock High Time	t <sub>HIGH</sub>	SCK		90	–	–	ns	(Note 12)
Input Signal Rise/Fall Time	t <sub>r</sub> / t <sub>f</sub>	nCS, SCK, SI		–	–	300	ns	(Note 12)
nCS Setup Time	t <sub>SU;NCS</sub>	nCS, SCK		90	–	–	ns	(Note 12)
SCK Clock Setup Time	t <sub>SU;SCK</sub>	nCS, SCK		90	–	–	ns	(Note 12)
Data Setup Time	t <sub>SU;SI</sub>	SCK, SI		20	–	–	ns	(Note 12)
Data Hold Time	t <sub>HD;SI</sub>	SCK, SI		30	–	–	ns	(Note 12)
nCS Hold Time	t <sub>HD;NCS</sub>	nCS, SCK		90	–	–	ns	(Note 12)
SCK Clock Hold Time	t <sub>HD;SCK</sub>	nCS, SCK		90	–	–	ns	(Note 12)
nCS Standby Pulse Width	t <sub>CPH</sub>	nCS		90	–	–	ns	(Note 12)
Output High Impedance Time from nCS	t <sub>CHZ</sub>	nCS, SO		–	–	80	ns	(Note 12)
Output Data Determination Time	t <sub>v</sub>	SCK, SO		–	–	80	ns	(Note 12)
Output Data Hold Time	t <sub>HD;SO</sub>	SCK, SO		0	–	–	ns	(Note 12)
Output Low Impedance Time from SCK Clock	t <sub>CLZ</sub>	SCK, SO		0	–	–	ns	(Note 12)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

12. Design-guaranteed values (not tested before shipment).

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### Power-On Reset (POR)

When power is turned on, power-on reset is enabled inside the LSI and its state is released after a certain power-on reset time,  $t_{POR}$ . Power-on reset operation condition: Power supply rise rate  $t_{VDD}$  must be at least 1 V/ms.

Since INTOUT pin changes from “High” to “Low” at the same time as the released of power-on reset, it is possible to verify the timing of release of power-on reset externally.

During power-on reset,  $C_{in}$ ,  $C_{ref}$  and  $C_{refAdd}$  are unknown.

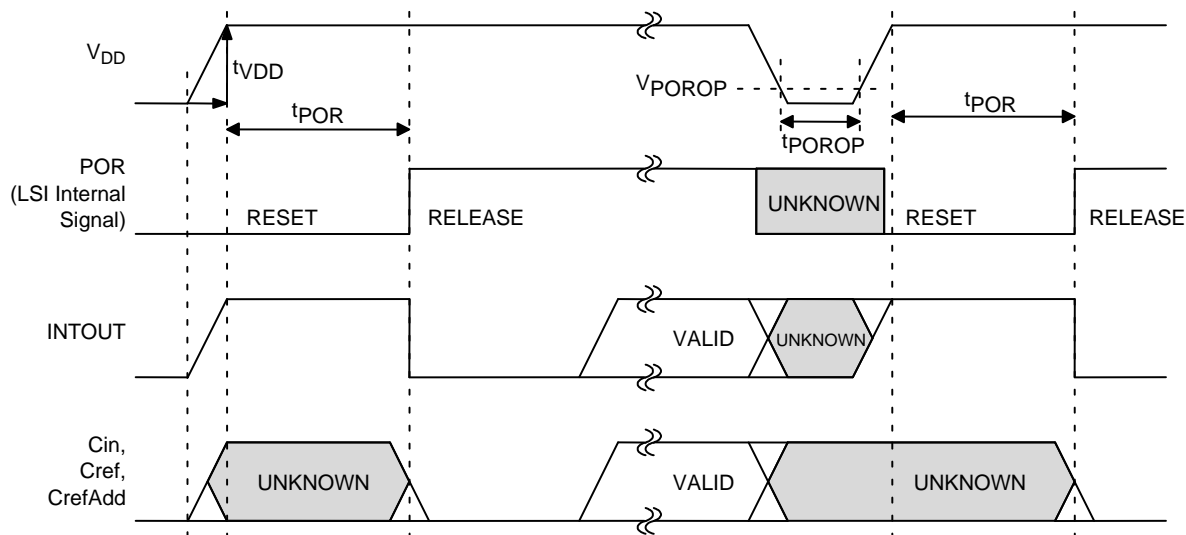


Figure 1.

### I<sup>2</sup>C Compatible Bus Data Timing

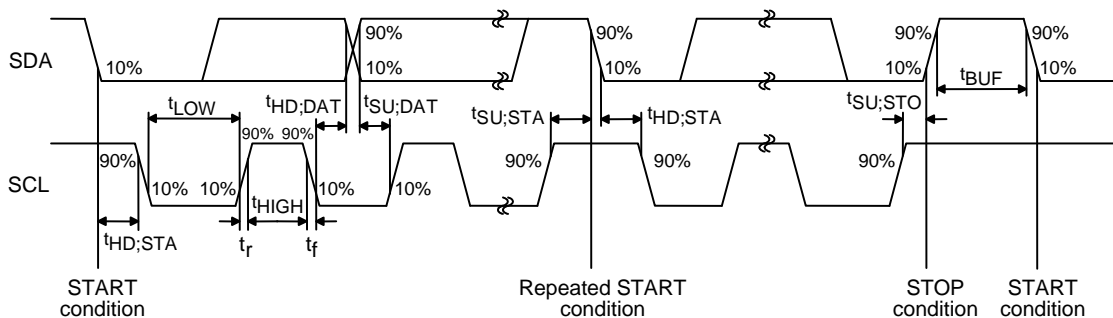


Figure 2.

### I<sup>2</sup>C Compatible Bus Communication Formats

- Write format (data can be written into sequentially incremented addresses)

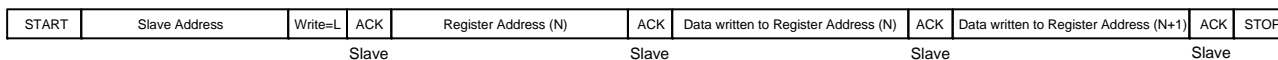


Figure 3.

- Read format (data can be read from sequentially incremented addresses)

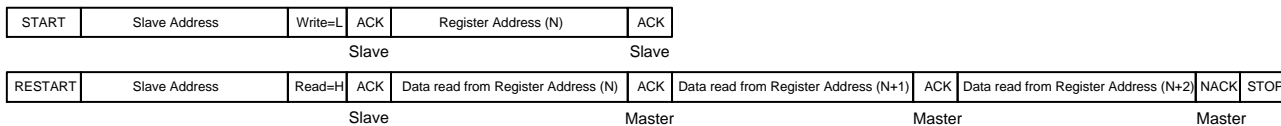


Figure 4.

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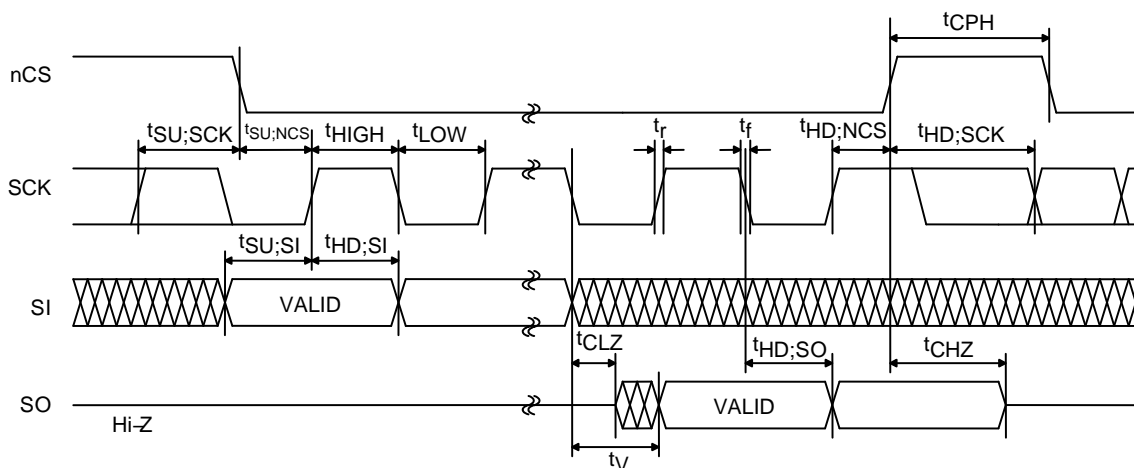
## I<sup>2</sup>C Compatible Bus Slave Address

Selection of four kinds of addresses is possible through the SA0 and SA1 terminals.

**Table 6.**

SA1 Pin Input	SA0 Pin Input	7-bit Slave Address	Binary Notation	8-bit Slave Address
Low	Low	0x16	00101100b (Write)	0x2C
			00101101b (Read)	0x2D
Low	High	0x17	00101110b (Write)	0x2E
			00101111b (Read)	0x2F
High	Low	0x18	00110000b (Write)	0x30
			00110001b (Read)	0x31
High	High	0x19	00110010b (Write)	0x32
			00110011b (Read)	0x33

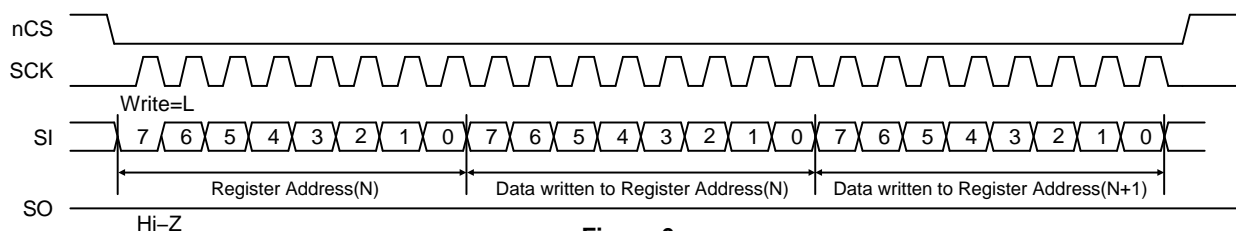
## SPI Data Timing (SPI Mode 0 / Mode 3)



**Figure 5.**

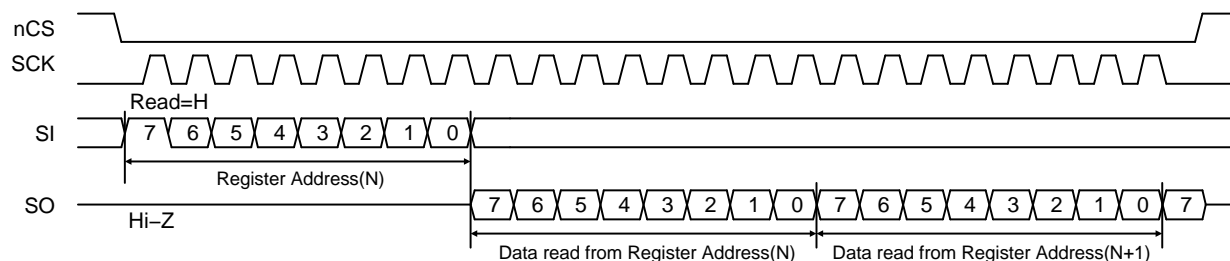
## SPI Communication Formats (Example of Mode 0)

- Write format (data can be written into sequentially incremented addresses while preserving nCS = L)



**Figure 6.**

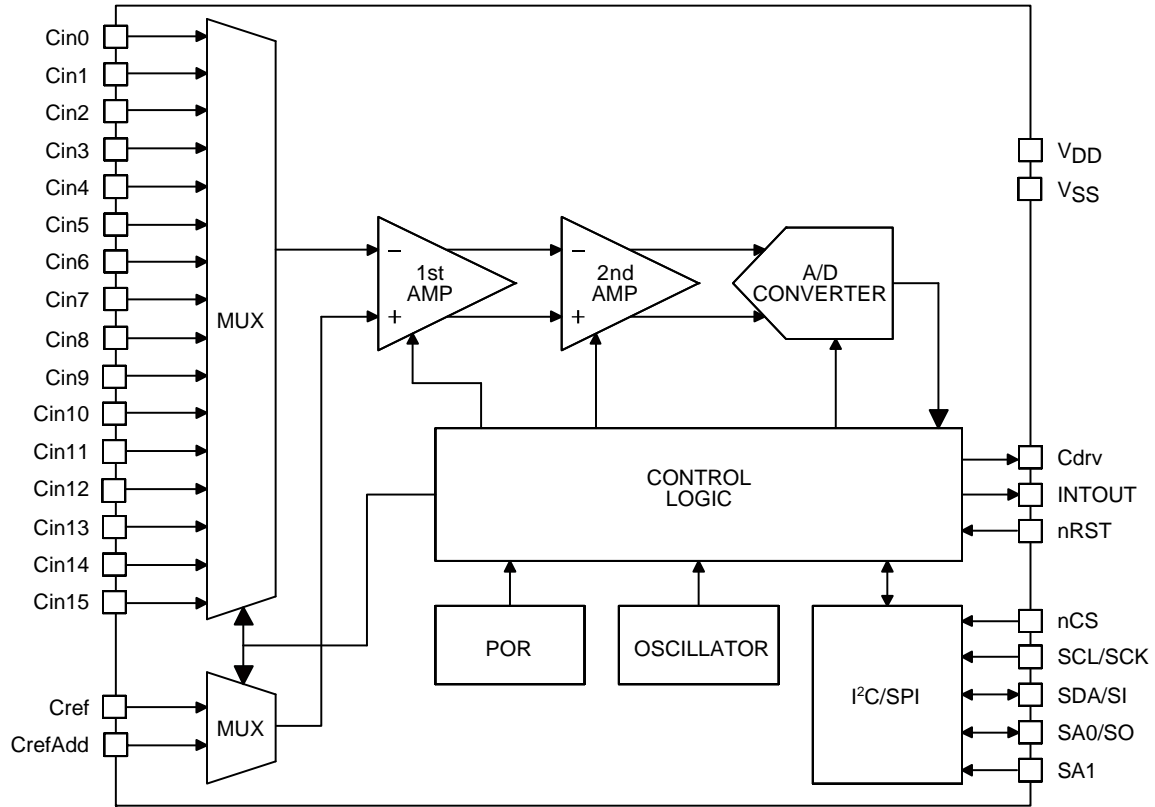
- Read format (data can be read from sequentially incremented addresses while preserving nCS = L)



**Figure 7.**

# LC717A10AR

## Block Diagram



**Figure 8. Simplified Block Diagram**

LC717A10AR is capacitance-digital-converter LSI capable of detecting changes in capacitance in the order of femto Farads. It consists of an oscillation circuit that generates the system clock, a power-on reset circuit that resets the system when the power is turned on, a multiplexer that selects the input channels, a two-stage amplifier that

detects the changes in the capacitance and outputs analog-amplitude values, a A/D converter that converts the analog-amplitude values into digital data, an I²C compatible bus or a SPI that enables serial communication with external devices and a control logic that controls the entire chip.

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## Pin Assignment

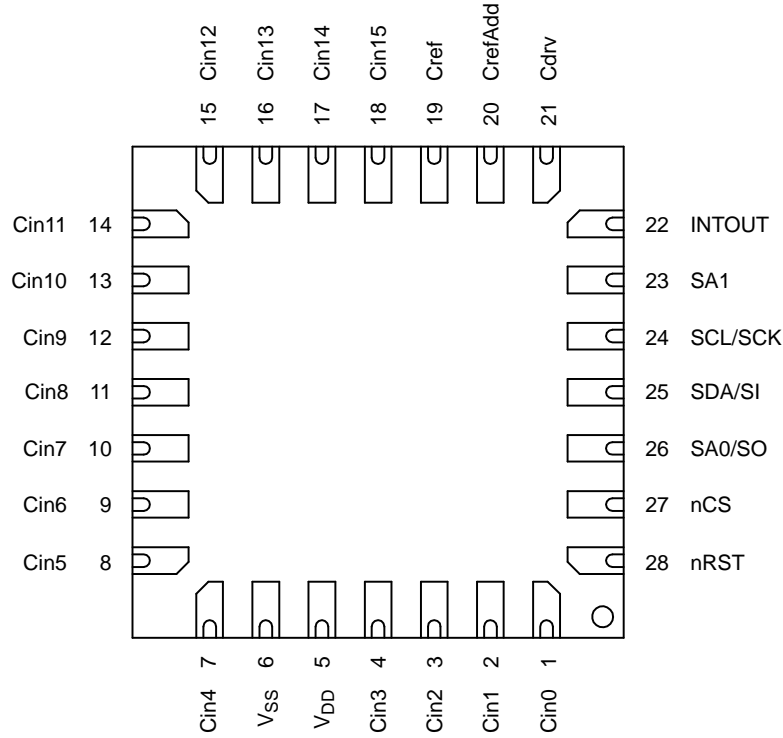


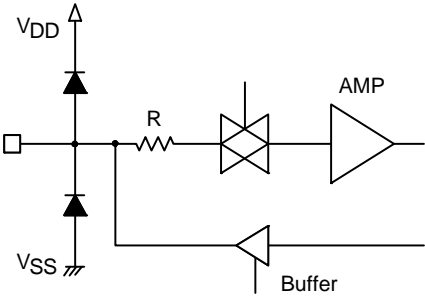
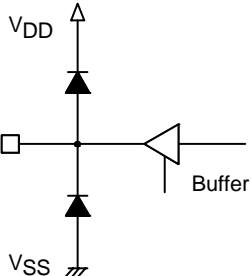
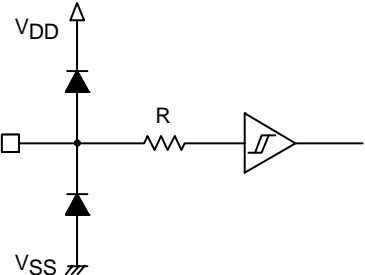
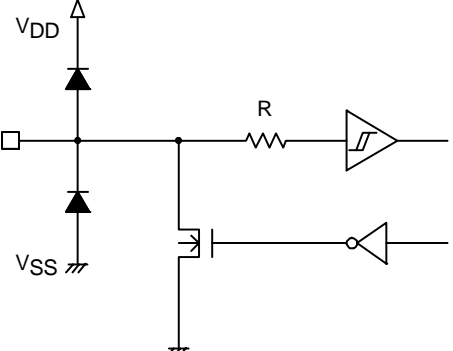
Figure 9. Pin Assignment (Bottom View)

Table 7. PIN ASSIGNMENT

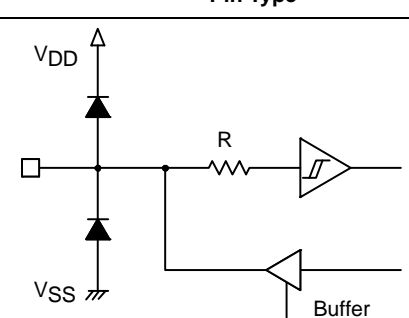
Pin No.	Pin Name	Pin No.	Pin Name
1	Cin0	15	Cin12
2	Cin1	16	Cin13
3	Cin2	17	Cin14
4	Cin3	18	Cin15
5	VDD	19	Cref
6	VSS	20	CrefAdd
7	Cin4	21	Cdrv
8	Cin5	22	INTOUT
9	Cin6	23	SA1
10	Cin7	24	SCL/SCK
11	Cin8	25	SDA/SI
12	Cin9	26	SA0/SO
13	Cin10	27	nCS
14	Cin11	28	nRST



Table 8. PIN FUNCTION

Pin Name	I/O	Pin Functions	Pin Type
Cin0	I/O	Capacitance sensor input	
Cin1	I/O	Capacitance sensor input	
Cin2	I/O	Capacitance sensor input	
Cin3	I/O	Capacitance sensor input	
Cin4	I/O	Capacitance sensor input	
Cin5	I/O	Capacitance sensor input	
Cin6	I/O	Capacitance sensor input	
Cin7	I/O	Capacitance sensor input	
Cin8	I/O	Capacitance sensor input	
Cin9	I/O	Capacitance sensor input	
Cin10	I/O	Capacitance sensor input	
Cin11	I/O	Capacitance sensor input	
Cin12	I/O	Capacitance sensor input	
Cin13	I/O	Capacitance sensor input	
Cin14	I/O	Capacitance sensor input	
Cin15	I/O	Capacitance sensor input	
Cref	I/O	Reference capacitance input	
CrefAdd	I/O	Reference capacitance input for addition	
Cdrv	O	Output for capacitance sensors drive	
INTOUT	O	Interrupt output	
SCL/SCK	I	Clock input (I <sup>2</sup> C) / Clock input (SPI)	
nCS	I	Interface selection / Chip select inverting input (SPI)	
nRST	I	External reset signal inverting input	
SA1	I	Slave address selection (I <sup>2</sup> C)	
SDA/SI	I/O	Data input and output (I <sup>2</sup> C) / Data input (SPI)	

**Table 8. PIN FUNCTION** (continued)

Pin Name	I/O	Pin Functions	Pin Type
SA0/SO	I/O	Slave address selection (I <sup>2</sup> C) / Data output (SPI)	
V <sub>DD</sub>		Power supply (2.6 V to 5.5 V) (Note 13)	
V <sub>SS</sub>		Ground (Earth) (Notes 13, 14)	

13. Inserting a high-valued capacitor and a low-valued capacitor in parallel between V<sub>DD</sub> and V<sub>SS</sub> is recommended. In this case, the small-valued capacitor should be at least 0.1  $\mu$ F, and is mounted near the LSI.

14. When V<sub>SS</sub> terminal is not grounded in battery-powered mobile equipment, detection sensitivity may be degraded.

## Details of Pin Functions

### *Cin0 to Cin15*

These are the capacitance-sensor-input pins. These pins are used by connecting them to the touch switch pattern. Cin and the Cdrv wire patterns should be close to each other. By doing so, Cdrv and Cin patterns are capacitively coupled. Therefore, LSI can detect capacitance change near each pattern as 8-bit digital data.

However, if the shape of each pattern or the capacitively coupled value of Cdrv is not appropriate, it may not be able to detect the capacitance change correctly.

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cin0 to Cin15 are connected to the inverting input of the 1<sup>st</sup> amplifier.

During measurement process, channels other than the one being measured are all in “Low” condition.

Leave the unused terminals open.

### *Cref, CrefAdd*

These are the reference-capacitance-input pins. These are used by connecting to the wire pattern like Cin pins or are used by connecting any capacitance between this pin and Cdrv pin.

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cref is connected to the non-inverting input of the 1<sup>st</sup> amplifier.

Due to the parasitic capacitance generated in the wire connections of Cin pins and their patterns, as well as the one generated between the wire patterns of Cin and Cdrv pins, Cref may not detect capacitance change of each Cin pin accurately. In this case, connect an appropriate capacitance between Cref and Cdrv to detect capacitance change accurately.

However, if the difference between the parasitic capacitance of each Cin pin is extremely large, it may not detect capacitance change in each Cin pin correctly.

CrefAdd can be used as additional terminal for Cref. Leave the CrefAdd open if not in used.

### *Cdrv*

It is the output pin for capacitance sensors drive. It outputs the pulse voltage which is needed to detect capacitance at Cin0 to Cin15.

Cdrv and Cin wire patterns should be close to each other so that they are capacitively coupled.

### *INTOUT*

It is the interrupt-output pin. It is used by connecting to a main microcomputer if necessary, and use as interrupt signal. (High Active).

Leave the terminal open if not in used.

### *SCL/SCK*

Clock input (I<sup>2</sup>C)/Clock input (SPI). It is the clock input pin of the I<sup>2</sup>C compatible bus or the SPI depending on the mode of operation.

### *nCS*

Interface selection/Chip-select-inverting input (SPI). Selection of I<sup>2</sup>C compatible bus mode or SPI mode is through this terminal. After initialization, the LSI is automatically in I<sup>2</sup>C compatible bus mode. To continually use I<sup>2</sup>C compatible bus mode, fix nCS pin to “High”. To switch to SPI mode after LSI initialization, change the nCS input “High”  $\rightarrow$  “Low”. The nCS pin is used as the chip-select-inverting input pin of SPI, and SPI mode is kept until LSI is again initialized.

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### *nRST*

It is the external-reset-signal-inverting-input pin. When nRST pin is “Low”, LSI is in the reset state.

Each pin (Cin0 to 15, Cref, CrefAdd) is “Hi-Z” during reset state.

### *SDA/SI*

Data input and output (I<sup>2</sup>C)/Data input (SPI). It is the data input and output pin of the I<sup>2</sup>C compatible bus or the data input pin of the SPI depending on the mode of operation.

### *SA0/SO*

Slave address selection (I<sup>2</sup>C)/Data output (SPI). It is the slave address selection pin of the I<sup>2</sup>C compatible bus or the data output pin of the SPI depending on the mode of operation.

### *SA1*

Slave address selection (I<sup>2</sup>C). It is the slave address selection pin of the I<sup>2</sup>C compatible bus.

When SPI mode, connect to the SA1 pin to GND.

**Table 9. ORDERING INFORMATION**

Device	Package	Shipping (Qty / Packing) <sup>†</sup>
LC717A10AR-NH	VCT28 3.5 × 3.5 (Pb-Free / Halogen Free)	2000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# MECHANICAL CASE OUTLINE

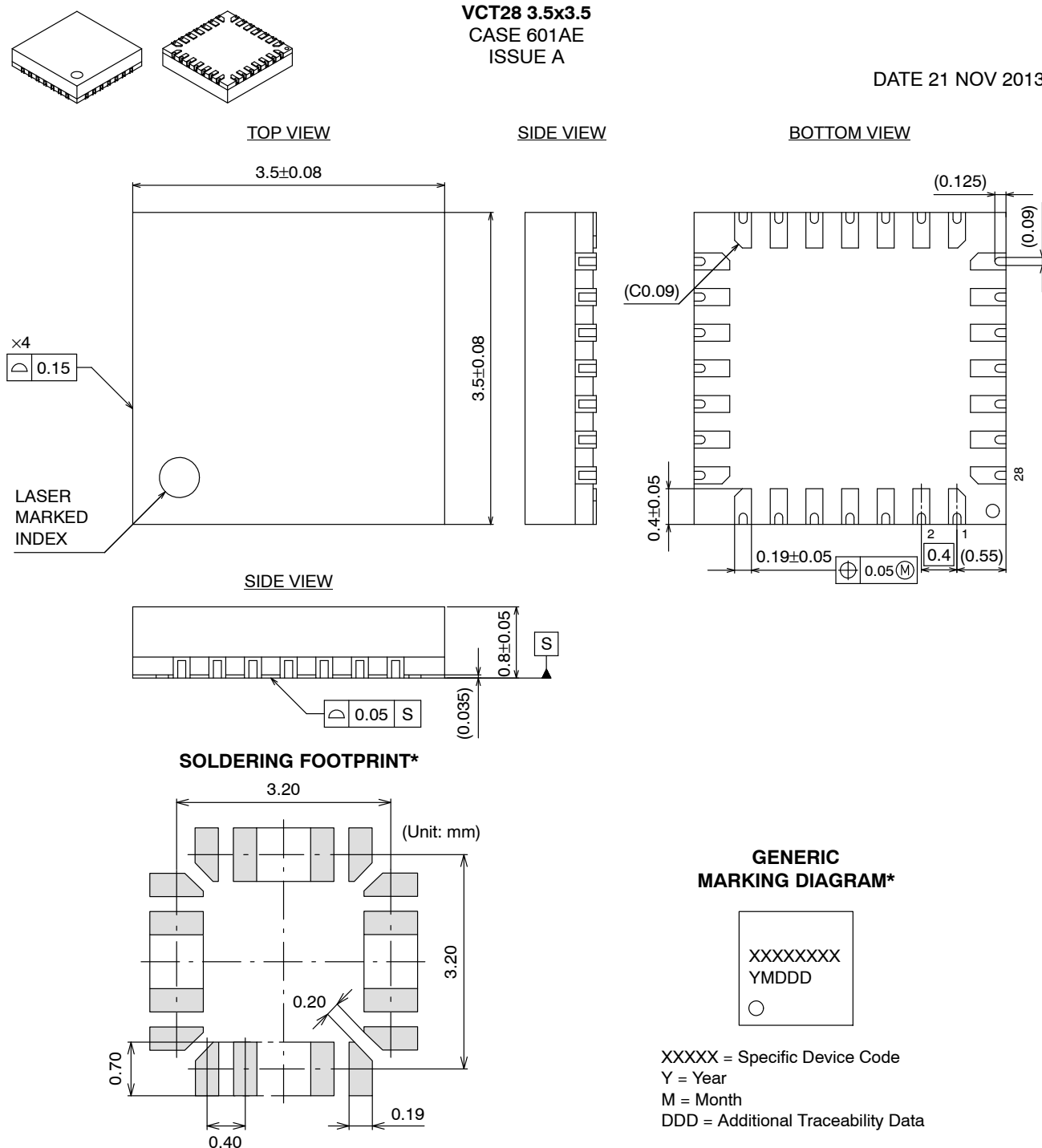
## PACKAGE DIMENSIONS

ON Semiconductor®

ON

**VCT28 3.5x3.5**  
CASE 601AE  
ISSUE A

DATE 21 NOV 2013




NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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