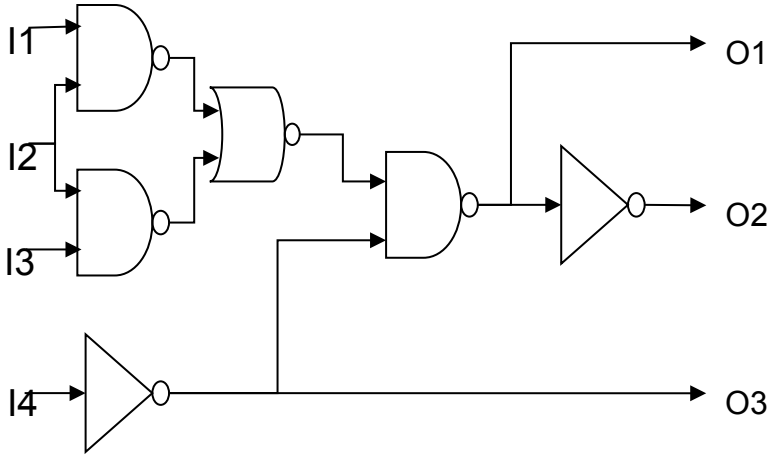
Electronic Design Automation

Highly Scalable Multi Threaded Incremental Static Timing Analysis

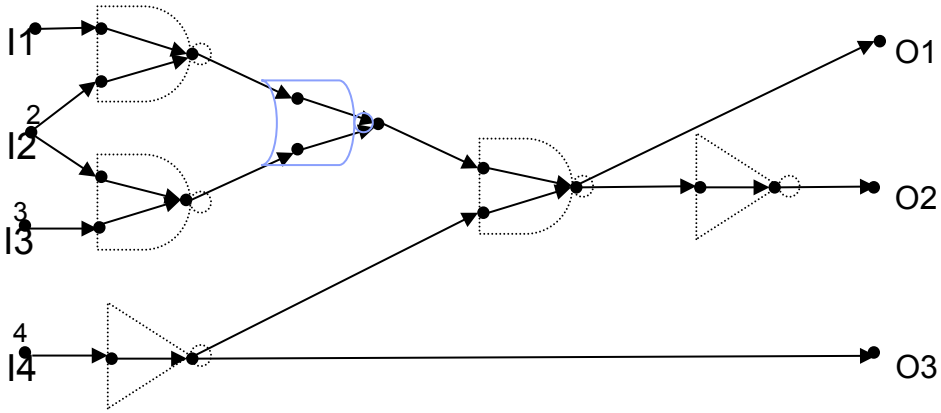
Daniel Beece +, Bijian Chen *, Hemlata Gupta *, David Hathaway *, Kerim Kalafala *, Douglas Keller *, Mark Lavin +, Jeff Piaget *, Peihua Qi *, Gregory Schaeffer *, Chandu Visweswariah* , Jeffrey Wilson *, Vladimir Zolotov +

+ IBM T.J. Watson Research Center, Yorktown Heights, NY
* IBM Systems and Technology Group, East Fishkill, NY and Burlington, VT

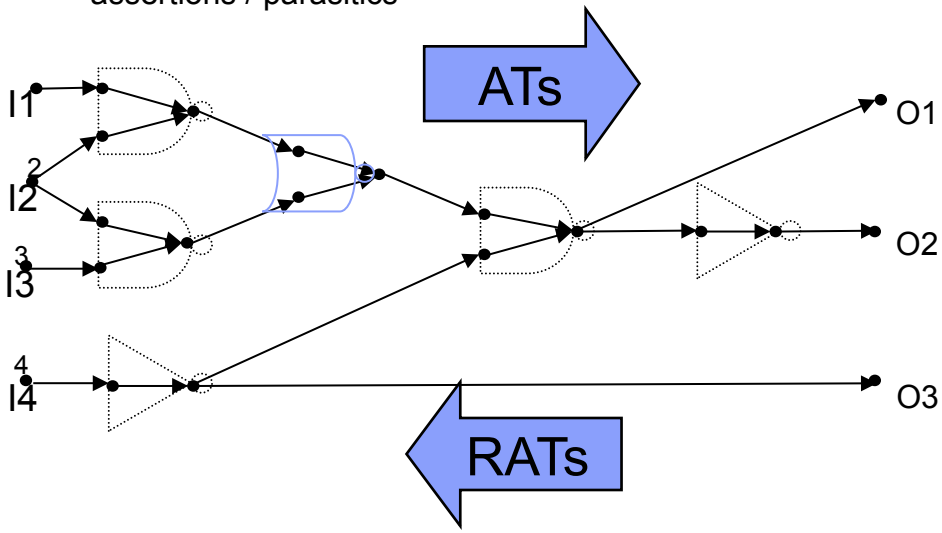
Static timing analysis 101



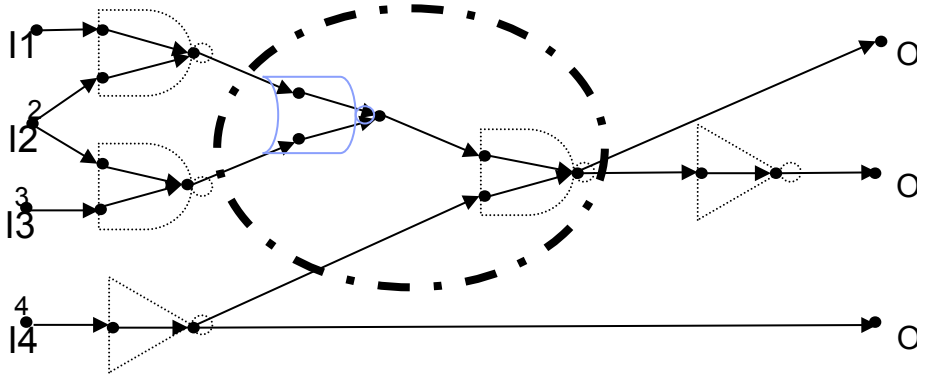
Step 1- Load netlist / assertions / parasitics



Step 2. – Create Timing graph (DAG) corresponding to the preceding circuit.

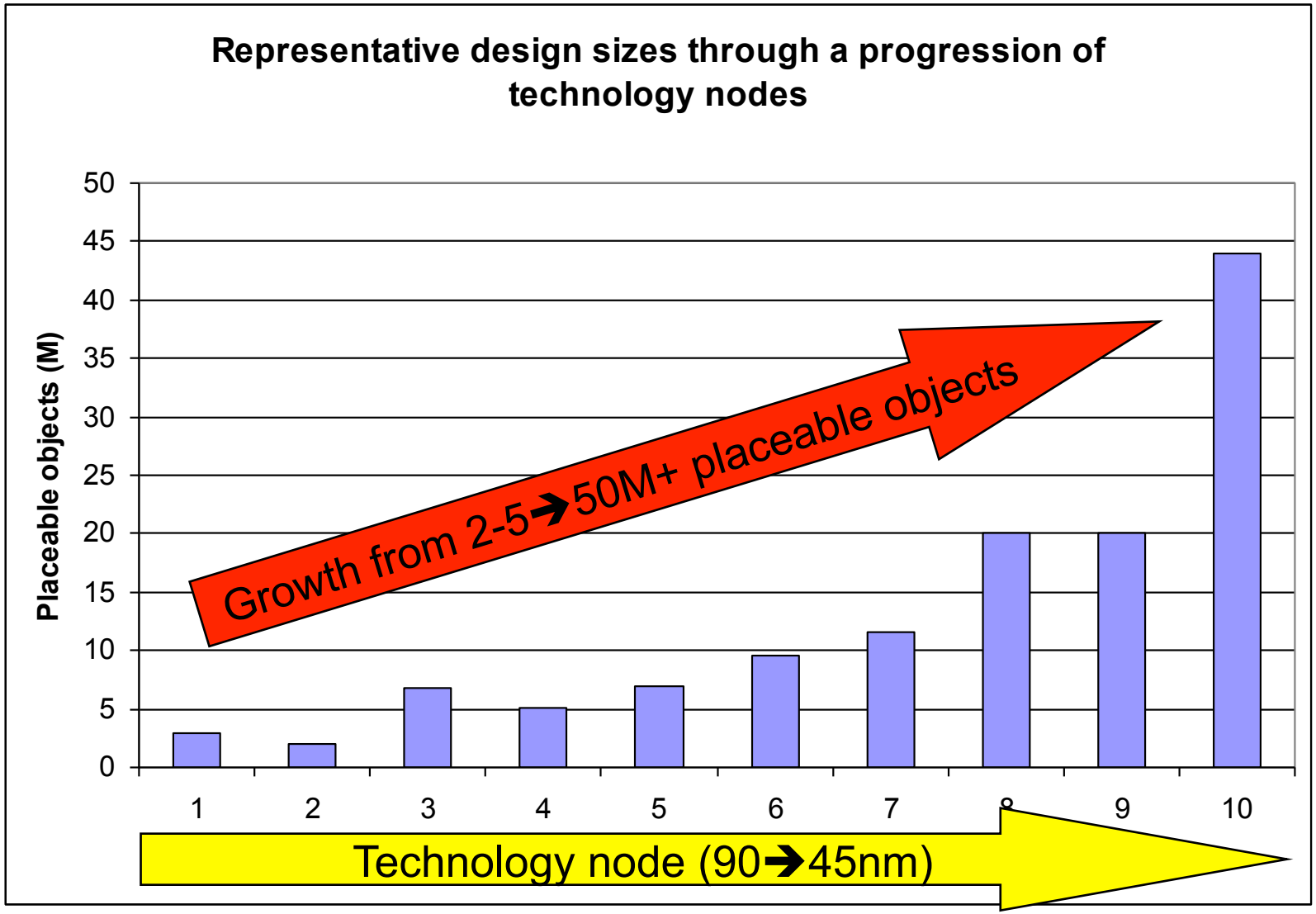


Step 3 – Propagate Arrival Times (ATs) Forward and Required Times (RATs) Backward

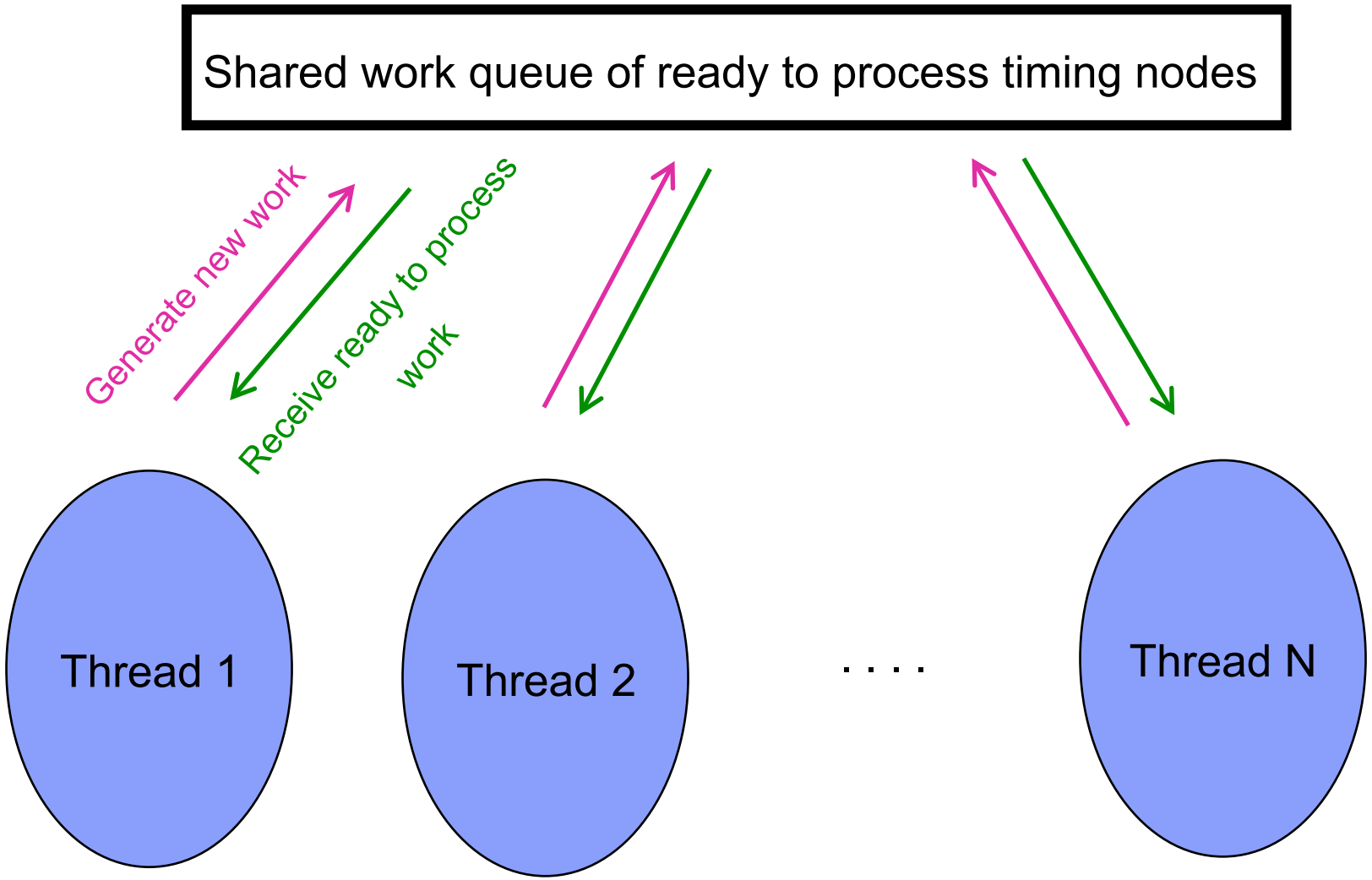


Step 4 – Fix-up and incremental re-analysis

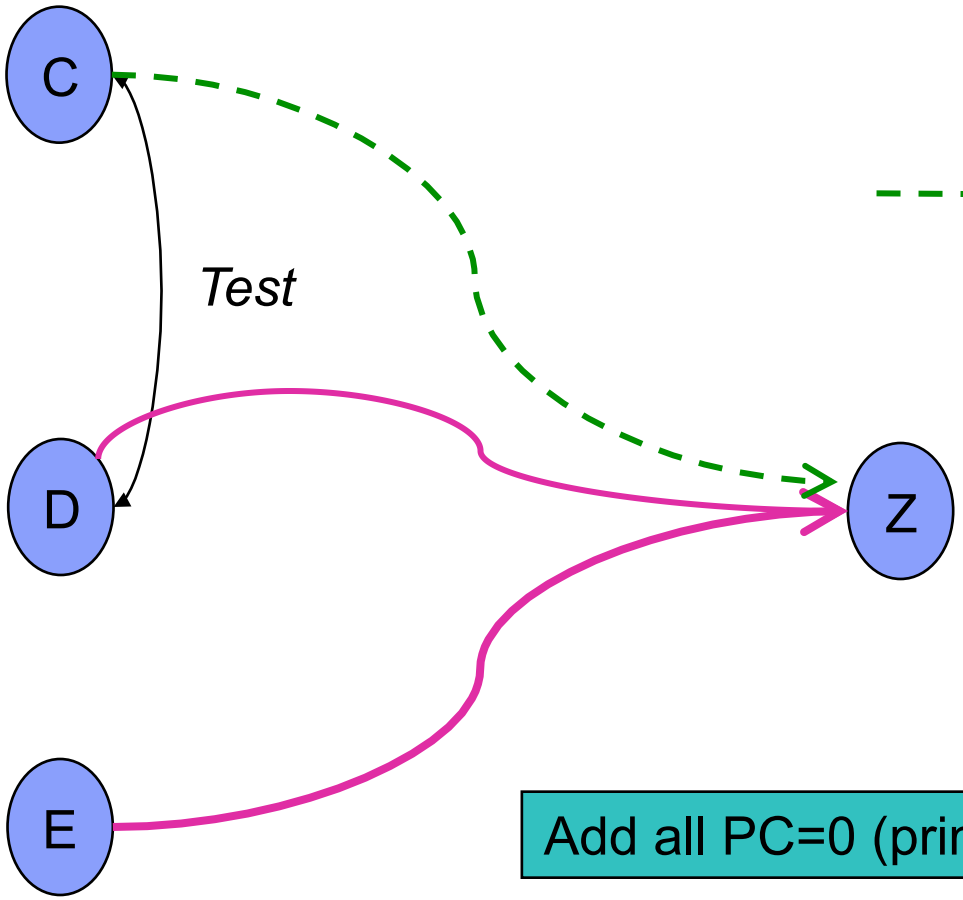
Challenge of increasing design size



Key idea for parallelizing base AT/RAT propagation: dynamic work queue processing



Calculation of initial predecessor counts



Direct dependency
(delay arc)

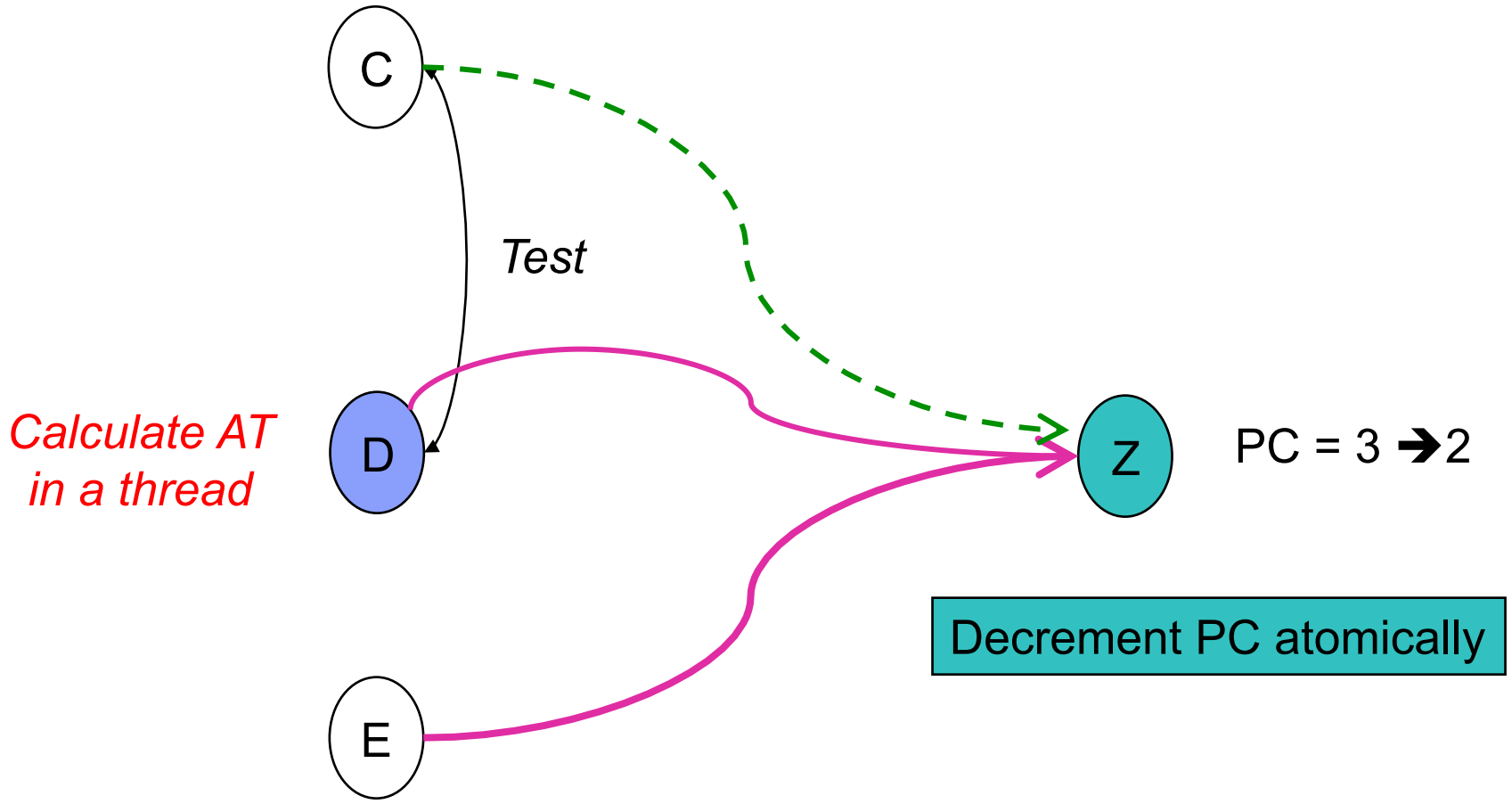
Indirect dependency
(e.g., clock limited
propagation)

Predecessor Count (initial value)

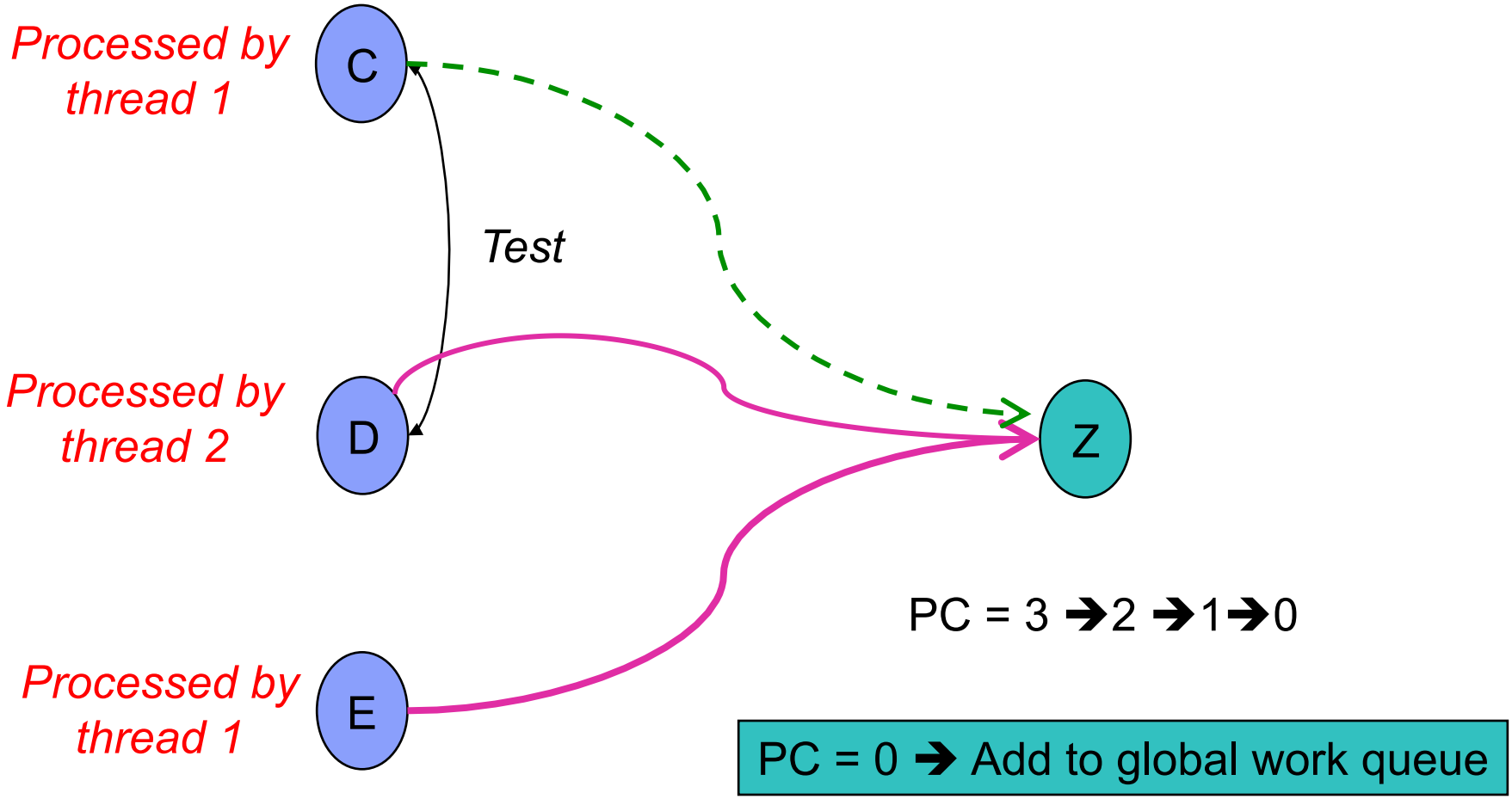
= # Incoming dependencies

Add all PC=0 (primary inputs) nodes to work queue

Updating predecessor count using atomic operations

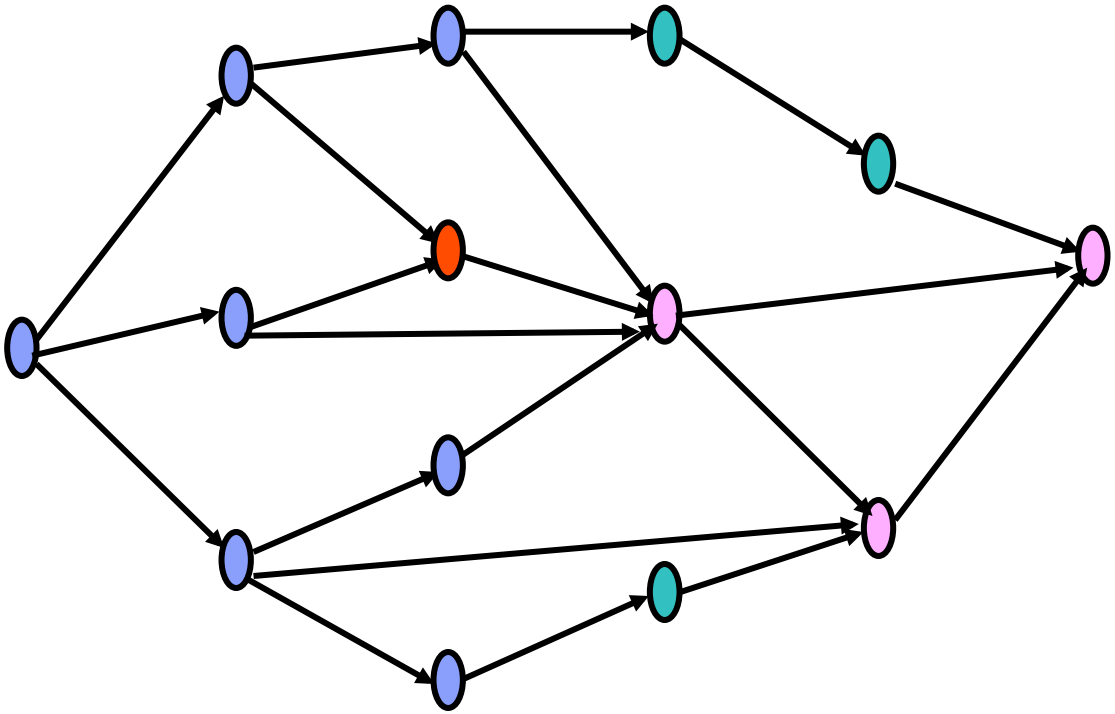


Generating new work based on updated predecessor counts

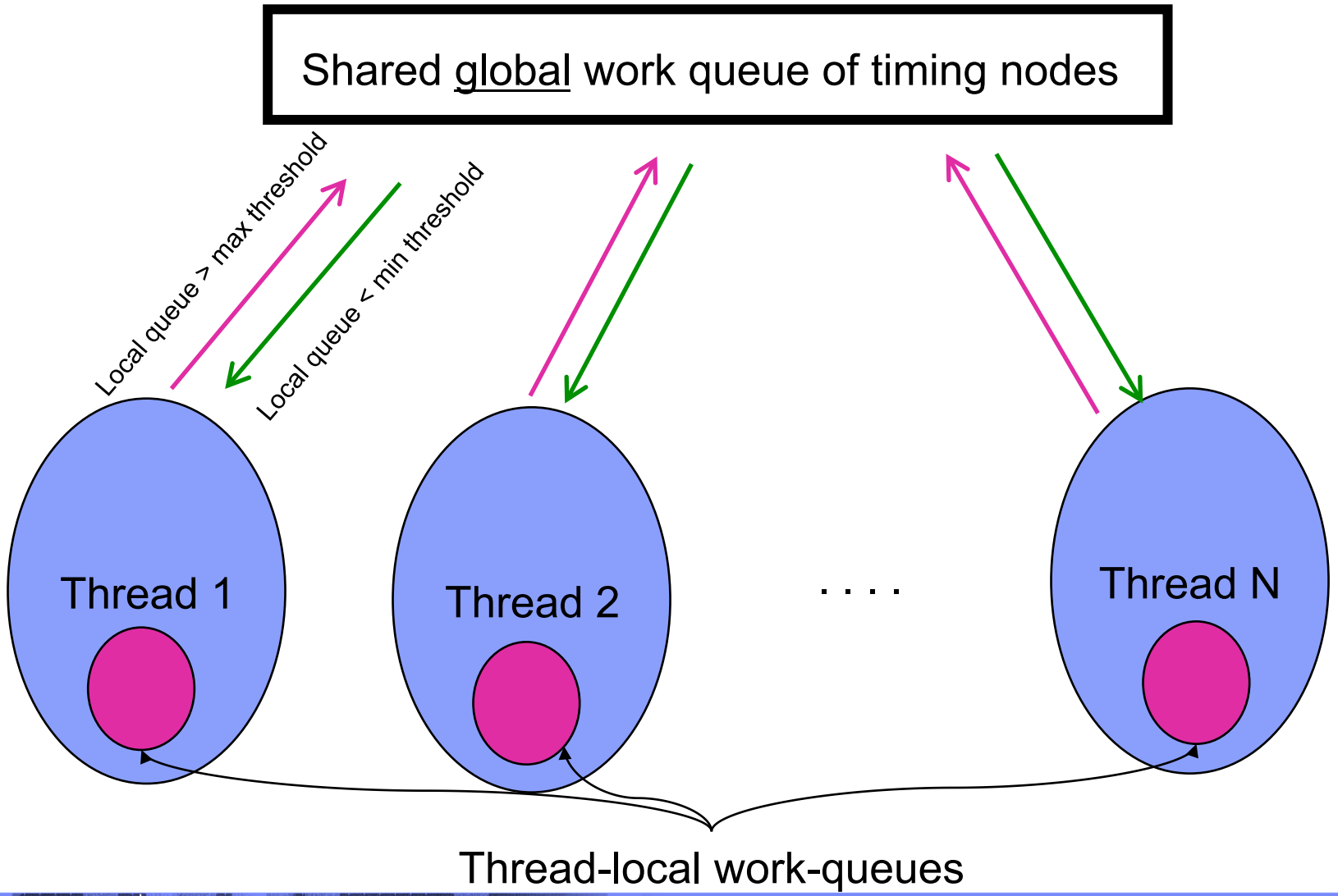


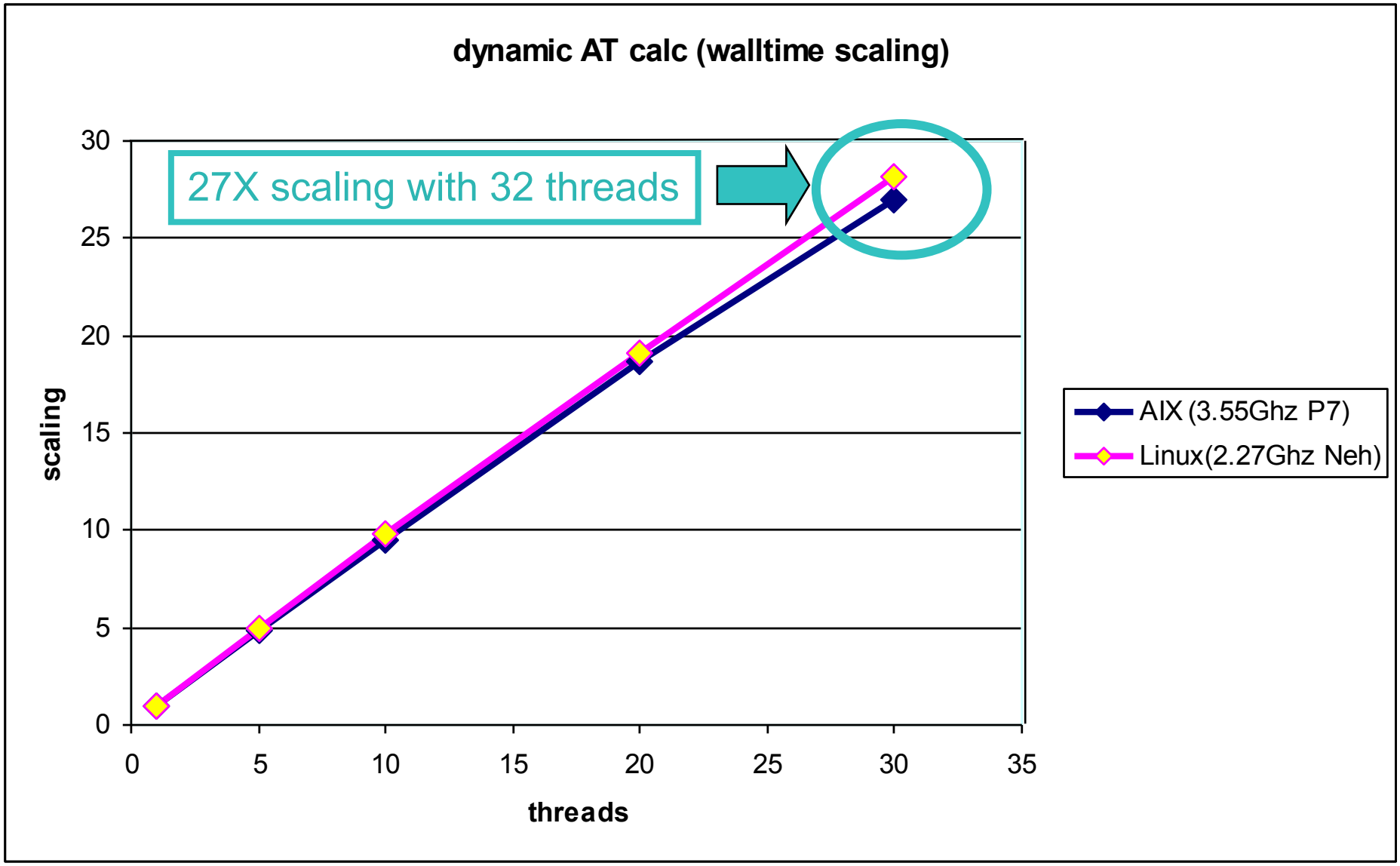
Benefit of dynamic processing

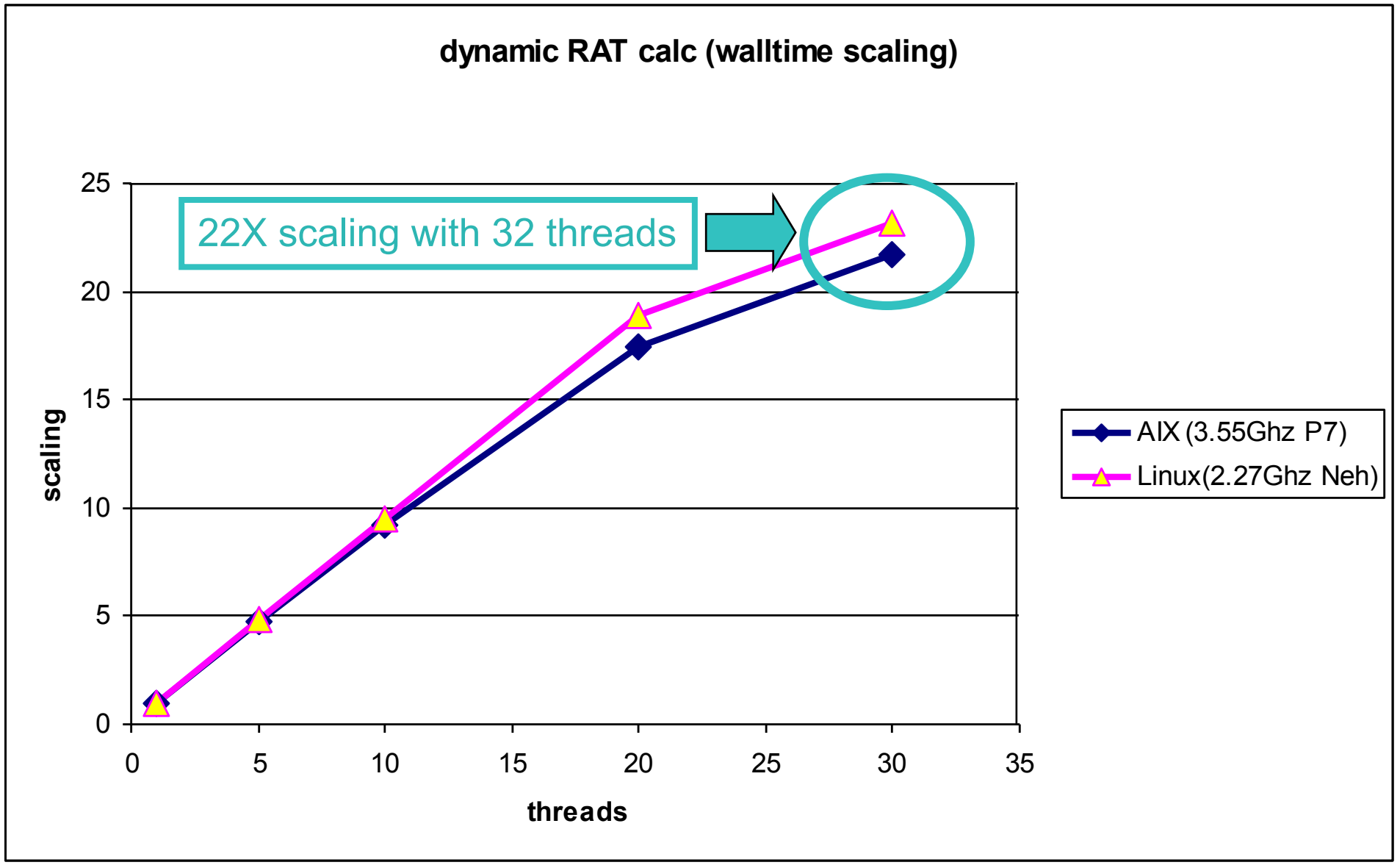
- Bottleneck (e.g., complex delay calculation)
- Nodes where work can proceed independent of bottleneck



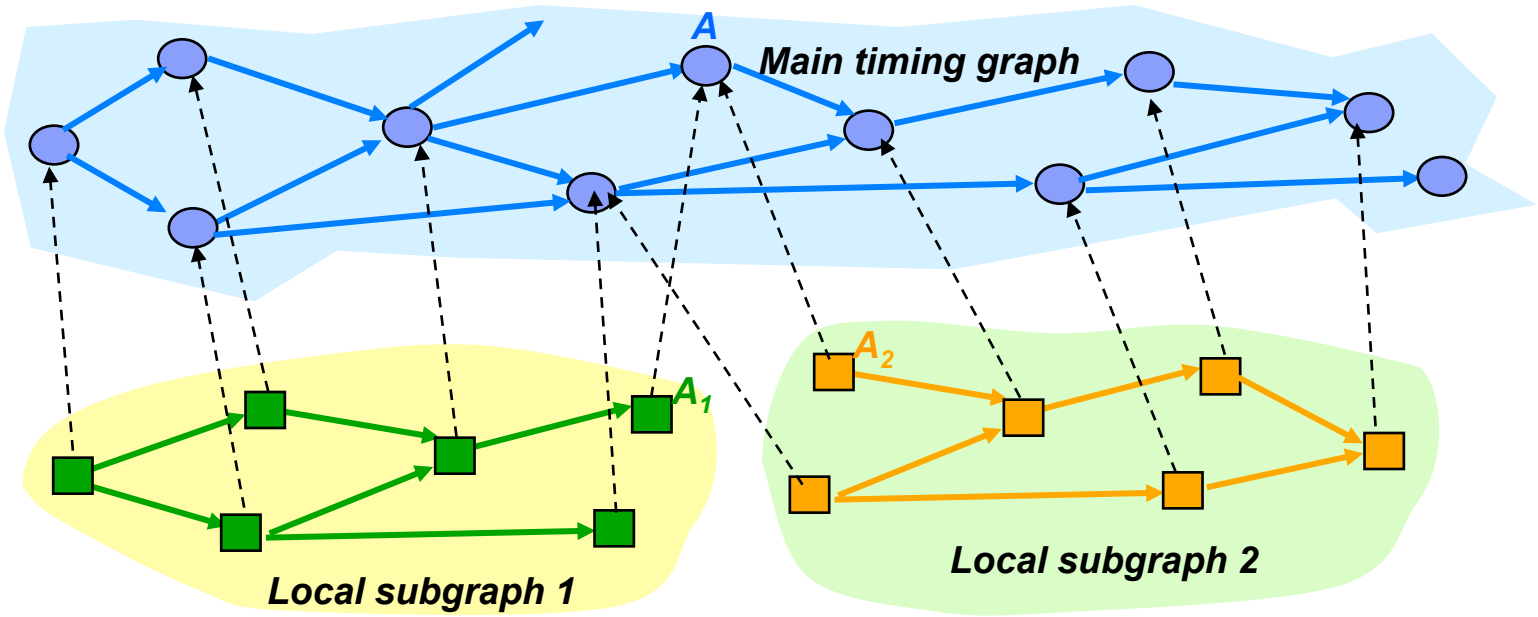
Use of local queues to minimize global queue locking





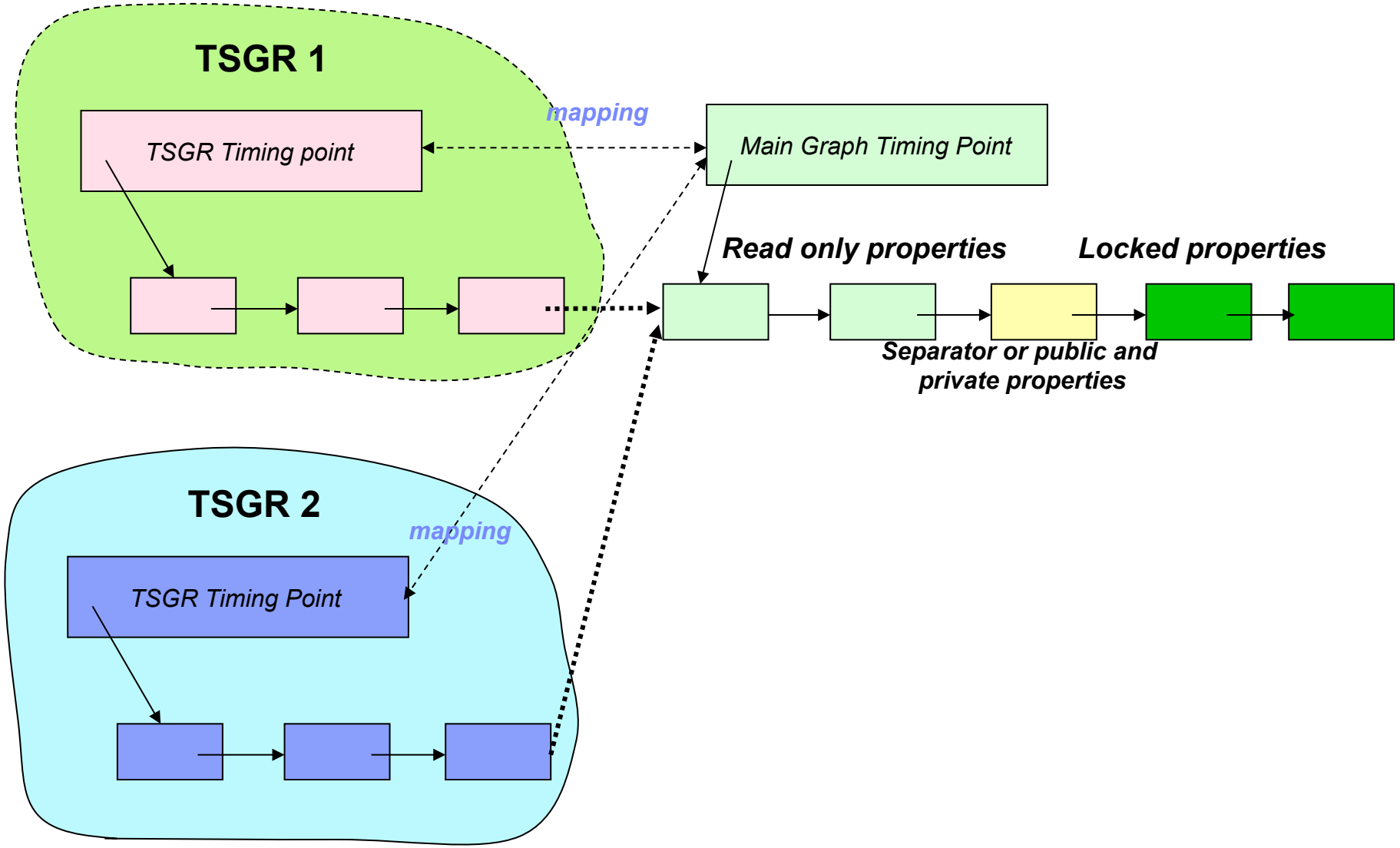


Thread Specific Timing Graph Concept

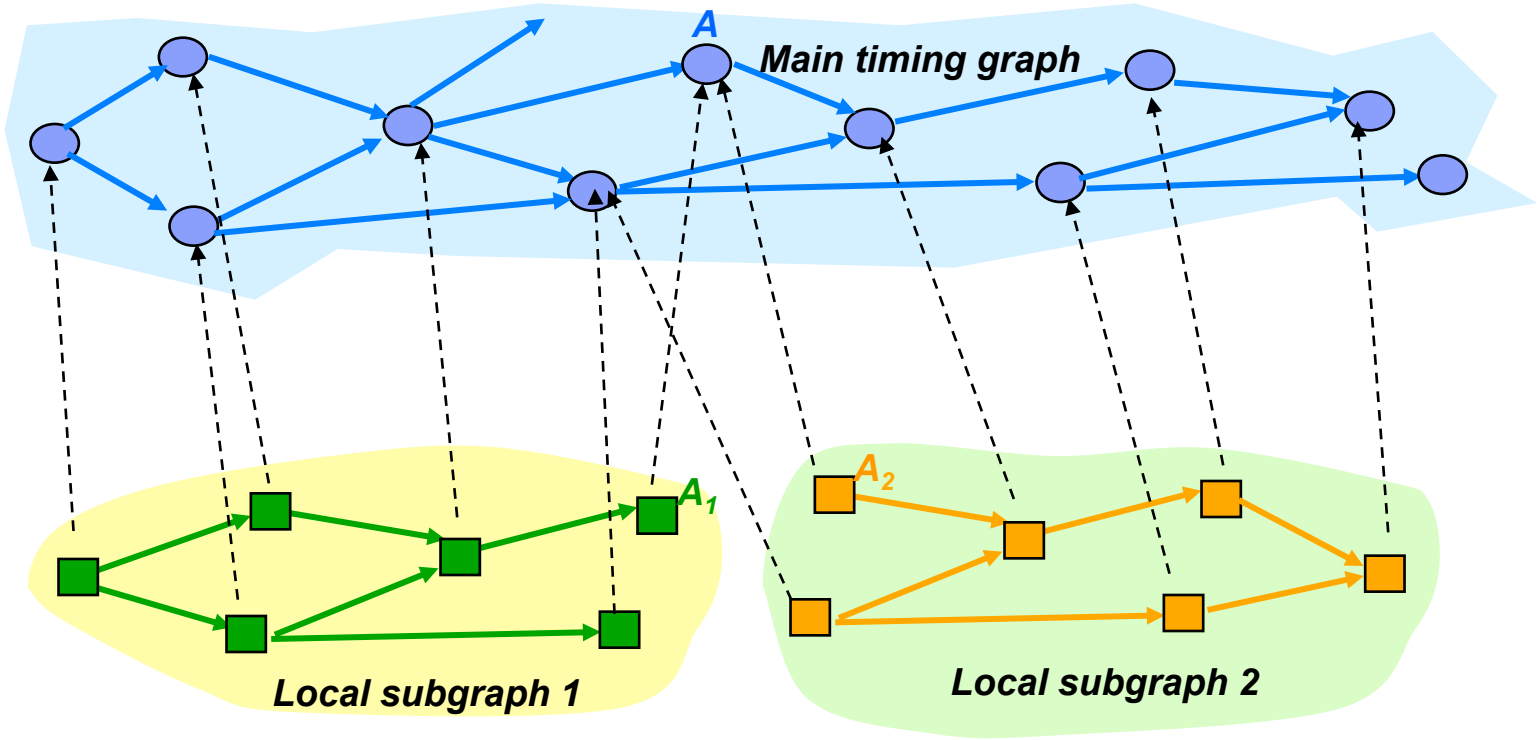


- **Subgraphs can be updated independently <u>without the need for locking</u>**

Properties in TSGR and main timing graph

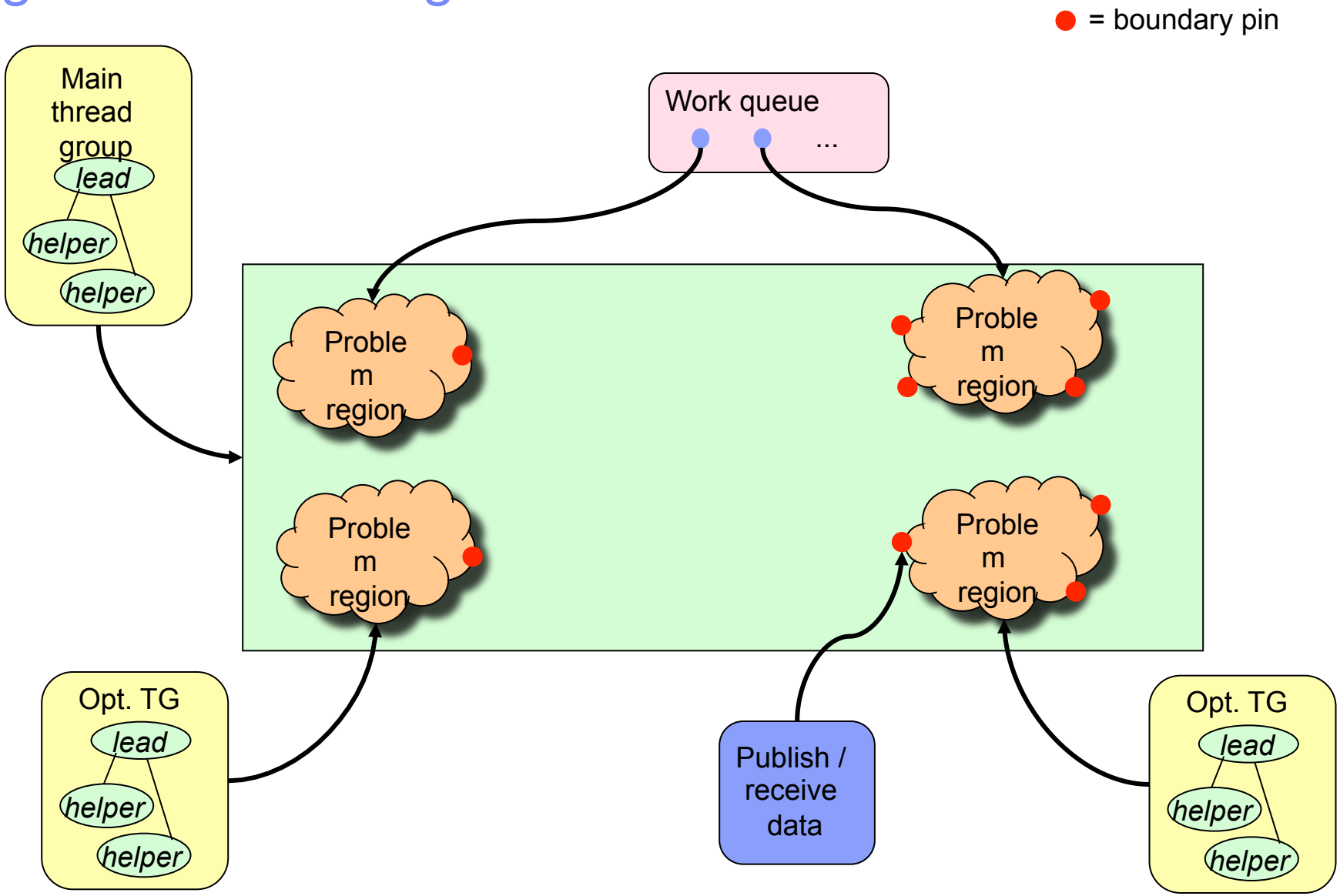


Back annotation of CPPR results to main timing graph



- **Back-annotation of results to the main graph requires locking specific nodes.**

Region-based timing overview



Use of regions in optimization

- **Boundary pins at inputs of usage boxes**
- **First level of usage boxes in region are unchangeable**
  - Helps isolate timing / electrical impacts of changes in other regions